Resumen de Tesis Doctoral

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(Mínimo 1 y màximo 4, podéis verlos en http://doctorat.upc.edu/gestion-academica/carpeta-impresos/tesis-matricula-y-deposito/codigos-unesco)

Resumen de la tesis de 4000 caracteres máximo (si se superan los 4000 se cortará automáticamente)

In 1925, Lilienfeld patented the basic principle of field effect transistor (FET). Thirty-four years later, Kahng and Atalla invented the MOSFET. Since that time, it has become the most widely used type of transistor in Integrated Circuits (ICs) and then the most important device in the electronics industry. Progress in the field for at least the last 40 years has followed an exponential behavior in accordance with Moore's Law. That is, in order to achieve higher densities and performance at lower power consumption, MOS devices have been scaled down. But this aggressive scaling down of the physical dimensions of MOSFETs has required the introduction of a wide variety of innovative factors to ensure that they could still be properly manufactured. Transistors have experienced an amazing journey in the last 10 years starting with strained channel CMOS transistors at 90nm, carrying on the introduction of the high-k/metal-gate silicon CMOS transistors at 45nm until the use of the multiple-gate transistor architectures at 22nm and at recently achieved 14nm technology node. But, what technology will be able to produce sub-10nm transistors?

Different novel materials and devices are being investigated. As an extension and enhancement to current MOSFETs some promising devices are n-type III-V and p-type Germanium FETs, Nanowire and tunnel FETs, graphene FETs and carbon nanotube FETs. Also, non-conventional FETs and other charge-based information carrier devices and alternative information processing devices are being studied.

This thesis is focused on carbon nanotube technology as a possible option for sub-10nm transistors. In recent years, carbon nanotubes (CNTs) have been attracting considerable attention in the field of nanotechnology. They are considered to be a promising substitute for silicon channel because of their small size, unusual geometry (1D structure), and extraordinary electronic properties, including excellent carrier mobility and quasi-ballistic transport. In the same way, carbon nanotube field-effect transistors (CNFETs) could be potential substitutes for MOSFETs. Ideal CNFETs (meaning all CNTs in the transistor behave as semiconductors, have the same diameter, and are aligned and well-positioned) are predicted to be 5x faster than silicon CMOS, while consuming the same power. However, nowadays CNFETs are also affected by manufacturing variability, and several significant challenges must be overcome before these benefits can be achieved. Certain CNFET manufacturing imperfections, such as CNT diameter and doping variations, mispositioned and misaligned CNTs, high metal-CNT contact resistance, the presence of metallic CNTs (m-CNTs), and CNT density and count variations, can affect CNFET performance and reliability and must be addressed.
The main objective of this thesis is to analyze the impact of the current CNFET manufacturing challenges, which result in CNT-specific variations, on multi-channel CNFET performance from the point of view of variability and reliability and at different levels, device and circuit level. Assuming that CNFETs are not ideal or non-homogeneous because of today CNFET manufacturing imperfections, we propose a methodology of analysis that based on a CNFET ideal compact model is able to simulate heterogeneous or non-ideal CNFETs; that is, transistors with different numbers of tubes that have different diameters, are not uniformly spaced, have different source/drain doping levels, and, most importantly, are made up not only of semiconducting CNTs but also metallic ones. This method will allow us to study how CNT-specific variations affect CNFET device characteristics and parameters and CNFET digital circuit performance. Furthermore, we also derive a CNFET failure model and propose an alternative technique based on fault-tolerant architectures to deal with the presence of m-CNTs, one of the main causes of failure in CNFET circuits.

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