Resumen de Tesis Doctoral

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Título de la tesis | Efficient multiprocessing architectures for Spiking Neural Network emulation based on configurable devices

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Códigos UNESCO

(Mínimo 1 y màximo 4, podéis verlos en http://doctorat.upc.edu/gestion-academica/carpeta-impresos/tesis-matricula-y-deposito/codigos-unesco)

Resumen de la tesis de 4000 caracteres máximo (si se superan los 4000 se cortará automáticamente)

The exploration of the dynamics of bioinspired neural networks has allowed neuroscientists to understand some clues and structures of the brain. Neural network implementations are useful tools for this exploration. However, appropriate architectures are necessary due to the extremely high complexity of those networks. There has been an extraordinary development in reconfigurable computing devices within a short period of time especially in their resource availability, speed, and configurability (FPGAs).

Reconfigurable parallel hardware architecture is proposed in this thesis in order to emulate in real time complex and biologically realistic spiking neural networks (SNNs). Some relevant SNN models and their hardware approaches have been studied, and analyzed in order to create an architecture that supports the implementation of these SNN models efficiently. The development of the proposed architecture takes into account the key factors in order to emulate SNN models efficiently. These factors involve flexibility in algorithm programmability, high performance processing, low area and power consumption. In order to boost the performance of the proposed architecture, several techniques have been developed: time to space mapping, neural virtualization, flexible synapse-neuron mapping, specific learning and execution modes, among others.

Besides this, an interface unit has been developed in order to build a bio-inspired system, which can process sensory information from the environment. The spiking-neuron-based system combines analog and digital multi-processor implementations. Several applications have been developed as a proof-of-concept in order to show the capabilities of the proposed architecture for processing this type of information.

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