



# Resum de Tesi Doctoral

DNI/NIE/Passaport	Y1655244V
Nom i cognoms	Gerhard Martin LANDAUER
Títol de la tesi	Opportunities for Radio Frequency Nanoelectronic Integrated Circuits using Carbon-Based Technologies
Unitat estructural	Departament d'Enginyeria Electrònica
Programa	Programa de Doctorat en Enginyeria Electrònica
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(Mínim 1 i màxim 4, podeu veure els codis a <http://doctorat.upc.edu/gestio-academica/impresos/tesi-matricula-i-diposit/codis-unesco>)

## Resum de la tesi de 4000 caràcters màxim (si supera els 4000 es tallarà automàticament)

This thesis presents a body of work on the modeling of and performance predictions for carbon nanotube field-effect transistors (CNFET) and graphene field-effect transistors (GFET). While conventional silicon-based CMOS is expected to reach its ultimate scaling limits during the next decade, these two novel technologies are promising candidates for future high-performance electronics. The main goal of this work is to investigate on the opportunities of using such carbon-based electronics for RF integrated circuits. This thesis addresses 1) the modeling of noise and process variability in CNFETs, 2) RF performance predictions for CNFETs, and 3) an accurate GFET compact model.

This work proposes the first CNFET noise compact model. Noise is of primary importance for RF applications and its description significantly increases the insight gained from simulation studies. Furthermore, a CNFET variability model is presented, which handles tube synthesis and metal tube removal imperfections. These two model extensions have been added to the Stanford CNFET compact model and allow for the variability-aware RF performance assessment of the CNFET technology.

Comprehensive RF performance projections for CNFETs are provided both on the device and circuit level. The overall set of ITRS RF-CMOS technology requirement FoMs is determined and shows that the CNFET performs excellently in terms of speed, gain, and minimum noise figure. Furthermore, for the first time FoMs are reported for the basic RF building blocks low-noise amplifier and oscillator. In addition, it is shown that CNFET downscaling yields significant performance improvements. Based on these analyses it is confirmed that the CNFET has the potential to outperform Si-CMOS in RF applications.

A third key contribution of this thesis is the development of an accurate GFET compact model. Previous compact models simplify several physical aspects, which can cause erroneous simulation results. Here, an accurate yet simple mathematical description of the GFET's current-voltage relation is proposed and implemented in Verilog-A. Comprehensive error analyses are done in order to highlight the advantages of the new approach. Furthermore, the model is verified against measurement results. The developed GFET model is an important step towards better understanding the characteristics and opportunities of graphene-based analog circuitry.

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