# Resumen de Tesis Doctoral

UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Escola de Doctorat

| | |
|---|---|
| DNI/NIE/Pasaporte | 46413733D |
| Nombre y apellidos | Joan Nicolás Apruzzese |
| Título de la tesis | Design and analysis of a novel multilevel active-clamped power converter |
| Unidad estructural | 710 Departamento de Ingeniería Electrónica |
| Programa | Doctorado en Ingeniería Electrónica |
| Códigos UNESCO | 330600 \| 330601 \| 330700 \| 330799 → convertidores electrónicos de potencia |

(Mínimo 1 y màximo 4, podéis verlos en http://doctorat.upc.edu/gestion-academica/carpeta-impresos/tesis-matricula-y-deposito/codigos-unesco)

Resumen de la tesis de 4000 caracteres máximo (si se superan los 4000 se cortará automáticamente)

Multilevel converter technology has been receiving increasing attention during the last years due to its important advantages compared to conventional two-level conversion. Multilevel converters reduce the voltage across each semiconductor. These converters also synthesize waveforms with better harmonic spectrum, and in most cases, increasing the efficiency of the power conversion system. However, a larger quantity of semiconductors is needed and the modulation strategy to control them becomes more complex. There are three basic multilevel converter topologies: diode clamped, flying capacitor, and cascaded H-bridge with separate dc sources. Numerous hybrid configurations combining them and other multilevel topologies have also been presented in the literature.

A novel multilevel active-clamped (MAC) topology is the subject of study of the present thesis. This topology is derived from the generalized multilevel topology by simply removing all flying capacitors. The topology can also be seen as an extension into an arbitrary number of levels of the three-level active neutral-point-clamped (ANPC) topology. The novel converter is controlled using a proper set of switching states and a switching state transition strategy, which permits to obtain the maximum benefits from the converter.

In this thesis, the performance and operating capabilities of the MAC topology are studied through comprehensive efficiency and fault-tolerance analyses.

The efficiency analysis comprises a study of power-device conduction and switching losses in the topology, followed by analytical and experimental efficiency comparisons between the MAC converter and conventional two-level converters.

In the analysis of the fault-tolerance capacity of the MAC topology both open- and short-circuit faults are considered and the analysis is carried out under single-device and two-simultaneous-device faults. Switching strategies to overcome the limitations caused by faults and topology variations to increment the fault-tolerance ability of the MAC converter are proposed.

The thesis also proposes guidelines to guarantee a proper MAC converter design and improve its performance.

Lugar: Barcelona  Fecha: 27 de junio de 2013

Firma: Joan Nicolás