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Doctoral thesis summary

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Title of the thesis	Contribution To The Architecture And Implementation Of Bi-NOC Routers For Multi-Synchronous GALS Systems
Structural unit	
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Thesis summary of a maximum of 4,000 characters (if you exceed this number it will automatically cut you off).

Networks-on-Chip (NoC) is an emerging on-chip interconnection centric platform that influences the modern high speed communication infrastructure to improve on-chip communication challenges in the recent many core System-on-Chip (SoC) designs. Continuing shrinkage of feature dimensions of Nano-scale semiconductor devices has been raised serious concerns of the reliability, signal integrity, and quality of services (QoS) of traditional bus based on-chip interconnect infrastructure. NoC represents a major standard move to address these concerns by incorporating state-of-the-art of high-speed data network components (such as routers and switches) and packet-based routing protocols in novel on-chip network infrastructure. A NoC's aim is to provide a reliable on-chip communication platform to facilitate scalable gigascale SoC design.

A multi-synchronous bi-directional NoC's router architecture is proposed in this thesis to enhance the performance of available on-chip communication platform. Using parameterized RTL implementation, we first divide microarchitecture into six blocks as multi-synchronous FIFO, Arbiters, Route Computation, Switch Allocator, Virtual channel Allocator, and Network Interface. Overall architecture of the proposed NoC router consists of five bi-directional ports which supports data transfer between two clock domain of completely arbitrary phase and frequency; and best suited for the Distributed Scalable Predictable Interconnect Networks (DSPIN). In this router, each communication channel allows itself to be dynamically reconfigured to transmit flits in either direction. This added flexibility promises better bandwidth utilization, lower packet delivery latency, and higher packet consumption rate.

We first evaluated performances of each blocks in terms of power, area, and delay with optimizes these blocks to satisfy network key parameters, as well as the impact of allocation on overall network performance. Using structural modeling style and parametric Verilog HDL, all blocks are individually implemented, tested and verified. Finally, all individual blocks are combined to implement bi-directional router's architecture as a whole. Here, we vary the number of nodes for performance evaluation.

A multi-synchronous bi-directional router microarchitecture have been implemented in this thesis, is sufficient to provide throughput challenges, interconnect issues, low latency and high bandwidth in the future Globally Asynchronous Locally Synchronous Systems (GALS) system.

In concise, to enhance the performance of on-chip communications of GALS Systems, a dynamic reconfigurable multi-synchronous router architecture is proposed and implemented to increase the NoC efficiency with changing the path of the communication link in the runtime traffic situation. In order to address GALS issues and bandwidth requirements, the proposed multi-synchronous bidirectional NoC's router is developed and it gives reliable higher packet consumption rate, better bandwidth utilization with lower packet delivery latency. All the input/output ports of the proposed router behave as a bi-directional ports and communicate through a novel multi-synchronous first-in first-out (FIFO) buffer. The bidirectional port is controlled by a dynamic channel control module which provides a dynamic reconfigurable channel to the router itself and associated with sub-modules.

This proposed multi-synchronous bidirectional router architecture is synthesized using Xilinx ISE 14.7 and FPGA Virtex 6 family device XC6VLX760 is considered as target technology. The performance of the proposed architecture is evaluated in terms of power, area, and delay.

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Signature