Resum de Tesi Doctoral

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(Mínim 1 i màxim 4, podeu veure els codis a http://doctorat.upc.edu/gestio-academica/impreses/tesi_matricula_i_dipositi/codis_unesco)

Resum de la tesi de 4000 caràcters màxim (si supera els 4000 es tallarà automàticament)

This doctoral thesis approaches the design requirements for future high / ultra-high data rate (from 100 Mbps to 100 Gbps) nanotransceivers (nanoTRx) applied to wireless nanonetworks which imply short/ultra-short distance ranges (3 cm – 3 m). It explores graphene field-effect-transistors (GFET), by simulation against measurement benchmarks, as a potential solution for implementing large-signal high-frequency circuits, by virtue of graphene's one-atom thickness and high carrier-mobility extraordinary properties. Finally, the thesis discusses the challenges faced by GFETs, such as zero-bandgap and high metal-graphene contact-resistance, to be able to propose improvements for achieving the initial proposed goals. Chemical-Vapour-Deposition (CVD) GFET fabrication is considered, which is very promising for large-scale manufacturing (CMOS process compatible), and for that fast-computing large-signal compact modeling for complex circuit design is analysed in depth and optimized, and consequently a set of diverse large-signal static and dynamic GFET circuits are simulated and benchmarked against available measurements assessing the accuracy of the proposed models and deriving scaling prospects. An optimization of the current-to-voltage (I-V) characteristic of a GFET compact model, based upon drift-diffusion carrier transport, is presented. The improved accuracy at the Dirac point extends the model usability for GFETs when scaling parameters such as voltage supply (Vdd), gate length (L), dielectric thickness (tox) and carrier mobility (Ω) for large-signal design exploration in circuits. The model accuracy is demonstrated through parameters fitting to measurements taken from CVD GFETs fabricated in the University of Siegen and Technical University of Milan. The script has been written in a standard behavioural language (Verilog-A), and extensively run in a commercial analog circuit simulator (Cadence environment) demonstrating its robustness. Besides a simple capacitance-to-voltage model (C-V), a small-signal parasitic capacitance model fitted to dynamic measurements for self-aligned CVD GFETs available in the literature is added, enabling to forecast maximum-frequency-of-oscillation (fmax) trends for future scaling. A design-oriented characterization of complementary inverter circuits (INV) based on GFETs is presented as well. Our proposed compact model is benchmarked at the circuit level against another compact model based on a virtual-source approach. Furthermore, a benchmark between simulations and measurements of already fabricated CVD GFET INVs is performed, and performance trends when scaling are derived. The same process is repeated for a more complex circuit, namely GFET ring-oscillators (RO). The transient regime simulations yield performance metrics in terms of oscillation frequency (fosc) and dynamic voltage range (ΦVosc), and consequently, against these metrics, a comprehensive design space exploration covering as input design variables parameters as tox, L, and Vdd is carried out. Being aware of the lack of voltage amplification shown by existing GFETs, the design exploration of a cascode amplifier (CAS) targeted to increase voltage gain (Av) by decreasing its output conductance (go) is presented. GFET CAS are simulated to provide design guidelines, they are accordingly fabricated and consequently measured. Performance metrics are provided in terms of go, transconductance (gm) and hence Av. Against these metrics, a quantitative comparison between CAS and GFETs is performed and conclusions are derived. Finally, conclusions on GFETs suitability for future nanoTRX are elaborated. The derived publications come from international collaborations with the Royal Institute of Technology (KTH) in Sweden from 2012 to 2014, and the University of Siegen in Germany from 2014 to 2016.

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