UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Departament d'Enginyeria Electrònica

MICROELECTRONICS SEMINAR

Departament d'Enginyeria Electrònica **UNIVERSITAT POLITECNICA DE CATALUNYA**

When: Friday, July 11th 2014 HOUR: 12:00

Where: DEE ETSEIB Diagonal, 647 Planta 9 BIBLIOTECA , 08028 BARCELONA

Title: **"Study on reliability and safety of LSIs "**

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ABSTRACT: Aging called NBTI, PBTI and CHC occurs in nanoscale transistors, which is a major factor for degrading the performance of LSIs. Aging decreases operating speed of transistors, and LSI malfunctions by an increased propagation delay. This paper presents a method for estimating the amount of increase in delay time of LSIs and a method for estimating the amount of increase in the threshold value of a transistor from change in the period of two ring oscillators. Effectiveness of the proposed method was verified by circuit simulation. A new flip-flop design, called a duration-observation master-slave flip-flop, is proposed and evaluated.
This dependable design takes into account a noise pulse induced on data signal lines. The proposed master-slave flip-flops monitor the duration time of the input signal when flip-flops change from a master-latch behavior to a slave-latch behavior, and thus they can prevent malfunction caused by the noise pulse.
The effectiveness of proposed design is demonstrated by circuit simulation. The proposed flip-flops are implemented using fewer transistors than that of a duplication structure and the width of the noise pulse to be blocked is adjustable.