UPC-UIB Doctorate Program in
Electronic Engineering

Doctoral Training Seminars:

Research Projects in Electronics at UPC

Track - Industrial and Power Electronics

Research samples by the Power Electronics Research Group (GREP)

Outline

- Vision
- MAC converter
- Activity in SiC
- Control of multilevel back-to-back converters

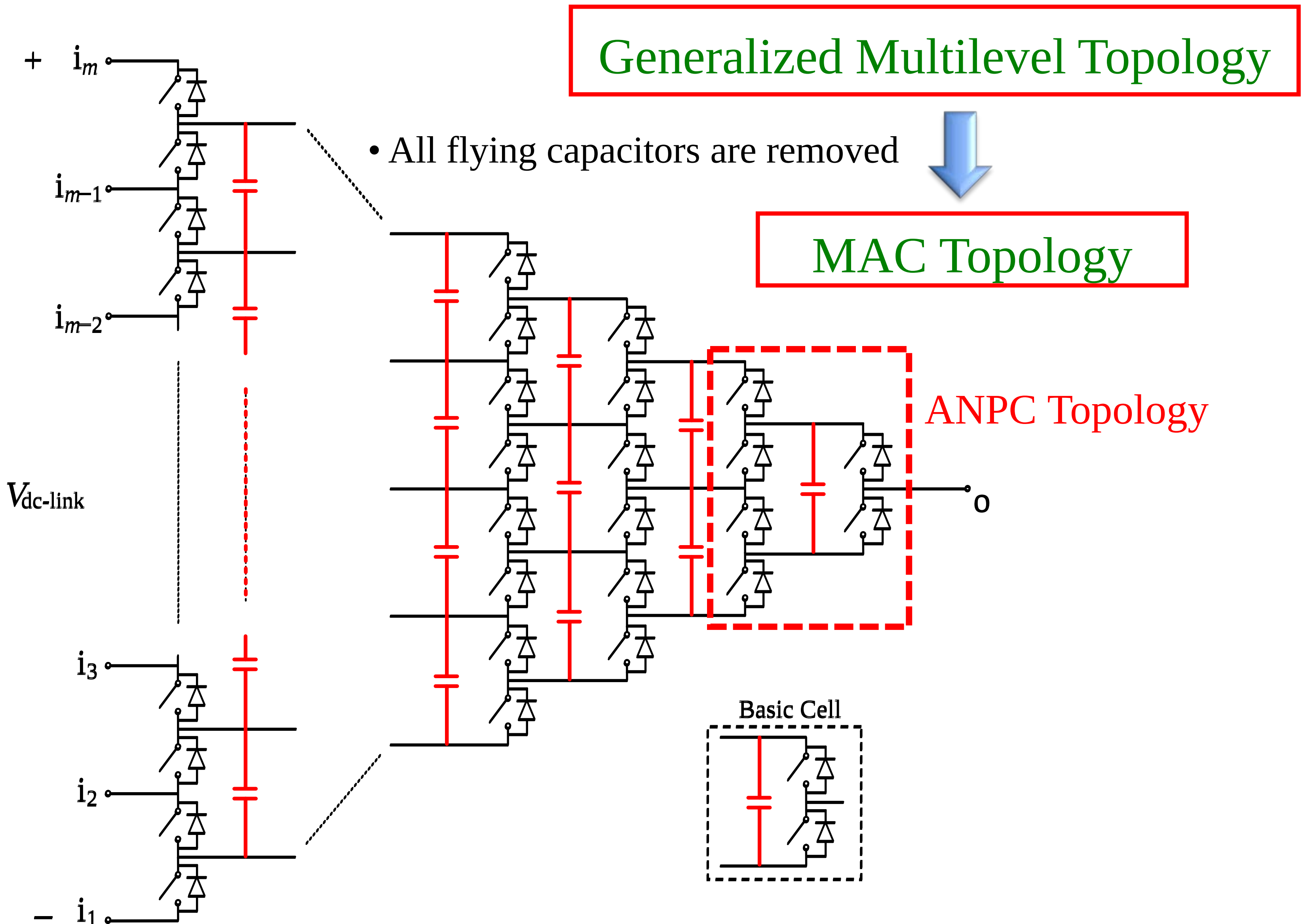
Vision

- Research focused to **multilevel** power electronics converters:
  - Topologies.
  - Modulation.
  - Control.
- Applications in:
  - Renewable energy conversion.
  - Electric and hybrid vehicles technology.
  - Industry applications.

Outline

- Vision
- **MAC converter**
- Activity in SiC
- Control of multilevel back-to-back converters

Multilevel Active Clamped (MAC) Topology



Operating Principle

Conduction losses are reduced

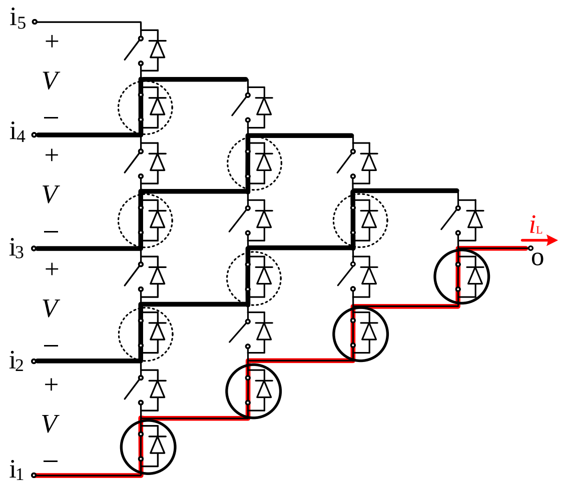
Fault-tolerance

Blocking Voltage = V

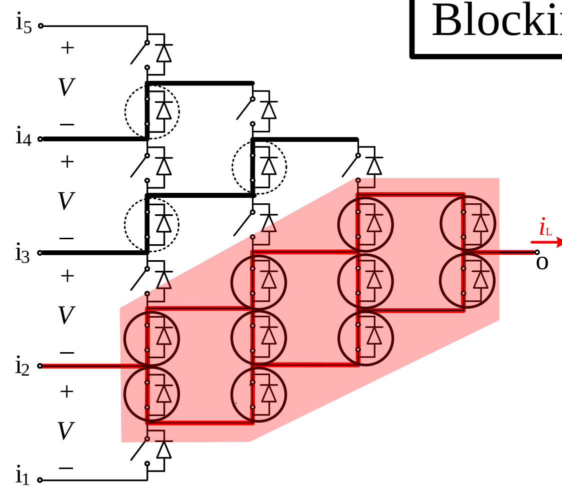
5-level leg

5 devices change their state

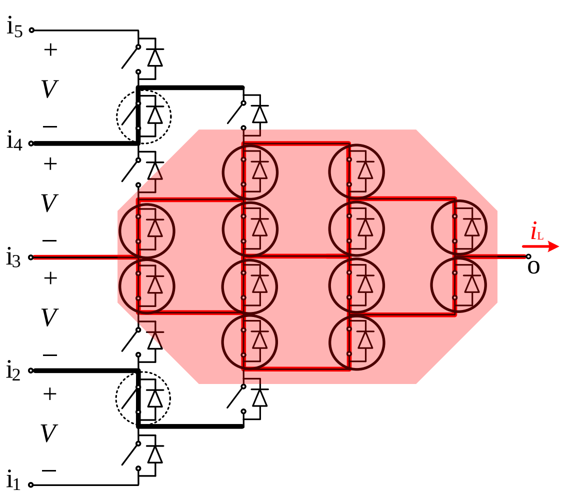
Switching losses concentrate on one device



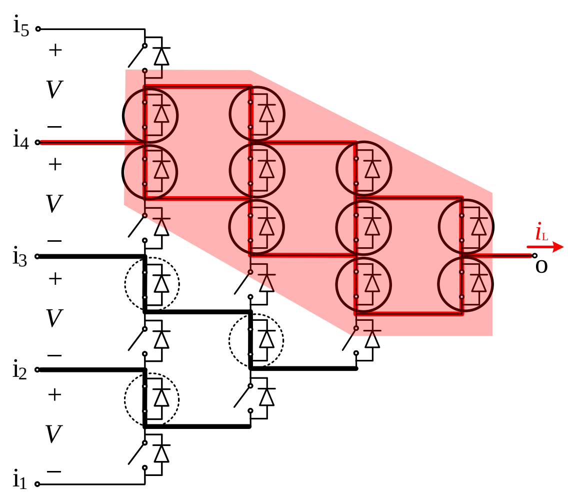
SS1: Connection to node i_1



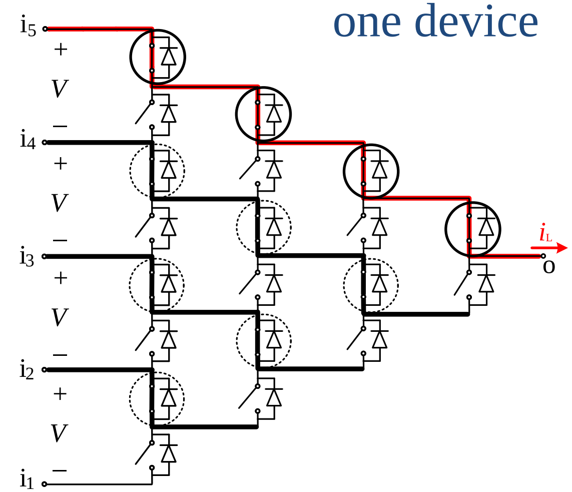
SS2: Connection to node i_2



SS3: Connection to node i_3



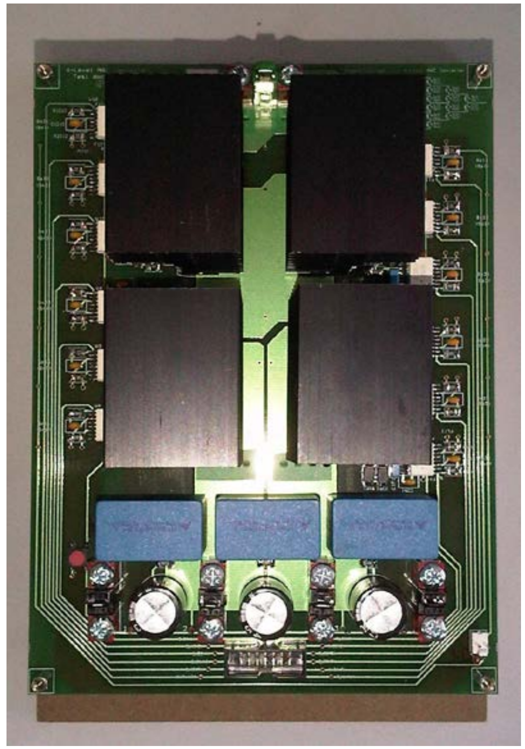
SS4: Connection to node i_4

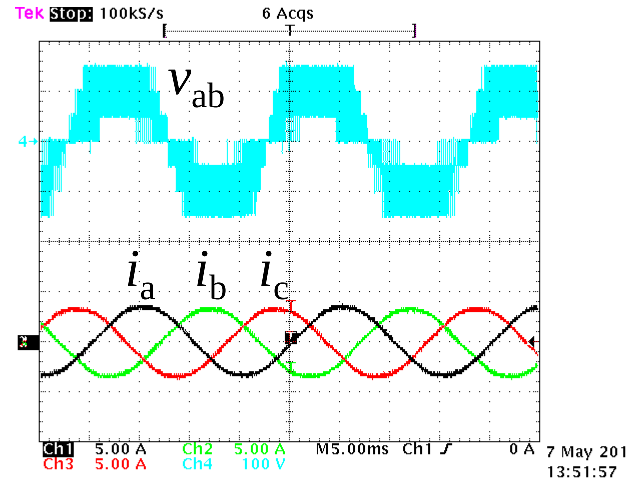


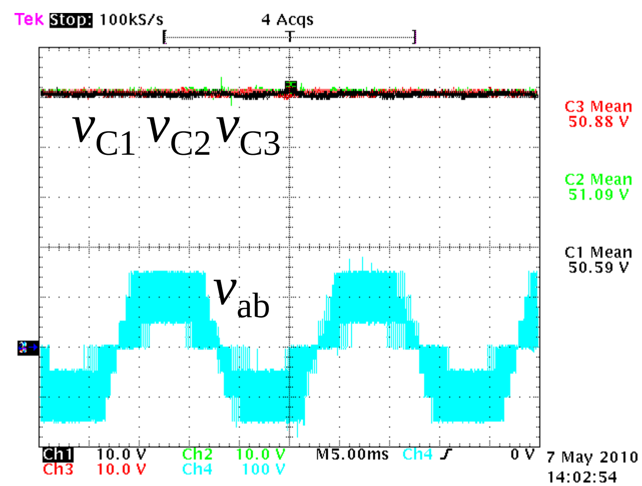
SS5: Connection to node i_5

Experimental Results

Four-Level Three-Phase Prototype





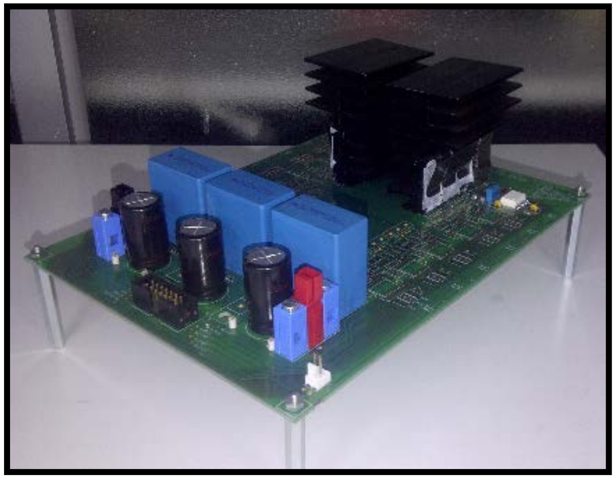


$m = 0.75$, $V_{\mathrm{dclink}} = 150$ V, $f_o = 50$ Hz, $f_s = 5$ kHz,
$C = 155$ μF, $R_L = 16.5$ Ω, and $L_L = 15$ mH

Experimental comparison under a simple operating mode

Main objective

Compare the efficiency of the MAC converter with a two-level converter in low voltage



2-level converter

4-level MAC converter

Experimental comparison under a simple operating mode

Methodology

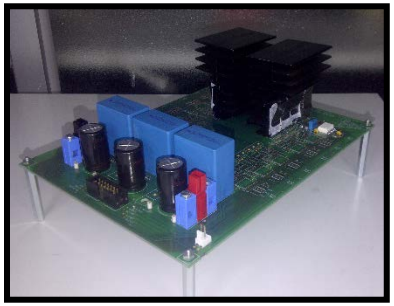
1) Estimation of Total Losses and Efficiency

Loss models

- Conduction losses.
- Switching losses (experimentally).
- Gate-driver losses.
- Other losses.

2) Experimental Tests to Measure Losses and Efficiency

- Measure input and output power.



2-level

4-level MAC

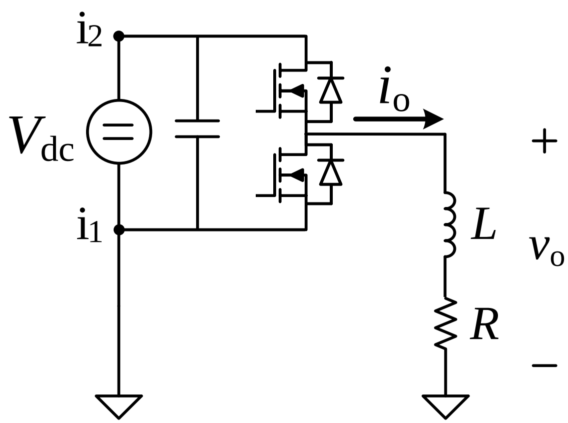
Comparison of both results

Validation of Loss Models

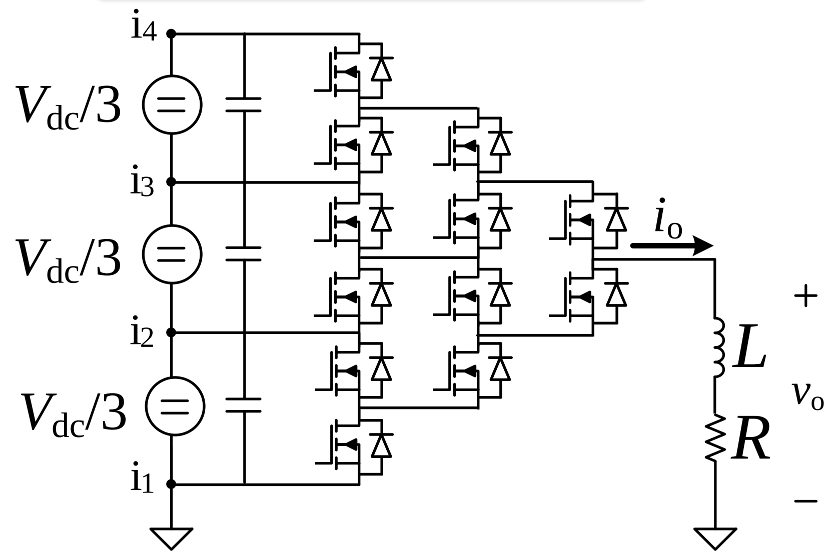
Experimental comparison under a simple operating mode

Efficiency Comparison Scenario

Two-level leg

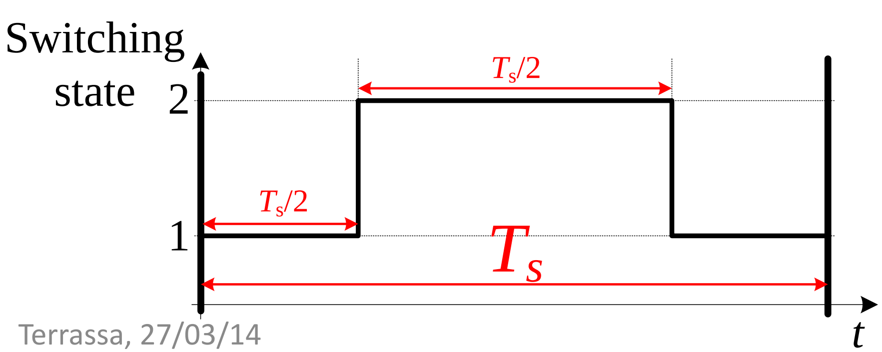


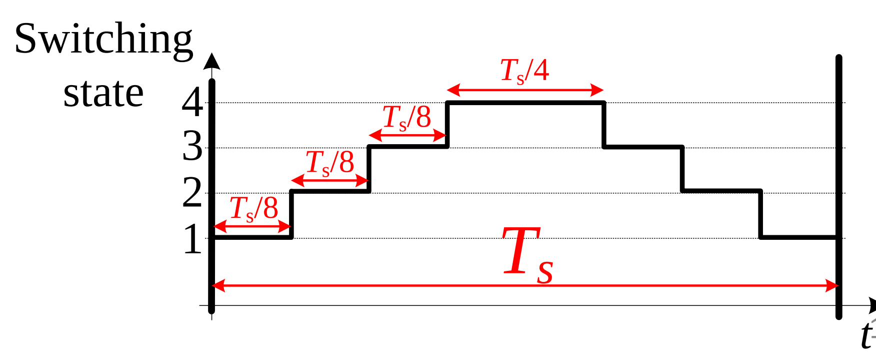
Four-level MAC leg



Buck dc-dc converters

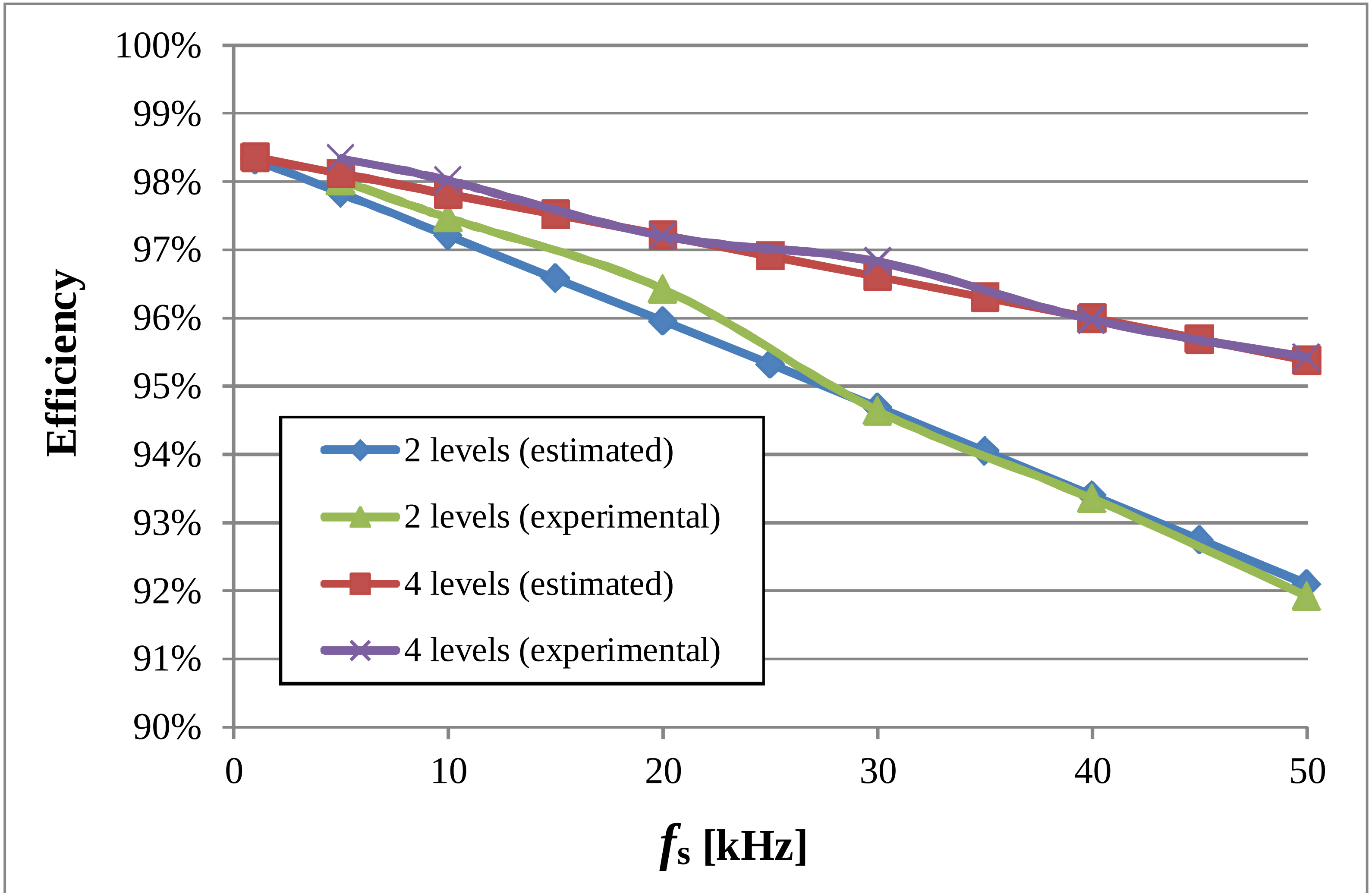
Output current constant





Experimental comparison under a simple operating mode

Analytical and experimental results



Conditions

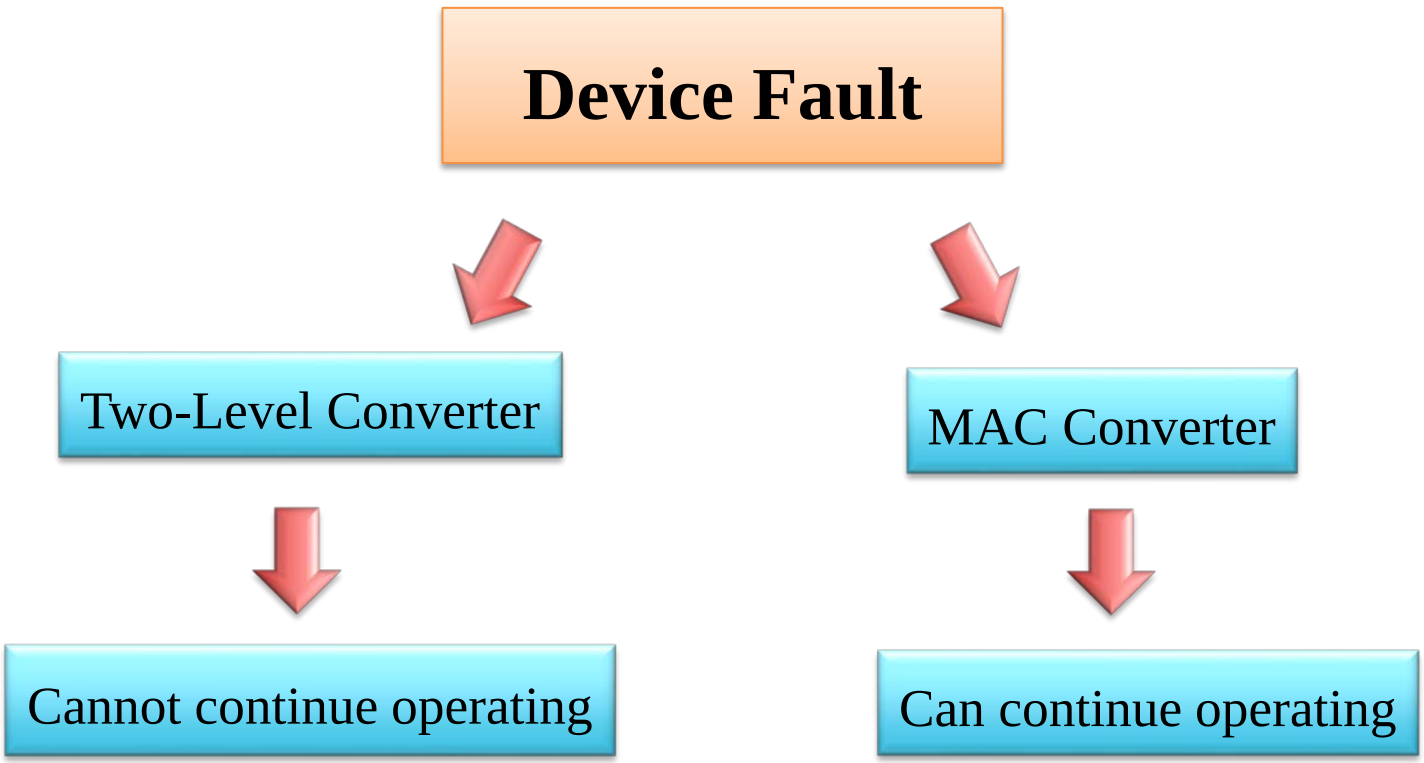
V_{dc} = 150 V

L = 60 mH

R = 16 Ω

Fault-Tolerance Analysis of the MAC converter

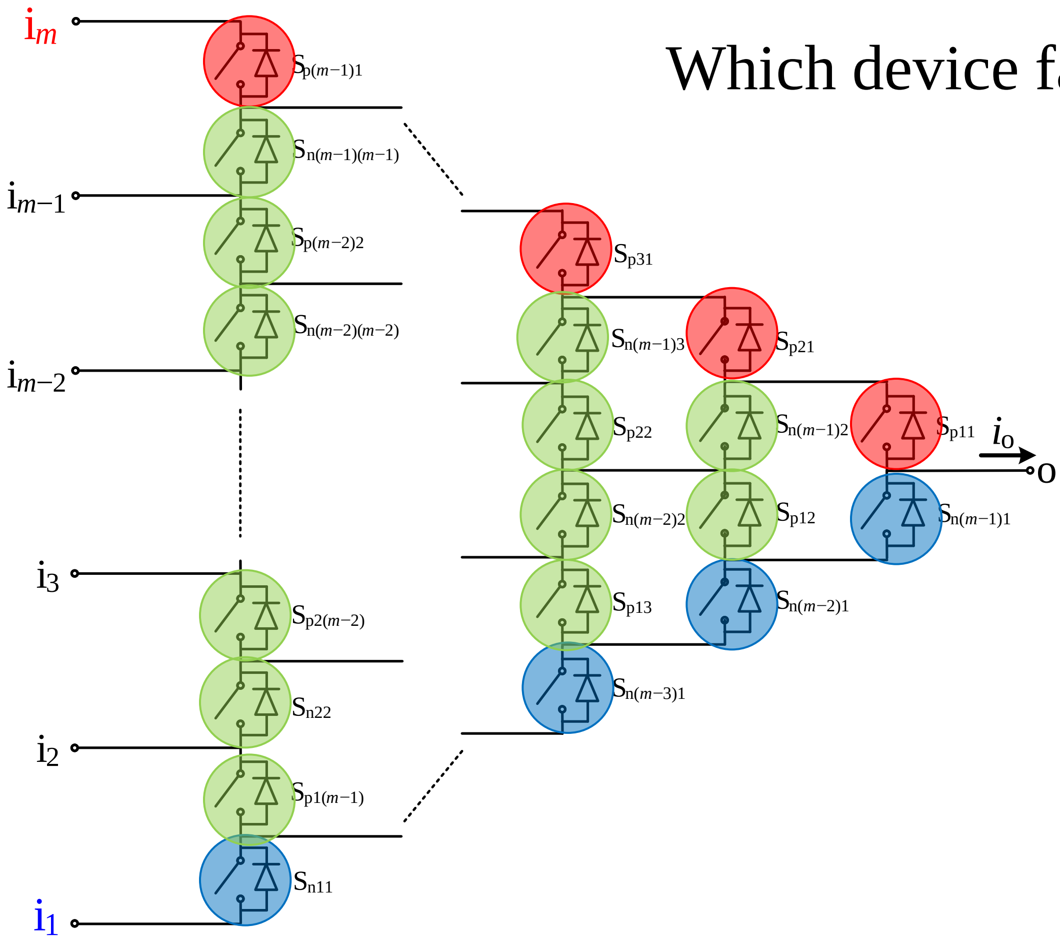
Motivation



Fault-Tolerance under Open-Circuit Faults

Open-circuit critical diagonals in an *m*-level leg

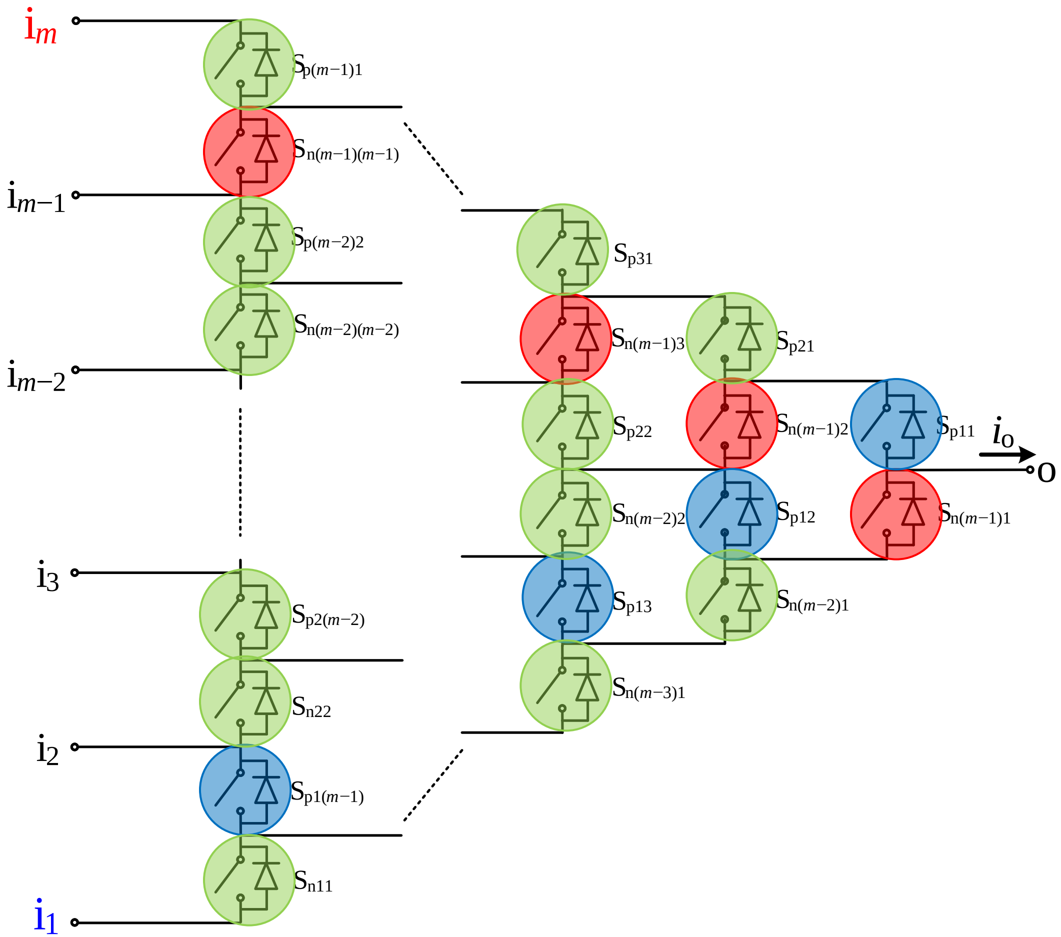
Which device faults imply to loose a level?



- Level *m* is lost
- Level 1 is lost
- No levels are lost

Fault-Tolerance under Short-Circuit Faults

Short-circuit critical diagonals in an *m*-level leg

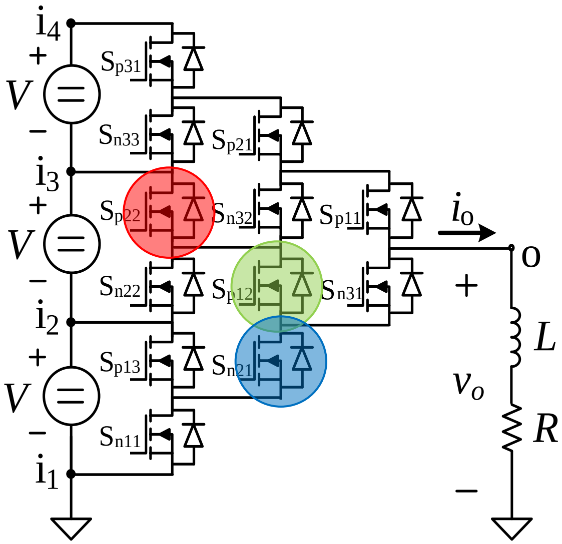


Which device faults imply to loose a level?

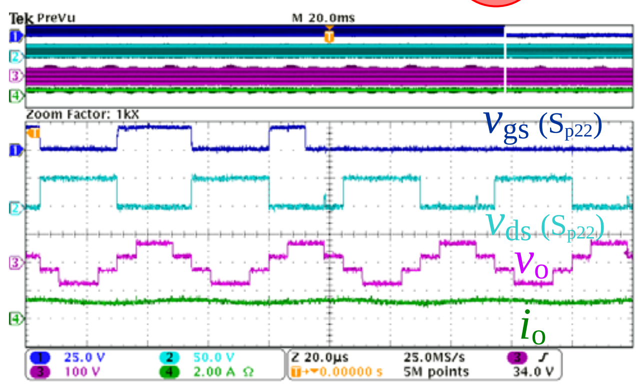
- Level *m* is lost
- Level 1 is lost
- New switching states can be defined to avoid losing levels, but the blocking voltage of some devices is increased.

Experimental Results

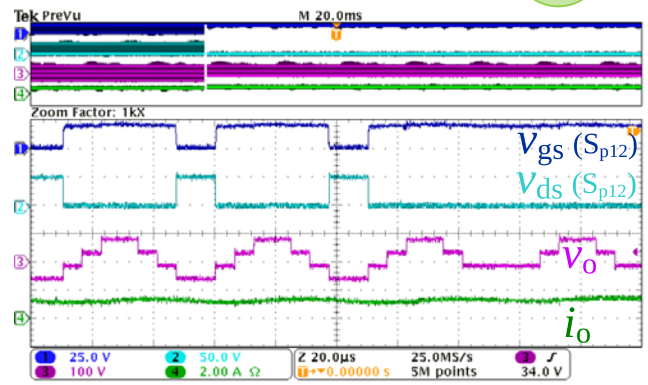
Emulation of short-circuit and open-circuit faults



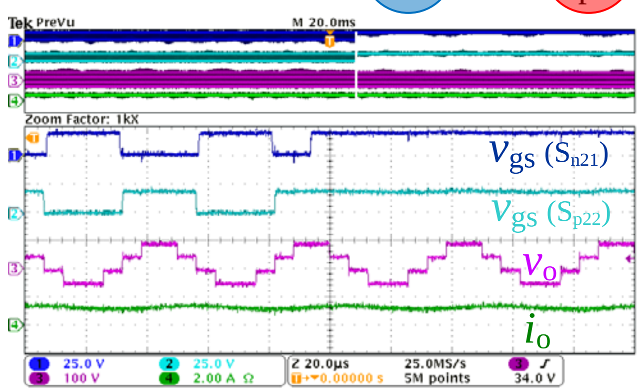
Emulation of a open-circuit fault in device S_{p22}.



Emulation of an short-circuit fault in device S_{p12}.



Emulation of a short-circuit fault in devices S_{n21} and S_{p22}



V=50 V
L=5 mH
R=33 Ω
f_S=20 kHz

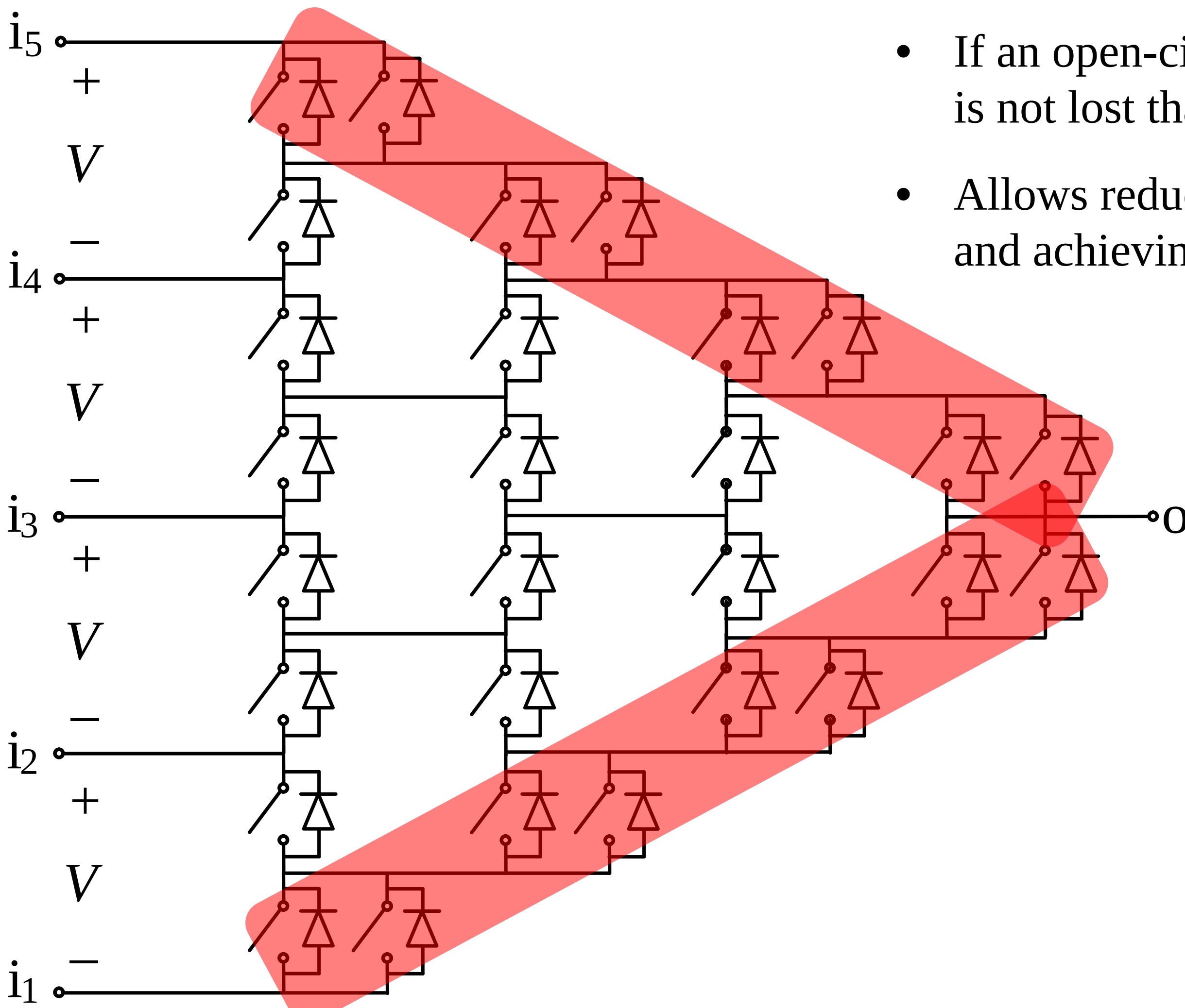
MAC Hardware Modifications

Solutions to improved the Fault-Tolerance Capacity

- Solution I: Parallelization of open-circuit critical diagonals.
- Solution II: Inclusion of two additional devices at input terminals i_2 and i_{m-1}.
- Solution III: Inclusion of one additional device at every input terminal

Hardware Modifications

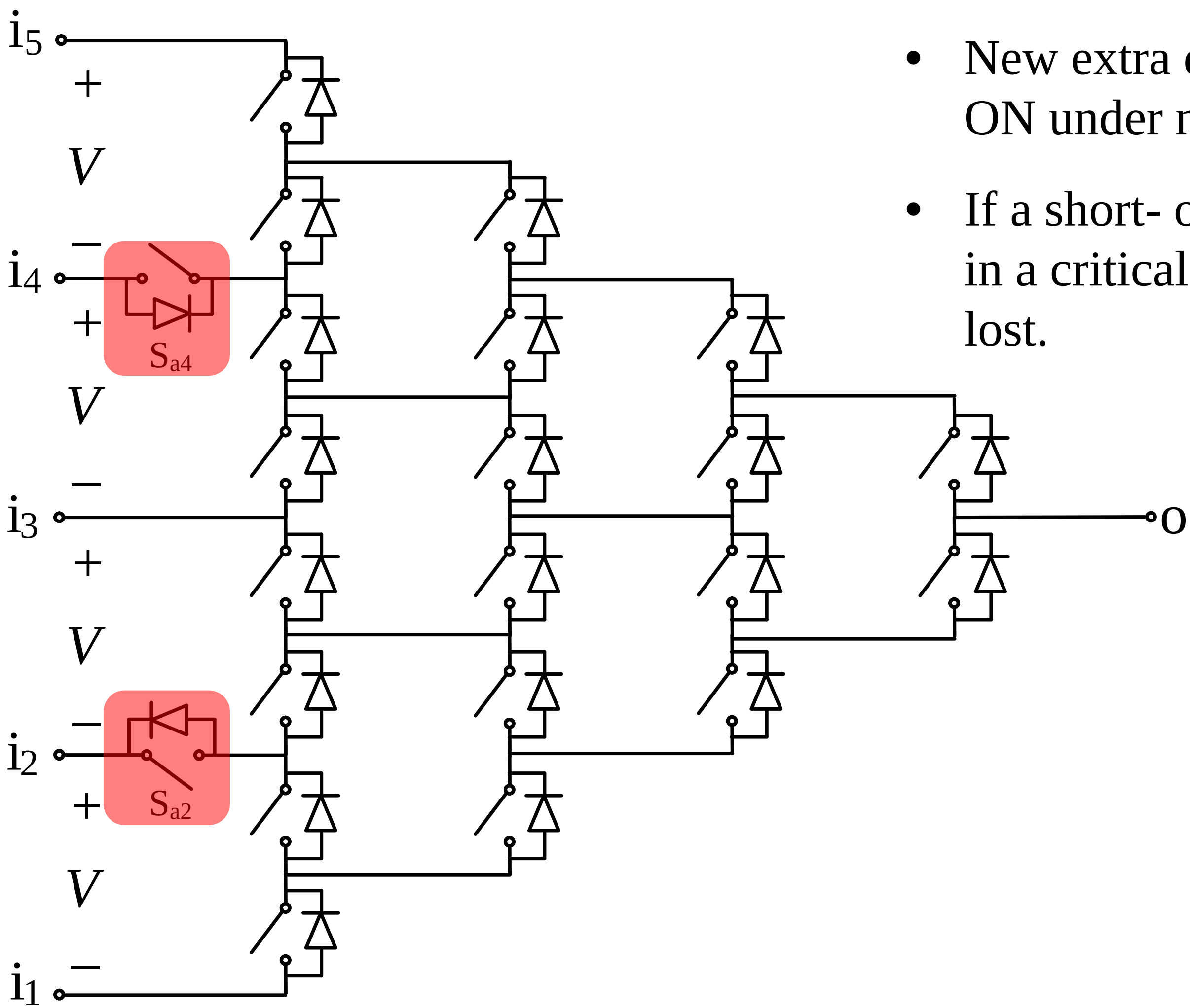
Solution I. Parallelization of open-circuit critical diagonals



- If an open-circuit fault occurs, the level is not lost thanks to the parallel device.
- Allows reducing the conduction losses and achieving a better loss distribution.

Hardware Modifications

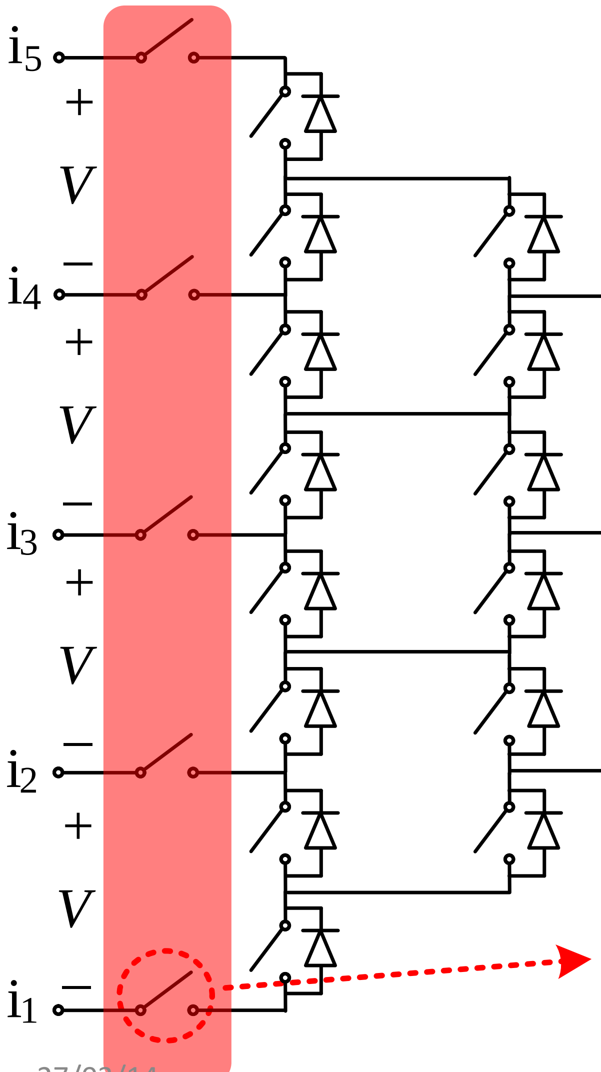
Solution II: Inclusion of two additional devices at input terminals i_2 and i_{m-1}



- New extra devices are permanently ON under normal operation.
- If a short- or open-circuit fault occurs in a critical diagonal, the levels are not lost.

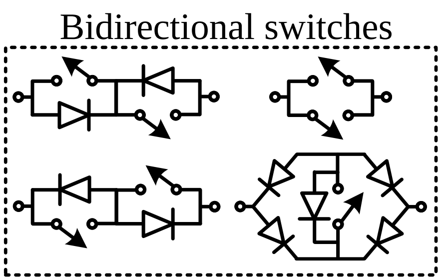
Hardware Modifications

Solution III: Inclusion of one additional device at every input terminal



- New extra devices are permanently ON under normal operation.
- All levels available under any number of simultaneous short-circuit faults using the original switching states.
- Under open-circuit faults, no advantages compared to Solution II.

Conduction losses are highly increased

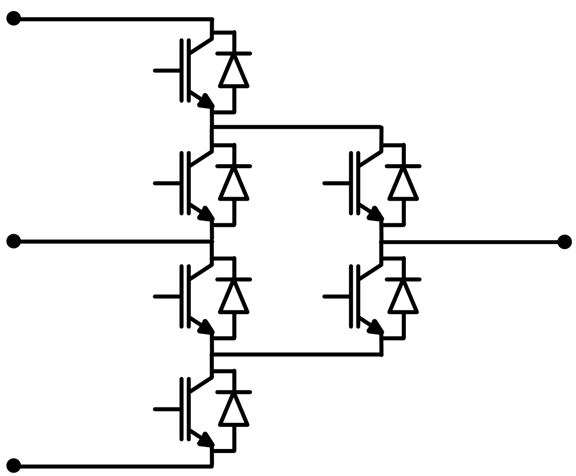


Outline

- Vision
- MAC converter
- **Activity in SiC**
- Control of multilevel back-to-back converters

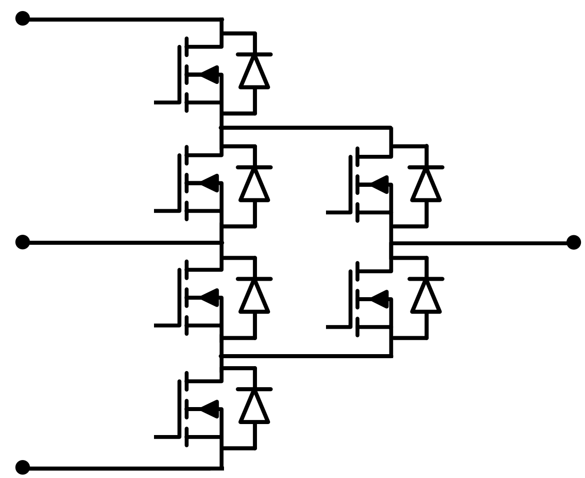
GREP - Work Objective in SiC

Efficiency comparison



ANPC built upon
1200 V Si IGBTs + Si diodes

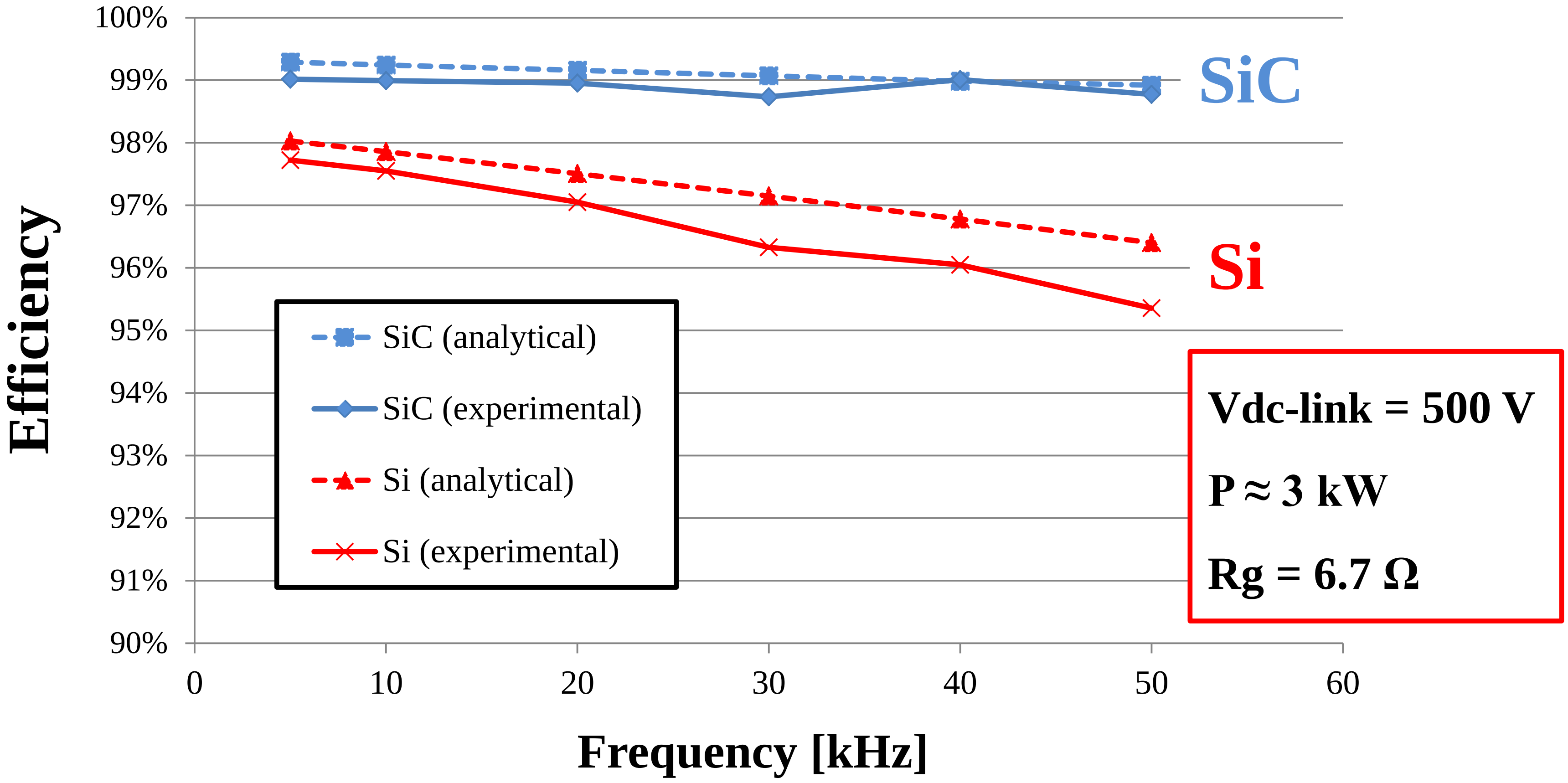
Device IRG7PH30K10PbF + diode DSEI 30
Driver IXYS IXDN609



ANPC built upon
1200 V SiC MOSFETs + SiC diodes

Device Cree C2M0080120D + diode C4D20120D
Driver IXYS IXDN609

Efficiency Results



Outline

- Vision
- MAC converter
- Activity in SiC
- **Control of multilevel back-to-back converters**

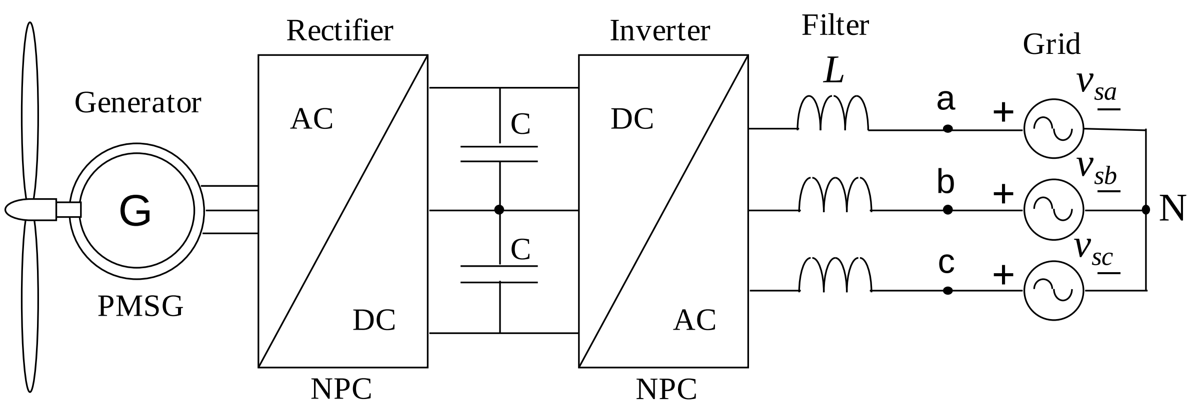
Introduction: wind generation system

Trends in wind power generation point to increase power and voltage:

- Multilevel converters well suited
- Full power converter to achieve complete system control

Wind power generation variable speed system:

Permanent magnet synchronous generator + back-to-back NPC



Advantages:

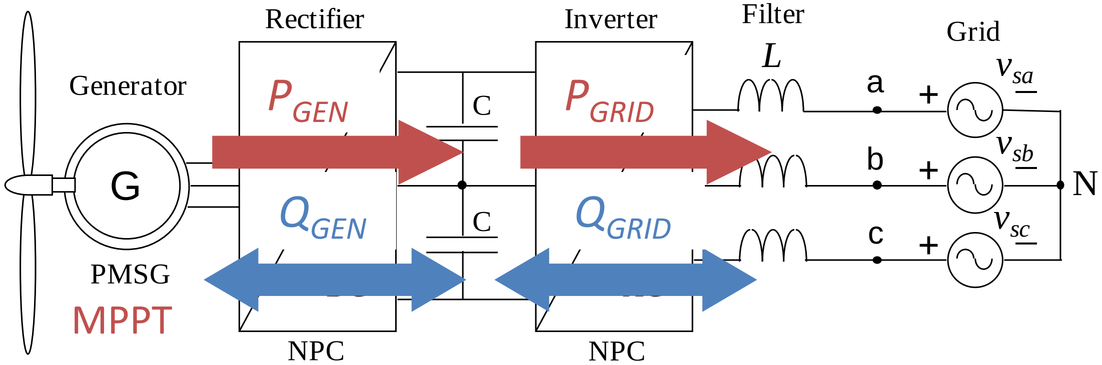
- Optimum power control
- 100% speed variability
- Without Gearbox

Drawbacks:

- Converter size
- Generator size and weight
- Expensive

Motivation

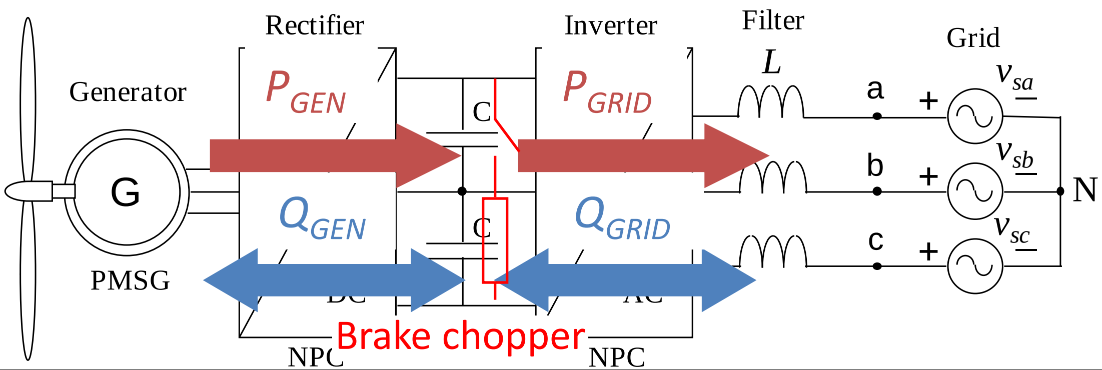
Steady-state operation (or "normal" operation):



P_{GRID}=P_{GEN}

P_{GEN} given by the MPPT

Operation under grid fault condition (to meet LVRT requirements)



P_{GEN} given by the MPPT

P_{GRID} , Q_{GRID} set by the GCR

$P_{GEN} > P_{GRID}$

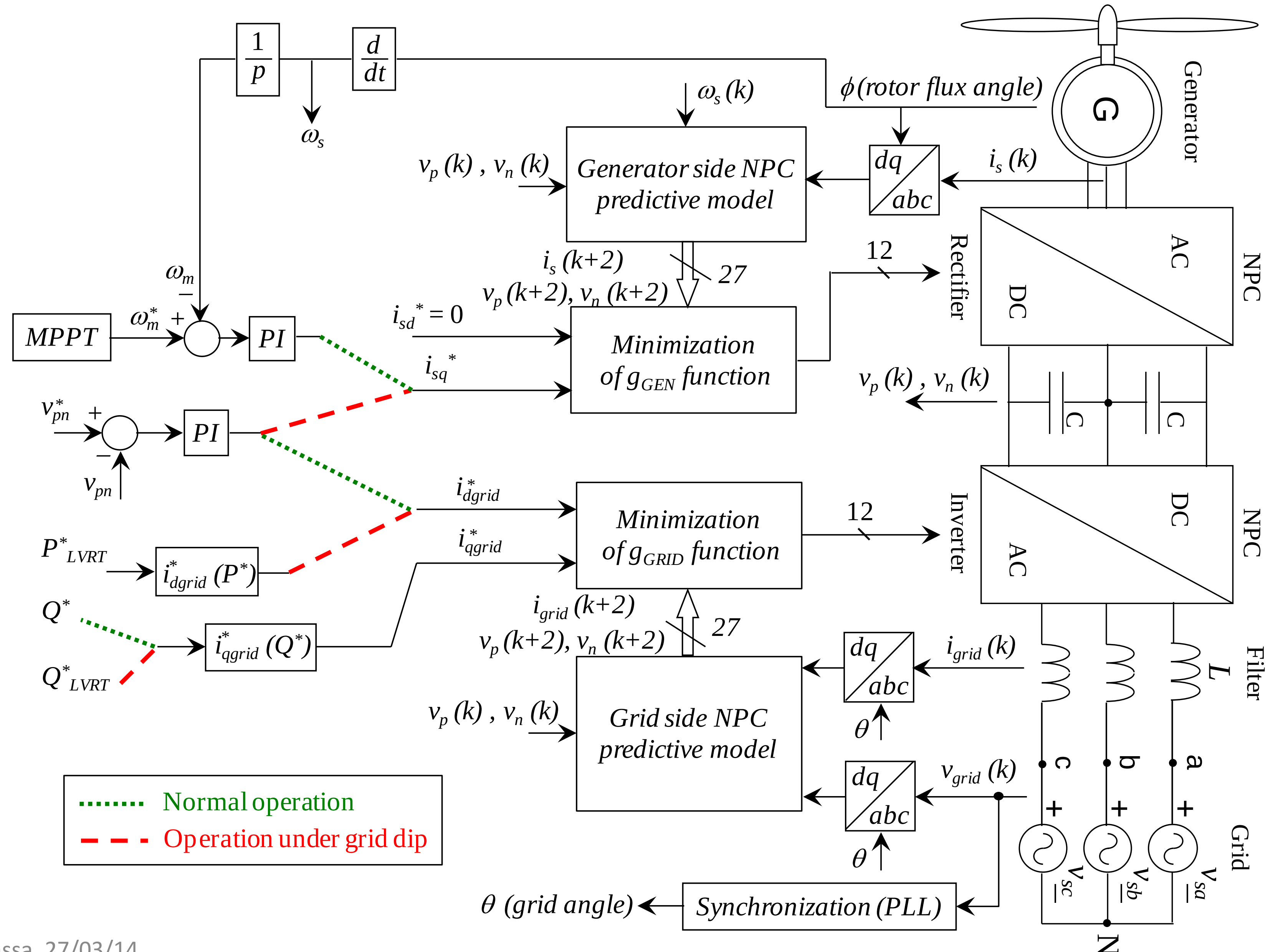
Active power surplus

under grid fault

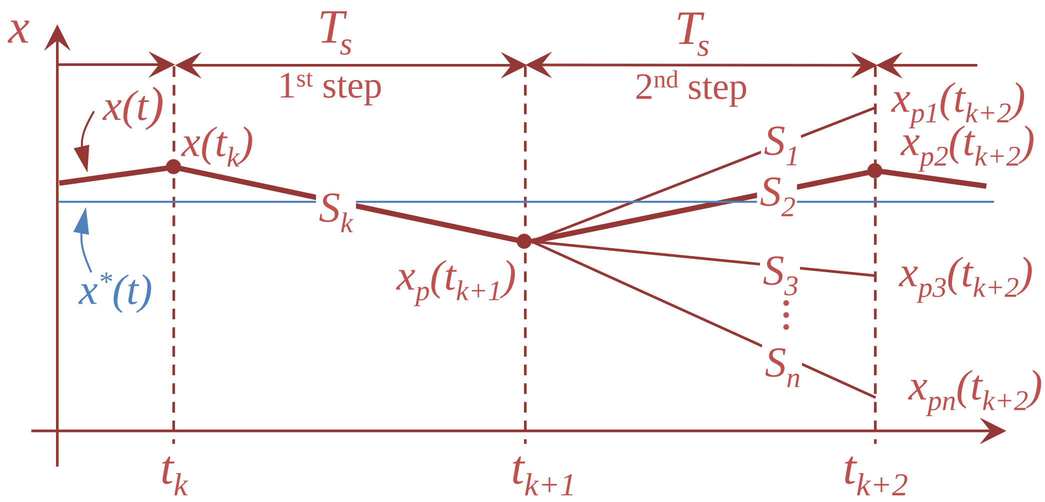
Motivation:

- Minimize the use of the dc-link brake chopper by storing energy in the rotor inertia.
- Predictive current control applied to both converters and dc-link balance control.

Proposed control block diagram



Predictive control method



- Measure variables at t_k: $x(t_k)$
- Apply the switching state S_k during the 1st step
- Calculate the predicted value $x_p(t_{k+1})$ at t_{k+1} with $x(t_k)$ and the current switching state S_k by using the discrete model
- Calculate the predicted value $x_{pi}(t_{k+2})$ at t_{k+2} for all the possible switching states, with $x_p(t_{k+1})$ by using the discrete model
- Evaluate the quality function g for all the predicted values $x_{pi}(t_{k+2})$ at t_{k+2}
- The switching state that minimizes g is selected and applied during the 2nd step

Simulation results

PMSG data: J = 0.0812 kg·m^2 ; L_s = 10 mH ; R_s = 0.5 Ω ; ψ_r = 0.382 Wb ; p = 4

Dc-link data: C = 2200 μF ; V_{pn} = 250 V

Grid-side data: L = 10 mH ; R_L = 0.1 Ω ; V_{GRID} = 72 V_{RMS} ; f = 50 Hz

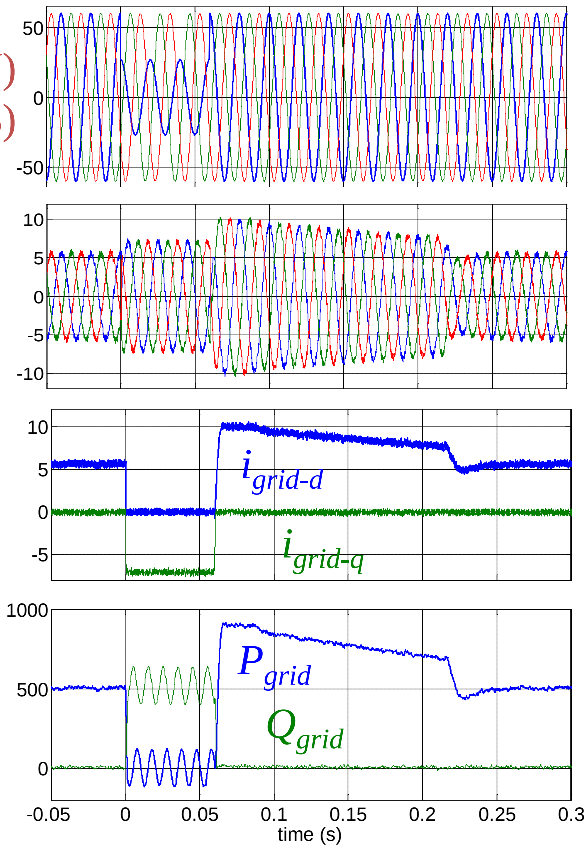
Grid side

Grid voltages (V) (V_a drops 55%)

Grid abc currents (A)

Grid dq currents (A)

P and Q grid power (W, VAR)



Generator side

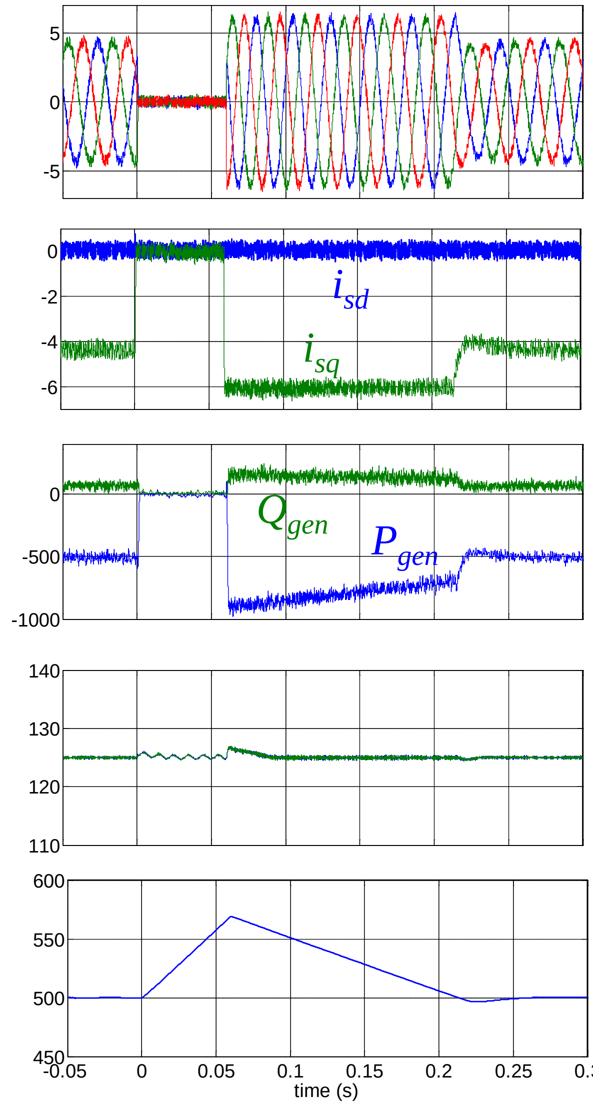
Generator abc currents (A)

Generator dq currents (A)

P and Q generator power (W, VAR)

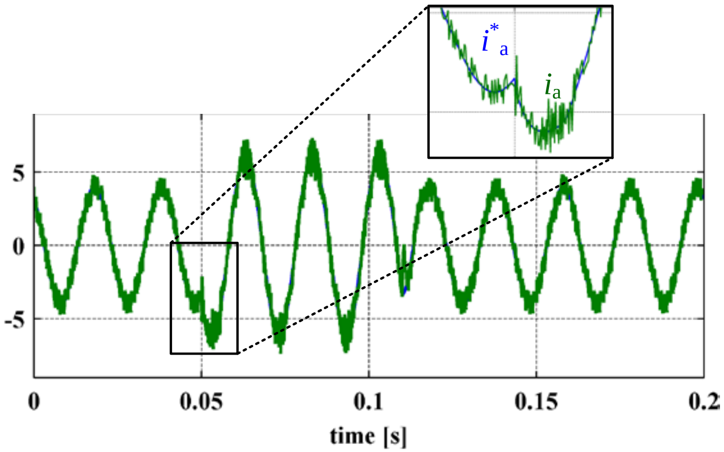
Dc-link capacitor voltages (V)

Shaft speed (rpm)

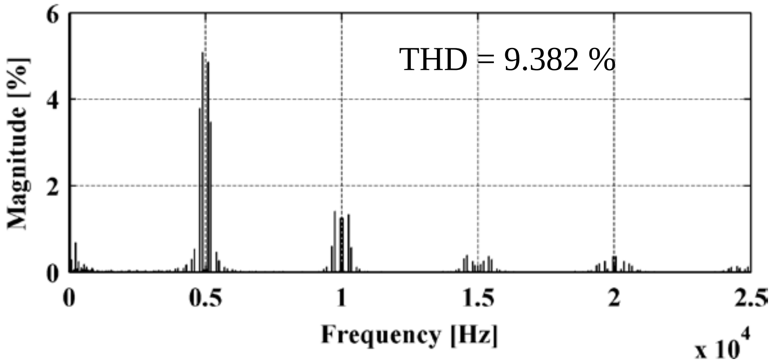


Simulation results

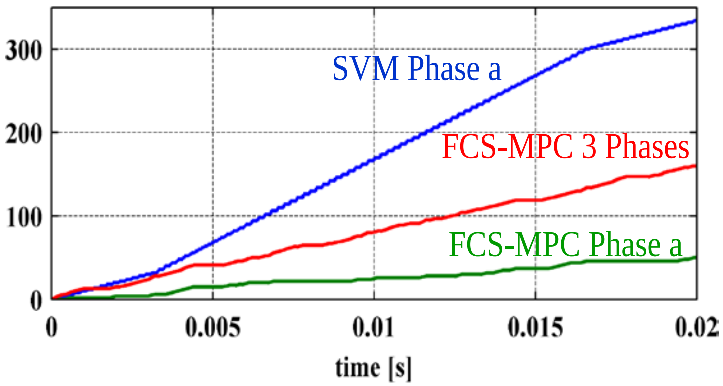
Current reference tracking



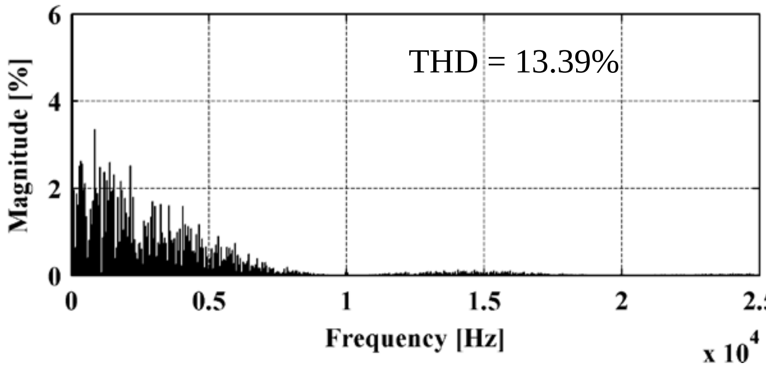
Phase *a* load current spectrum for SVM



Number of commutations

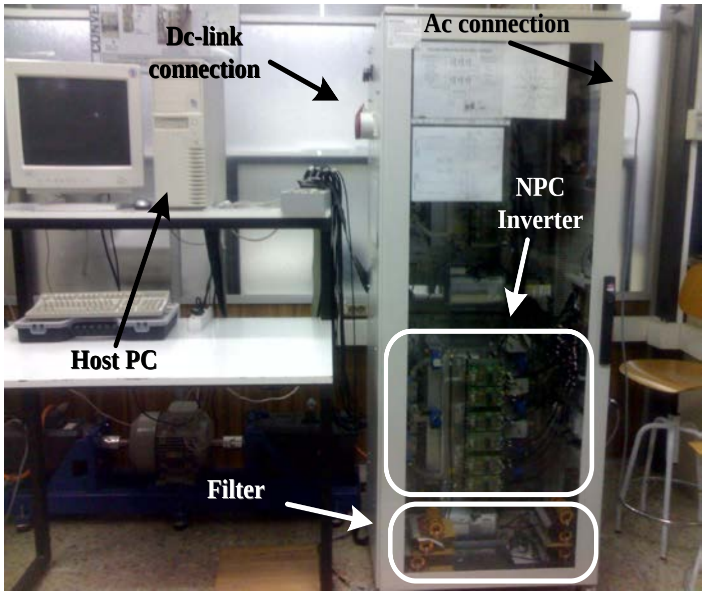


Phase *a* load current spectrum for predictive control



Experimental results: Grid side converter

Experimental setup overview



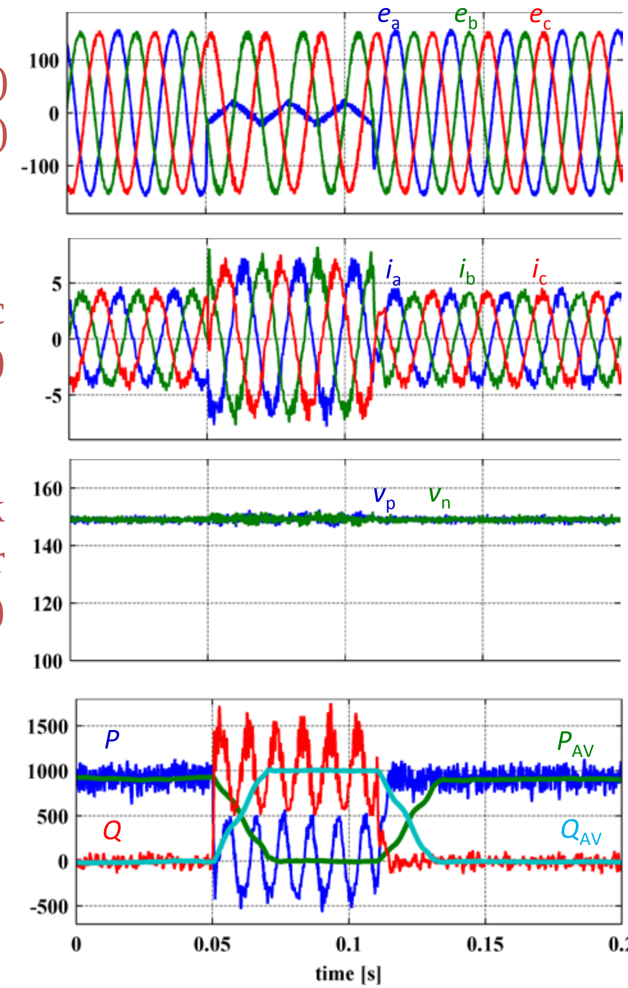
V_{pn} = 300 V ; C = 2.2 mF ; L = 5.5 mH ; R = 0.5 Ω ; V_{grid} = 152 V_{RMS} ; f_{grid} = 50 Hz ; T_s = 100 µs.

Grid voltages (V)
(V_a drops 90%)

Grid abc currents (A)

Dc-link capacitor voltages (V)

P and Q grid power (W, VAR)



Conclusions

- PMSG + back-to-back NPC applied to wind generation
  - no gearbox, 100% speed variability, well suited for high voltage/power
- Low Voltage Ride-Through compliance
  - Slow generator-side power regulation due to the mechanics
  - Fast grid-side power regulation
  - Active power excess during the dip must be dissipated/stored
  - Dc-link brake chopper allows power excess dissipation
- Proposed control approach:
  - Active power excess is stored in the rotor inertia
  - Dc-link brake chopper activation can be avoided if the rotor speed is below the limit (cut-off speed)
  - Pitch control should work concurrently to reduce rapidly the generated active power
  - Predictive converter current control allows reduced number of converter commutations with same performance as conventional control

Thanks for your attention!!!