BASIC INFO ON TIEG

11 PhD Prof.+ 3 Senior Prof + 3 PhD Students

SGR 2014 EMC en CI

SGR 2014 TIEG Power + EMC en CI

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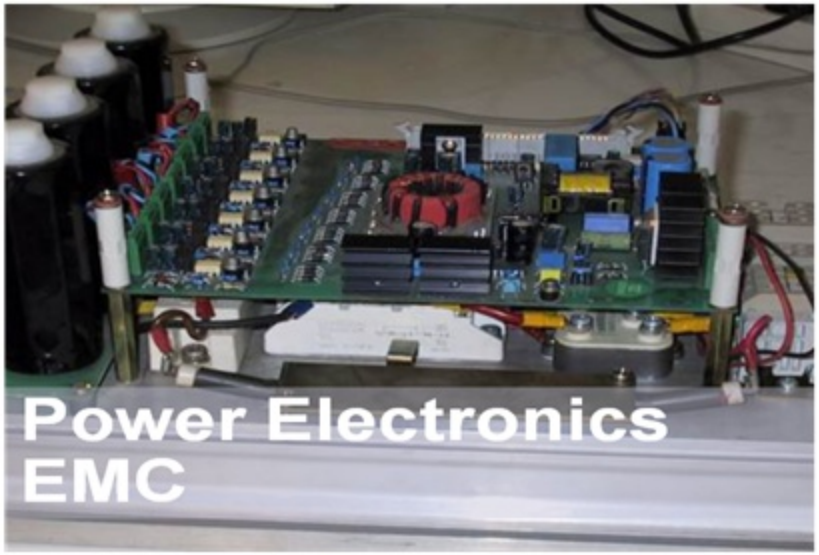
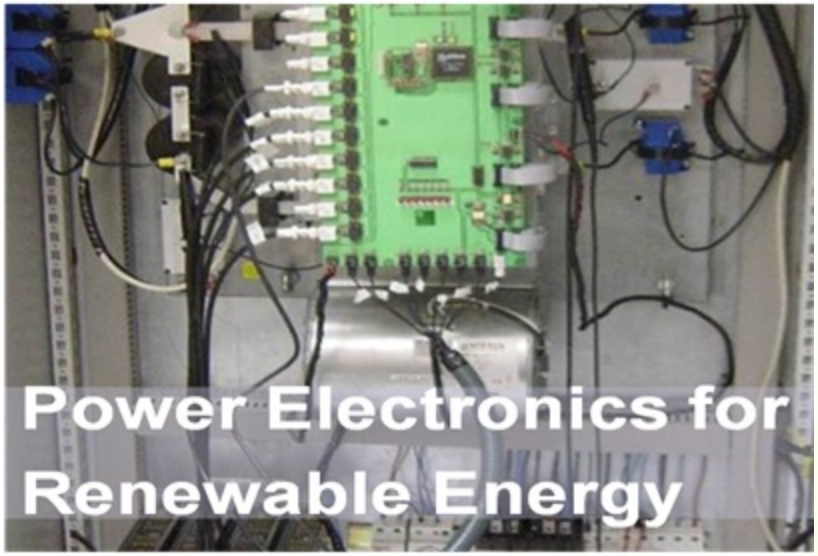
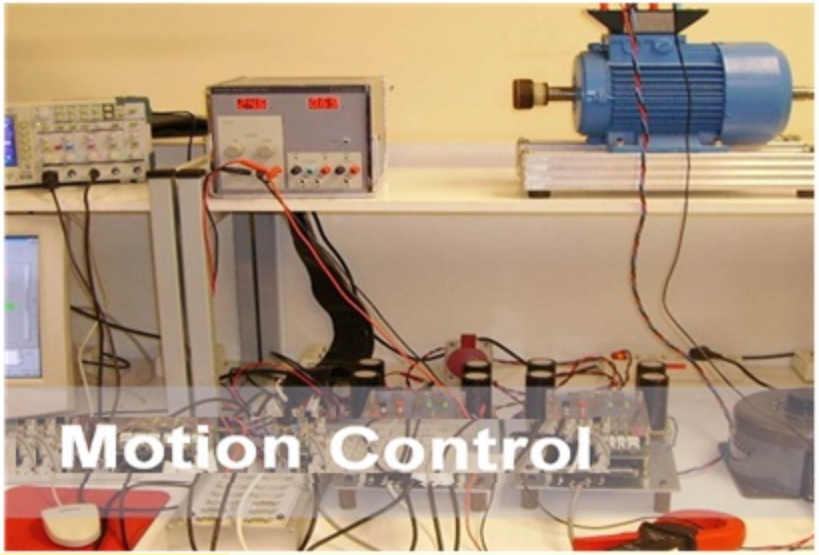
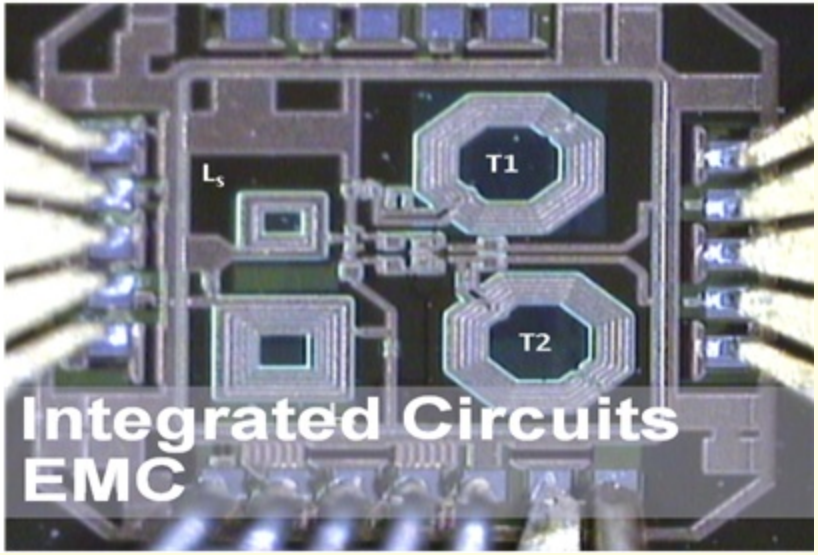
Research Topics









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FIGURES (last 5 years)

- 63 papers in JCR journals
- 183 papers in international conferences
- 12 PhD Thesis
- 2 Books
- 5 Book Chapters
- 5 Public funded projects
- 8 Private funded projects
- 3 Patents

Contact: josep.balcells@upc.edu

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Facilities & Singular Equipment

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UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

TIEG-UPC
Terrassa Industrial Electronics Group

CONSOLIDER -INGENIO 2010
RUE

Advanced Wide Band Gap Semiconductor Devices for Rational Use of Energy (RUE)

WP3:Proof of concept

- EMI behaviour comparison of Si vs. SiC MOS Switches
- MMC and Matrix converters based on SiC

Group TIEG - UPC

J. Balcells, J. Zaragoza,

17 Marzo 2014

Why SiC and GaN semiconductors? (WBG)

- Si devices are limited to operation at junction temperatures lower than 150ºC to 200 ºC.
- Si power devices are not suitable at very high frequencies.
- SiC and GaN offer the potential to overcome both the temperature, frequency and power management limitations of Si.
- SiC&GaN process technologies are more “mature”
- At present, SiC shows the best trade-off between properties and commercial maturity.

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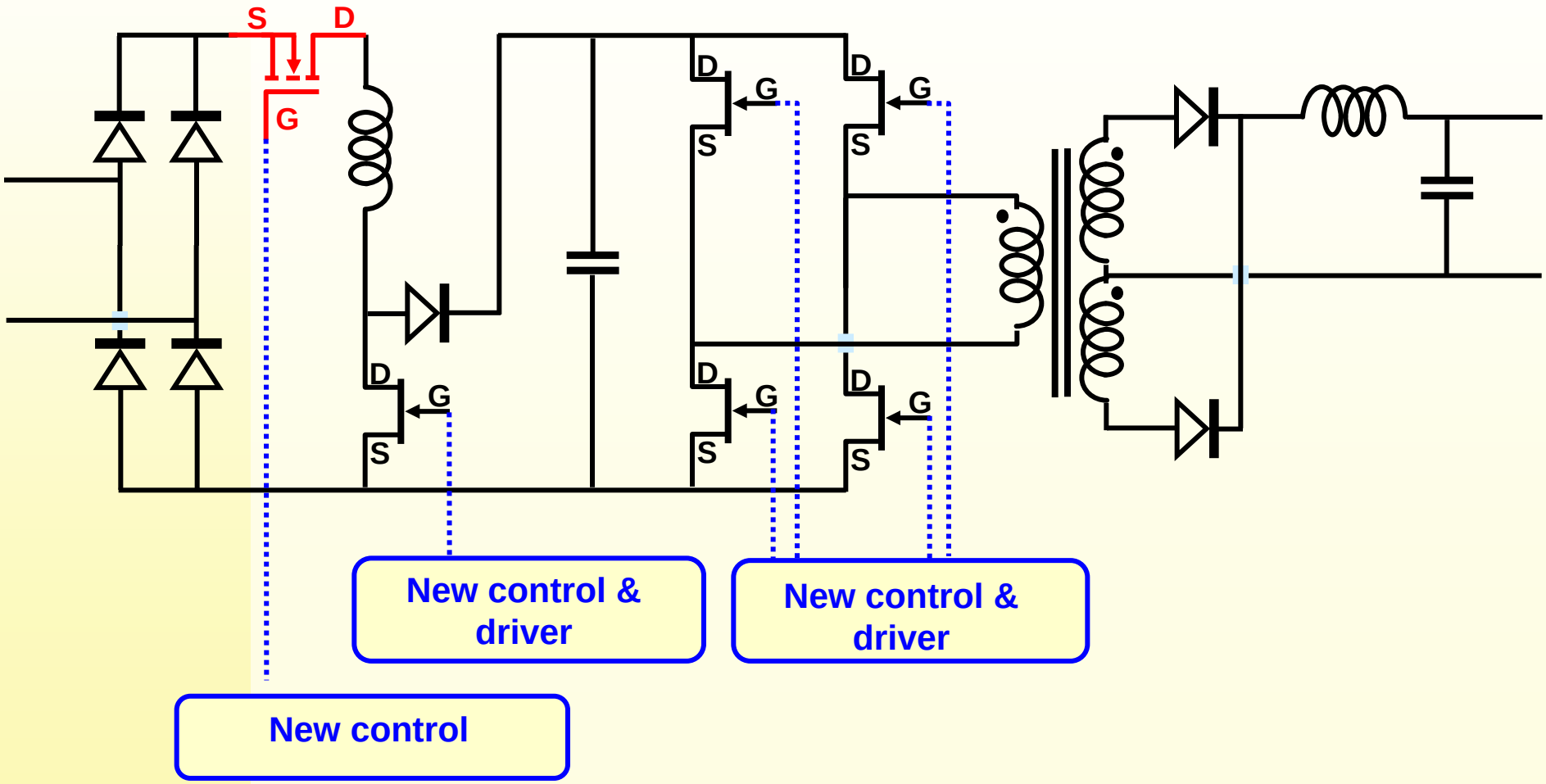
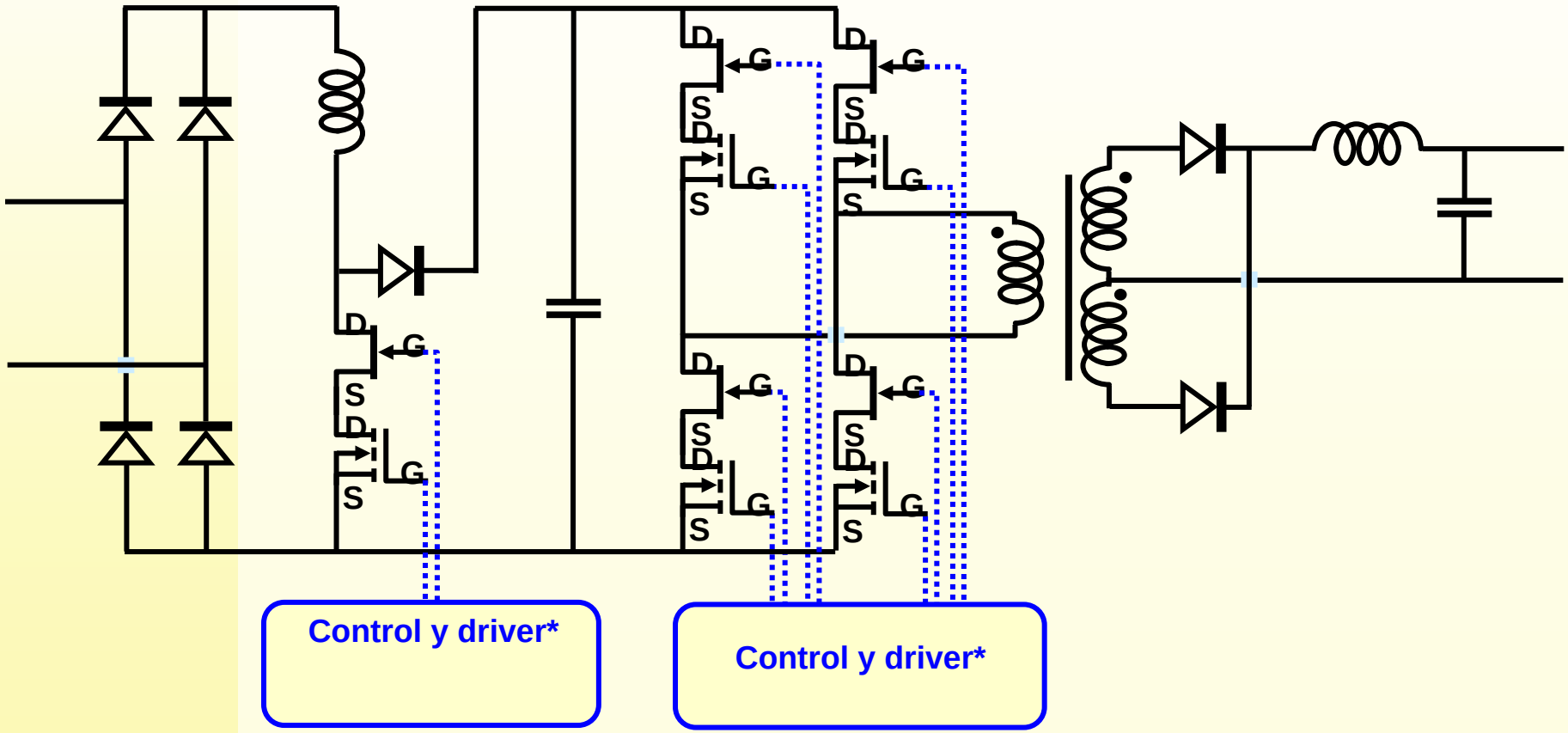
SiC new topologies

- *Use of normally closed devices. Requires new topologies*
- *Need of new drivers and controllers*

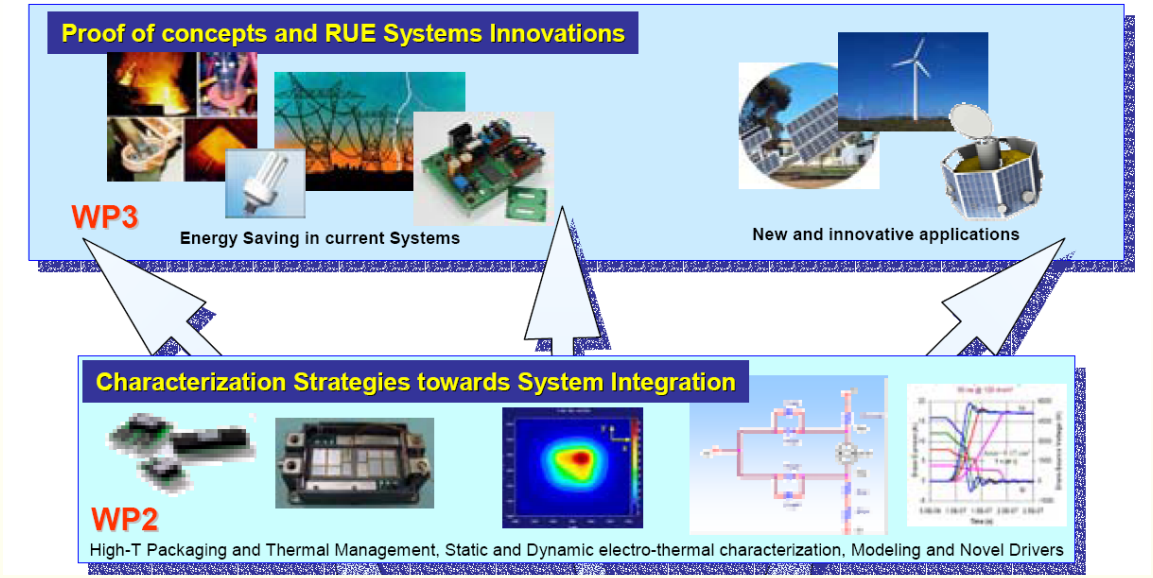


SiC new topologies: Cascode

- ***Cascode is another alternative, but temperature advantages are lost if packed in a single package***



TIEG Tasks in the concept proof



TIEG Group is involved in WP3 (Proof of Concept)

Activity of TIEG is concentrated on:

- EMI tests using different drivers and driver to MOS coupling circuits
- Comparative tests of SiC vs Si on MMC converters

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EMI Task

- Comparison of EMI generated by a boost converter using SiC MOS FET (CMF20120) and Si Diode (STTH30R06CW), when using different driver/coupling circuits to drive MOS-FET gate.
- The basic driver circuit was an IXYS IXDN609SI
- Parameters changed were:

A. Gate negative bias voltage (tests with -2V and -5V)

B. Driver to Gate coupling series resistance: Different values tested: R=(0 Ω, 5 Ω, 10 Ω and 15Ω)

C. Driver to Gate coupling series RC (parallel): Different values tested: R=15 Ω, C=(100 pF, 1 nF, 10 nF and 100 nF)

D. Driver to Gate coupling with different gate resistors for turn-on and turn-off

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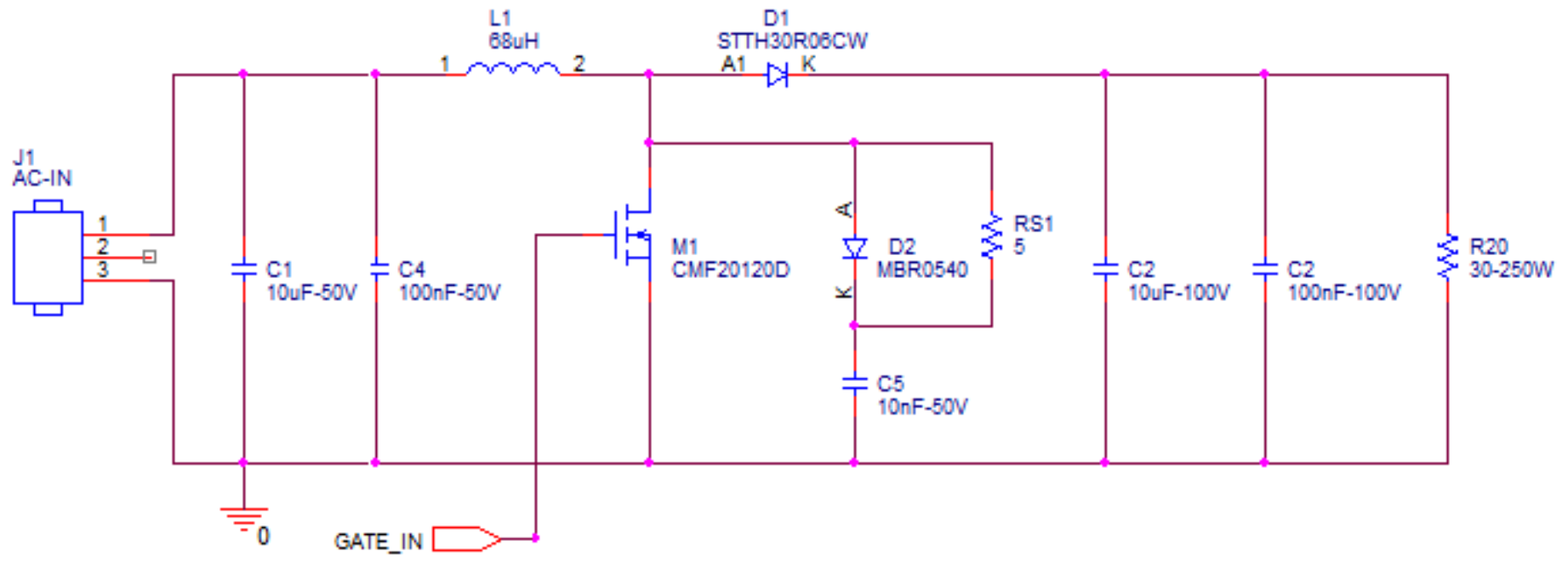
Experimental Plant 1: Boost Converter



Vin: 30 V ; Vout: 60 V ; Iout: 2 A ; fs: 100 kHz
SiC MOS FET: CMF20120D
Si Diode: STTH30R06CW

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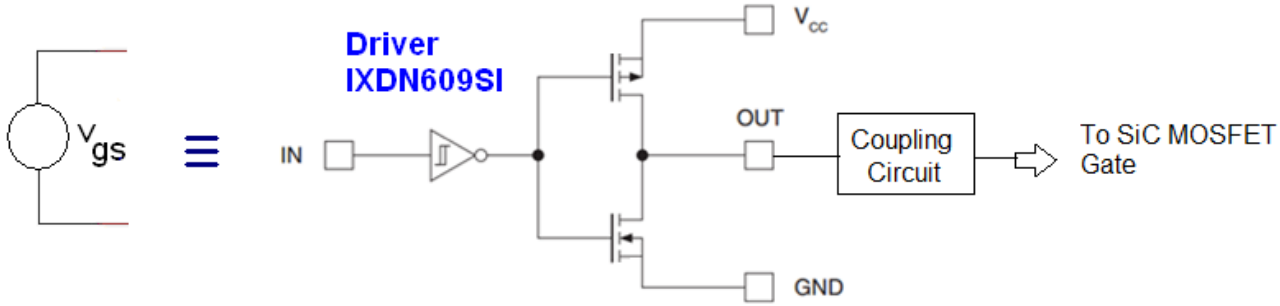
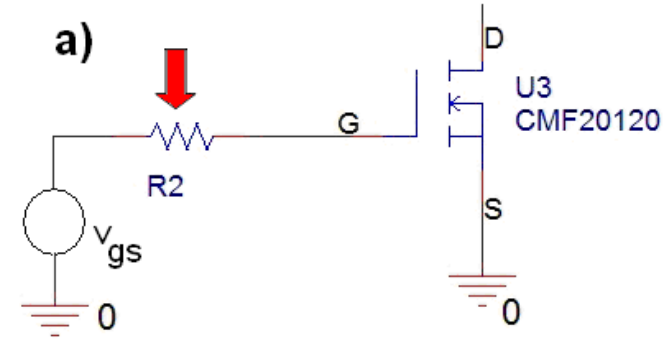
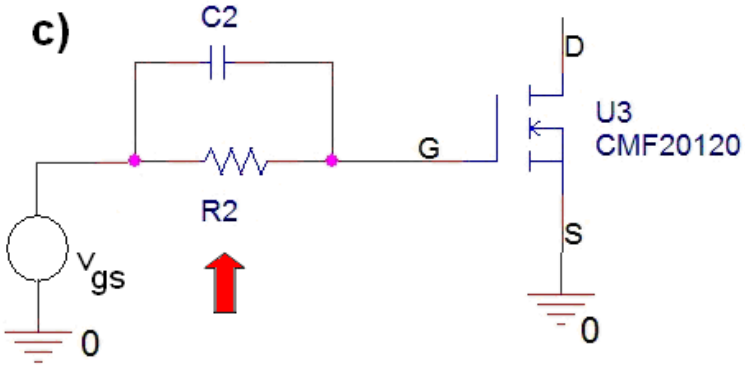
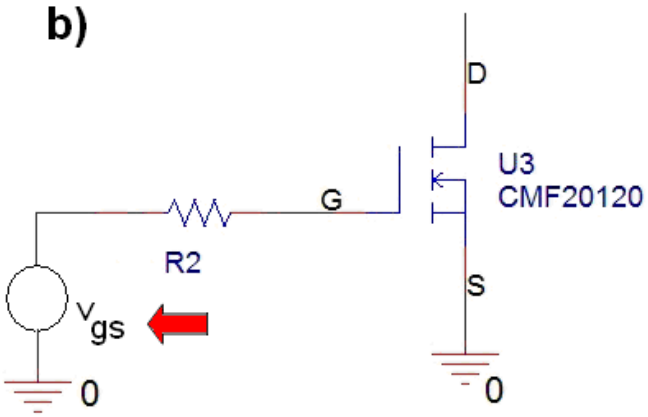
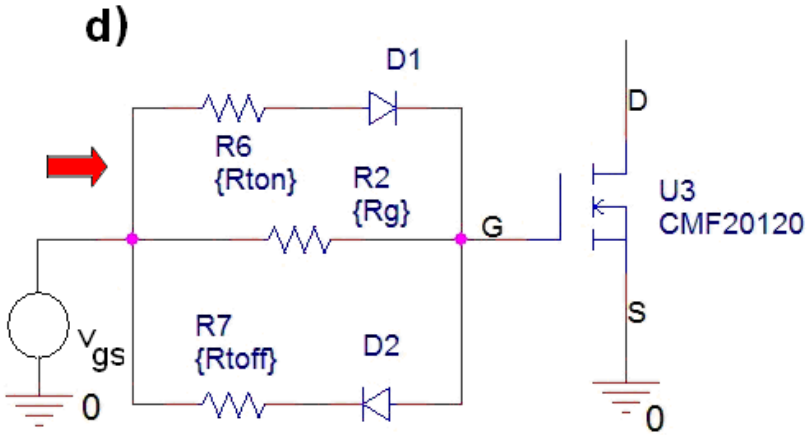
Different tests: Vgs driver IXYS IXDN609SI



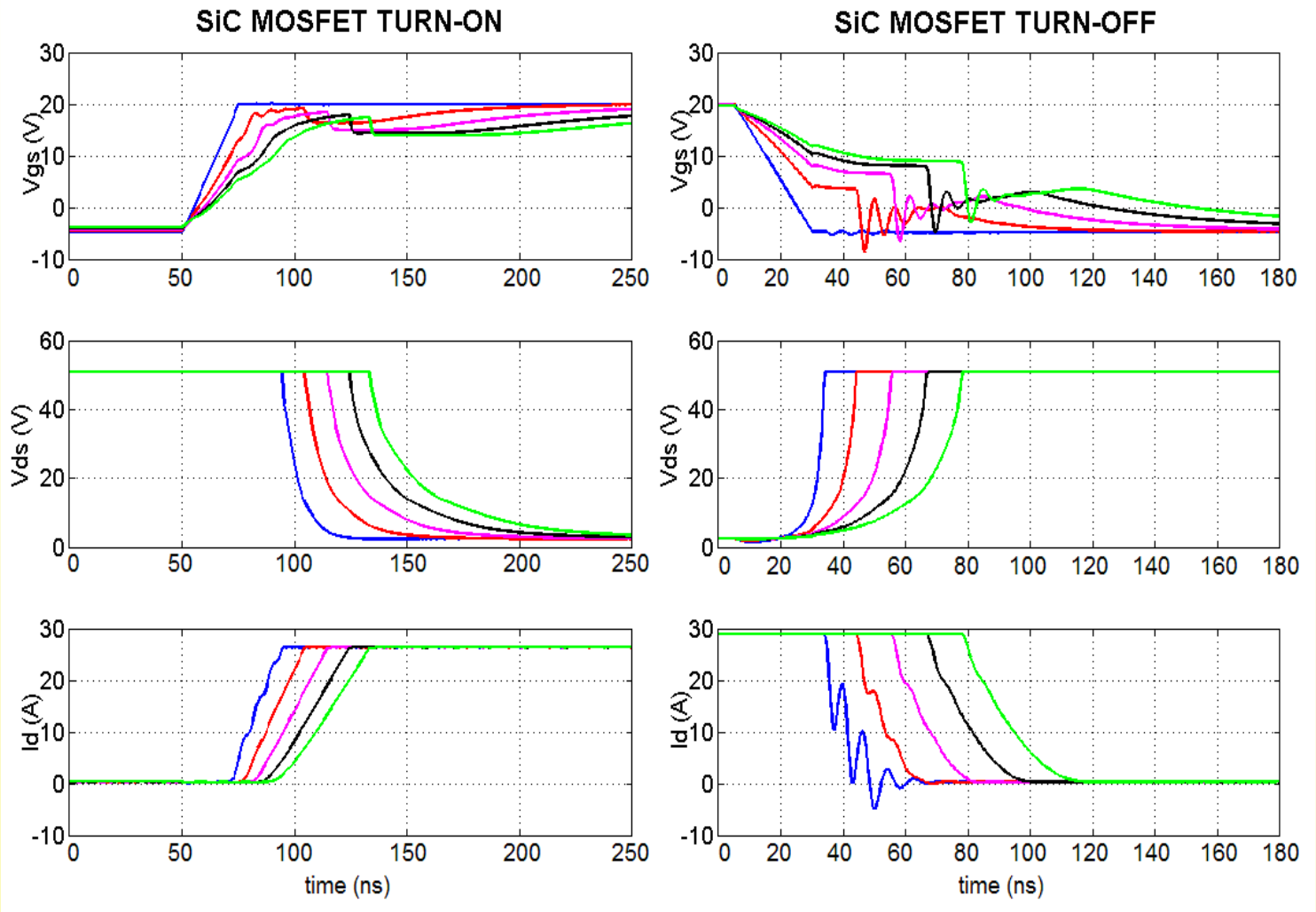








CREE MODELS VALIDATION: SIMULATION
Effect of gate series resistor (Vgs=-2 to 20V)



Rg too low causes Vgs and Id oscillations at turn OFF

Rg too high increase turn ON and turn OFF delays

Optimum: Rg between 5 and 10 Ω

Rg = 0 Ω (blue trace), Rg = 5 Ω (red trace), Rg = 10 Ω (pink trace), Rg = 15 Ω (black trace) and Rg = 20 Ω (green trace). Vgs=-2 to 20V

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CREE MODELS VALIDATION: MEASURED
Effect of gate series resistor (Vgs=-2 to 20V)

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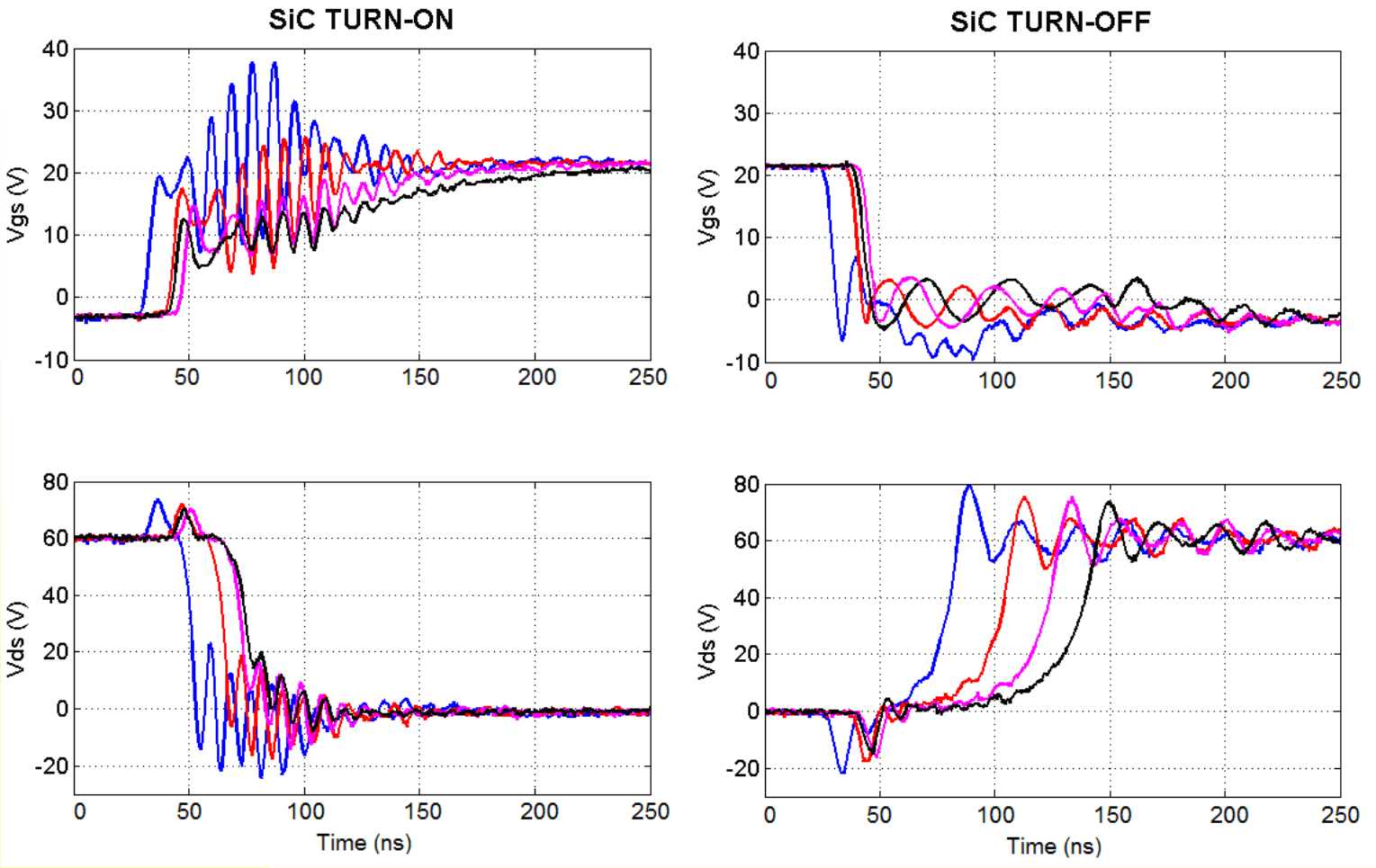

Filtering the signals with a LP filter below 100MHz the signals are reasonably equal

Rg = 0 Ω (blue trace), Rg = 5 Ω (red trace), Rg = 10 Ω (pink trace), Rg = 15 Ω (black trace) and Rg = 20 Ω (green trace). Vgs=-2 to 20V

Simulation with PSpice models vs. Experimental

Filtering the signals of experimental test with a LP filter below 100MHz the simulated and measured signals are reasonably equal in time domain

CONCLUSION:

- **Predictions in the conducted band, using PSpice models, will be good.**
- **Predictions in the radiated band shall not be good when using the model for the MOS-FET**
- **In the following, in order to evaluate coupling circuits we shall use simulation for time domain results but experimental results for conducted and radiated EMI**

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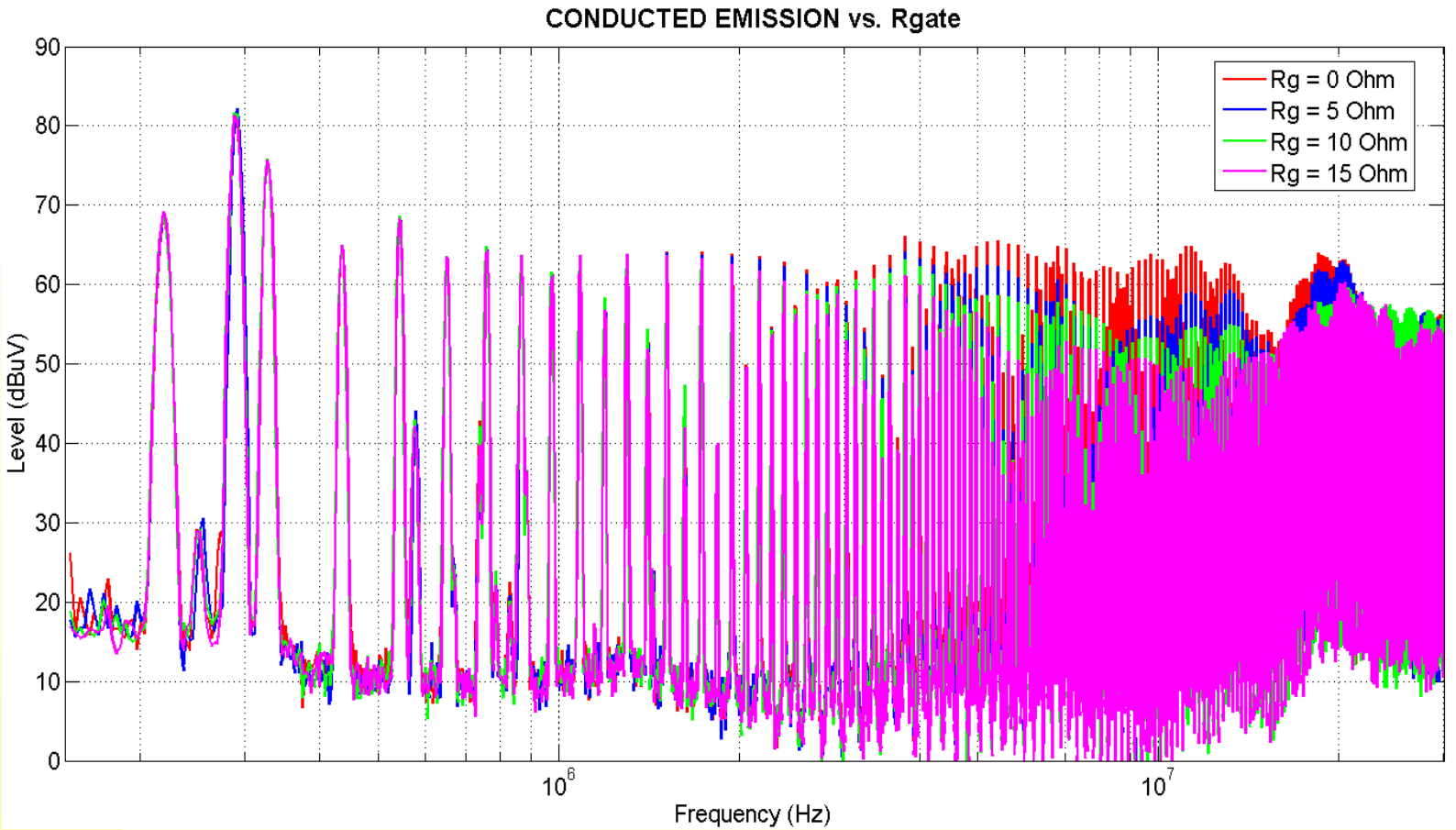
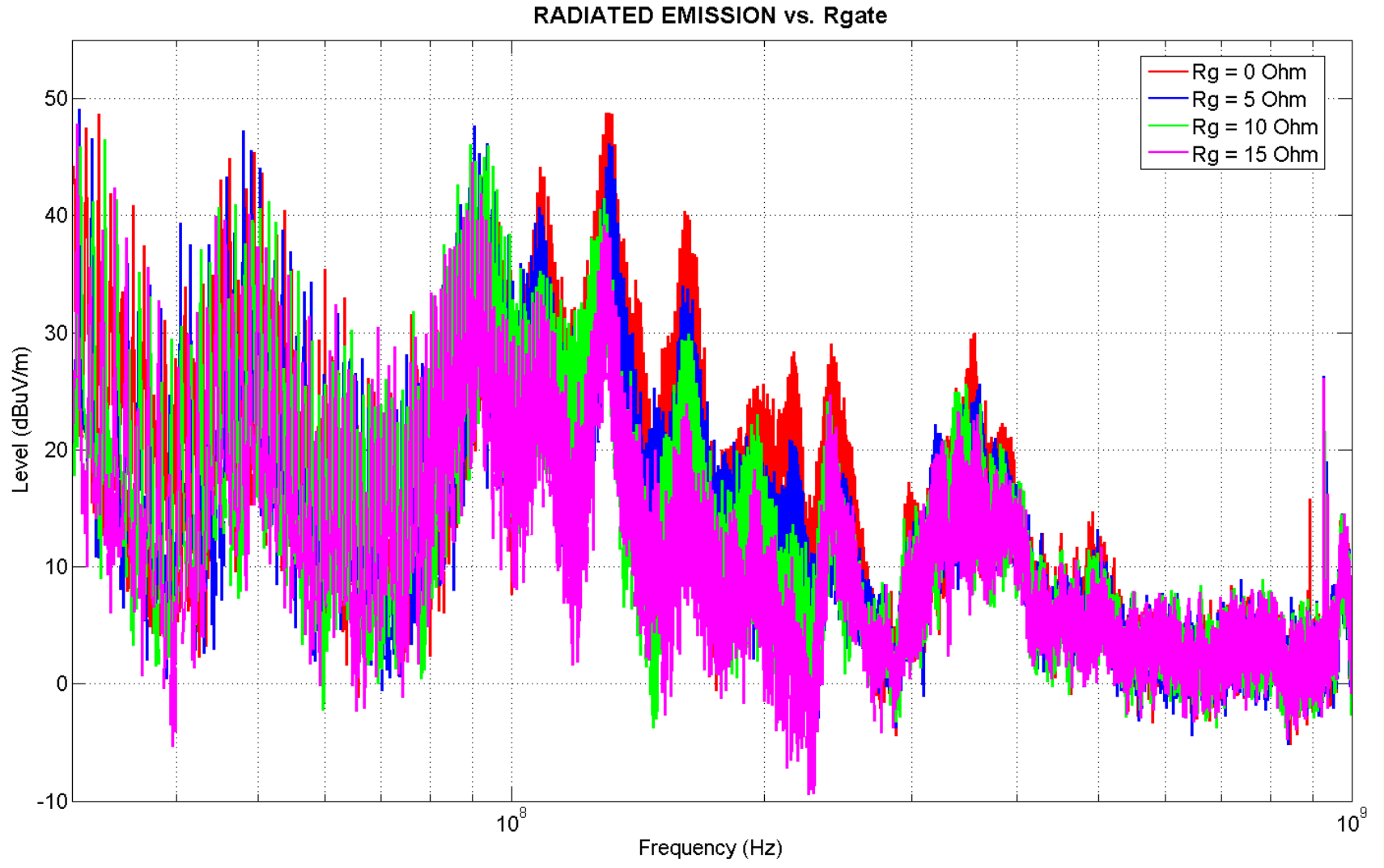
Example: Effect of gate series resistor on conducted EMI



EMI reduction in the range of 5 to 20MHz (max 10dBμV) for Rg between 15Ω . Need to slow commutation

Example: Effect of gate series resistor on Radiated EMI



NO SIGNIFICANT REDUCTION IN THE RADIATED BAND

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Conclusions

- Low Rg is desirable to reduce losses and EMI in conducted band (best option is a low value of Rg. About 5Ω)
- Vgs negative bias → No significant changes observed for (-2 to 20V) and (-5 to 20V)
- In all cases SiC devices are faster than Si devices and driver circuits must be delayed in order to lower EMI . Trade off EMI and losses

Results presented in the Conference

EMC Europe 2013, 1-4 Sept. Brugge

- In boost converter the switch ON (di/dt) is limited by L. To test the MOS switch we made new tests on a buck converter

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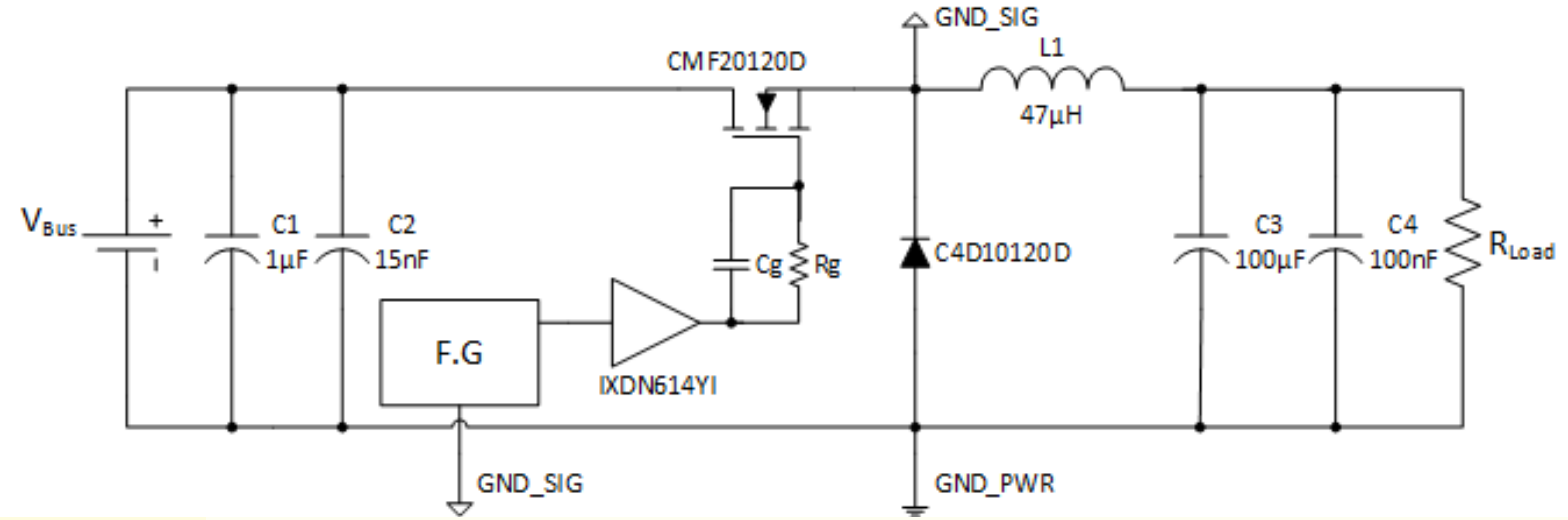
Experimental Plant: Buck Converter



V_{Bus}: 100 V

Vout: 24 V

f_s: 50 kHz

Iout: 3.25 A

Driver: IXYS IXDN614YI

R_g: 10 Ω ; C_g: 10 nF, 100 nF, 470 nF

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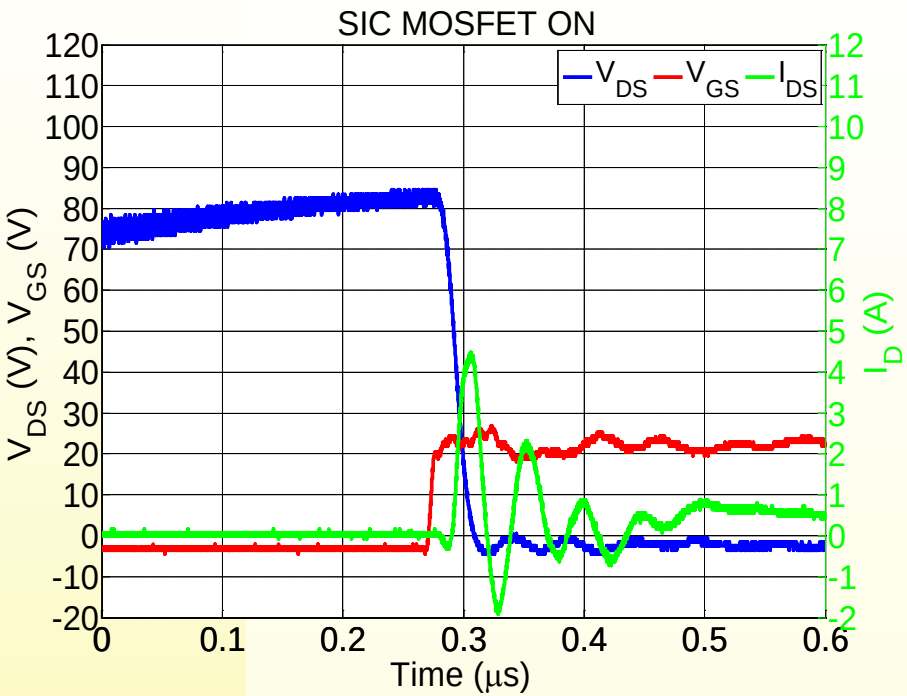
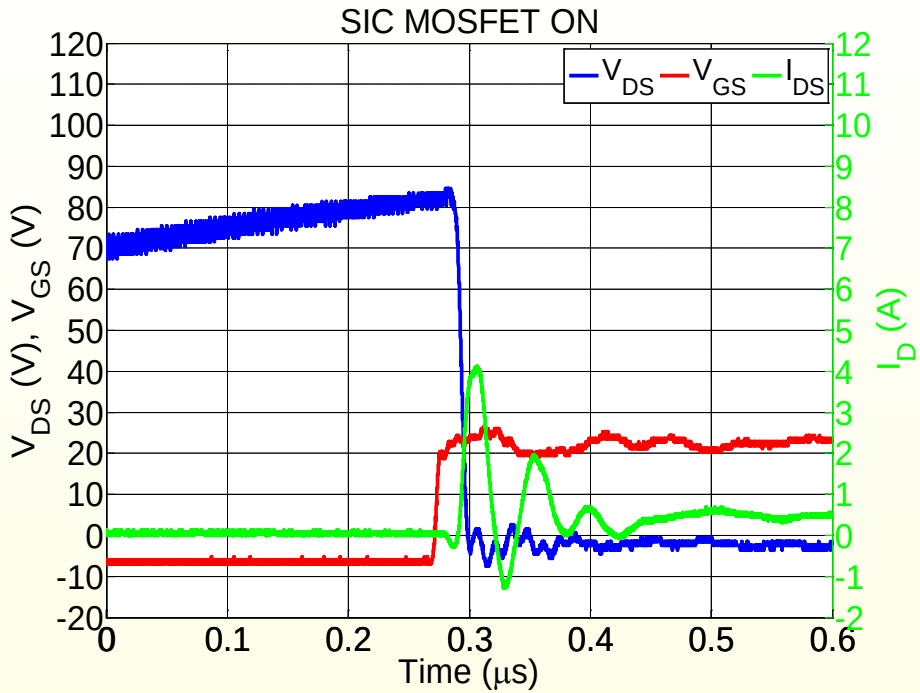
Effect of the V_{GS} negative voltage C_g= 100 nF

V_{DS} and I_D response with V_{GS} = 20 V/-2 V



V_{DS} and I_D response with V_{GS} = 20 V/-5 V



	V_{GS}= +20 V/-2 V	V_{GS}= +20 V/-5 V
Fall time	7 ns	7 ns
Delay time (turn-on)	20 ns	20 ns
E ON losses	0.7 µJ	0.7 µJ

Effect of the V_{GS} negative voltage C_g= 100 nF

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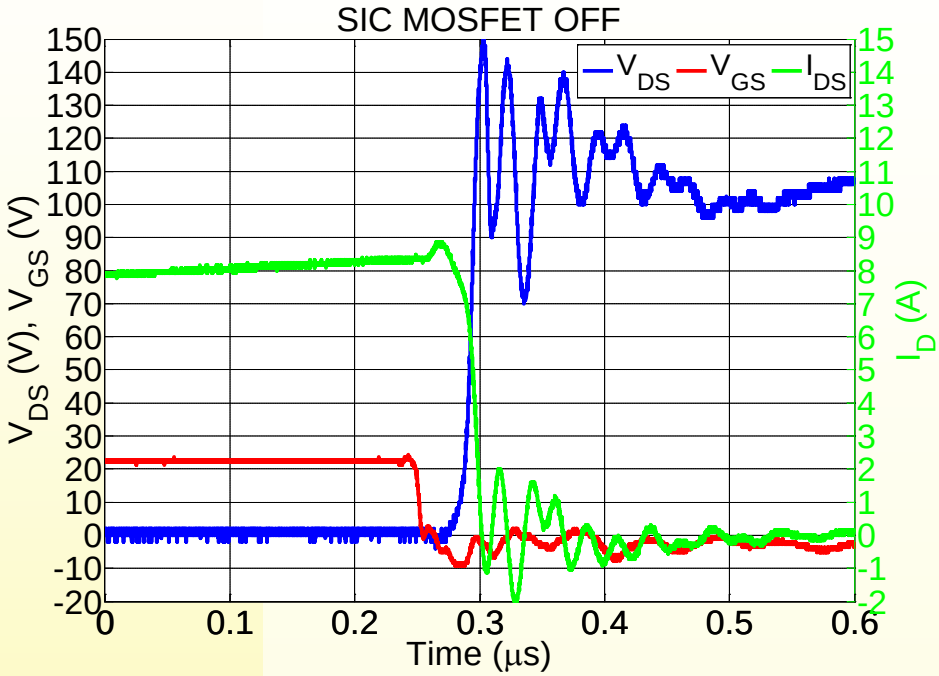
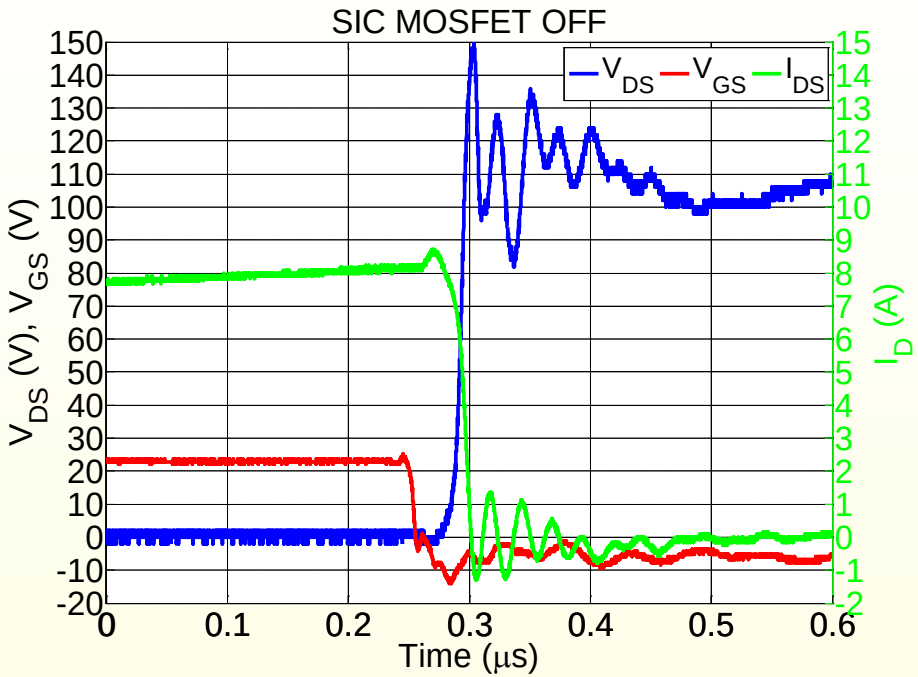
V_{DS} and I_D response with V_{GS} = 20 V/-2 V



V_{DS} and I_D response with V_{GS} = 20 V/-5 V



	V_{GS}= +20 V/-2 V	V_{GS}= +20 V/-5 V
Rise time	10 ns	10 ns
Delay time (turn-off)	40 ns	38 ns
E OFF losses	15.4 µJ	11.7 µJ

Conclusions and Future work

- SiC devices are very fast . Too fast to reduce EMI
- In resonant converters using ZVS this may lead to high overcurrent during turn ON
- We are working on a new driver allowing the device to work temporarily in the linear region, in order to decrease such overcurrent.
- This will cause some extra losses , but will minimize the cost drastically.
- We are also applying SSFM techniques and interliving in order to reduce EMI

These results will be presented in ISE 2014

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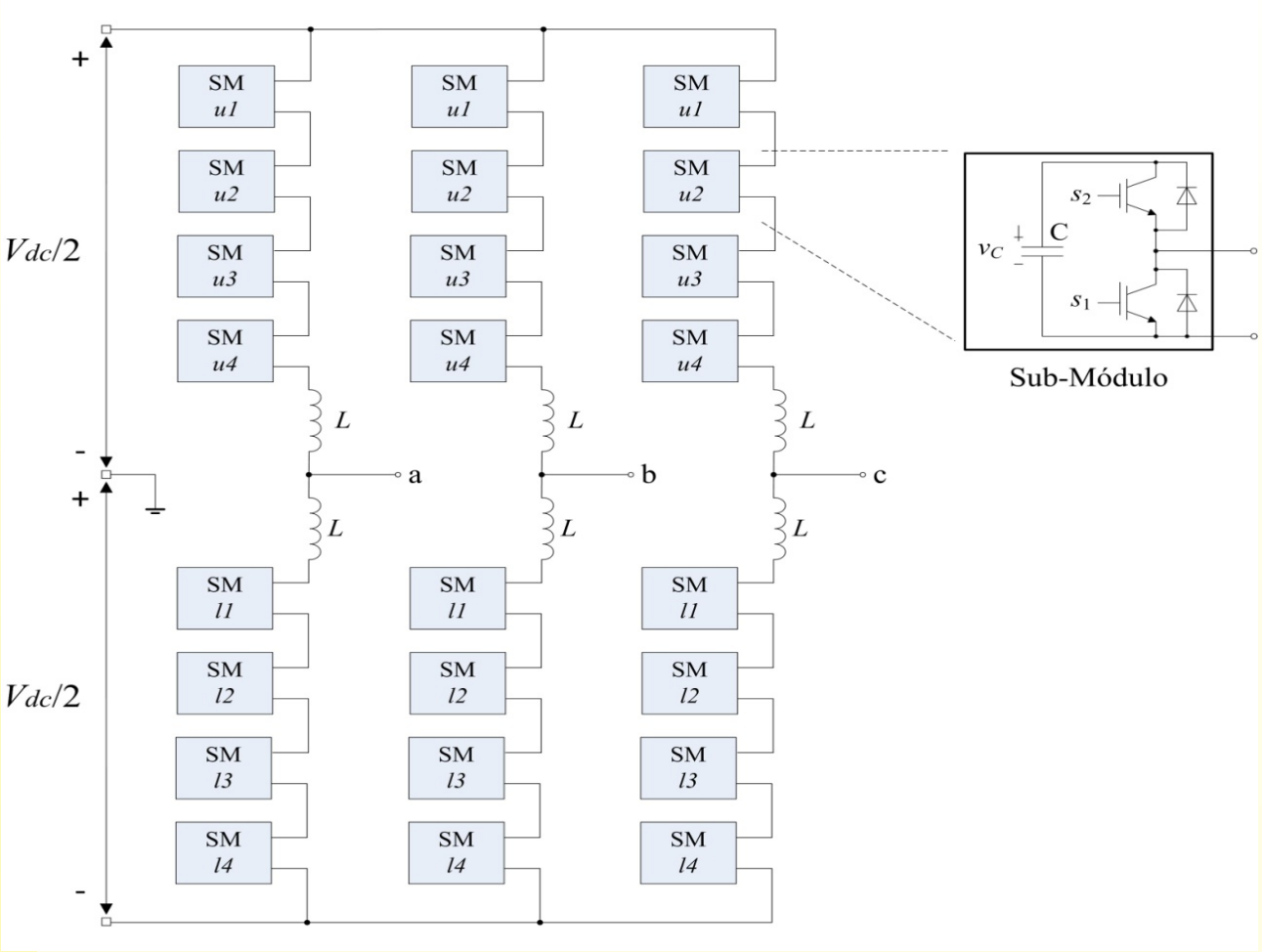
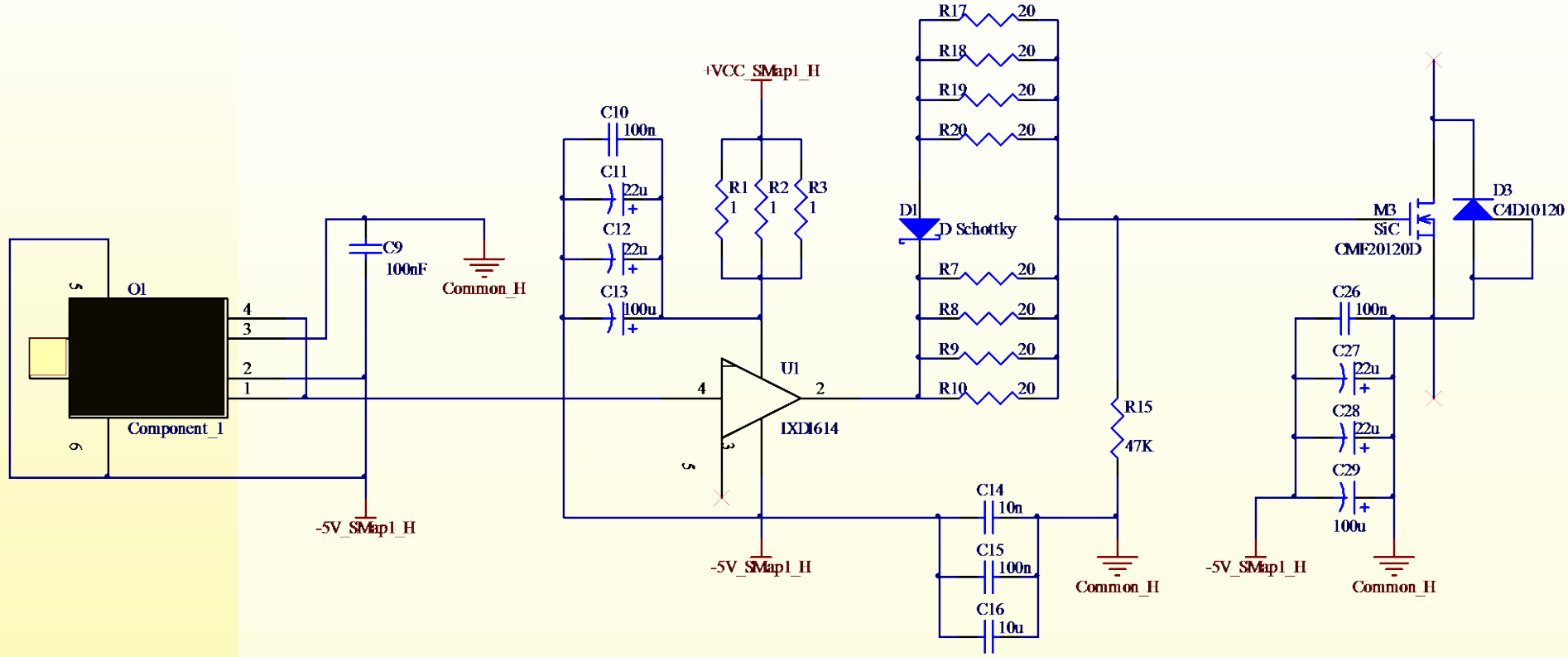
Future work. MMC converter

- MMC three phase with N=4



Future work. MMC converter

- **Optical fiber control**
- **Driver IXDN614 (IXYS).**



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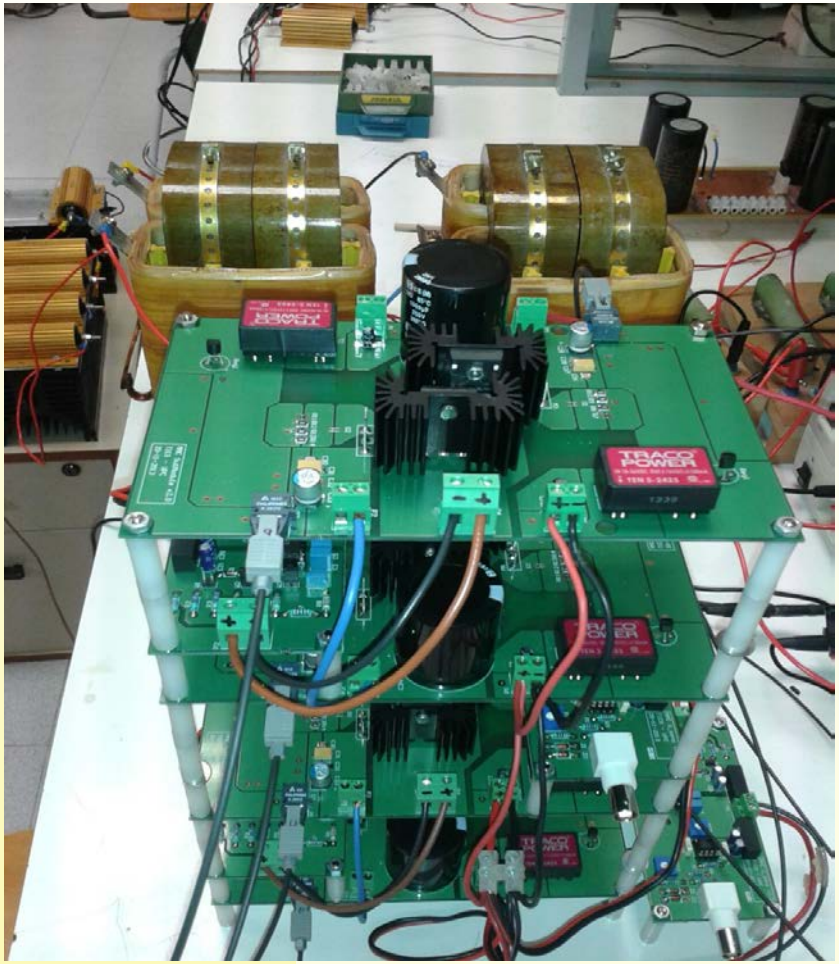
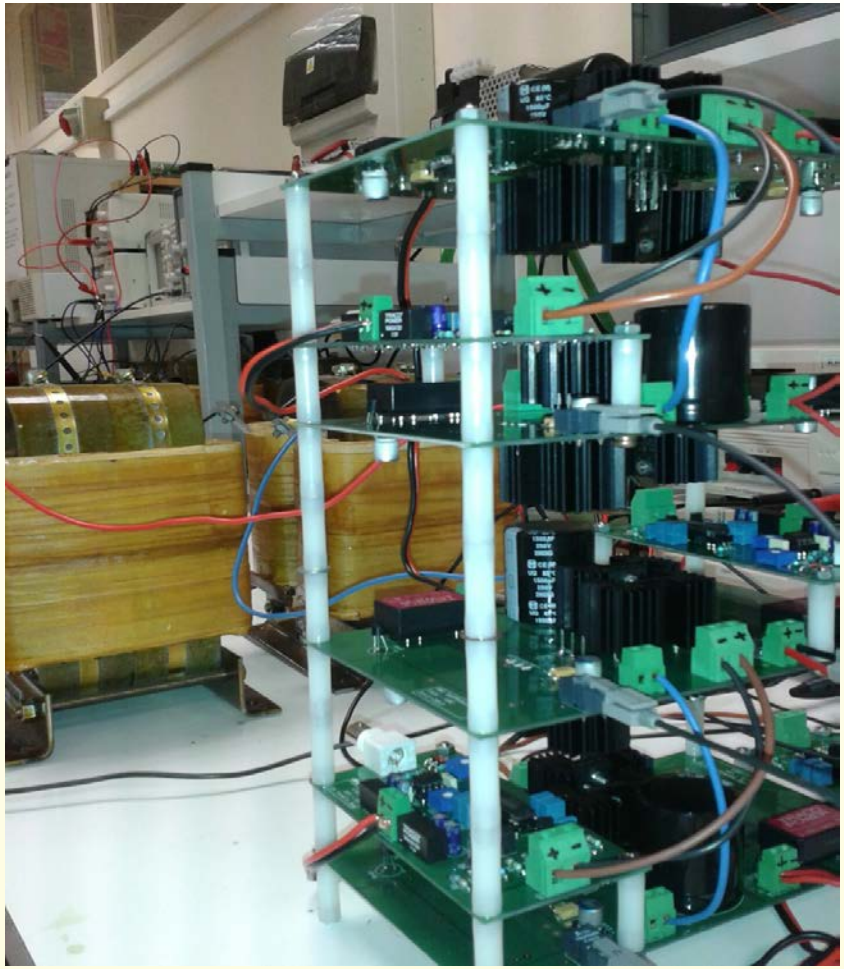
Future work. MMC converter

- **Prototype 3 level MMC (N=2 per leg)**





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Objectives 2014

- Drive the MMC from Dspace (done)
- Study of commutation
- Develop new modulation techniques to reduce ripple and EMI

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Thank you for your attention

TIEG-UPC
Terrassa
Industrial
Electronics
Group

Prototipo Convertidor Multinivel

- **Topología: Convertidor Multinivel Modular (MMC: *Modular Multilevel Converter*)**
- **Número de Sub-Módulos por semi-fase (*N*): 4**
- **Número de niveles: 5 (9 con interleaving)**
- **Potencia nominal (*P*): 10 kVA**
- **Tensión nominal de bus (V_{dc}): 750 V**
- **Semiconductores con tecnología de carburo de silicio (SiC):**
  - **48 MOSFET CREE CMF20120D**
  - **48 diodos CREE C4D10120**

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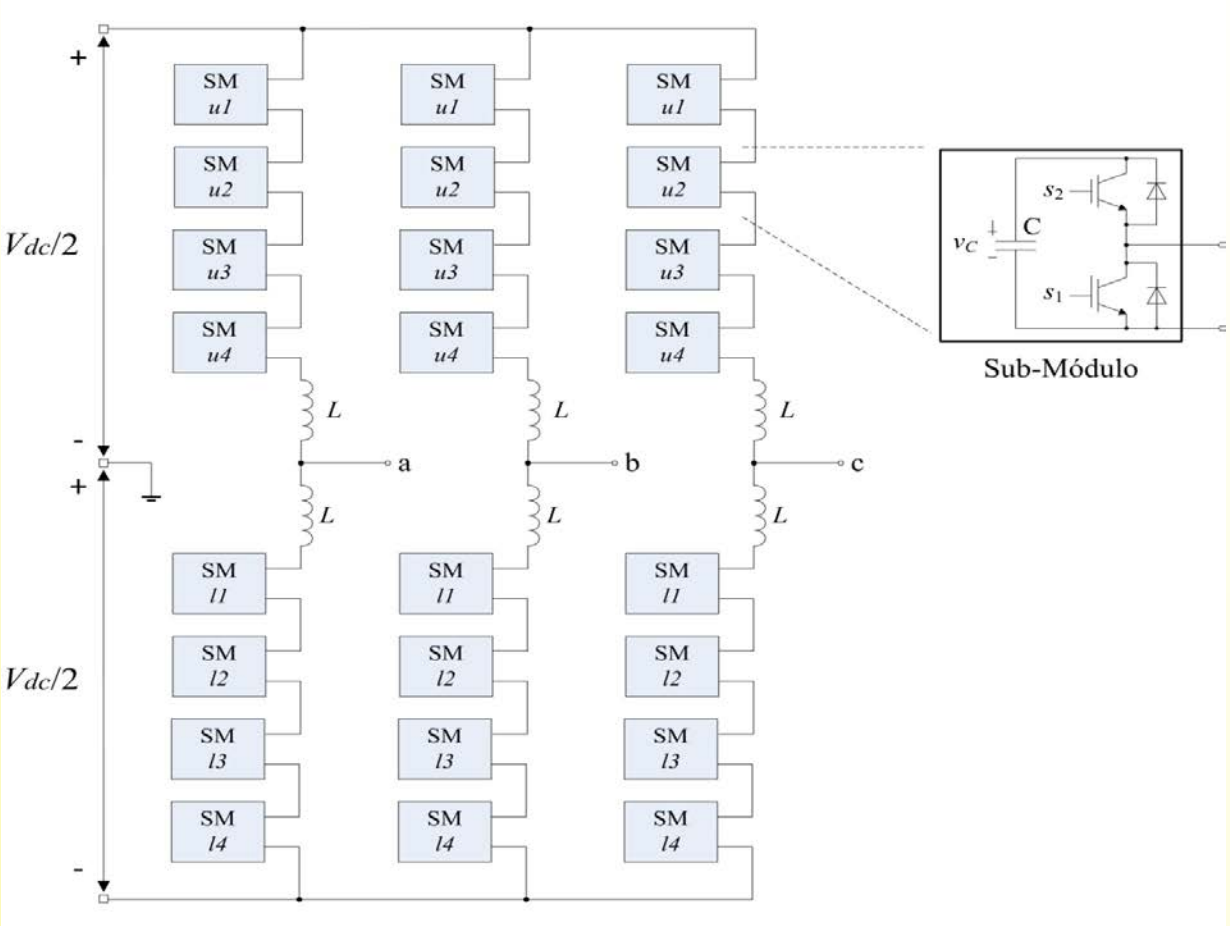
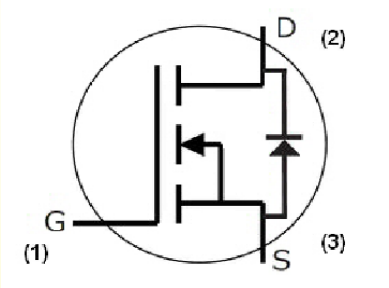
Esquema Prototipo MMC

- **Esquema de un convertidor MMC trifásico con N=4**

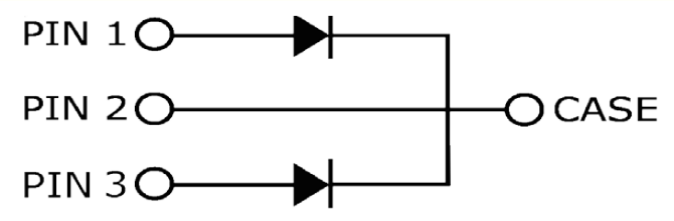


Componentes SiC

MOSFET CMF20120D



DIODO C4D10120



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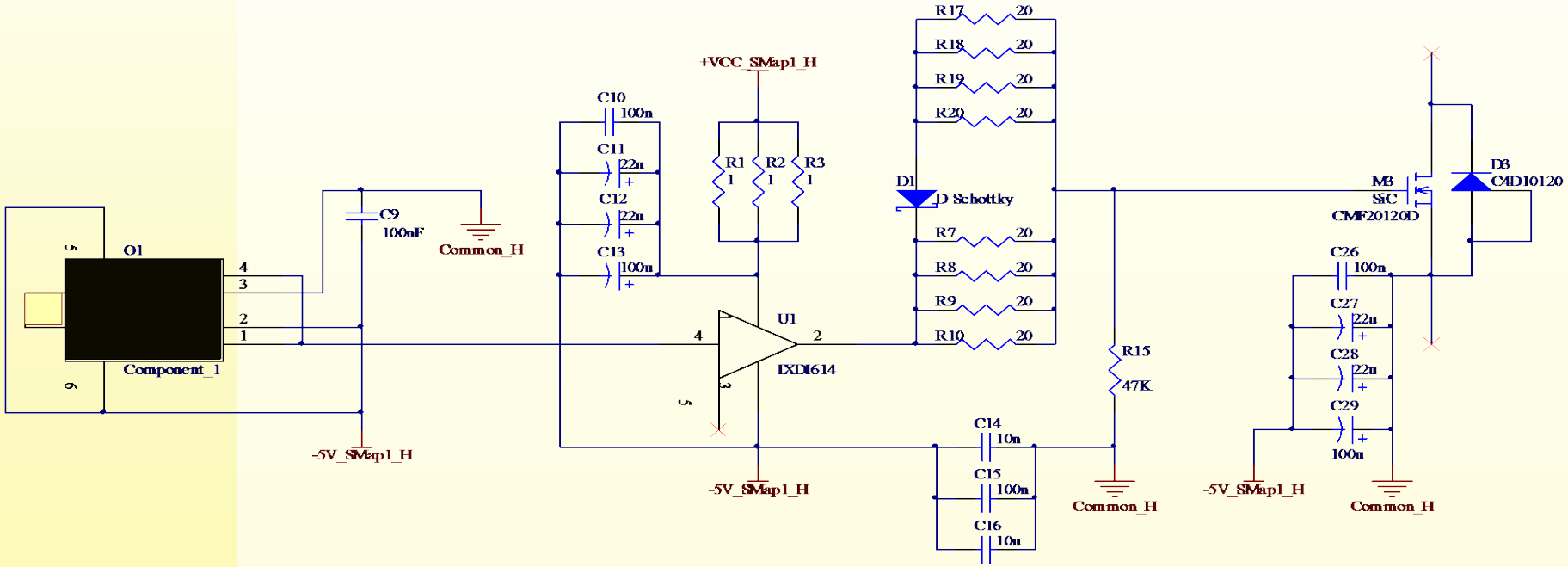
Circuito de activación

- Control por fibra óptica.
- Driver de puerta IXDN614.
- Tensiones de encendido y apagado entre 15V i -5V.



Esquema de Sub-Módulo

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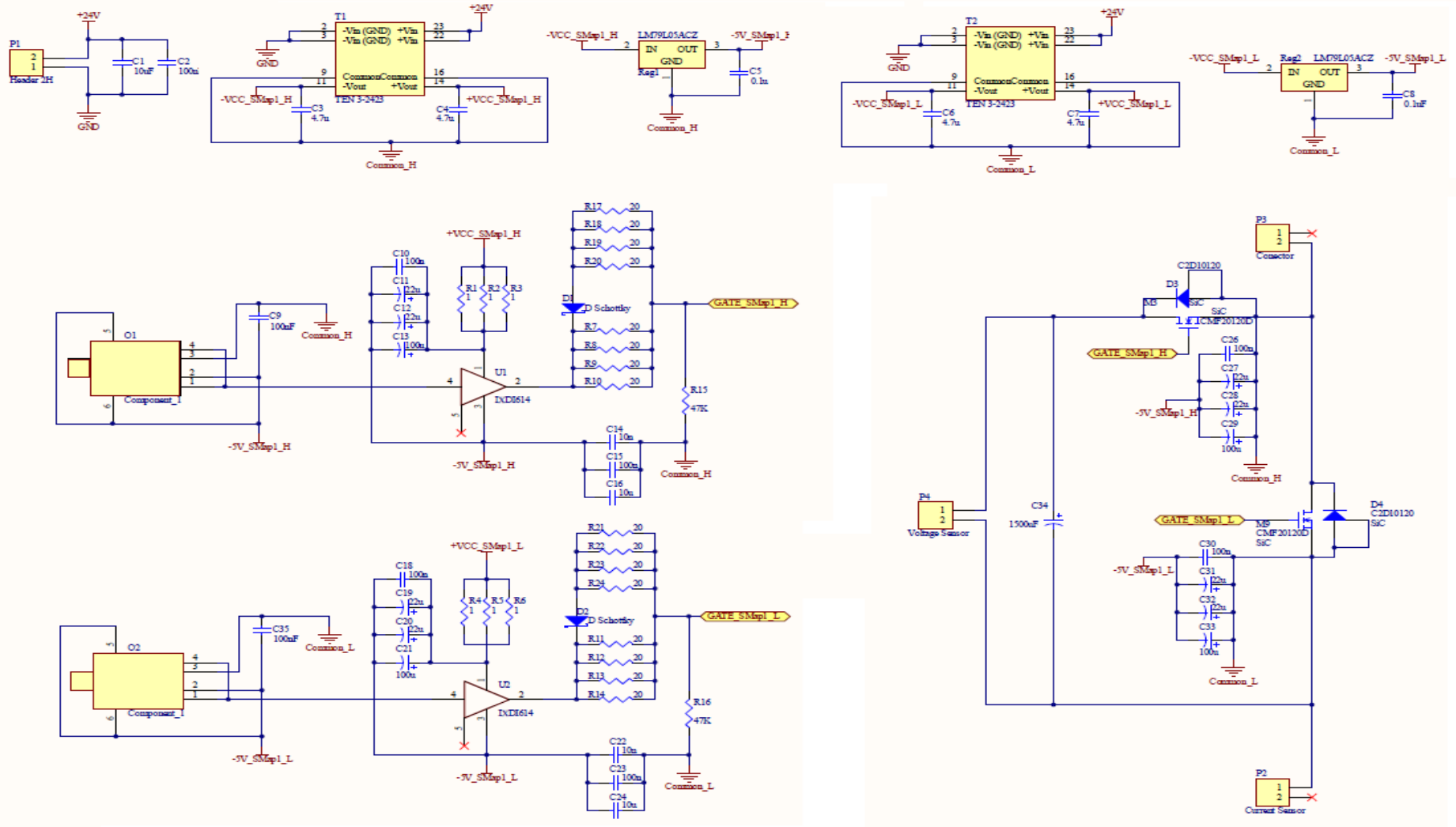
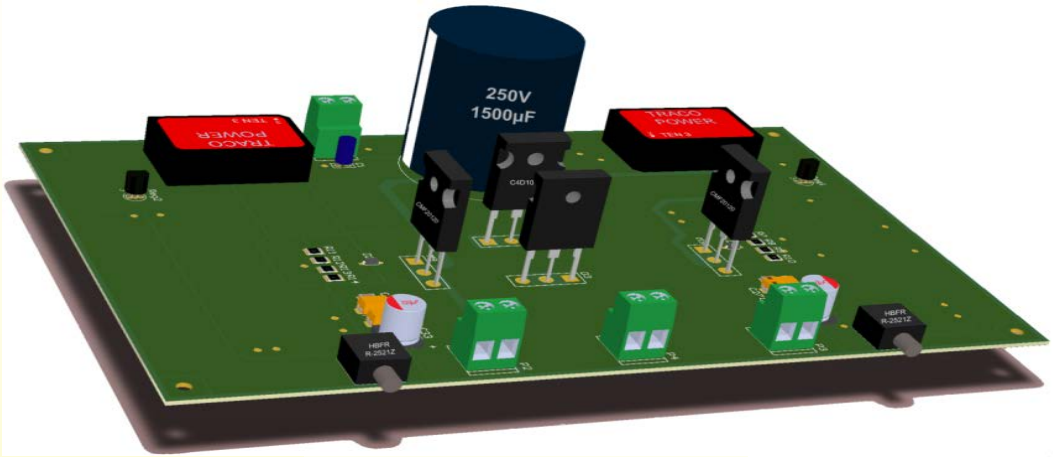


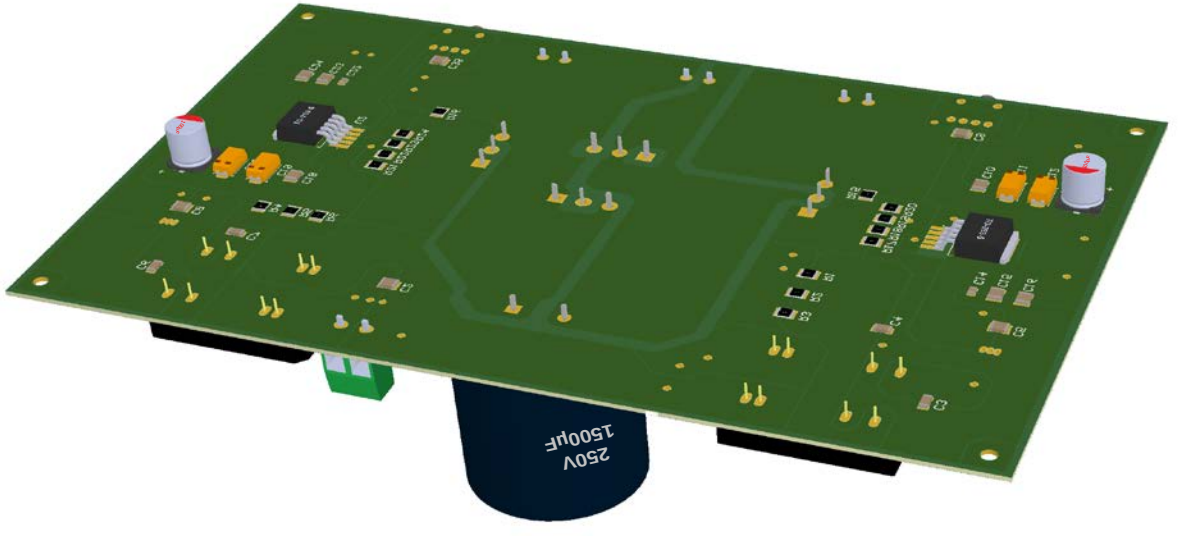
Diseño del prototipo

- **Modelo 3D de un Sub-Módulo**



Cara superior

Cara inferior



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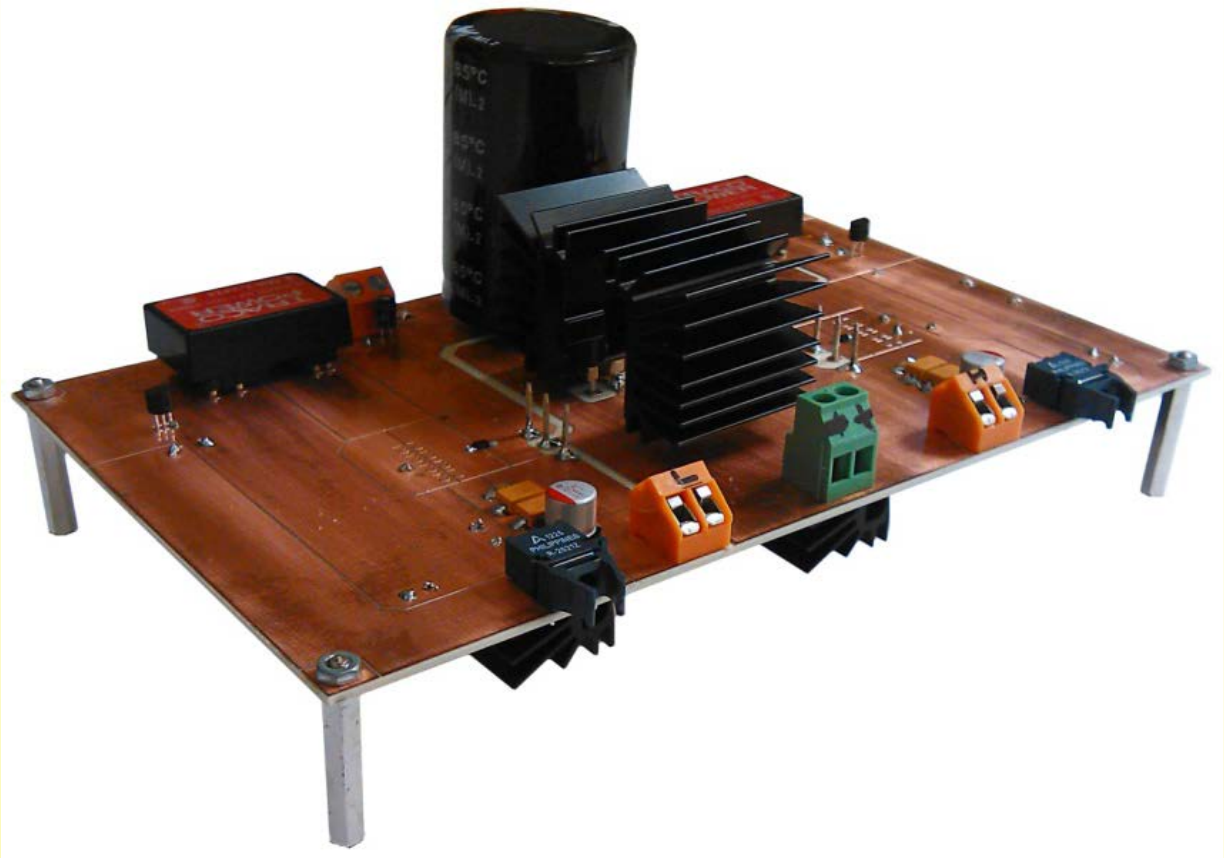
Diseño del prototipo

- **Versión inicial del Sub-Módulo**



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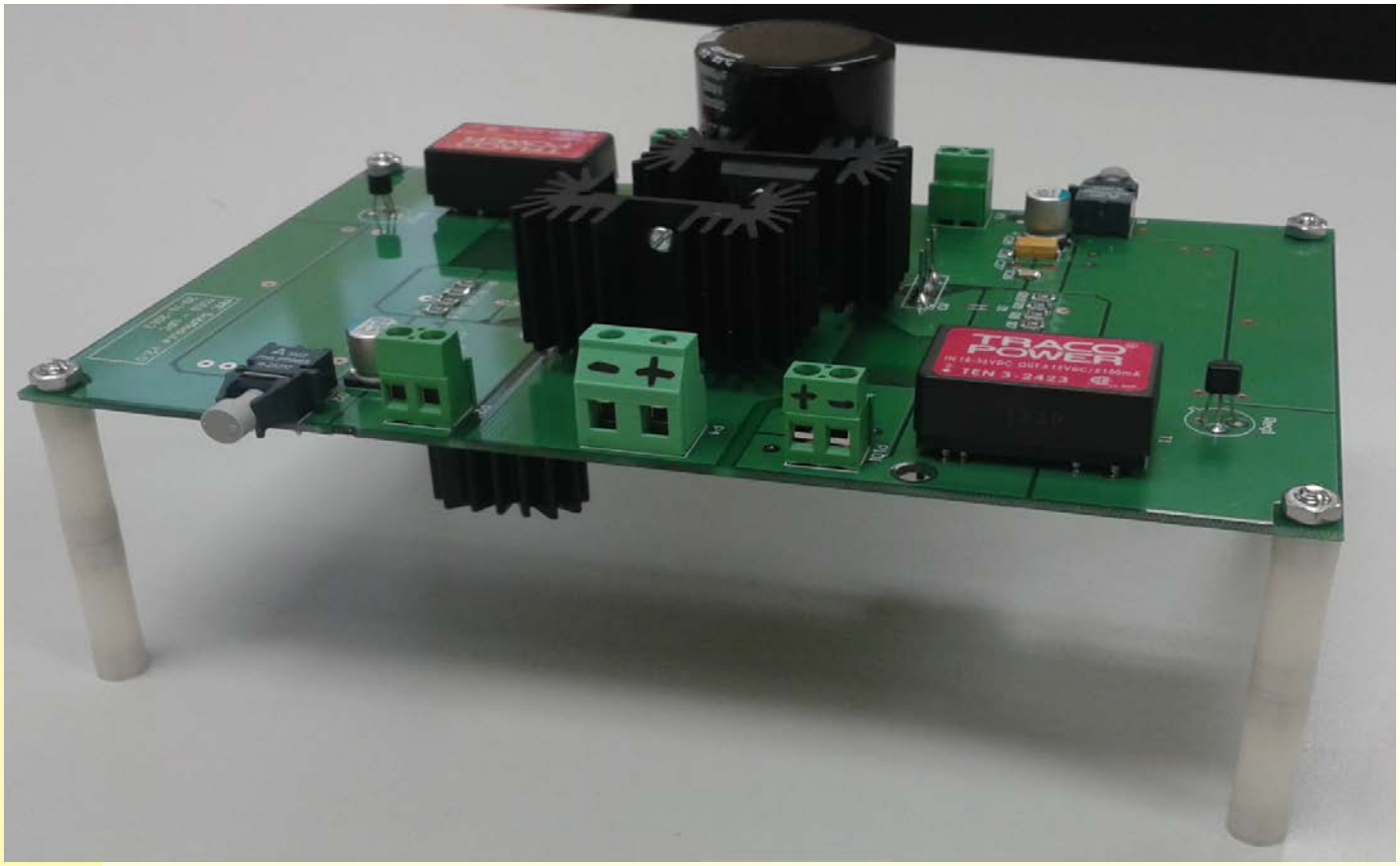
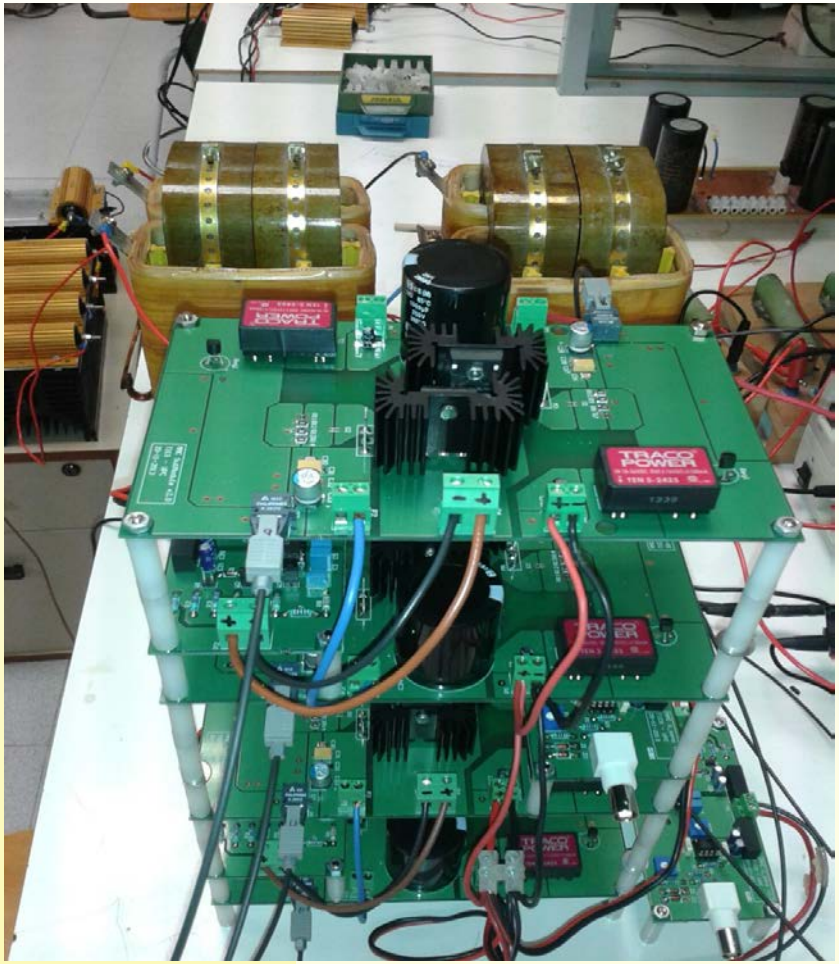
Diseño del prototipo

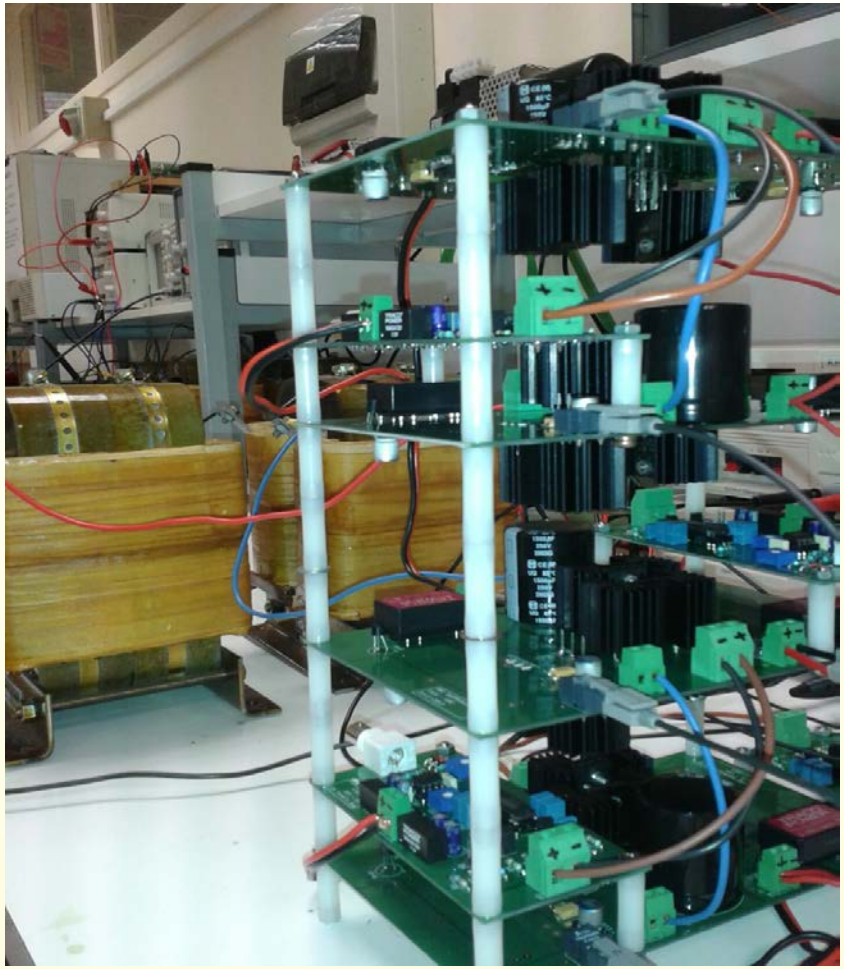
- **Segunda versión de Sub-Módulo**



Diseño del prototipo

- **Estado actual del prototipo MMC (una fase con N=2)**





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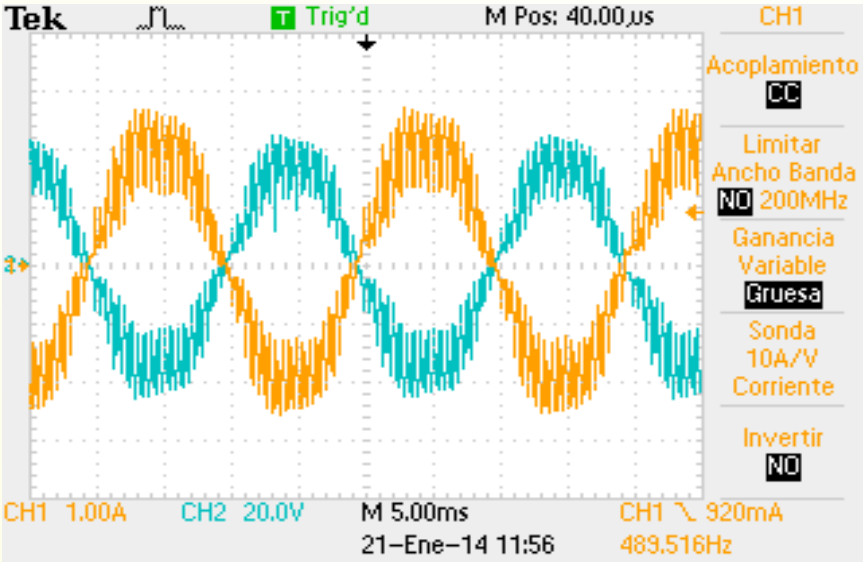
Resultados experimentales

- **Características del prototipo**

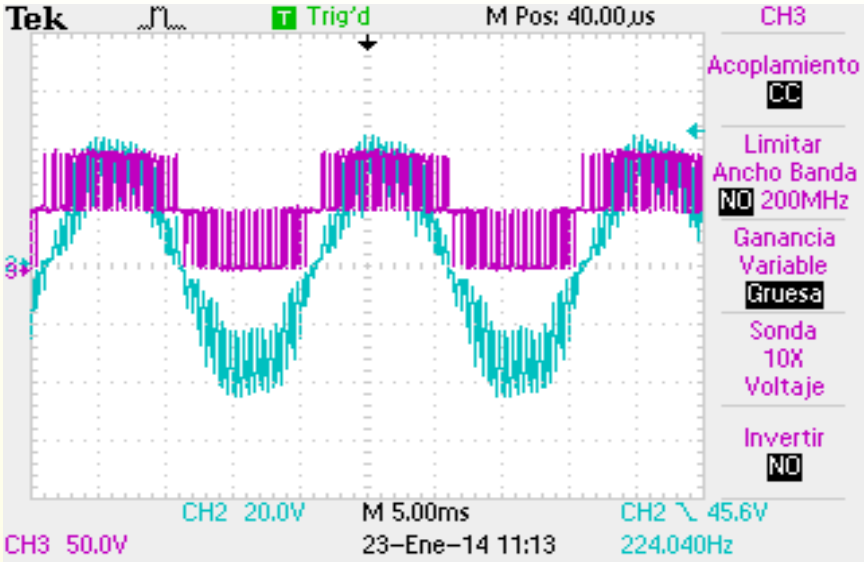
Parámetro	Valor
Número de celdas por semi-fase, *N*	2
Tensión de bus, V_{dc}	100 V
Inductancia interna, L	6 mH
Capacidad de Sub-Módulo, C	1500 µF
Frecuencia de conmutación, f_s	5 kHz
Resistencia de carga, R_L	17 Ω

Resultados experimentales

- **Formas de onda en el convertidor MMC**



Tensión (azul, invertida) y corriente de salida (amarillo)



Tensión de salida (azul) y en los extremos de las inductancias (morado)

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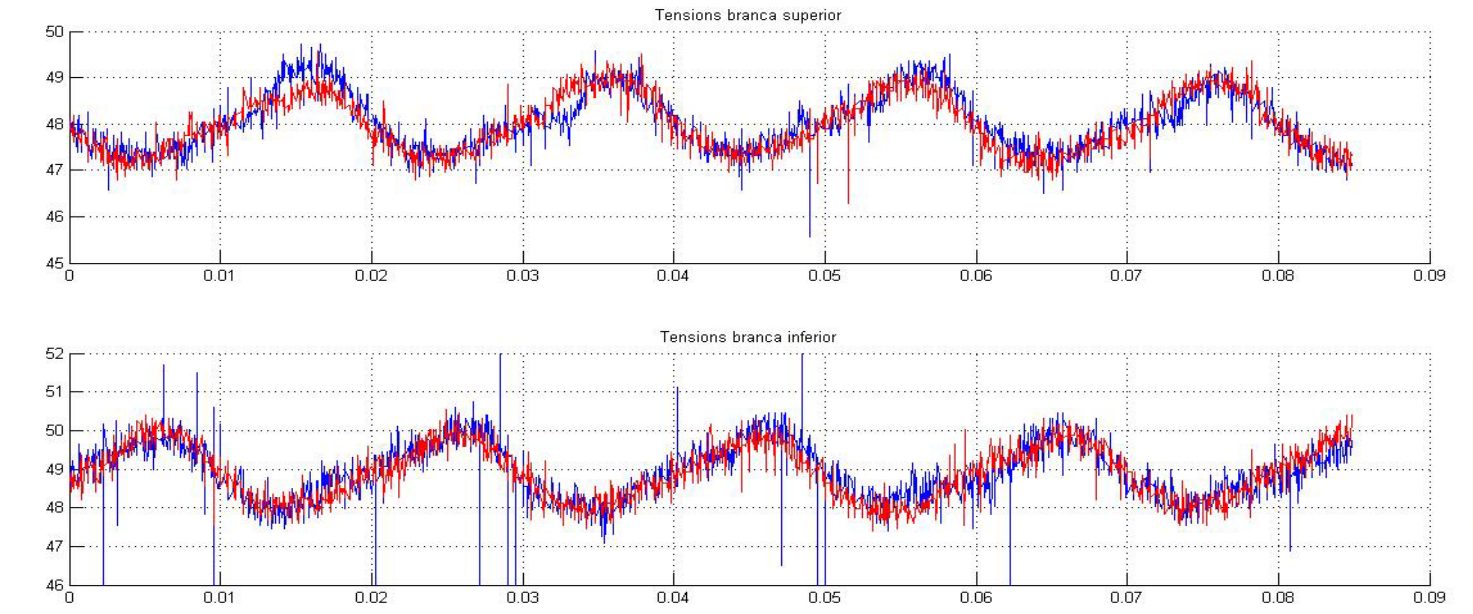
Resultados experimentales

- **Formas de onda en el convertidor MMC**



Tensiones en los condensadores de las semi-fases superior e inferior

Objetivos 2014

- Estudiar la conmutación de los Sub-Módulos y ajustar el circuito de activación.
- Finalizar el montaje y programación del convertidor MMC trifásico (24 Sub-Módulos).
- Desarrollar circuitos complementarios del prototipo: circuito de activación de fibra óptica y de medida de corriente.
- Estudiar las pérdidas de conmutación y conducción del convertidor prototipo.
- Aplicar técnicas de modulación y control para convertidores trifásicos y para convertidores monofásicos con un gran número de Sub-Módulos (N=12).

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