Research Projects in Electronic Engineering at UPC
Track – Industrial Electronics

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Sala de Conferències ETSEIAT

Hybrid Modulators for conducted EMI suppression in modular-parallel topology

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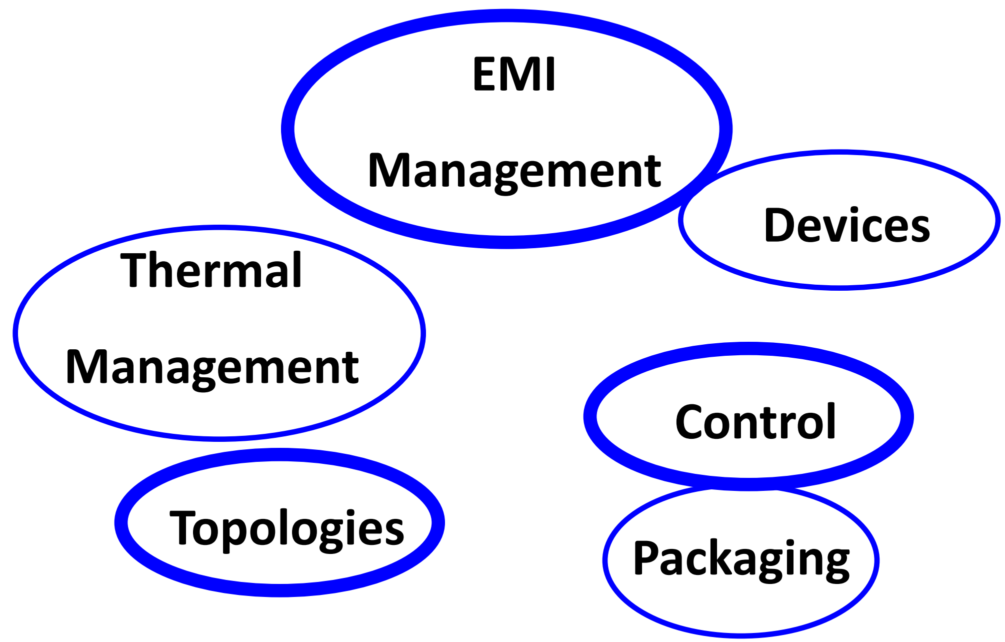
Presentation Index

1.- Introduction

The present trend in Power Electronics to improve performance is

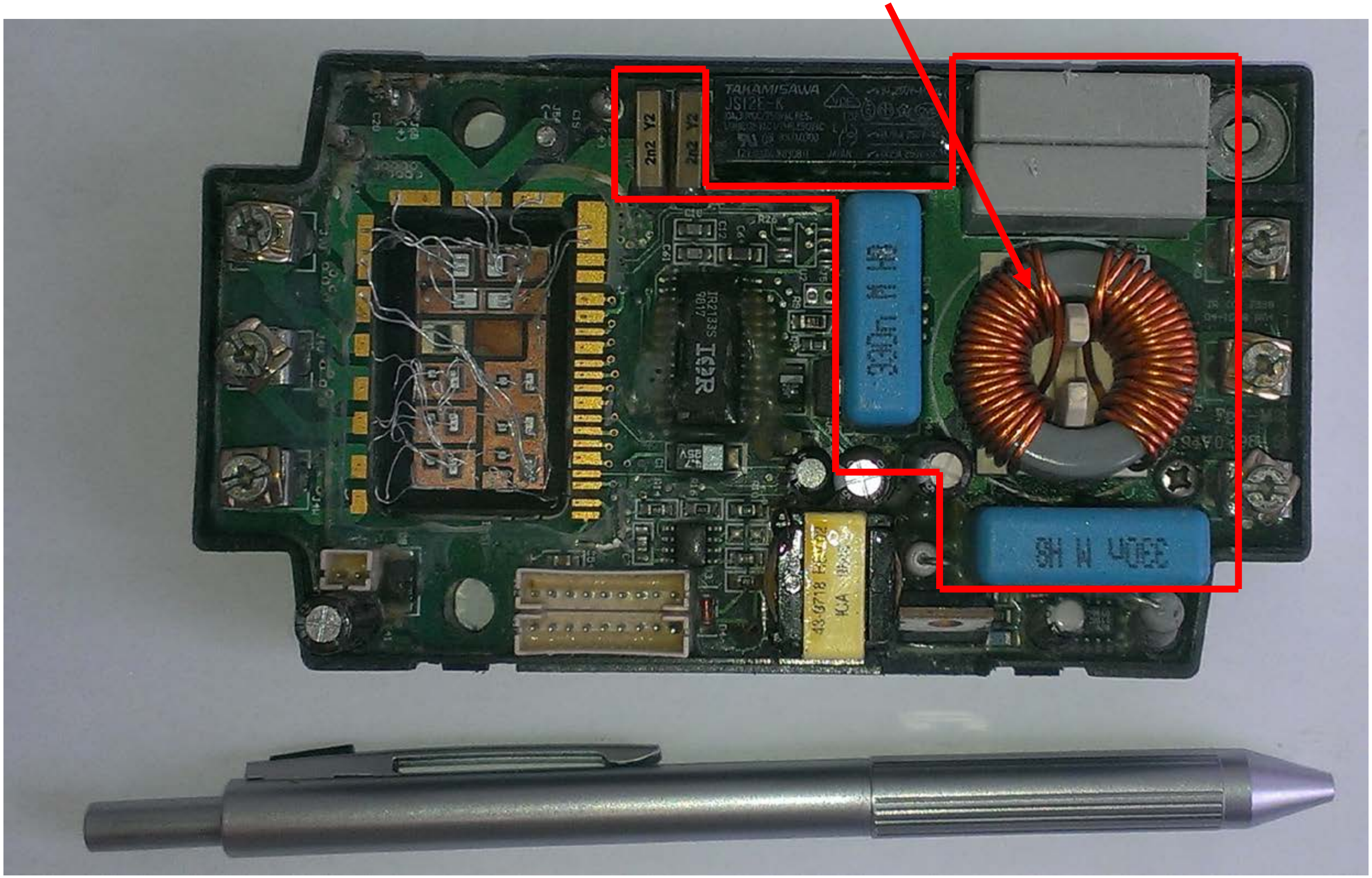
SYSTEM INTEGRATION

- Power density [kW/dm^3]
- Power per unit weight [kW/kg]
- Relative cost [€/kW]
- Relative losses [%]
- Failure rate [h^{-1}]



1.- Introduction

EMI FILTER

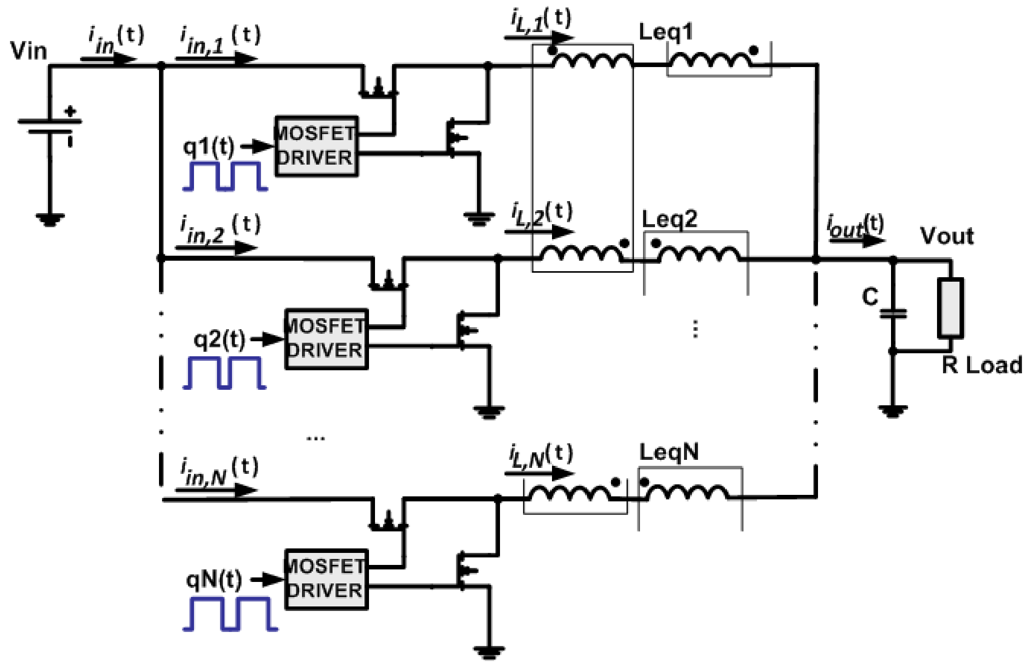


1.- Introduction

- Switching Frequency Modulation (SFM) is a worthy way to suppress EMI in power converters
- SFM applied to parallel arrangement should be combined with interleaving. This will result in Variable Delay Frequency Modulation (VDFM)
- This technique is suitable for new devices (SiC)

- Parallel arrangement is a disruptive topology that breaks frequency barrier. Moreover, Coupled Interleaved Multicellular Parallel Converters (CIMPC) show several advantages in terms of system integration and dynamic response
- CIMPC require a **SYMETRIC** operation

2.- SFM in Parallel Arrangement

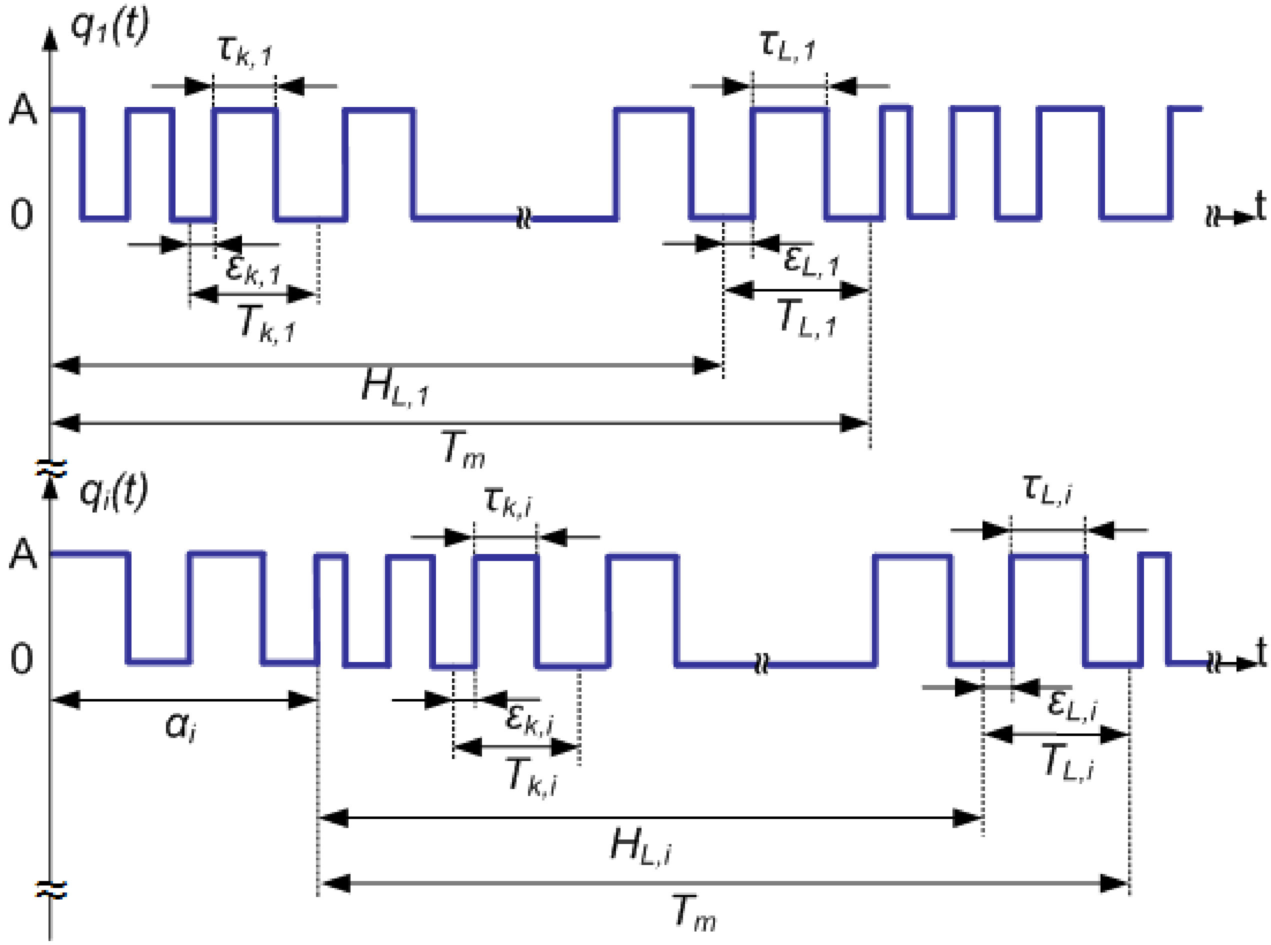


Breaks frequency barrier

Increased control dynamics

Redundancy without impairing reliability

2.- SFM in Parallel Arrangement



Periodic modulation function of period T_m

2.- SFM in Parallel Arrangement

TABLE I
CHARACTERISTICS OF DIFFERENT MODULATIONS

Modulations	$\varepsilon_{k,i}$	$T_{k,i}$	$\tau_{k,i}$	α_i
CDFM-Tm	$0 \;\forall i,k$	$T_c+\Delta T_k \;\forall i$	$D_c \cdot T_k \;\forall i$	$\frac{T_m}{N}(i-1)$
CDFM-Tc	$0 \;\forall i,k$	$T_c+\Delta T_k \;\forall i$	$D_c \cdot T_k \;\forall i$	$\frac{T_c}{N}(i-1)$
VDFM	$\frac{T_{k,i}}{N}(i-1)$	$T_c+\Delta T_k \;\forall i$	$D_c \cdot T_k \;\forall i$	$0 \;\forall i$

Periodic modulation function of period T_m

3.- Variable Delay Frequency Modulation

VDFM combines interleaving and SFM

$$S_{CDFM-Tm}(w)=F\left\{\sum_{i=1}^{N} q_i(t)\right\}=NAD_c\partial(w)+\left[\sum_{n=1}^{\infty}\left[\frac{A}{j\pi n}\left(\frac{1-e^{-j2\pi n}}{1-e^{\frac{-j2\pi n}{N}}}\right)\sum_{k=1}^{L}\left[e^{\frac{-j2\pi nH_k}{T_m}}\left(1-e^{\frac{-j2\pi n\tau_k}{T_m}}\right)\right]\partial(w-nw_m)\right]=\right.$$

$$=NAD_c\partial(w)+N\cdot E_{CDFM-Tm}(w)\left[\sum_{n=1}^{\infty}\left[\frac{A}{j\pi n}\sum_{k=1}^{L}\left[e^{\frac{-j2\pi nH_k}{T_m}}\left(1-e^{\frac{-j2\pi n\tau_k}{T_m}}\right)\right]\partial(w-nw_m)\right]\right],$$

$$S_{CDFM-Tc}(w)=F\left\{\sum_{i=1}^{N} q_i(t)\right\}=NAD_c\partial(w)+\left[\sum_{n=1}^{\infty}\left[\frac{A}{j\pi n}\left(\frac{1-e^{-\frac{j2\pi n}{L}}}{1-e^{\frac{-j2\pi n}{NL}}}\right)\sum_{k=1}^{L}\left[e^{\frac{-j2\pi nH_k}{T_m}}\left(1-e^{\frac{-j2\pi n\tau_k}{T_m}}\right)\right]\partial(w-nw_m)\right]=\right.$$

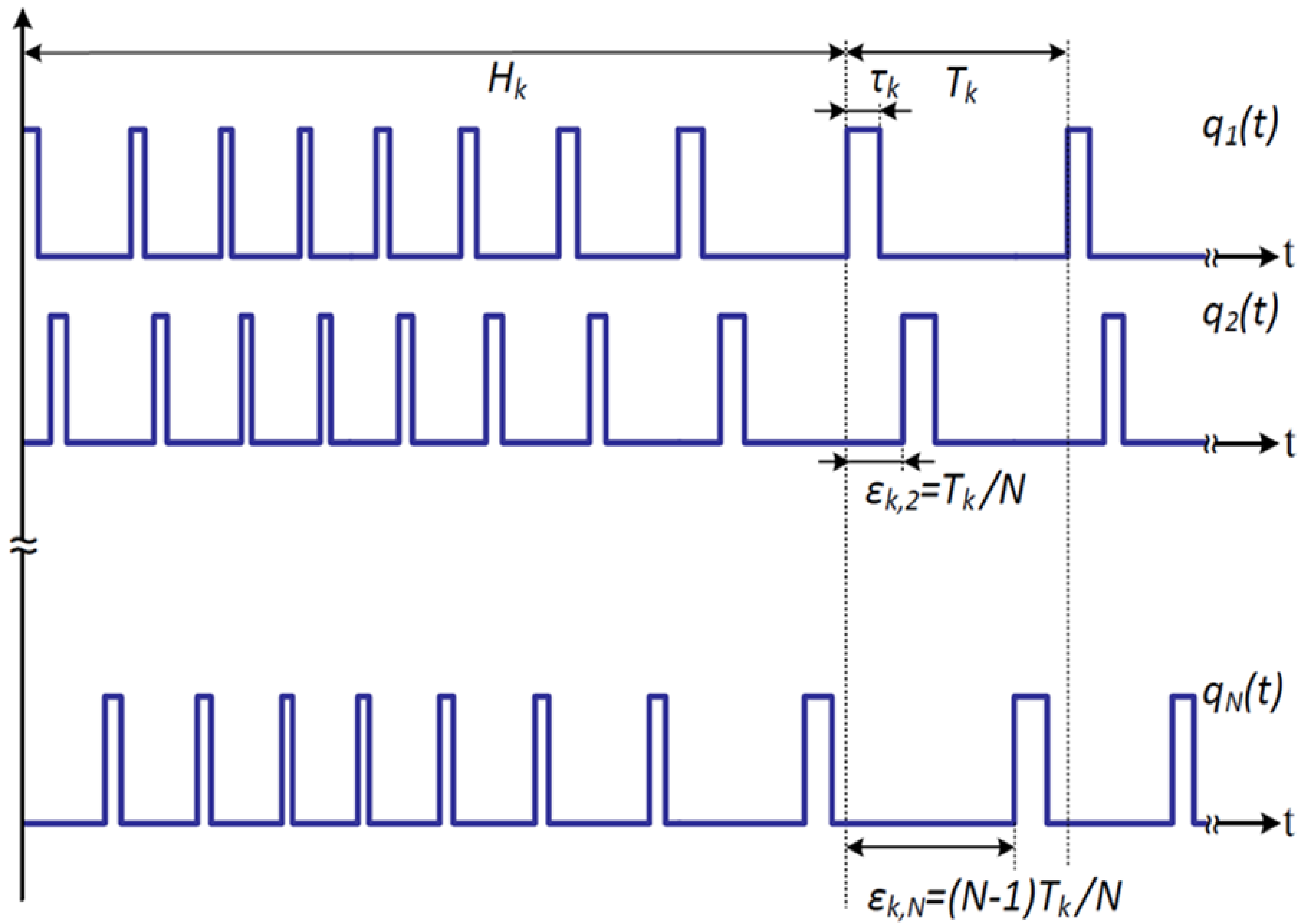
$$=NAD_c\partial(w)+N\cdot E_{CDFM-Tc}(w)\left[\sum_{n=1}^{\infty}\left[\frac{A}{j\pi n}\sum_{k=1}^{L}\left[e^{\frac{-j2\pi nH_k}{T_m}}\left(1-e^{\frac{-j2\pi n\tau_k}{T_m}}\right)\right]\partial(w-nw_m)\right]\right]$$

$$S_{VDFM}(w)=F\left\{\sum_{i=1}^{N} q_i(t)\right\}=NAD_c\partial(w)+\sum_{n=1}^{\infty}\left[\frac{A}{j\pi n}\sum_{k=1}^{L}\left[\left(\frac{1-e^{-\frac{j2\pi nT_k}{T_m}}}{1-e^{\frac{-j2\pi nT_k}{NT_m}}}\right)e^{\frac{-j2\pi nH_k}{T_m}}\left(1-e^{-\frac{j2\pi n\tau_k}{T_m}}\right)\right]\partial(w-nw_m)\right]$$

$\alpha_i=0$; τ_k control ; T_k modulated, $\varepsilon_k=(i-1)T_k/N$

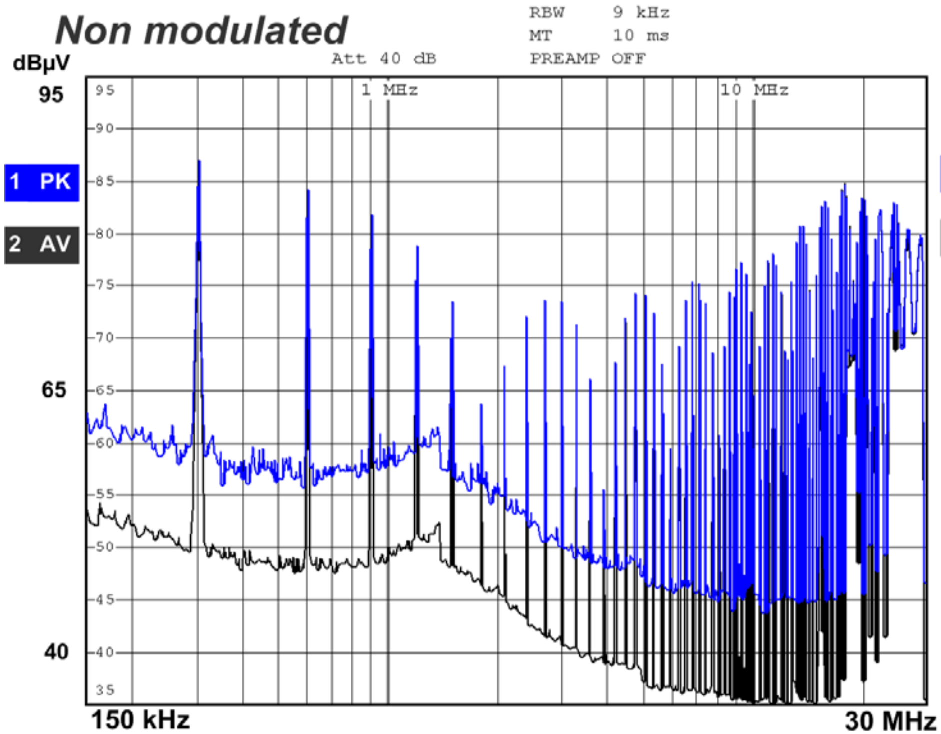
3.- Variable Delay Frequency Modulation

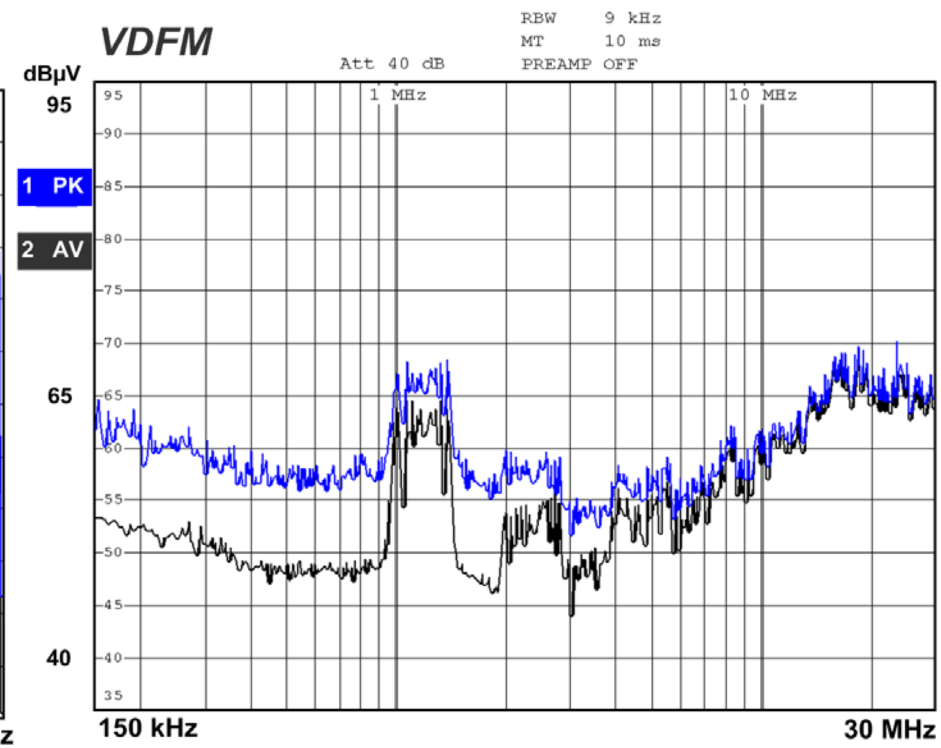
VDFM combines interleaving and SFM



$\alpha_i=0$; τ_k control ; T_k modulated, $\varepsilon_k=(i-1)T_k/N$

3.- Variable Delay Frequency Modulation

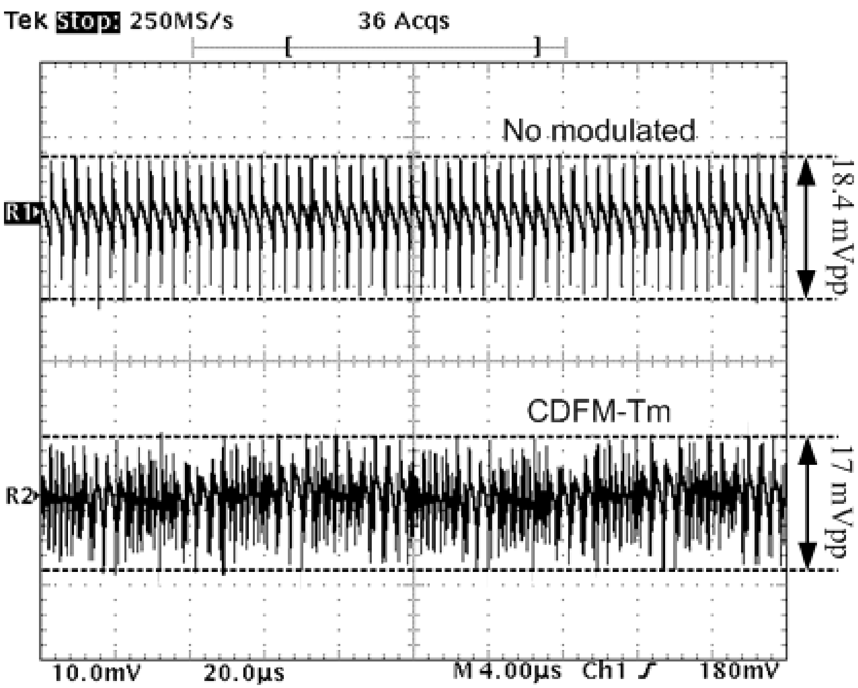


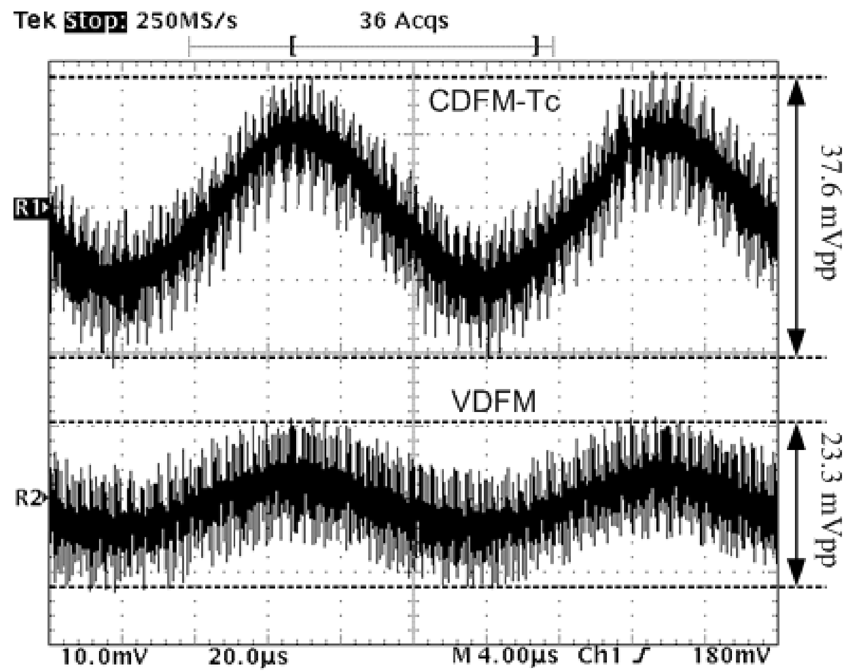


Example of VDFM performance:

$N=4$; $f_C=300kHz$; $m=6$

3.- Variable Delay Frequency Modulation



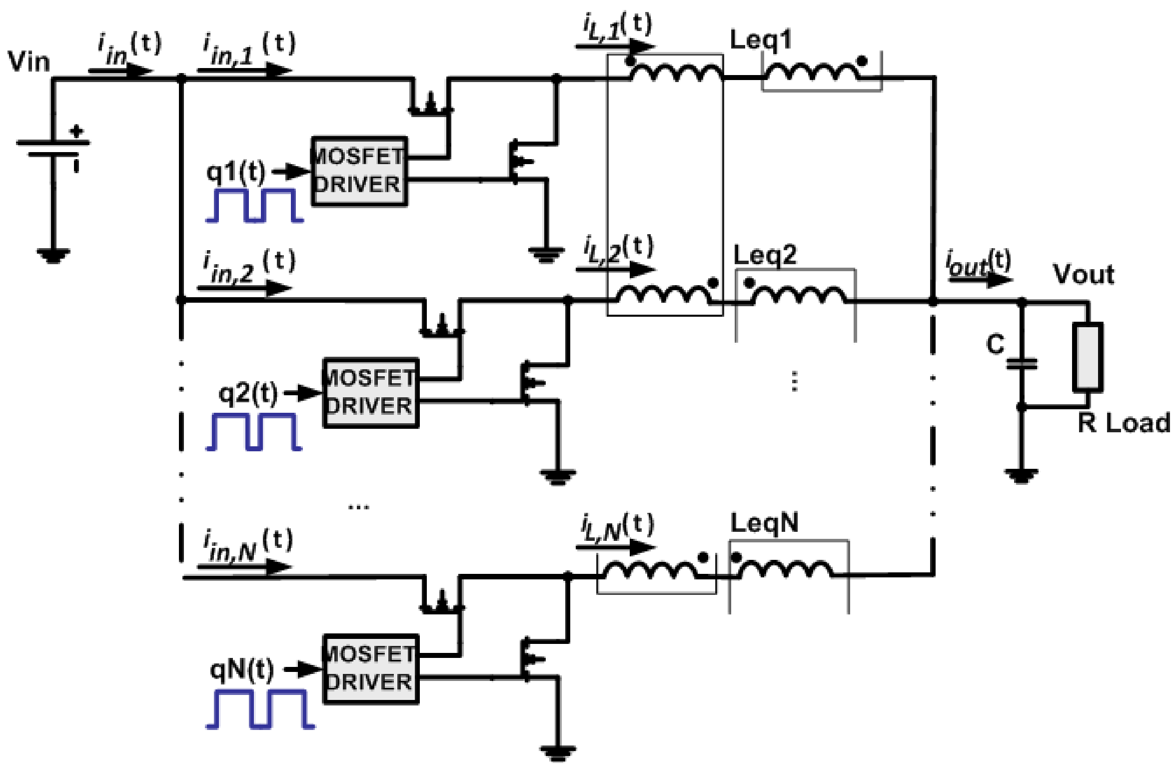


Example of VDFM performance:

$N=4$; $f_C=300kHz$; $m=6$

4.- Coupled Interleaved Multicellular Parallel Converter

We need a **SYMETRIC** system in order to prevent couplers saturation, that could lead to a catastrophic failure.



SYMETRIC

-Construction

- Gates drive

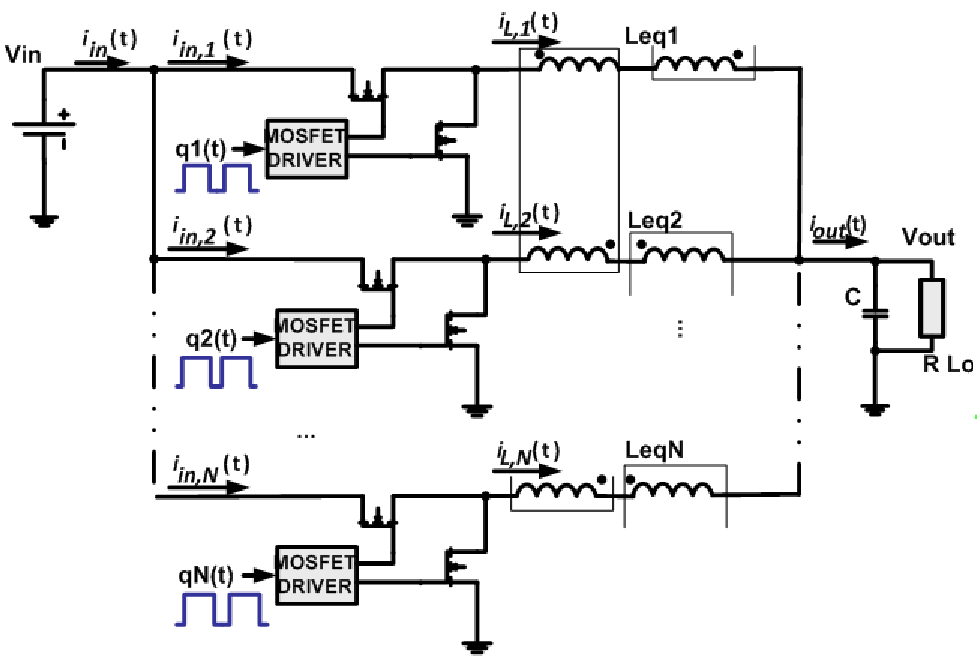
-Switching

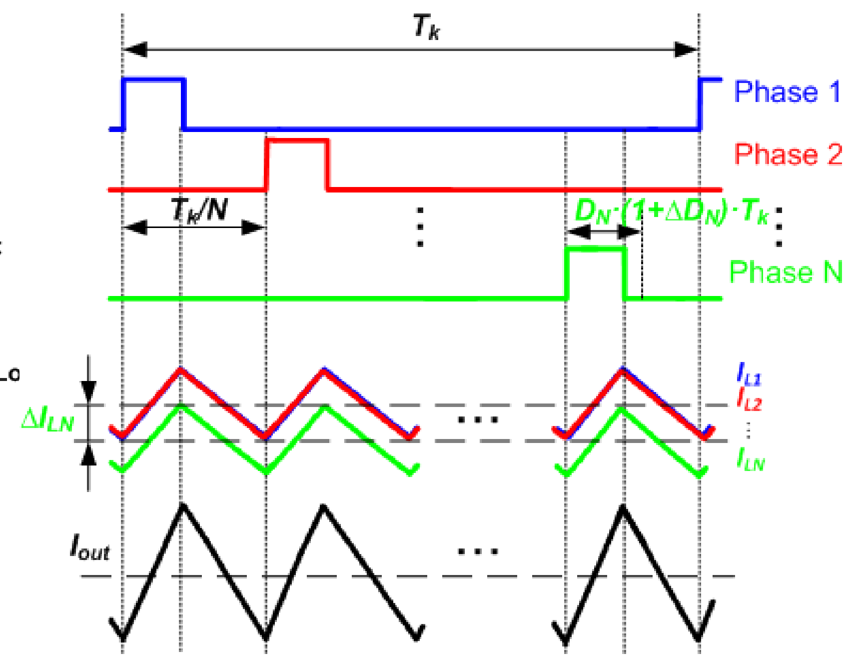
4.- Coupled Interleaved Multicellular Parallel Converter

Duty-cycle

For phase *N*

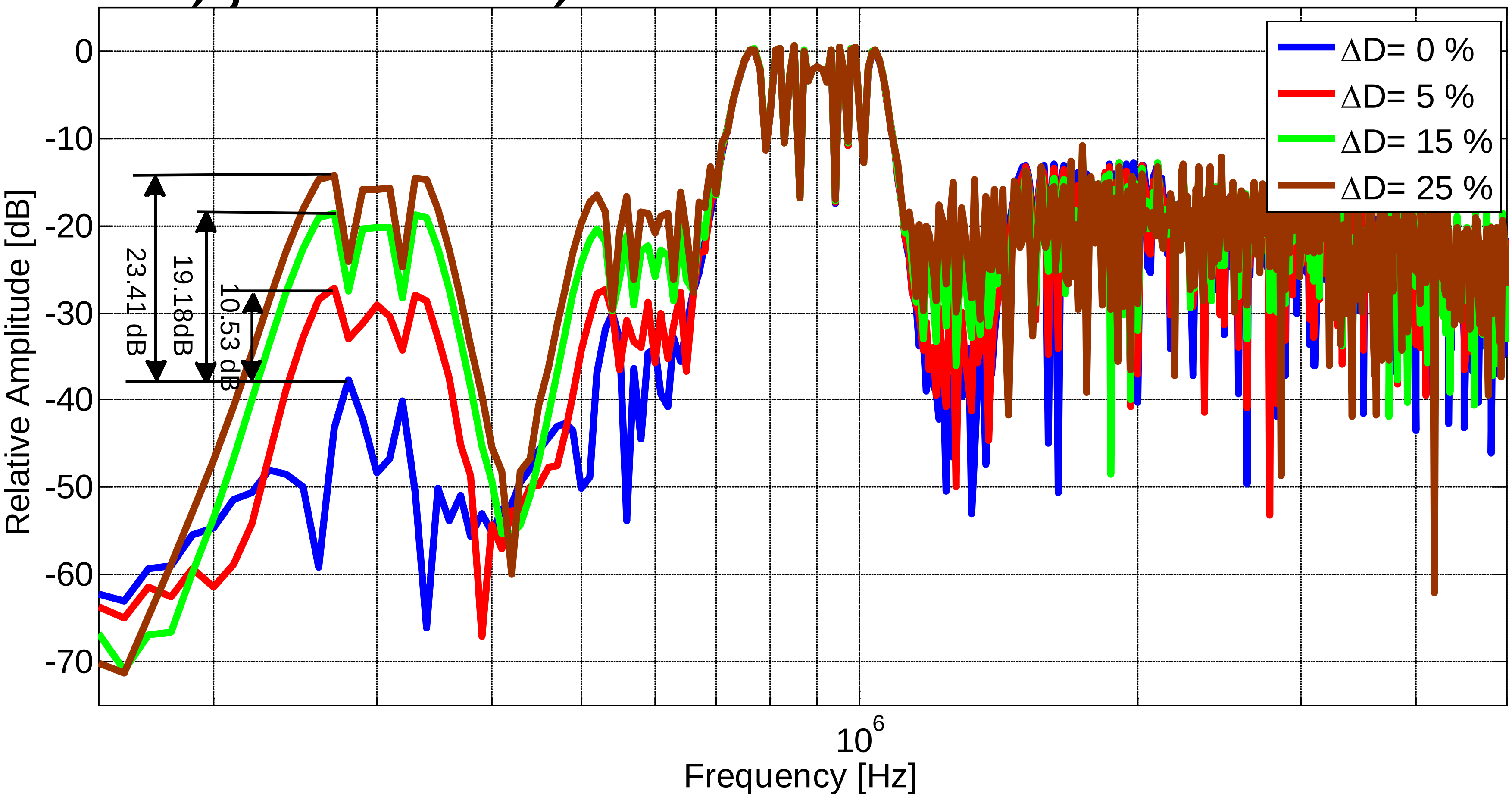
$$D_N = D_c \cdot (1 + \Delta D)$$





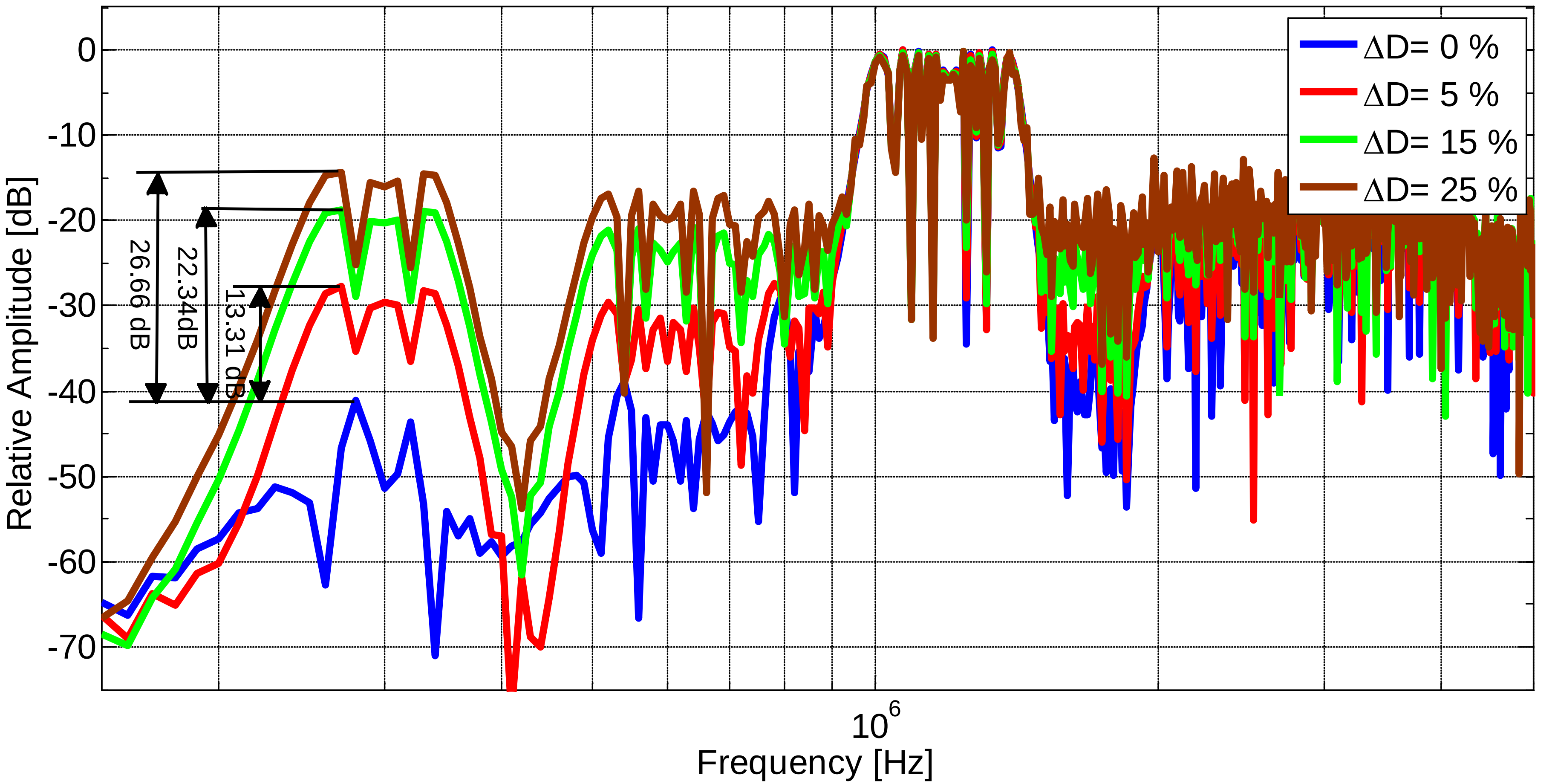
4.- Coupled Interleaved Multicellular Parallel Converter

N=3 ; fc=300kHz ; m=6



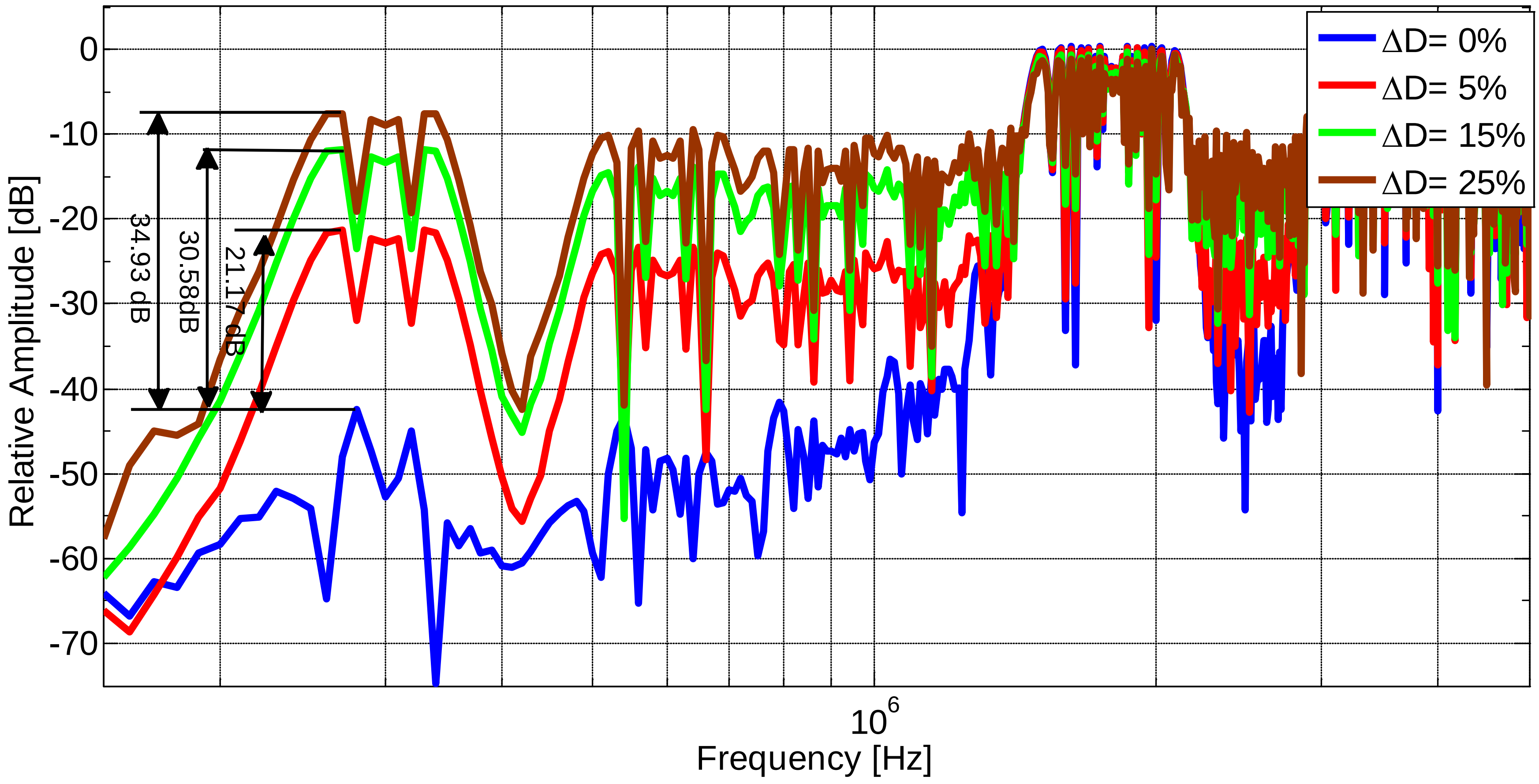
4.- Coupled Interleaved Multicellular Parallel Converter

N=4 ; fc=300kHz ; m=6

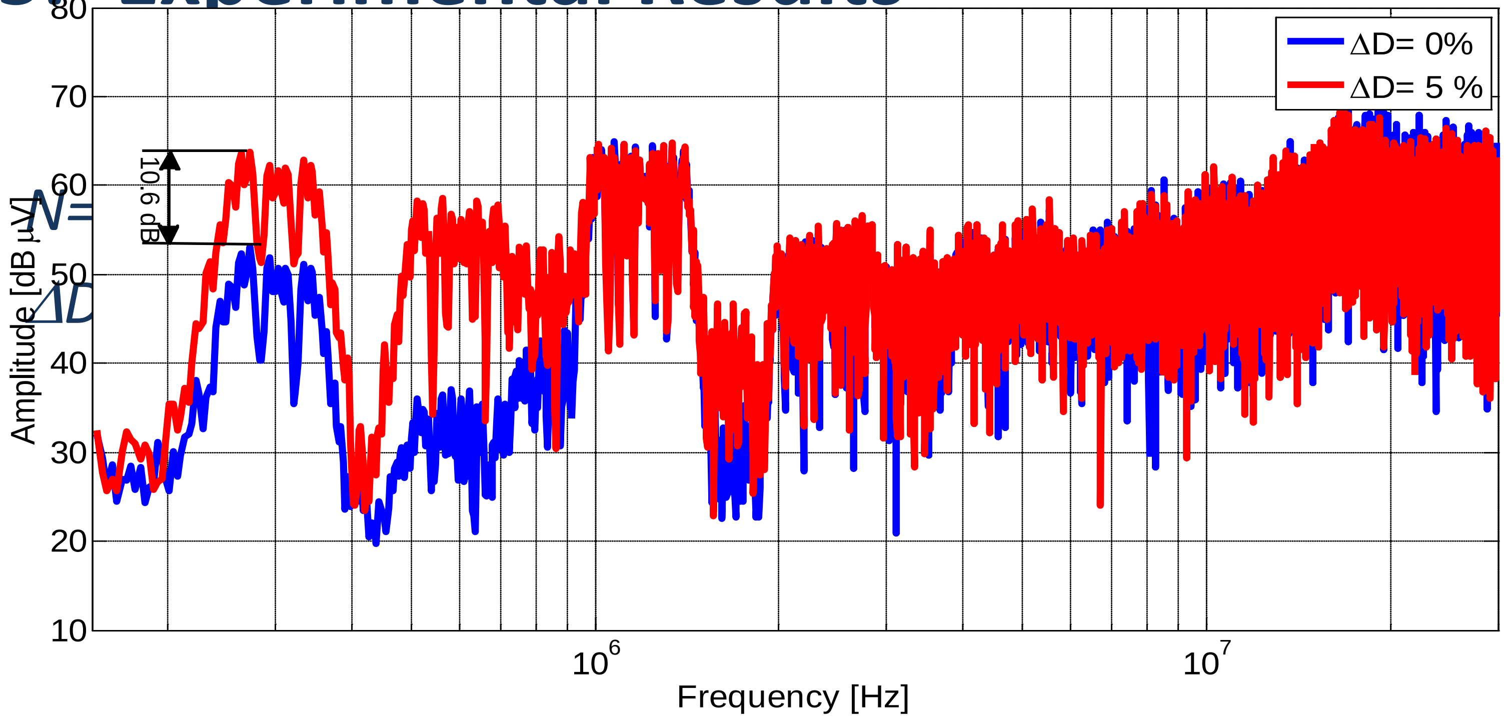


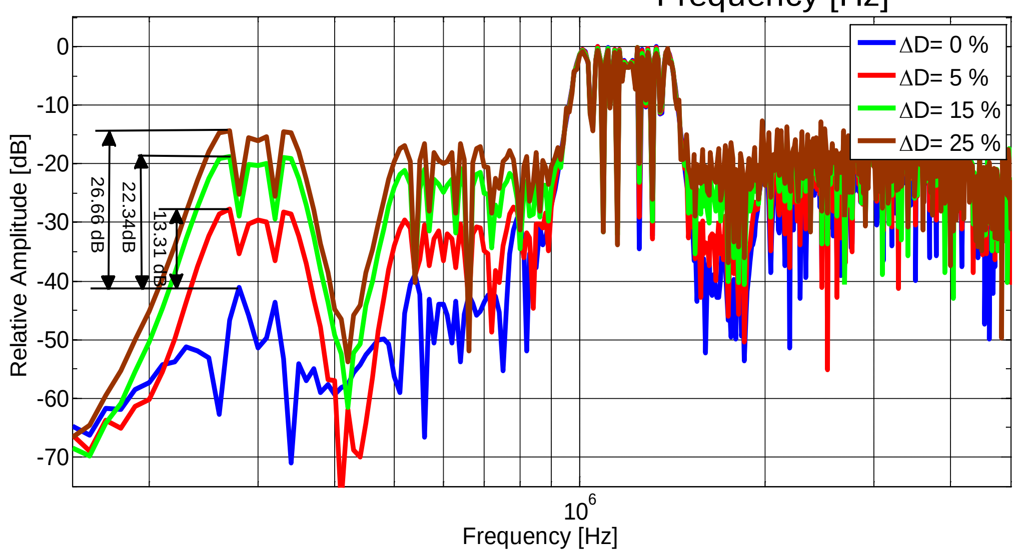
4.- Coupled Interleaved Multicellular Parallel Converter

N=6 ; fc=300kHz ; m=6

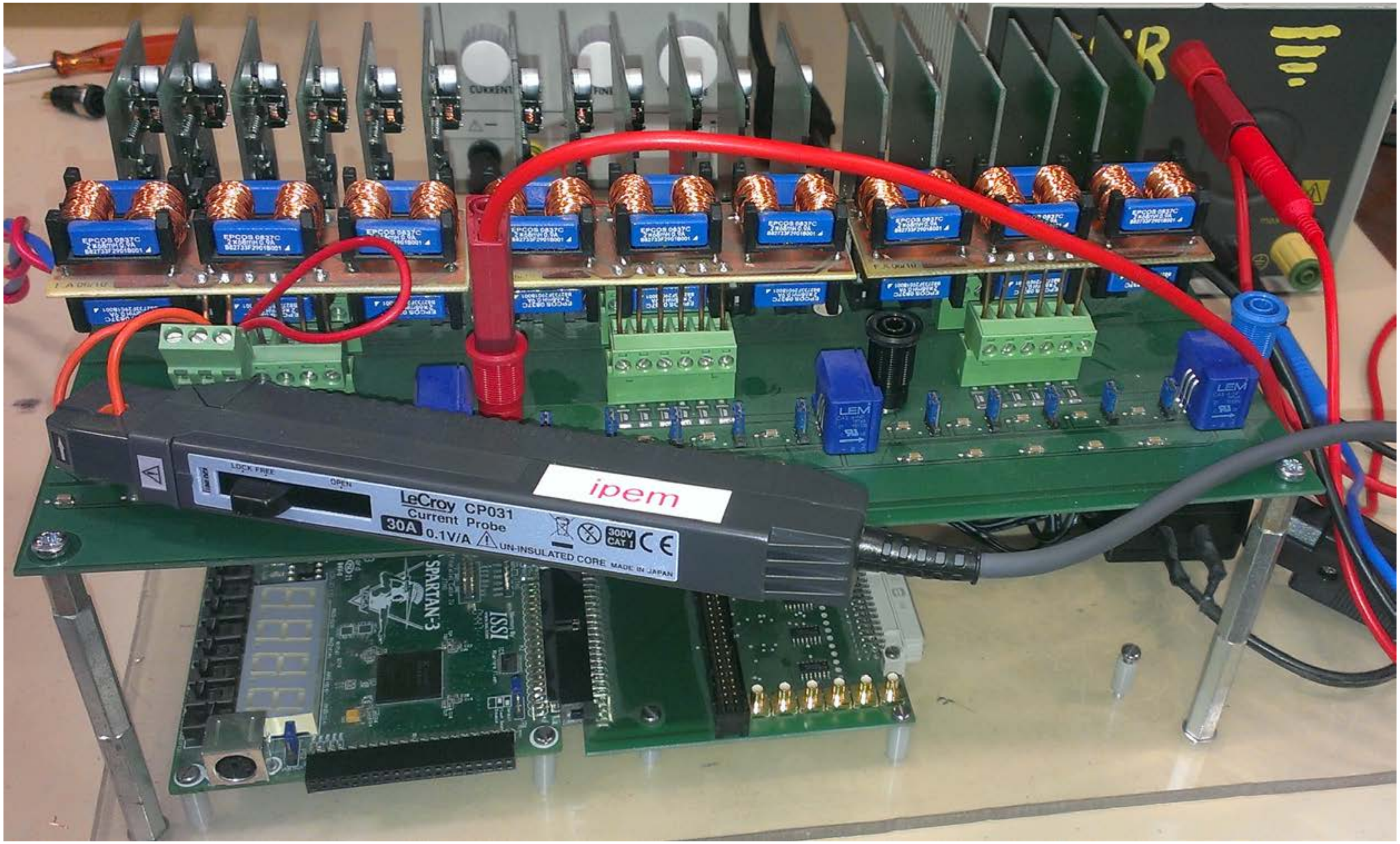


5.- Experimental Results



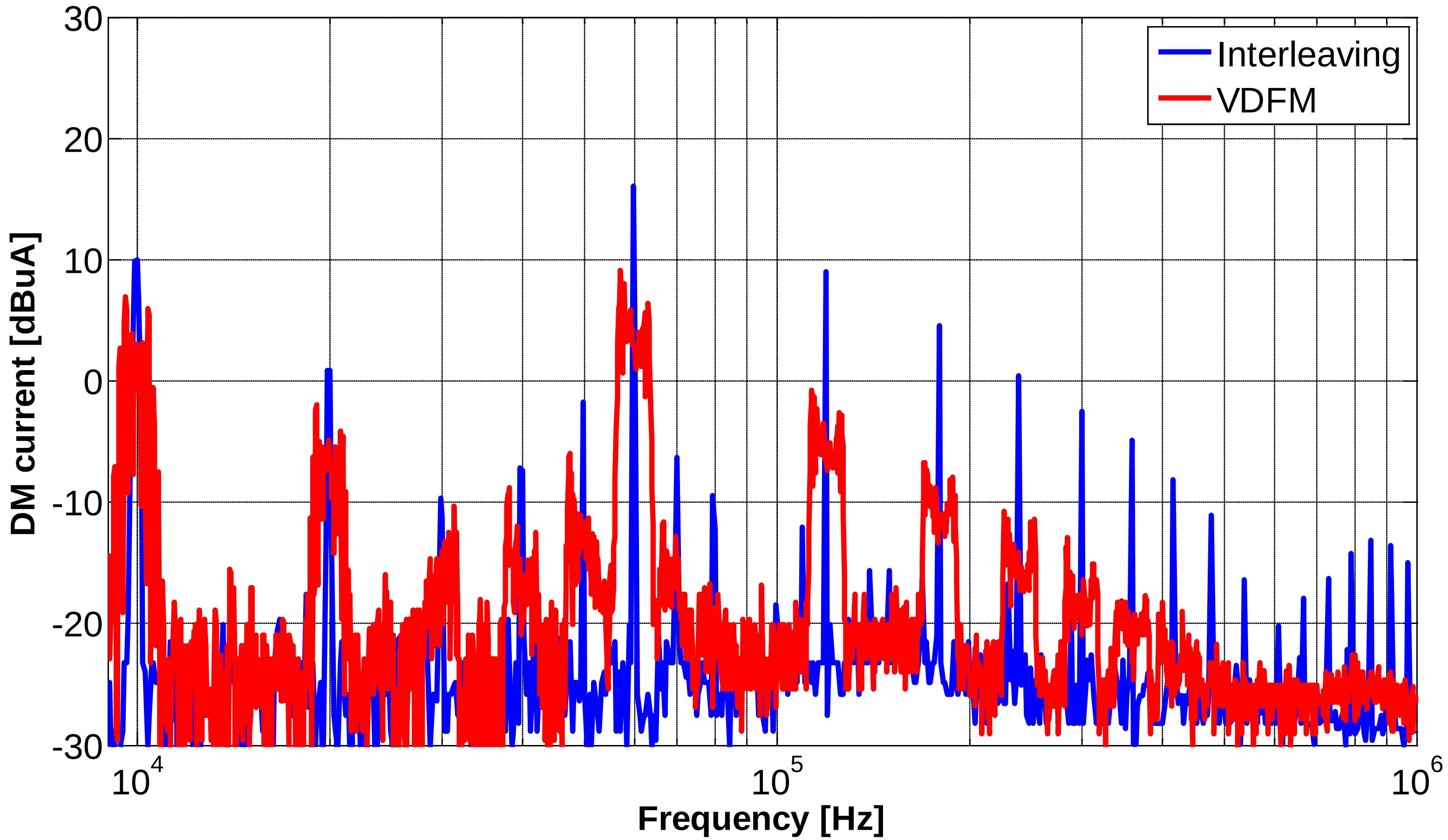


5.- Experimental Results



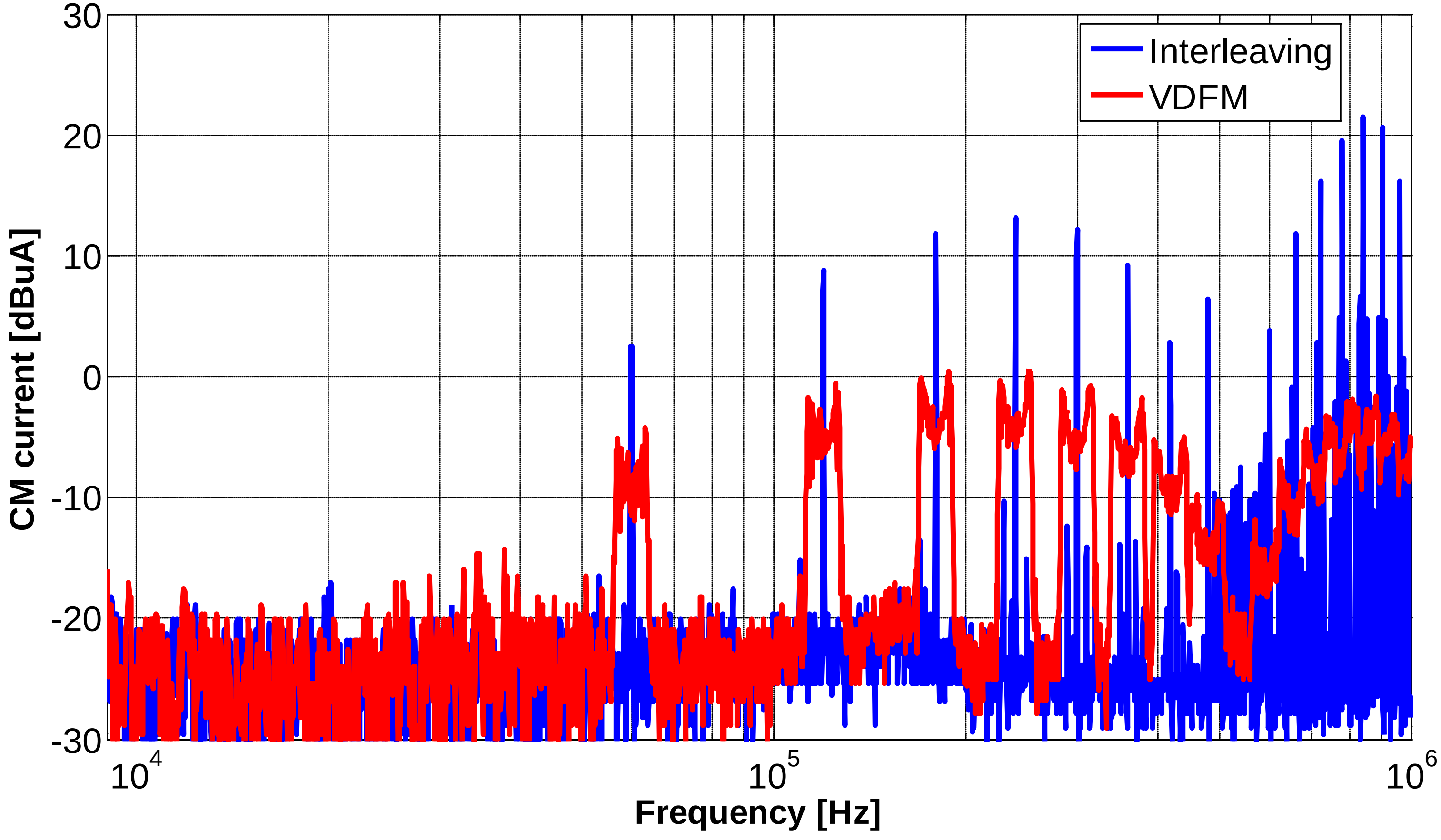
CIMPC N=6 ; DC/DC ; Vin= 311V ; Vout= 48V ; Po=250W

5.- Experimental Results



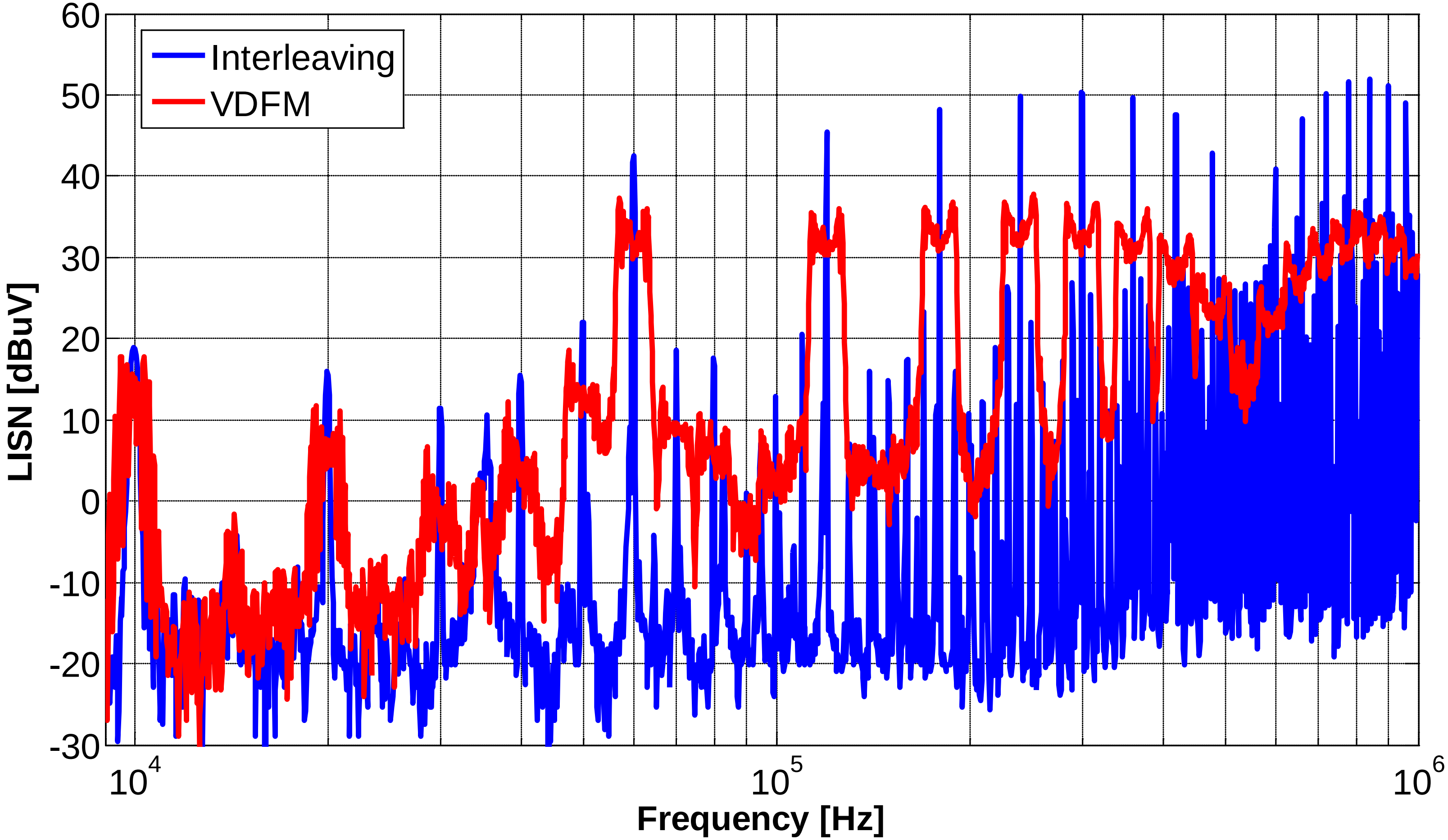
N=6 ; fc=10kHz ; m=6

5.- Experimental Results



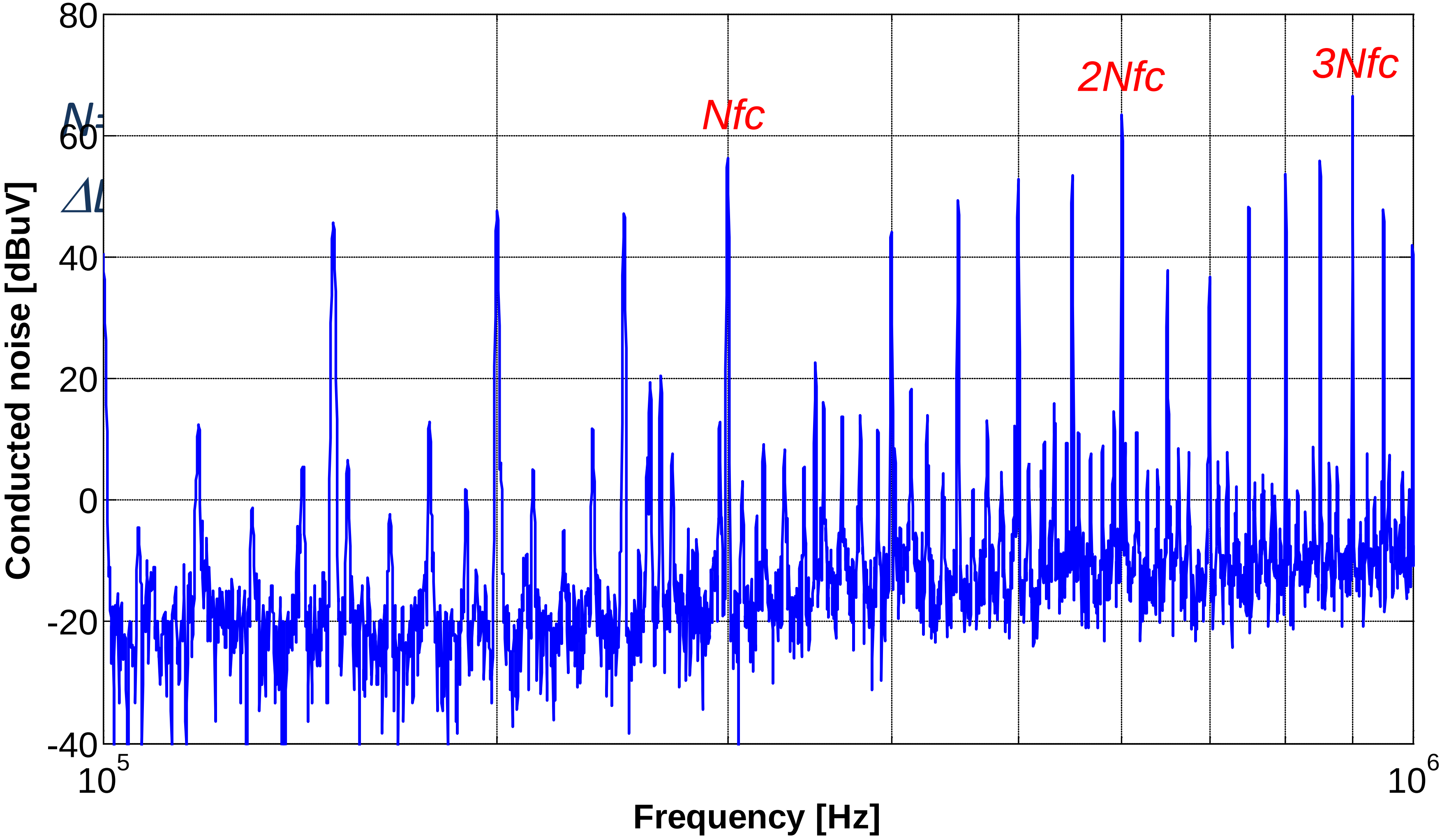
N=6 ; fc=10kHz ; m=6

5.- Experimental Results



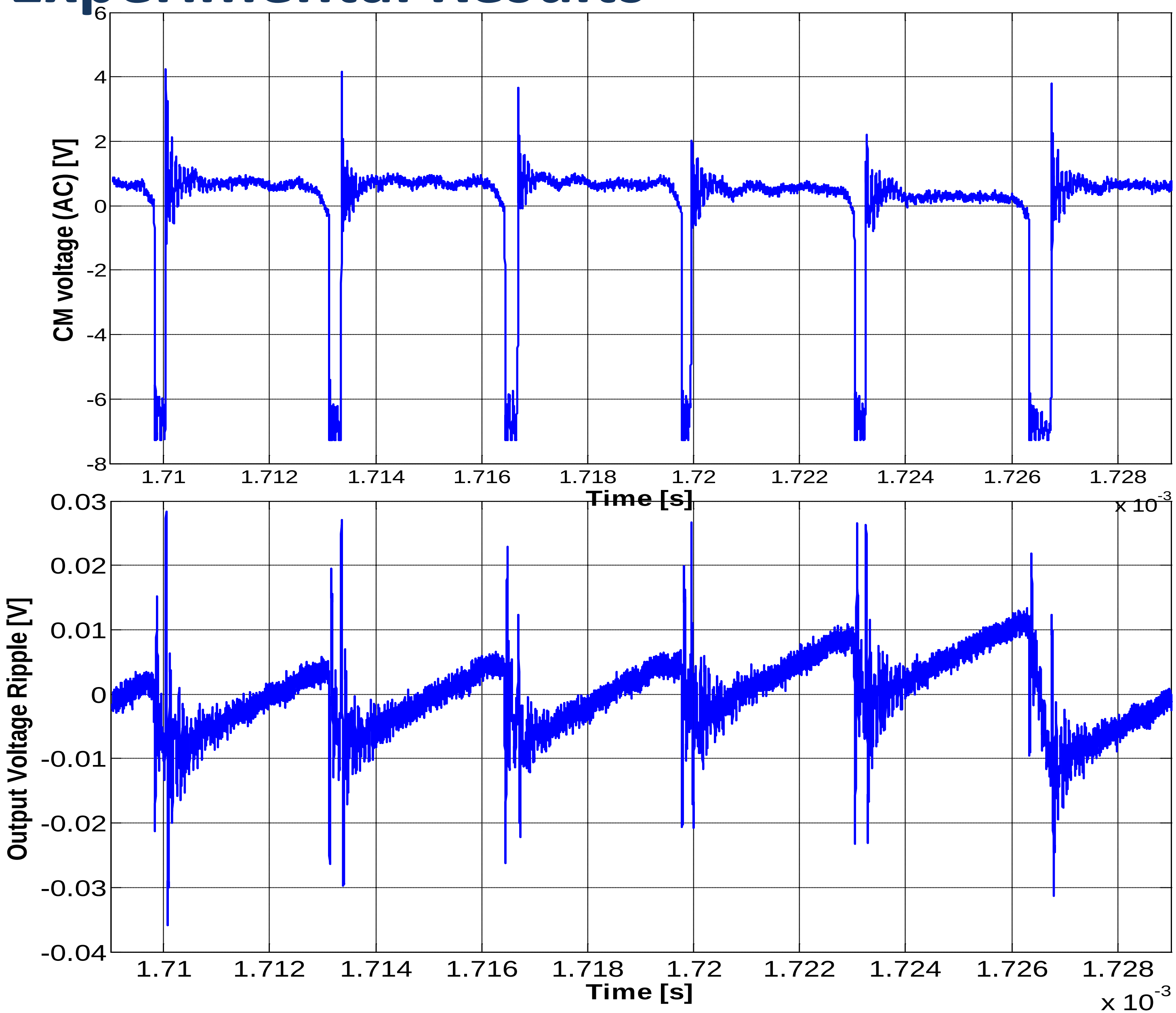
N=6 ; fc=10kHz ; m=6

5.- Experimental Results



N=6 ; fc=50kHz ; m=6

5.- Experimental Results



5.- Conclusions

-VDFM could be applied successfully to CIMPC to suppress conducted noise

-New Devices (SiC, GaN) are candidates to use this technique

-Duty-cycle deviations (ΔD) produce the following effects:

- *None at Nfc*
- *Attenuation degradation is noticed below Nfc*
- *Attenuation degradation increases with N*

- Precise timing in gate-drive signals is a keypoint for this particular application