



DOCTORATE PROGRAM IN **ELECTRONIC ENGINEERING**

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**DOCTORAL TRAINING SEMINARS:** RESEARCH PROJECTS IN  
THE DEPARTMENT OF ELECTRONIC ENGINEERING

**TERASCALE MEMORY SYSTEMS IN FUTURE CMOS AND  
POST-CMOS TECHNOLOGIES**

**Antonio Rubio**

**February 11th, 2014**

PROGRAMA DE DOCTORAT EN **ENGINYERIA ELECTRÒNICA**

*Jornades formatives 2014: Projectes de recerca al Departament d'Enginyeria Electrònica*



UNIVERSITAT POLITÈCNICA DE CATALUNYA  
BARCELONATECH  
Departament d'Enginyeria Electrònica

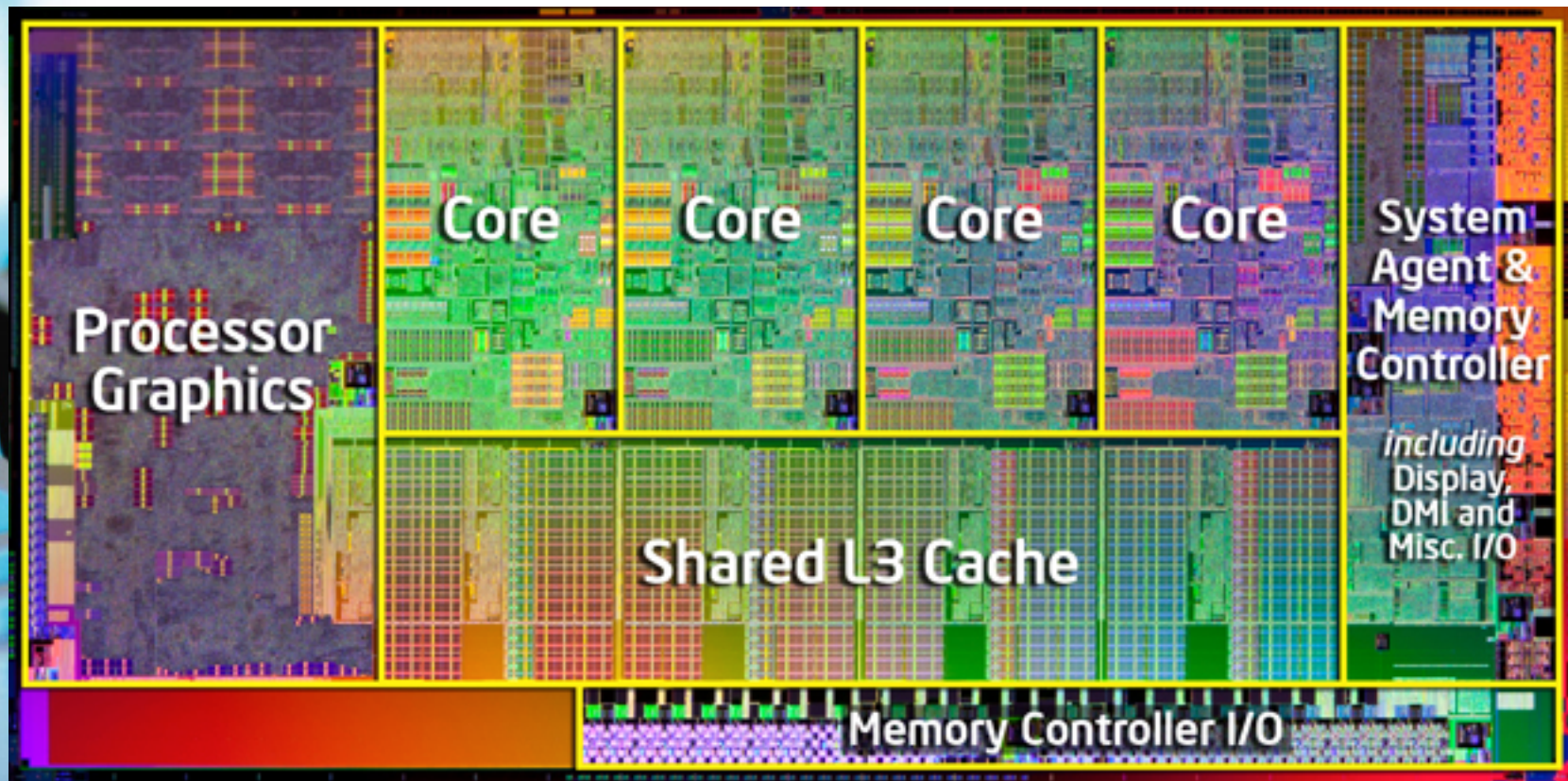
# 1. Introduction

## MOTIVATION

Memories are a key technology driver in semiconductor industry, having an extremely important role in terascale multicore microprocessors

In such systems cores and memory may exhibit high failure rates due to process variations and devices degradation mechanisms.

# 1. Introduction



Intel i7

# 1. Introduction

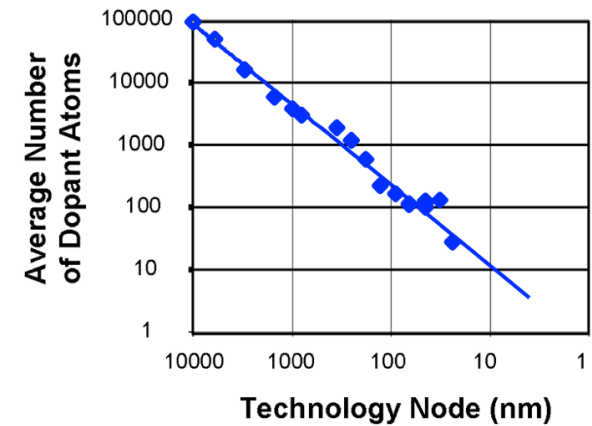
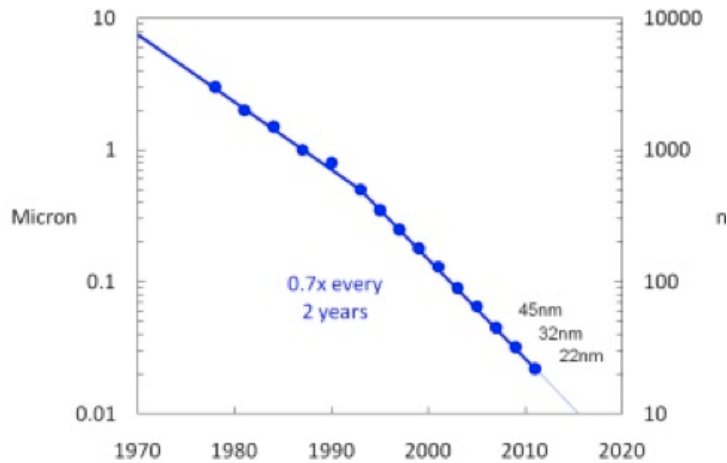
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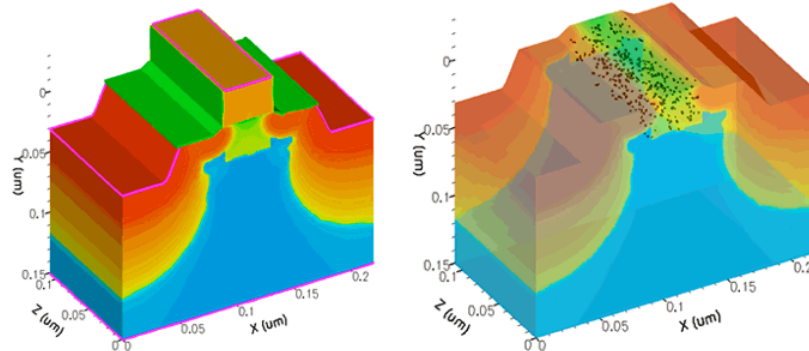
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# 1. Introduction

## MOTIVATION

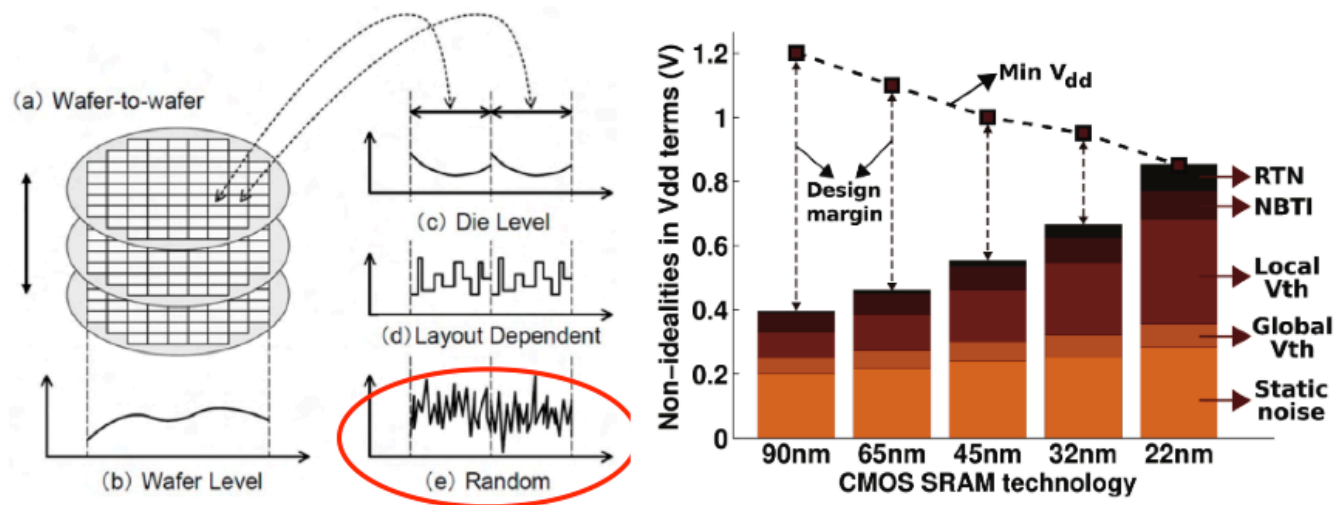


Caption: Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor.



# 1. Introduction

The dramatic Variability drawback



After K. Takeuchi (NEC)

# 1. Introduction

## Technology Outlook

High Volume Manufacturing	2008	2010	2012	2014	2016	2018	2020	2022
Technology Node (nm)	45	32	22	16	11	8	6	4
Integration Capacity (BT)	8	16	32	64	128	256	512	1024
Delay Scaling	>0.7			~1?				
Energy Scaling	~0.5			>0.5				
Transistors	Planar			3G, FinFET				
Variability	High			Extreme				
ILD	~3			towards 2				
RC Delay	1	1	1	1	1	1	1	1
Metal Layers	8-9	0.5 to 1 Layer per generation						

Source: Intel's Corporate Technology Group

# 1. Introduction

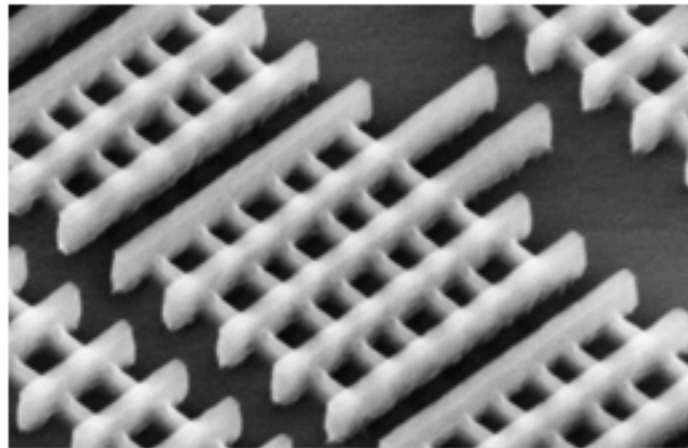
A real sophisticated solution for at least 3 generations!!!

## Intel Increases Transistor Speed by Building Upward

By JOHN MARKOFF

Published: May 4, 2011

HILLSBORO, Ore. — Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.



Intel's new transistors have tiny pillars, or fins, that rise above the chip's surface.



## 2.- Description of the problem addressed

### Objectives of the TRAMS project

To investigate the impact of statistical variability and reliability of near and beyond the end of the ITRS devices on Terabit memory design.  
(Sub-16nm bulk (18,13nm) CMOS, Sub 10nm Finfet, 15nm III-V/Ge and CNT)  
(WP1-WP2)

To design, implement, deploy and assess compensating techniques and countermeasures at circuit and microarchitectural level for memories used in multicore processors  
(WP3-WP4)

To develop a methodology for specifying and implementing performance-, power- and reliability –aware reconfiguration policies for multicore processor.  
(WP4)

# 3.- How we addressed the problem – technical justification

**TRAMS**

**TERASCALE RELIABLE ADAPTIVE  
MEMORY SYSTEMS**

**EU COLABORATIVE PROJECT**

**FET FP7 248789**

**1/1/2010 to 31/12/2012**



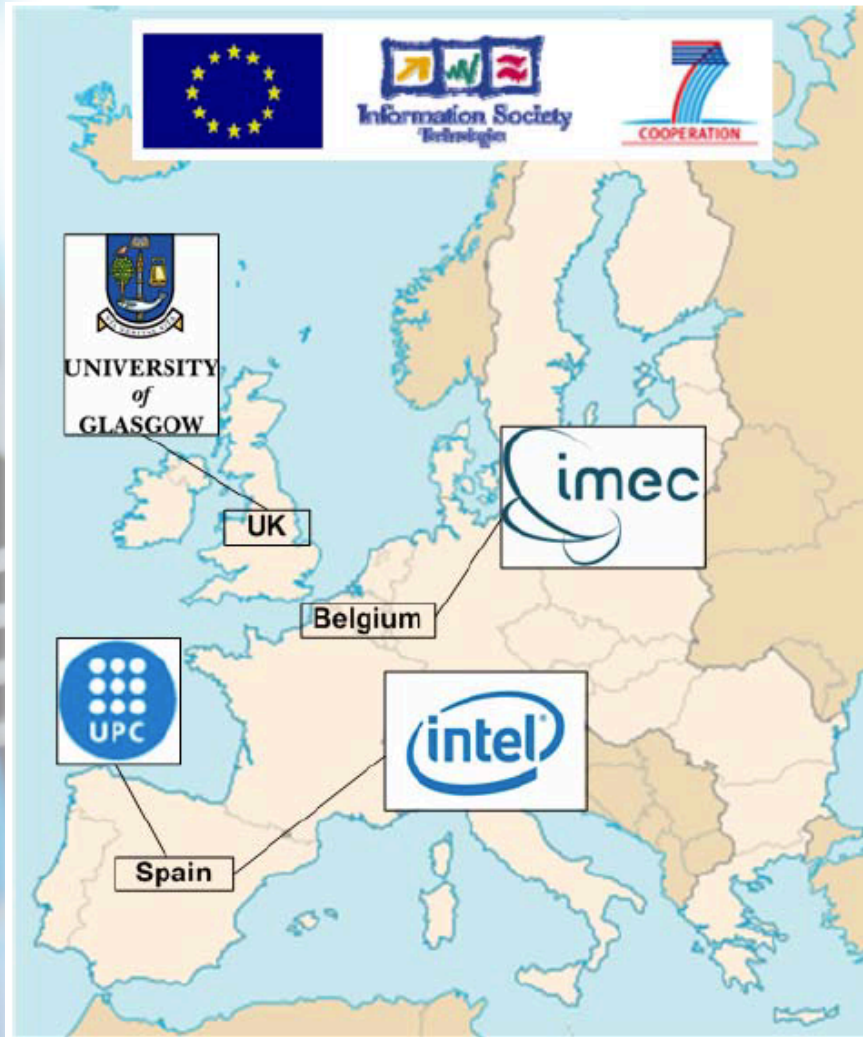
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### 3.- How we addressed the problem – technical justification




#### THE CONSORTIUM



# 4. What have we done – project description

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To develop a methodology for specifying and implementing performance-, power- and reliability –aware reconfiguration policies for multicore processor. (WP4)

PDK for
18, 13nm Bulk MOSFET
32, 16nm CNT MOSFET
10nm FinFET MOSFET
15nm III-V/ Ge MOSFET
<b>Memory cells</b>
6T
3T1D
 UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Departament d'Enginyeria Electrònica

# 4. What have we done – project description

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<b>Mechanisms</b>
regular layout
design rules
redundancy
latency detection
reconfiguration
compensation
T, performance, time violation, particles impact sensors
monitor injection

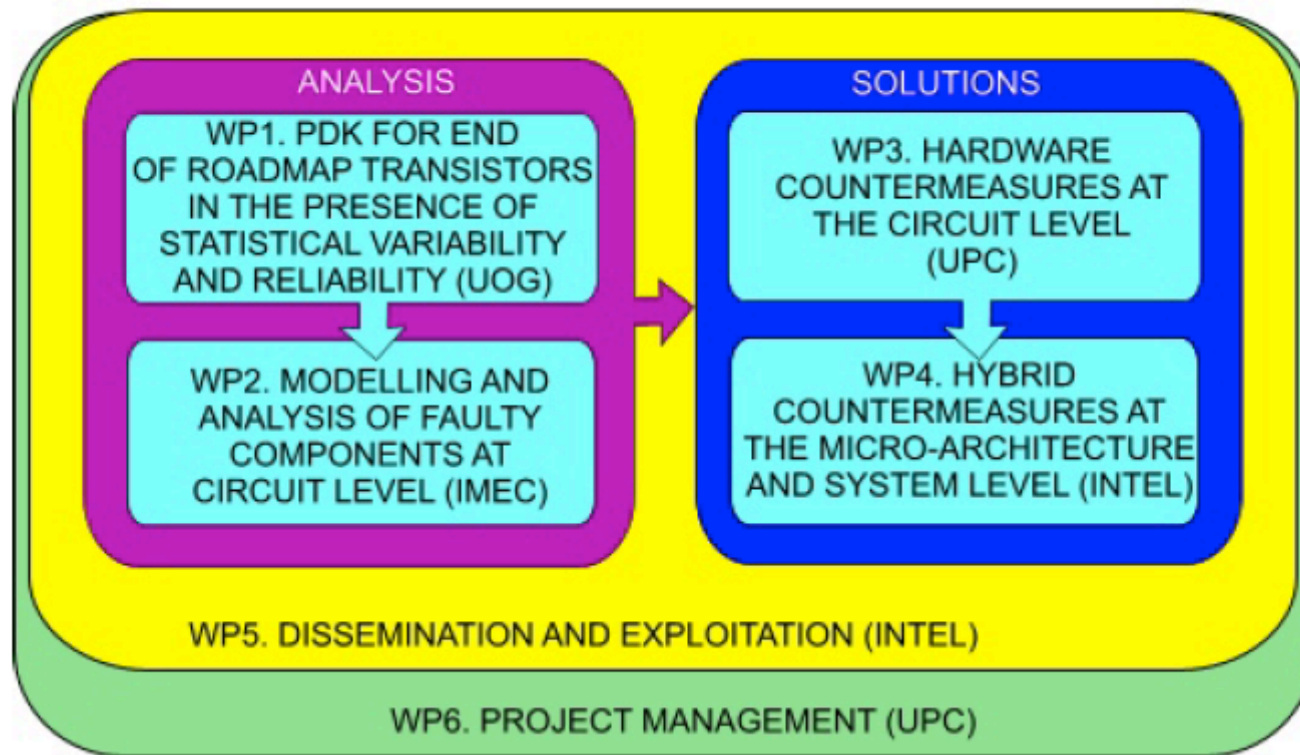
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To design, implement, deploy and assess compensating techniques and countermeasures at circuit and microarchitectural level for memories used in multicore processors (WP3-WP4)
To develop a methodology for specifying and implementing performance-, power- and reliability –aware reconfiguration policies for multicore processor. (WP4)

Mechanisms
Phase identifier mechanisms
Memory blocks reconfiguration
Hybrid counter-measures
Multicore platform policies
Live demo

# 5. How – resources used

## TRAMS WPs



# 5. How – resources used

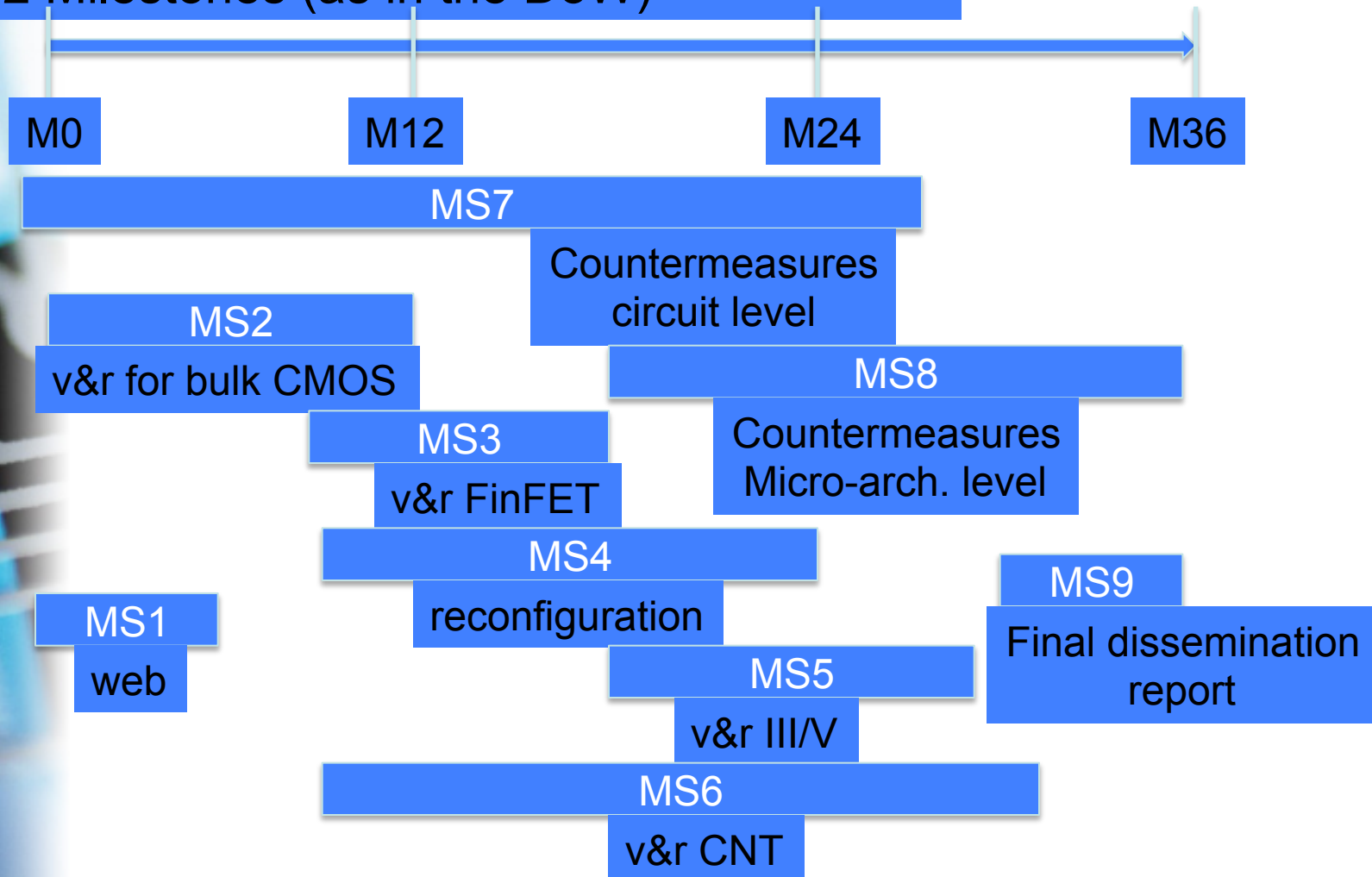
## WT1 List of work packages

Project Number <sup>1</sup>	248789	Project Acronym <sup>2</sup>	TRAMS			
LIST OF WORK PACKAGES (WP)						
WP Number <sup>53</sup>	WP Title	Type of activity <sup>54</sup>	Lead beneficiary number <sup>55</sup>	Person-months <sup>56</sup>	Start month <sup>57</sup>	End month <sup>58</sup>
WP 1	PDK for end of roadmap transistors in the presence of statistical variability and reliability	RTD	4	81.00	1	36
WP 2	Modelling and analysis of faulty components at circuit level	RTD	2	41.00	1	36
WP 3	Hardware countermeasures at the circuit level	RTD	1	105.00	1	36
WP 4	Hybrid countermeasures at the micro-architecture and system level	RTD	3	134.00	1	36
WP 5	Exploitation and Dissemination	OTHER	3	19.00	1	36
WP 6	Management	MGT	1	12.50	1	36
Total				392.50		



# 5. How – resources used

## 1.2 Milestones (as in the DoW)



# 5. How – resources used

The research team at UOG

The research team at UPC

Name	Position	Role
Antonio RUBIO	Professor	PC, research WP1,2,3 and leader WP3
Joan FIGUERAS	Professor	Research WP3
Ramon CANAL	Ass. professor	Research WP3,4
Luz BALADO	Ass. Professor	Finfets circuits
Esteve AMAT	Postdoctoral	1T3D
Ioana VATAJELU	PhD student	SRAM robustness evaluation
Carmen GARCIA	PhD student	CNTFETs
Nivard Aymerich	PhD student	Hardware redundancy
Peyman Pouvan	PhD student	Reconfiguration
Shrikanth Ganapathy	PhD student	Adaptive mechanisms
Zoran Jacksic	PhD student	Finfet circuits
Enric AMATLLER	Undergraduate	Layout level
Santi PEREZ	Technician	Web administrator

Name	Position	Role
J-Llorenç Cruz	Ass. professor	Researcher
Tanausu Ramirez	Researcher	Researcher
Enric Herrero	Researcher	Researcher
Nicholas Axelos	Researcher	Researcher
Antonio Calomarde	Ass. Professor	Dynamic memories
Jordi Tubella	Ass. Professor	Researcher

Name	Position	Role
Asen Asenov	Professor	Leader WP1
Binjie Cheng	Researcher	Compact model extraction strategy and technology
Andrew Brown	Researcher	FinFET simulation including statistical variability
Si-Yu Liao	Researcher	Drift-diffusion and Monte Carlo simulation of III-V
Daryoosh Dideban	Researcher	Statistical compact model extraction
Hamid Amini Moghedaban	Researcher	Physical FinFET simulation
Negin Moezi	Researcher	Nominal and statistical compact model extraction

The research team at Imec

Name	Position	Role
Mustafa Badaroglu	Team leader	Technical contributor
Miguel Miranda	Principal Scientist	Project responsible
Paul Zuber	Senior Researcher	WP2 leader
Arindam Mallik	Researcher	Technical contributor

The research team at Intel

Name	Position	Role
Antonio Gonzalez	Senior PE	Leader Intel
Xavier Vera	Senior Research Scientist	WP3, WP4 Leader WP4
Javier Carretero	Research Scientist	AVF models
Matteo Monchiero	Senior Research Scientist	Reconfiguration engine
Tana Ramirez	Senior Research Scientist	UserX
Enric Herrero	Senior Research Scientist	Demos

# 6. Main results

Intense research, intensive dissemination



## STRATEGIC PLAN OF TRAMS PROJECT (DOW)

The TRAMS project will deliver circuit, microarchitecture and system level countermeasures for unreliable components by utilizing hybrid solutions and better than worst-case design.

## DISSEMINATION OF FOREGROUND (DOW)

Actions to disseminate results of the project:

- ✓ Technical and scientific publications
- ✓ Reports (public, private)
- ✓ Organization of international workshops and seminars to promote TRAMS results
- ✓ Web page (public docs, description of the project, publications, agenda, ...)
  
- ✓ No patent or trademark has been generated with exception of the TRAMS logo  
Trademark
- ✓ TRAMS does not contribute directly to specific standards

# DISSEMINATION OF RESULTS

## WEB PAGE

www.trams-project.eu

Description, agenda, activities, publications, public docs, intranet

The screenshot shows the homepage of the Terascale Reliable Adaptive Memory Systems Project (TRAMS). It features a header with navigation links (HOME, SITE MAP, CONTACT, LOG IN) and a search bar. Below the header is a banner image of a circuit board. The main content area includes a navigation menu (CONTACT, CONSORTIUM, OBJECTIVES, DESCRIPTION, PUBLICATIONS, PUBLIC DELIVERABLES, INTRANET) and a large text block describing the project's goals and challenges. A sidebar on the right contains a calendar and a list of recent news items. At the bottom, there are logos for partner institutions like the University of Glasgow and funding opportunities from ESSDERC 2012.

This screenshot displays the 'Publications' section of the TRAMS website. It features a navigation menu and a list of research papers. Each entry includes a title, authors, and a brief abstract. The list covers various topics such as 'Multi-obligant nanoscale architecture based on linear threshold gates with redundancy', 'Adaptive fault-tolerant architecture for unreliable technologies with heterogeneous variability', and 'Process variability-aware proactive reconfiguration techniques for mitigating aging in nano-scale SRAM memories'. The page also includes a sidebar with 'Project leaflets and posters' and 'TRAMS intranet manual'.

The screenshot shows the TRAMS project intranet. It features a header with navigation links and a search bar. The main content area includes a navigation menu (CONTACT, CONSORTIUM, OBJECTIVES, DESCRIPTION, PUBLICATIONS, PUBLIC DELIVERABLES, INTRANET) and a large text block. A sidebar on the right contains a list of links for 'PMB and PTC meetings and documents', 'PMB planned actions', 'Internal documents by Workshops', and 'Reviewer's area'. The page also includes a 'Welcome to the TRAMS project intranet' message and a 'last modified' timestamp.

PROC

IRAT

!4: Proje

CTF

d'Enginyeria Electrònica

ALUNYA

## EXPLOITABLE FOREGROUND

PDK for 18, 13nm bulk CMOS technology, BSIM models	Technology, SRAM, FinFET assessments
PDK for 32 and 16nm CNTFET technology, BSIM models	Injection methods
PDK for 10nm FinFET technology, BSIM models	3T1D DRAM assessment (FinFET)
PDK for 15nm III-V/Ge technology, BSIM models	New full error recovery memory
Advanced process variations sensors, + particle strike	New Hybrid fault recovery mechanisms
Dynamic fine-grain body bias adaption	Advance performance power/robust. prediction
Degradation redundancy principles	Functional mitigation for streaming
New mechanisms to extend life time of memory systems	AVF models for memory structures
New fault tolerant architectures, degradation resonance	2-LEVEL reconfiguration engine
Delay and temperature sensors	SER assessment tool

# Pieces of Work

- CNT and FinFET modelling
- Circuit level countermeasures to compensate variability and improve reliability