DOCTORATE PROGRAM IN ELECTRONIC ENGINEERING

DOCTORAL TRAINING SEMINARS: RESEARCH PROJECTS IN THE DEPARTMENT OF ELECTRONIC ENGINEERING

TERASCALE MEMORY SYSTEMS IN FUTURE CMOS AND POST-CMOS TECHNOLOGIES

Antonio Rubio

February 11th, 2014

PROGRAMA DE DOCTORAT EN ENGINYERIA ELECTRÒNICA

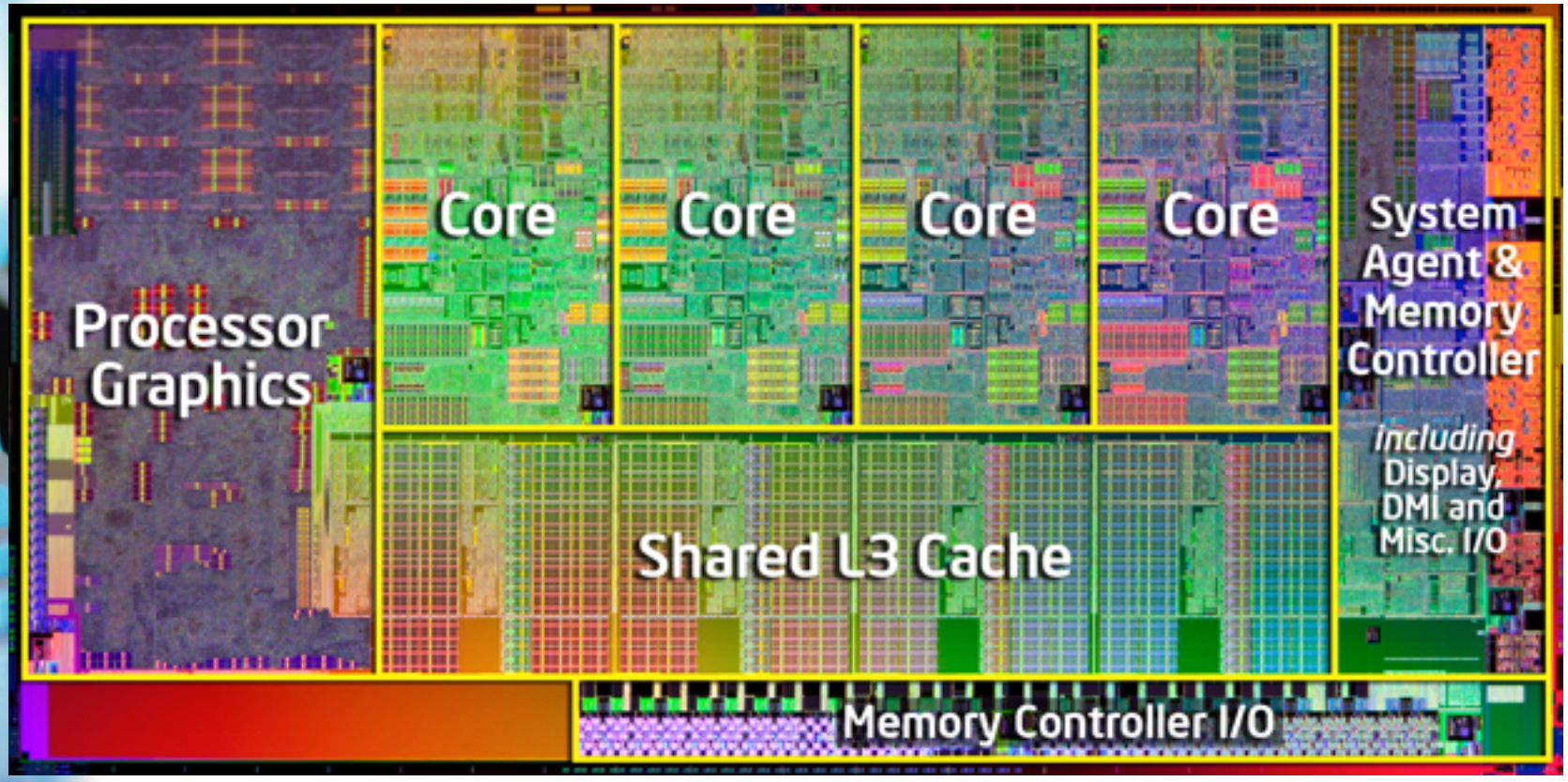
Jornades formatives 2014: Projectes de recerca al Departament d'Enginyeria Electrònica

UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Departament d'Enginyeria Electrònica

1. Introduction

MOTIVATION
Memories are a key technology driver in semiconductor industry, having an extremely important role in terascale multicore microprocessors
In such systems cores and memory may exhibit high failure rates due to process variations and devices degradation mechanisms.

1. Introduction



Intel i7

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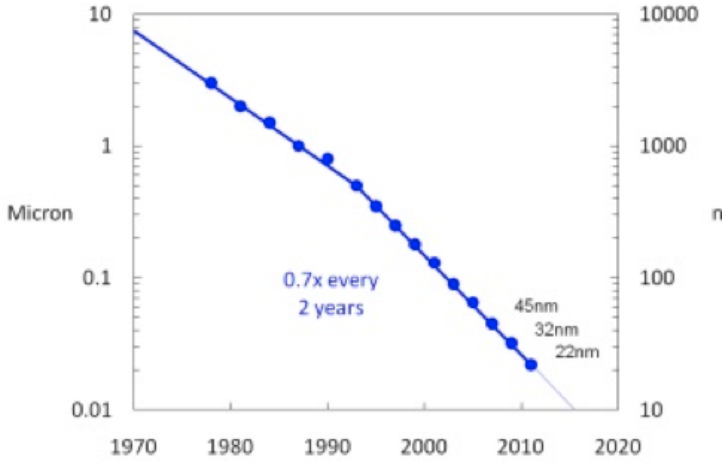
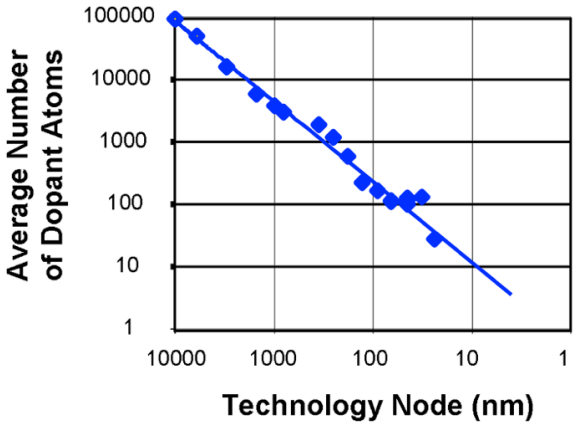
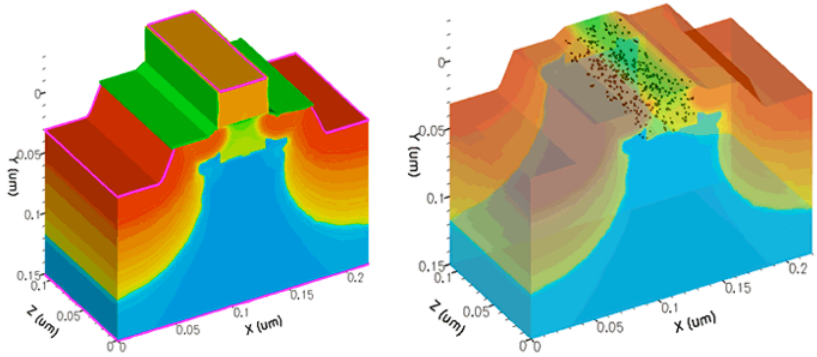


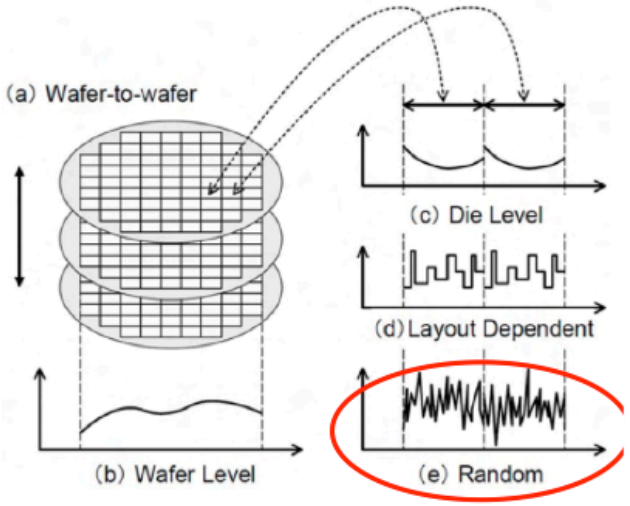


Caption: Transistor dimensions scale to improve performance, reduce power and reduce cost per tra

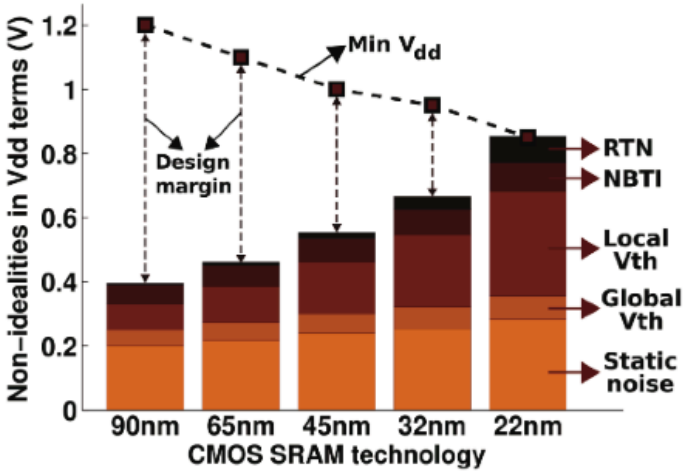


1. Introduction

The dramatic Variability drawback



After K. Takeuchi (NEC)



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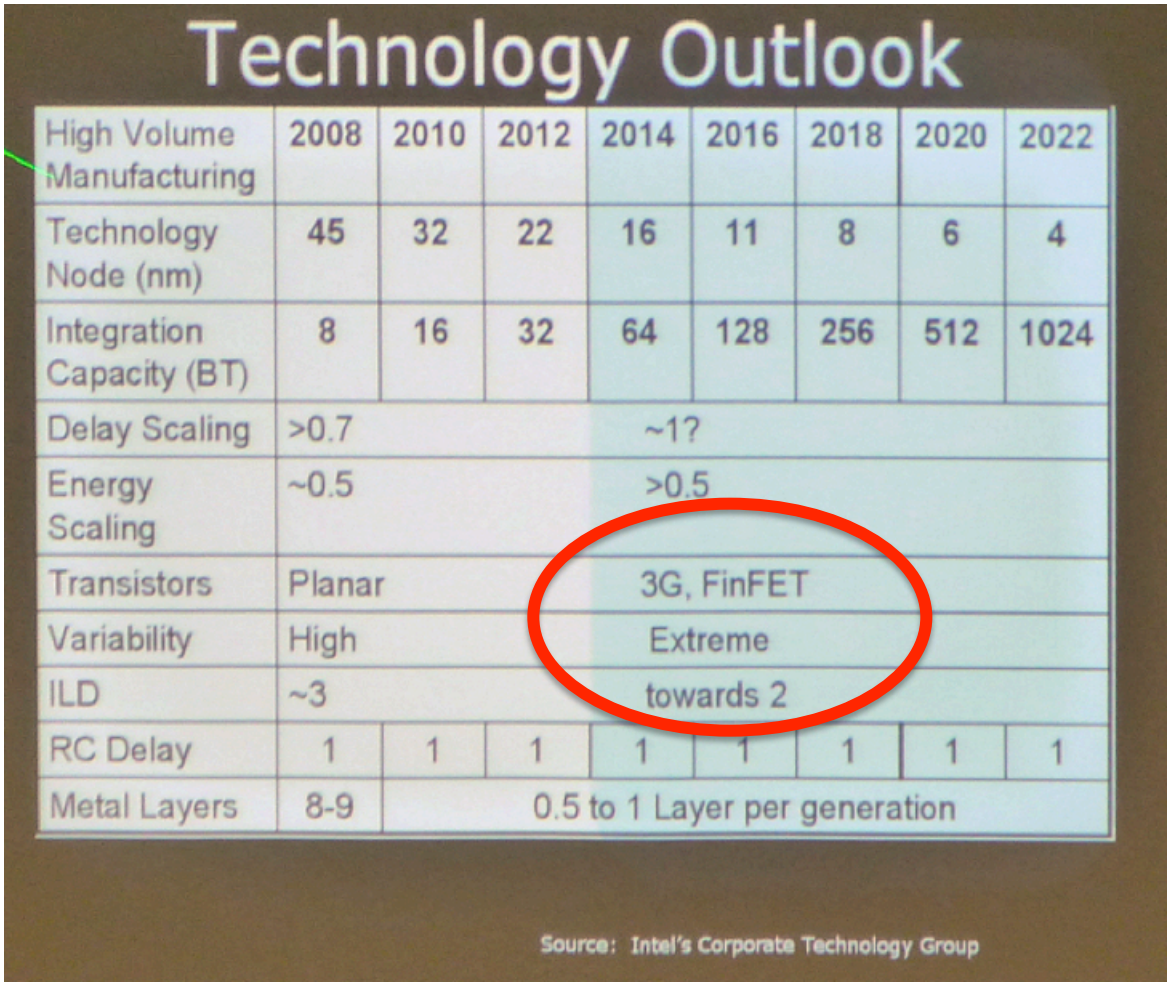


1. Introduction

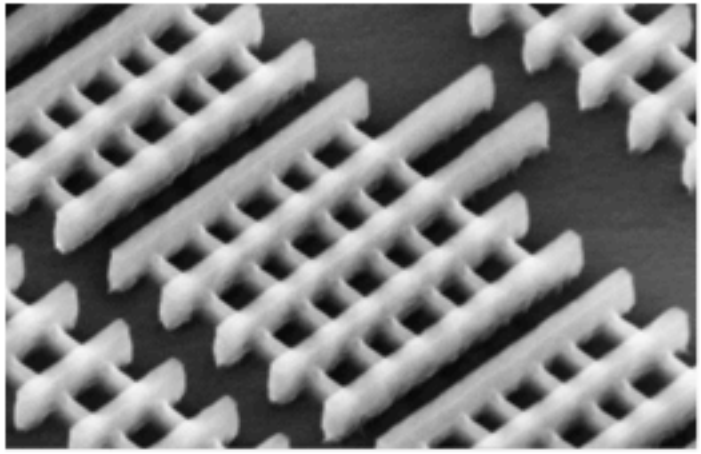
A real sophisticated solution for at least 3 generations!!!

Intel Increases Transistor Speed by Building Upward

By JOHN MARKOFF

Published: May 4, 2011

HILLSBORO, Ore. — Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.



Intel's new transistors have tiny pillars, or fins, that rise above the chip's surface.

2.- Description of the problem addressed

Objectives of the TRAMS project
To investigate the impact of statistical variability and reliability of near and beyond the end of the ITRS devices on Terabit memory design. (Sub-16nm bulk (18,13nm) CMOS,Sub 10nm Finfet, 15nm III-V/Ge and CNT) (WP1-WP2)
To design,implement, deploy and assess compensating techniques and countermeasures at circuit and microarchitectural level for memories used in multicore processors (WP3-WP4)
To develop a methodology for specifying and implementing performance-, power- and reliability –aware reconfiguration policies for multicore processor. (WP4)

3.- How we addressed the problem – technical justification

TRAMS

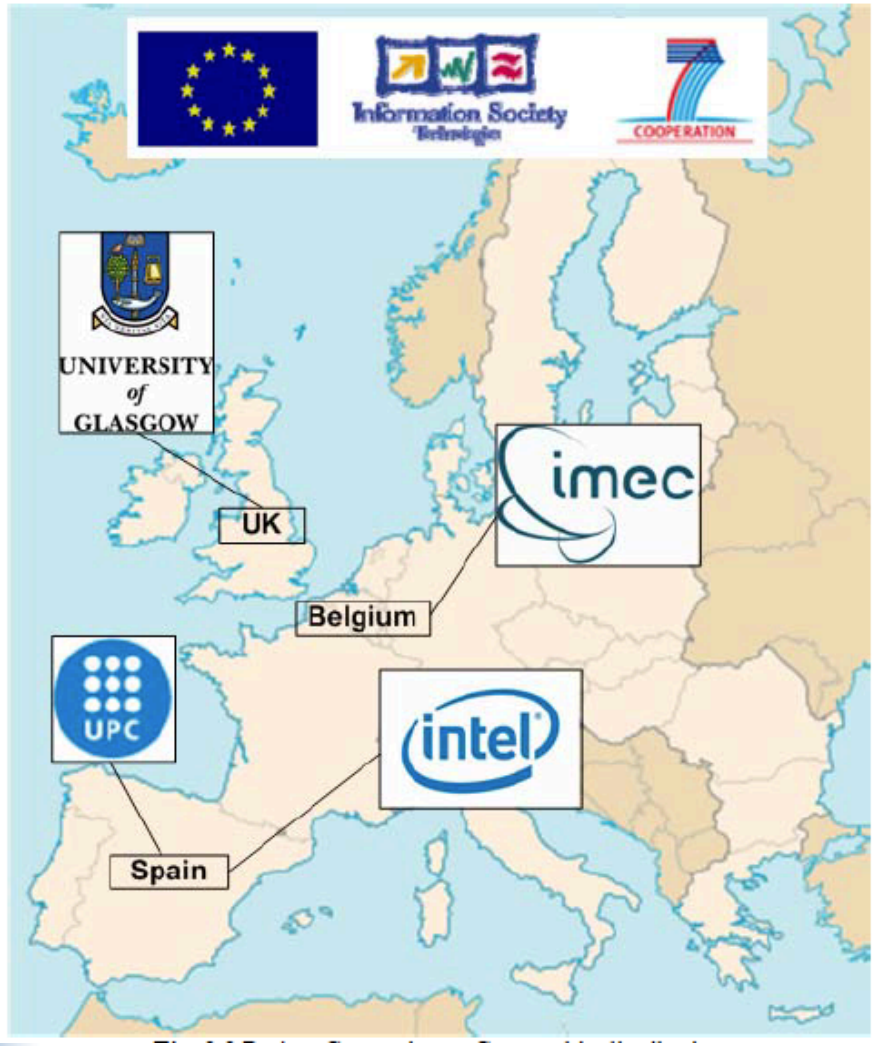
TERASCALE RELIABLE ADAPTIVE MEMORY SYSTEMS

EU COLABORATIVE PROJECT

FET FP7 248789

1/1/2010 to 31/12/2012

3.- How we addressed the problem – technical justification



THE CONSORTIUM

UPC

University of Glasgow

imec

intel

4.What have we done – project description

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PDK for
18, 13nm Bulk MOSFET
32, 16nm CNT MOSFET
10nm FinFET MOSFET
15nm III-V/ Ge MOSFET
Memory cells
6T
3T1D

4.What have we done – project description

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Mechanisms
regular layout
design rules
redundancy
latency detection
reconfiguration
compensation
T, performance, time violation, particles impact sensors
monitor injection

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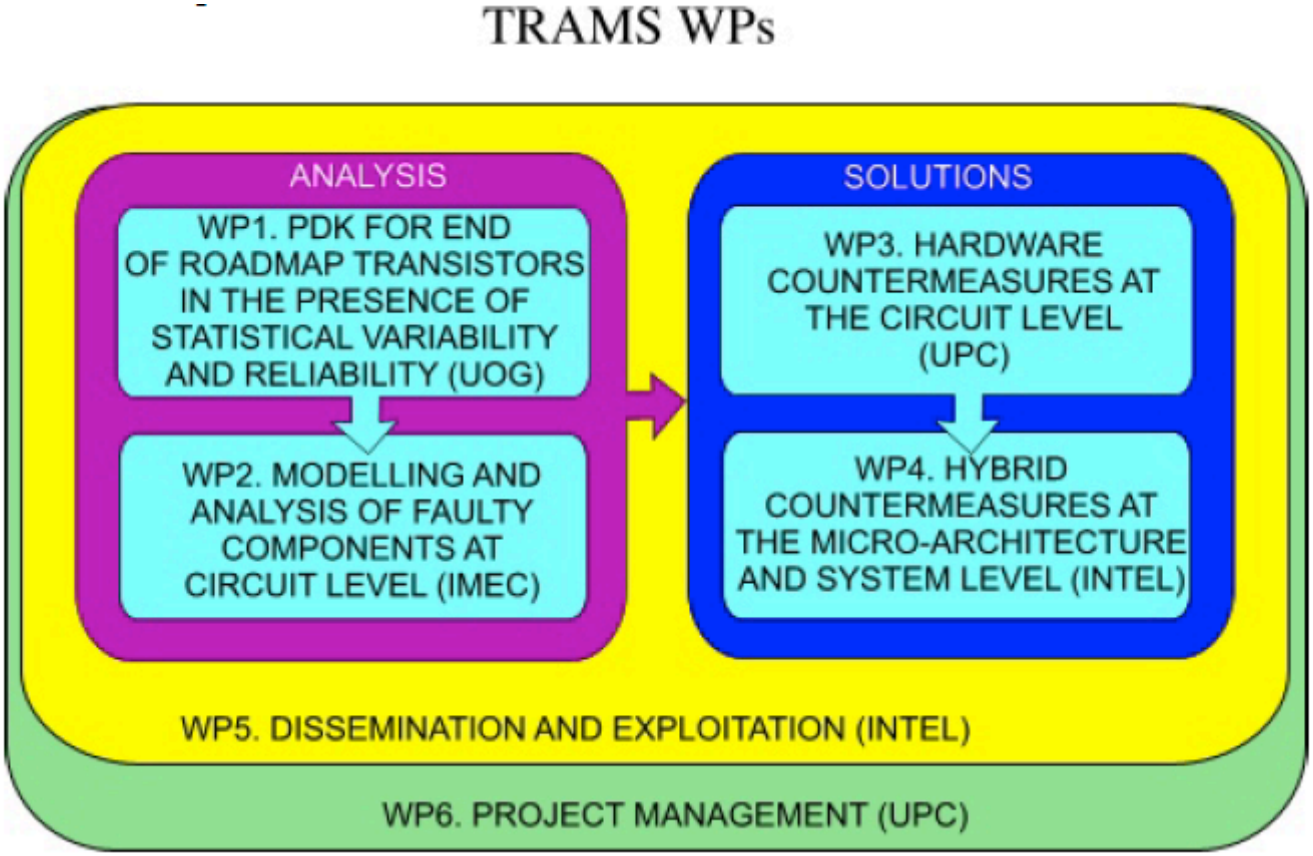
Mechanisms
Phase identifier mechanisms
Memory blocks reconfiguration
Hybrid counter-measures
Multicore platform policies
Live demo

5. How – resources used



5. How – resources used

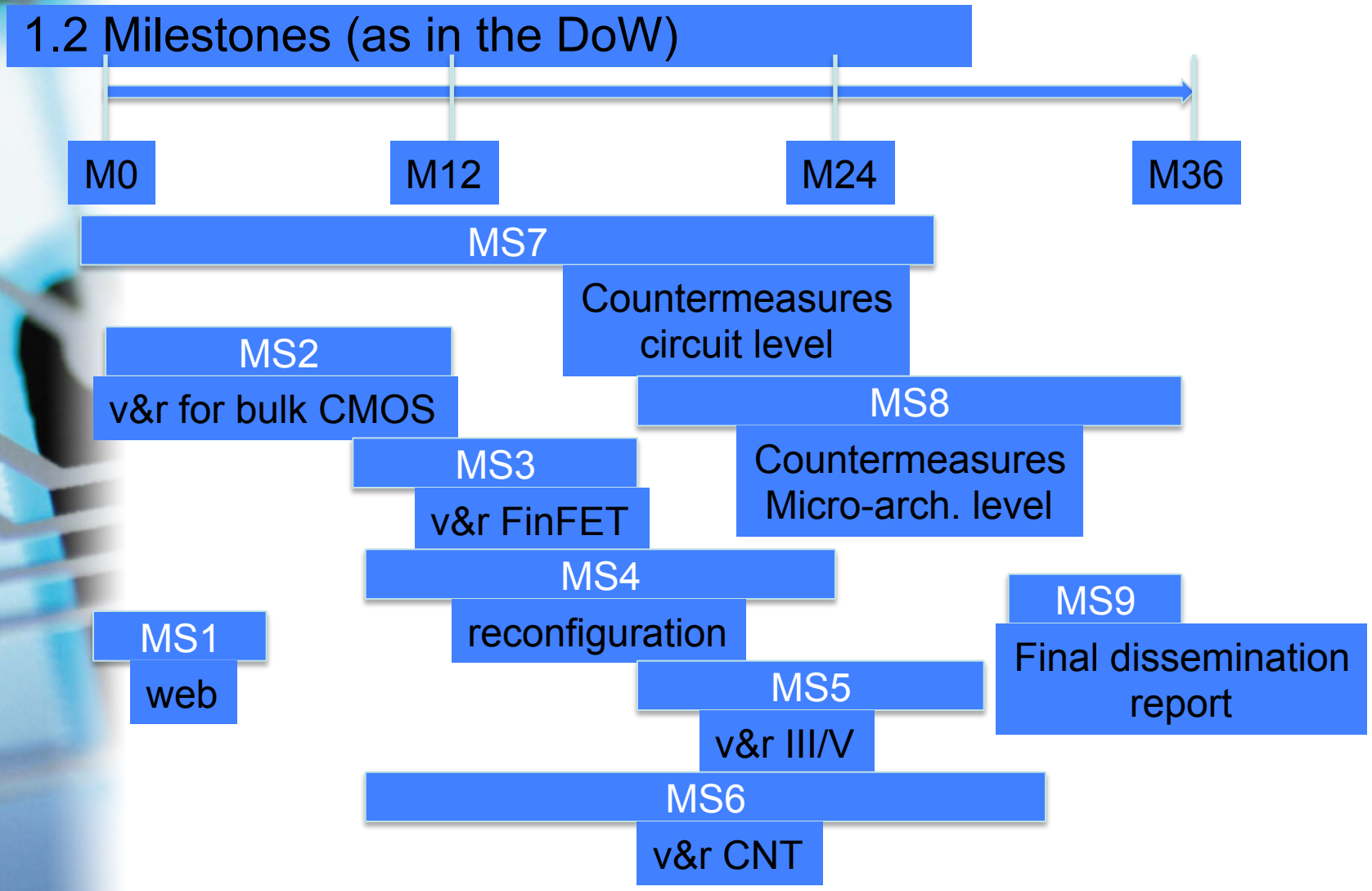
WT1
List of work packages

Project Number [1]	248789	Project Acronym [2]	TRAMS

LIST OF WORK PACKAGES (WP)

WP Number [53]	WP Title	Type of activity [54]	Lead beneficiary number [55]	Person-months [56]	Start month [57]	End month [58]
WP 1	PDK for end of roadmap transistors in the presence of statistical variability and reliability	RTD	4	81.00	1	36
WP 2	Modelling and analysis of faulty components at circuit level	RTD	2	41.00	1	36
WP 3	Hardware countermeasures at the circuit level	RTD	1	105.00	1	36
WP 4	Hybrid countermeasures at the micro-architecture and system level	RTD	3	134.00	1	36
WP 5	Exploitation and Dissemination	OTHER	3	19.00	1	36
WP 6	Management	MGT	1	12.50	1	36
			Total	392.50		

5. How – resources used



5. How – resources used

The research team at UPC

Name	Position	Role
Antonio RUBIO	Professor	PC, research WP1,2,3 and leader WP3
Joan FIGUERAS	Professor	Research WP3
Ramon CANAL	Ass. professor	Research WP3,4
Luz BALADO	Ass. Professor	Finfets circuits
Esteve AMAT	Postdoctoral	1T3D
Ioana VATAJELU	PhD student	SRAM robustness evaluation
Carmen GARCIA	PhD student	CNTFETs
Nivard Aymerich	PhD student	Hardware redundancy
Peyman Pouyan	PhD student	Reconfiguration
Shrikanth Ganapathy	PhD student	Adaptive mechanisms
Zoran Jacksic	PhD student	Finfet circuits
Enric AMATLLER	Undergraduate	Layout level
Santi PEREZ	Technician	Web administrator
Name	**Position**	**Role**
J-LLorenç Cruz	Ass. professor	Researcher
Tanausu Ramírez	Researcher	Researcher
Enric Herrero	Researcher	Researcher
Nicholas Axelos	Researcher	Researcher
Antonio Calomarde	Ass. Professor	Dynamic memories
Jordi Tubella	Ass. Professor	Researcher

The research team at UOG

Name	Position	Role
Asen Asenov	Professor	Leader WP1
Binjie Cheng	Researcher	Compact model extraction strategy and technology
Andrew Brown	Researcher	FinFET simulation including statistical variability
Si-Yu Liao	Researcher	Drift-diffusion and Monte Carlo simulation of III-V
Daryoosh Dideban	Researcher	Statistical compact model extraction
Hamid Amini Moghedaban	Researcher	Physical FinFET simulation
Negin Moezi	Researcher	Nominal and statistical compact model extraction

The research team at Imec

Name	Position	Role
Mustafa Badaroglu	Team leader	Technical contributor
Miguel Miranda	Principal Scientist	Project responsible
Paul Zuber	Senior Researcher	WP2 leader
Arindam Mallik	Researcher	Technical contributor

The research team at Intel

Name	Position	Role
Antonio Gonzalez	Senior PE	Leader Intel
Xavier Vera	Senior Research Scientist	WP3, WP4 Leader WP4
Javier Carretero	Research Scientist	AVF models
Matteo Monchiero	Senior Research Scientist	Reconfiguration engine
Tana Ramirez	Senior Research Scientist	UserX
Enric Herrero	Senior Research Scientist	Demos

6. Main results

Intense research, intensive dissemination

STRATEGIC PLAN OF TRAMS PROJECT (DOW)

The TRAMS project will deliver circuit, microarchitecture and system level countermeasures for unreliable components by utilizing hybrid solutions and better than worst-case design.

DISSEMINATION OF FOREGROUND (DOW)

Actions to disseminate results of the project:

- ✓ Technical and scientific publications
- ✓ Reports (public, private)
- ✓ Organization of international workshops and seminars to promote TRAMS results
- ✓ Web page (public docs, description of the project, publications, agenda, …)

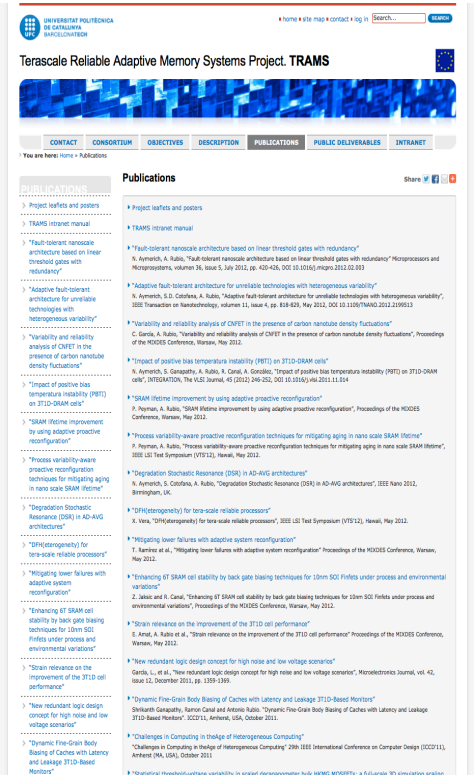
- ✓ No patent or trademark has been generated with exception of the TRAMS logo Trademark
- ✓ TRAMS does not contribute directly to specific standards

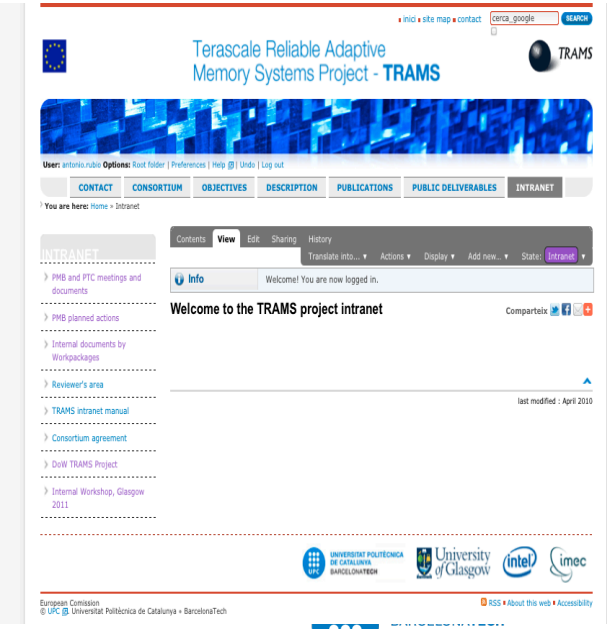
DISSEMINATION OF RESULTS

WEB PAGE

www.trams-project.eu

Description, agenda, activities, publications, public docs, intranet





EXPLOITABLE FOREGROUND

PDK for 18, 13nm bulk CMOS technology, BSIM models	Technology, SRAM, FinFET assessments
PDK for 32 and 16nm CNTFET technology, BSIM models	Injection methods
PDK for 10nm FinFET technology, BSIM models	3T1D DRAM assessment (FinFET)
PDK for 15nm III-V/Ge technology, BSIM models	New full error recovery memory
Advanced process variations sensors, + particle strike	New Hybrid fault recovery mechanisms
Dynamic fine-grain body bias adaption	Advance performance power/robust. prediction
Degradation redundancy principles	Functional mitigation for streaming
New mechanisms to extend life time of memory systems	AVF models for memory structures
New fault tolerant architectures, degradation resonance	2-LEVEL reconfiguration engine
Delay and temperature sensors	SER assessment tool
Memory IP & Specifications	

Pieces of Work

- CNT and FinFET modelling
- Circuit level counteremasures to compensate variability and improve reliability