Wideband Continuous-Time Multi-Bit Delta-Sigma ADCs

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Thanks to All our Graduate Students that generate these ideas and make possible to test the concepts, and report them in the ISSCC-2009, and JSSC: June 2010, September 2010 and March 2011.

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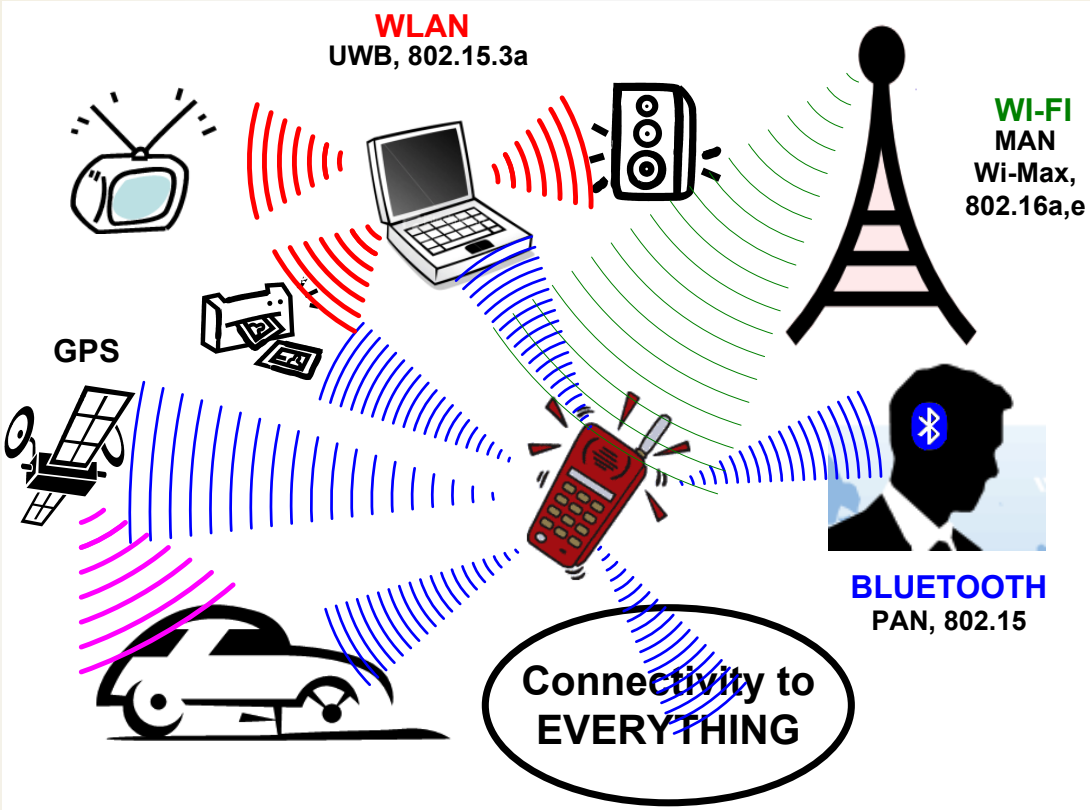
Outline

- Introduction
- Design techniques for a 3th order Low-Power 10MHz Low-Pass ΣΔ ADC in 65nm Technology
- Design techniques for a 5th Order 25MHz ΣΔ ADC with SNDR>68 dB
- Conclusions

Introduction: Connectivity



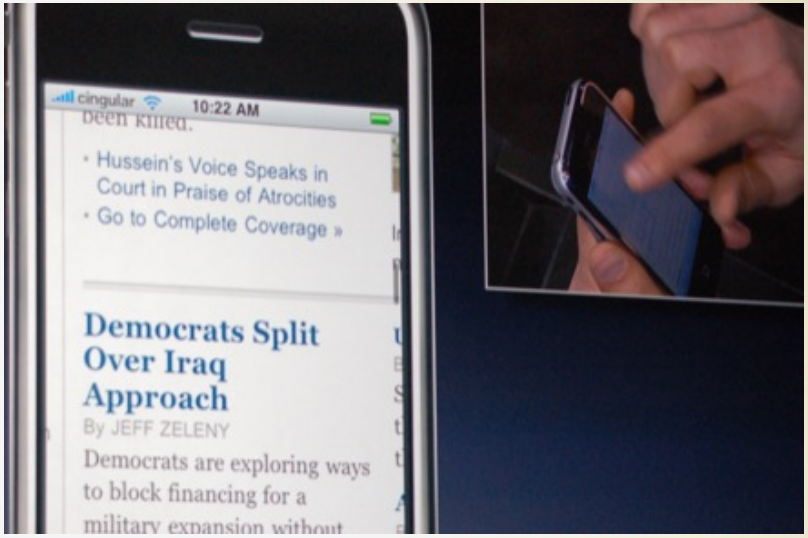
- Increasing number of wireless standards
- Support of multiple-standards on the same chip
- Advances in Integrated RF design towards universal devices
- Software Radio: easy addition of new standards

Introduction: Design considerations

- Numerous systems will be included into the next generation receiver.
  - Cell phone standards (GSM, WCDMA, DECT, EDGE etc)
  - Communication network (802.11 a/b/g, bluetooth, WiMax, UWB etc)
  - Satellite services (GPS)
- Different technologies are used to achieve the receiver
  - **CMOS**, BiCMOS, III-IV Compounds (GaAs, InP, etc.)
- Strong push to the digital domain
  - Digital circuit: **accurate & robust**
- In a complete System-on-Chip: 90% is digital circuitry
  - **only 10% is analog**
- Variations of receiver architecture are proposed.
  - Direct conversion, software-radio, **High-IF receiver**

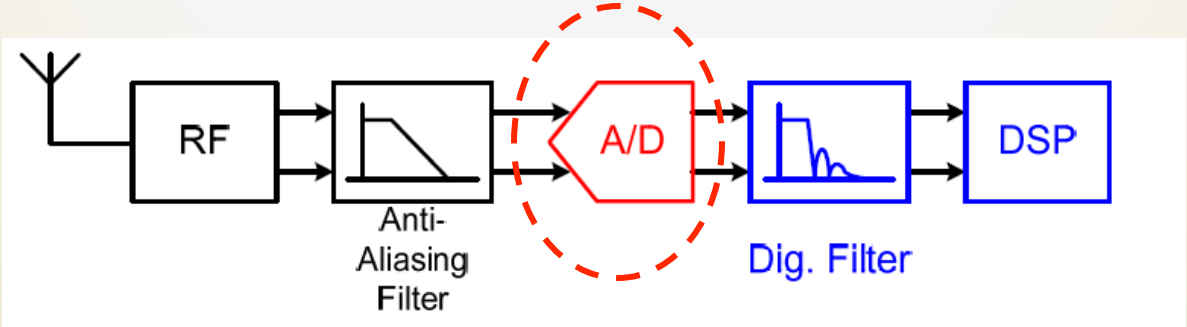
Motivation

- Low power, low cost WLAN ADC for ultra-mobiles
- Conventional ADC architectures are often unsuitable for nanometric technologies (feature size <100nm)
- New architecture for low power ADC compatible with nanometric technology is desired



Internet surfing on mobile device

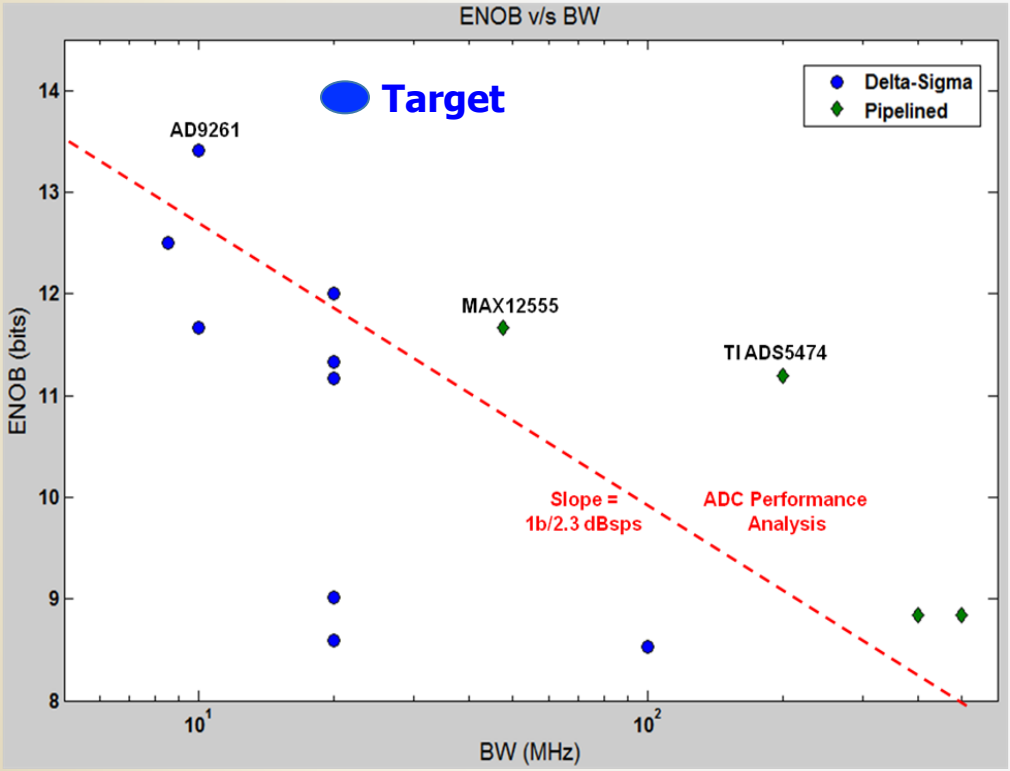
20MHz BW, >12bit ADC



Existing Solutions for Baseband ADC

- $\Delta\Sigma$ architecture is preferred for nanometric digital technology
  - Does not rely on component matching and complex analog circuits
  - Digital decimation filter scales well with technology
- 1-bit $\Delta\Sigma$ impractical for wideband application
  - Order of modulator is limited by overloading effects
  - Large Over Sampling Ratio (OSR) increases power dissipation
- Typical Multi-bit $\Delta\Sigma$ architecture gives up “Digital friendly” advantages
  - Front-end filter and feedback DAC linearity are major issues

State-of-the-art and Target



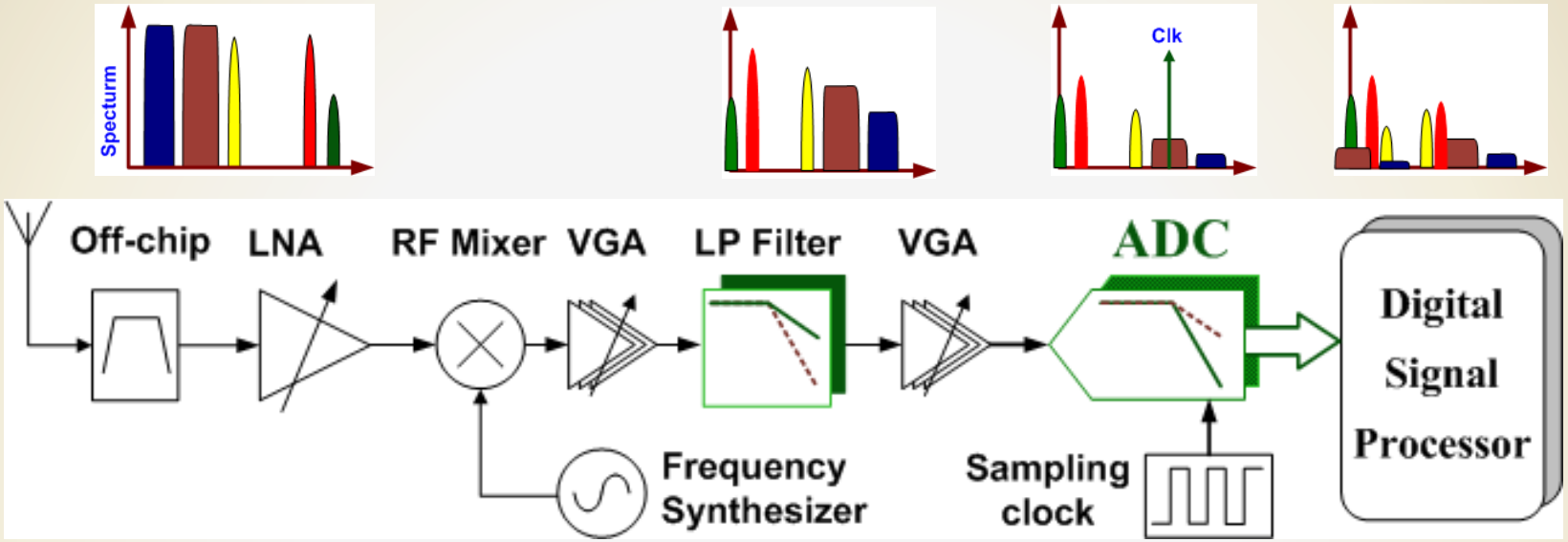
Sigma-Delta ADC

- Power efficient and cost effective
- Inherent "**anti-aliasing**" filtering
- Digital post-processing capability

On-going research

- **14 bit, 20MHz** ADC in 90nm technology with auto-calibration
- Total Power consumption < **50 mW**
- Robust performance with on-chip master clock having **5-10 psec jitter**
- Figure of merit in the range of **250 fJ/conversion step**

Direct Conversion Multi-Standard Receiver



System issues in broadband systems:

High frequency filtering is especially critical in broadband applications

Rejection of Blockers: ADC filtering must be complemented by LP filtering

Neighbor channels are quite relevant even if heavy filtering is used

Trade-offs:

Light filtering in front demands an ADC with higher SNR and higher SDR

Higher SNDR-ADC implies more power and more circuit complexity

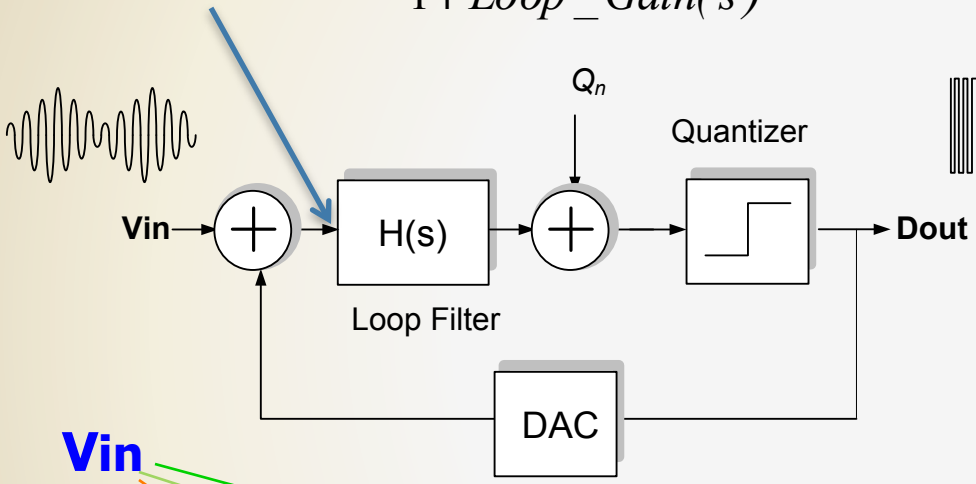
Design issues in Low-pass ΣΔ ADC

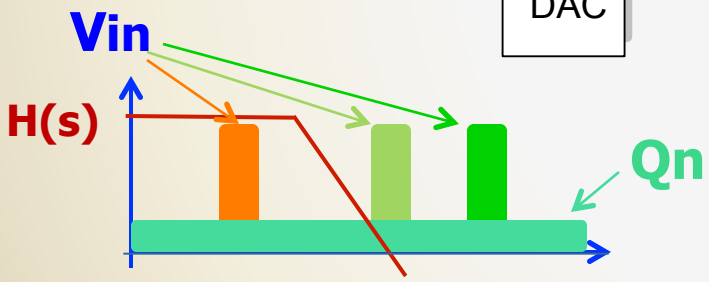
$$Error = Vin - Vout = \frac{Vin + Qn}{1 + Loop\_Gain(s)} = NTF * (Vin + Qn)$$

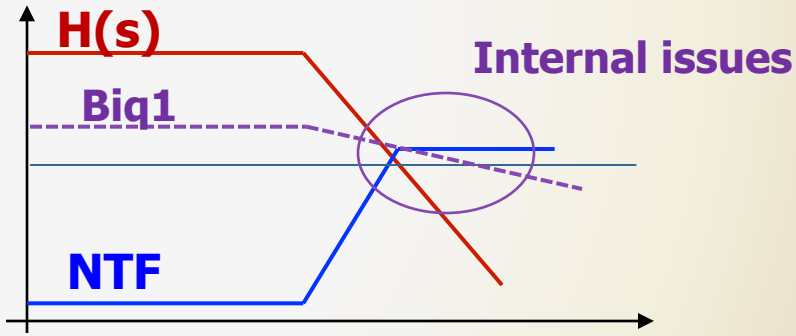
$$D_{out} = STF * V_{in} + NTF * Q_n$$

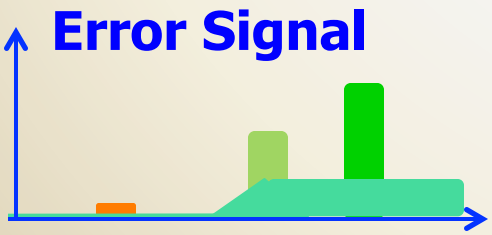
$$NTF = \frac{1}{1 + Loop\_Gain(s)}$$

$$STF = \frac{H(s)}{1 + Loop\_Gain(s)} = NTF * H(s)$$







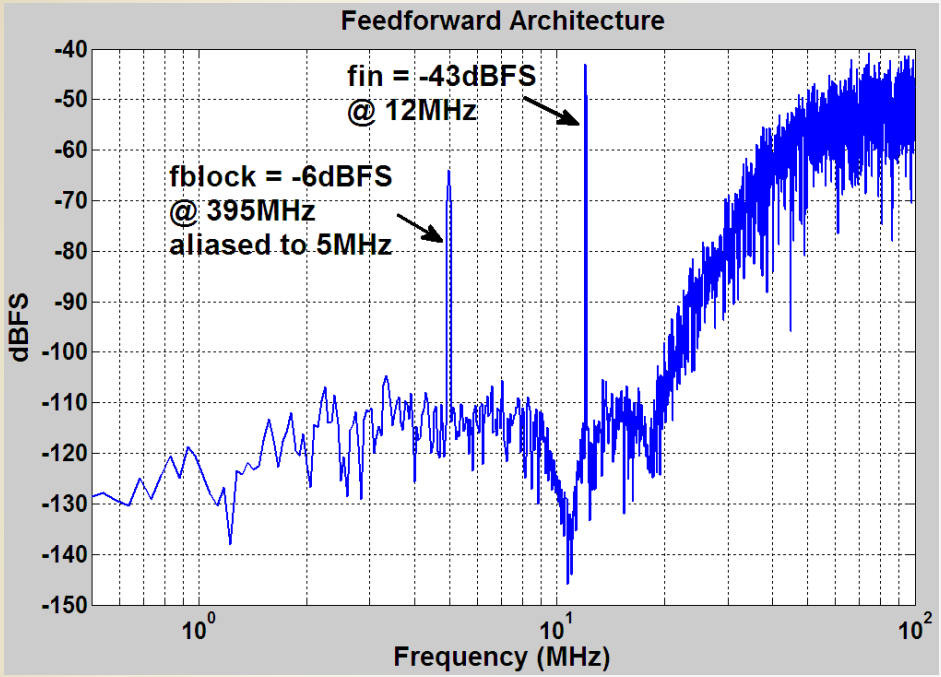


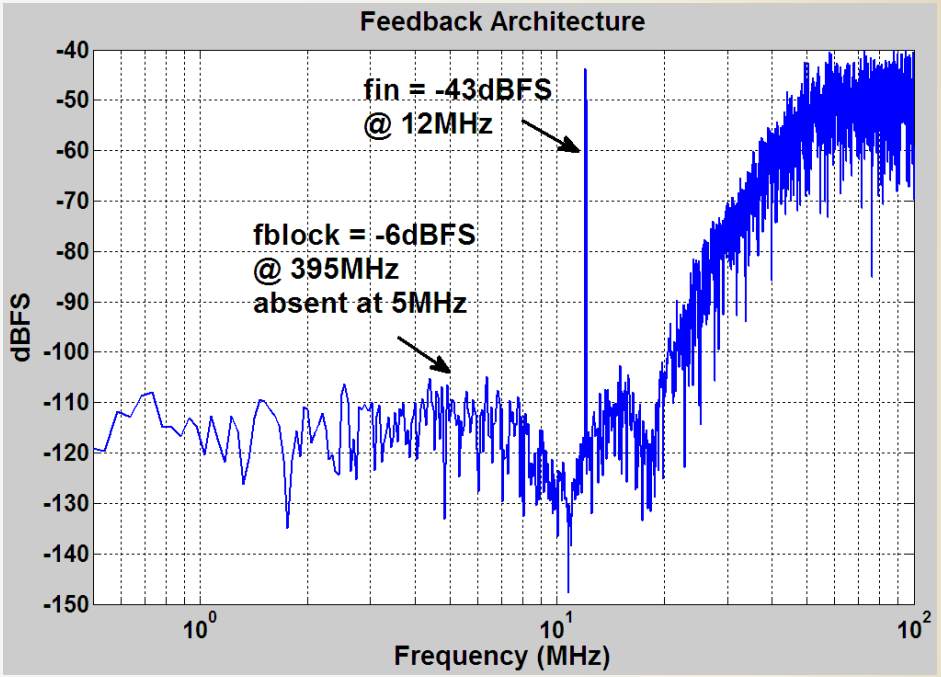
NTF gain increases at high frequency

HF Power at filter input maybe excessive

Error signal is mainly at high frequency and the filter must deal with that!

Blocker Rejection: Feedforward vs. Feedback





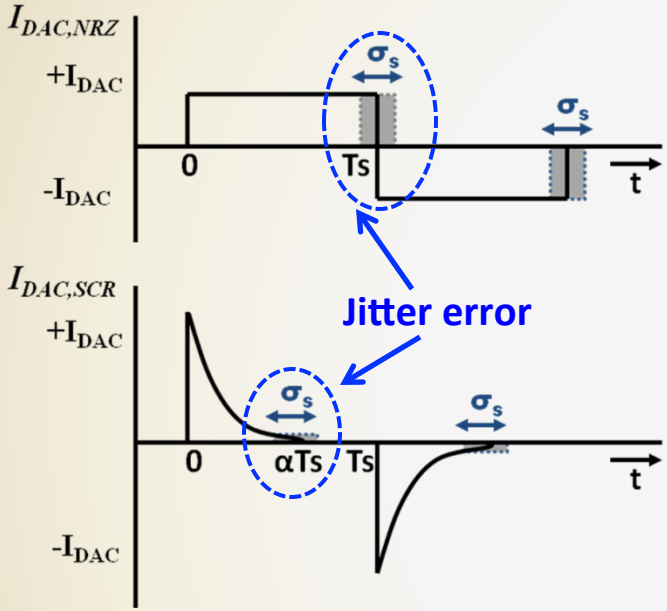
Input signal: Weak in-band component (-43dBFS @12MHz) and a strong out-of-band component (-6dBFS @395MHz). Clock frequency = 400MHz.
In-band alias signal at 5 MHz.

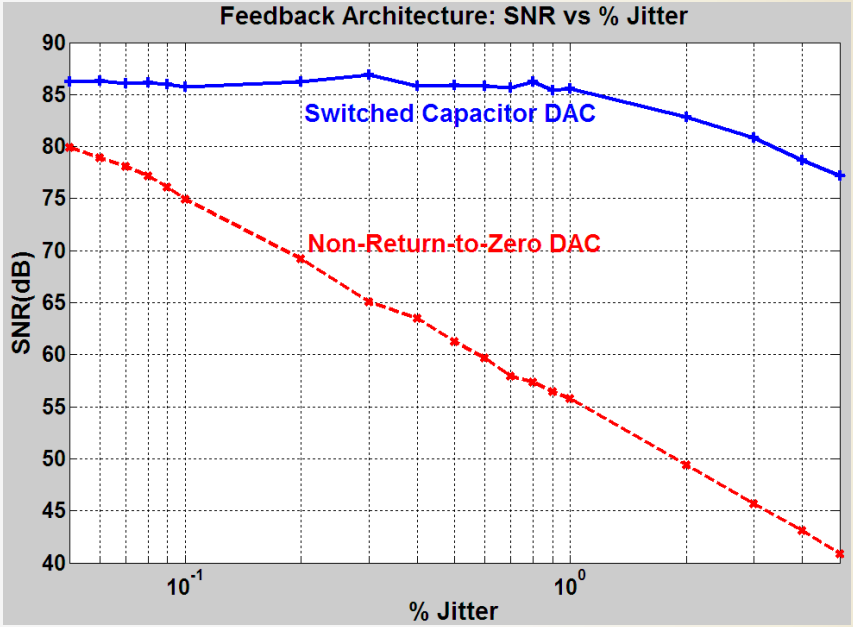
Feedback architecture clearly has significant advantages:

- **Excellent Blocker Rejection :** Feedback STF provides Nth order filtering for blockers
- **Improved Dynamic Range:** Better filtering of out-of-band channels reduces input power in filter stages

Jitter Insensitivity of Switched-Capacitor DACs

Non-Return-to-Zero vs. Switched-Capacitor





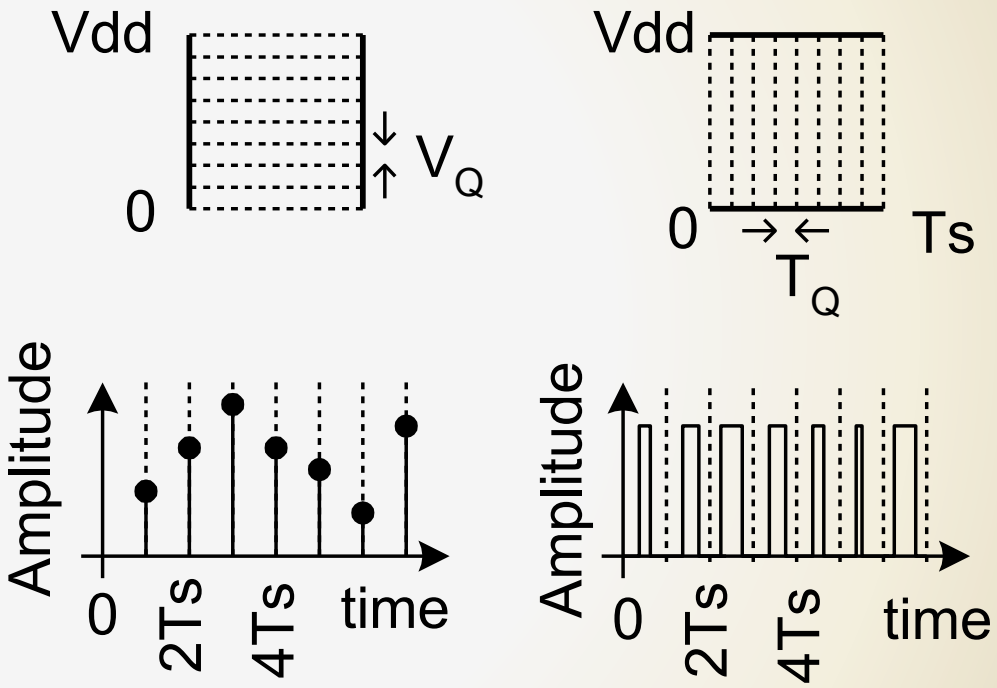
- Clock jitter causes a variation in the width of the feedback pulse resulting in a random variation in the amount of charge fed back per clock cycle

- Jitter noise is directly proportional to jitter variance and **DAC pulse magnitude**

- Switched Capacitor (SC) DACs present **excellent jitter performance but demands large slew-rate and faster OPAMPs**

Strategy for nanometric technologies

- Make use of time domain signal representation
- Small supply voltage limits the dynamic range of analog signals
- Fast switching gates provide fine time precision, which provide alternate means for high DR signal representation
- Also takes advantage of CV^2f

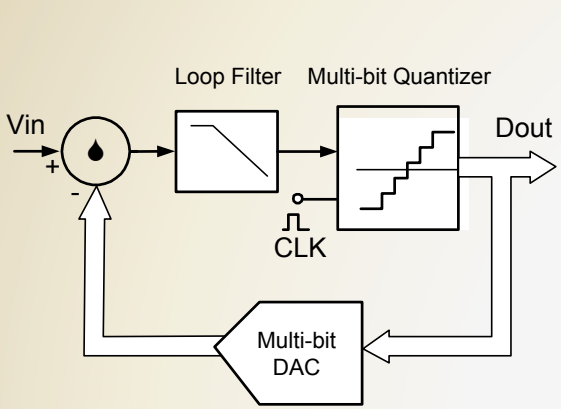


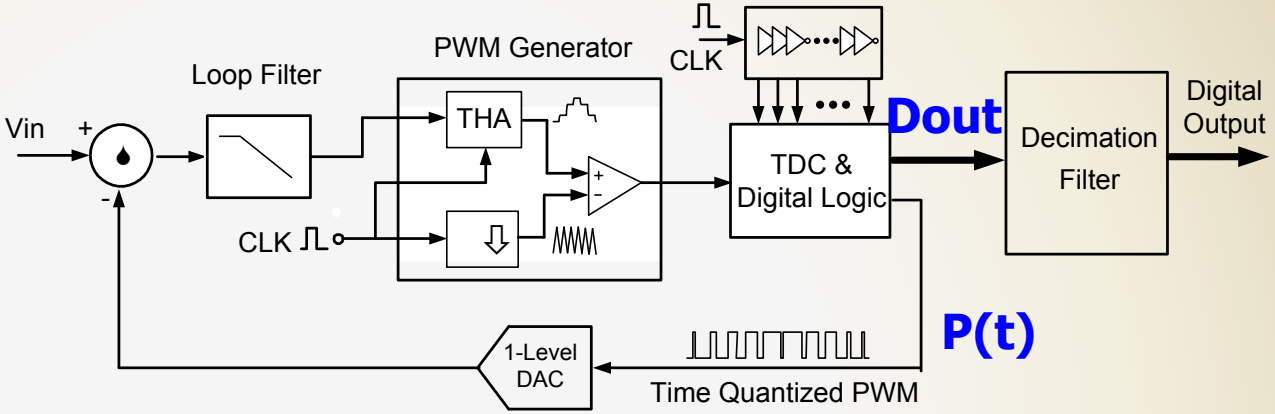
Time domain signal representation

A 20MHz Signal Bandwidth 68dB Dynamic Range Continuous Time $\Delta\Sigma$ ADC Based On Multi-bit Time Domain Quantizer and Feedback Element

V. Dhanasekaran, et.al. ISSCC-2009; JSSC March 2011

Proposed ADC Architecture



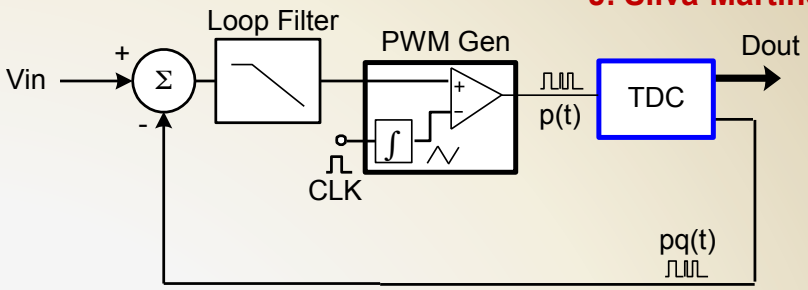


Conventional ΔΣ

Time domain Quantizer-DAC

- **Multi-level quantizer and Digital to Analog Converter (DAC) is replaced by PWM generator and Time to Digtal Converter (TDC)**
- **Width of p(t) is proportional to the amplitude of the signal in a given clock period**
- **Output code (Dout) represents "quantized pulse" edges with a quantization step size = T_Q**

Why ΔΣ Noise Shaping



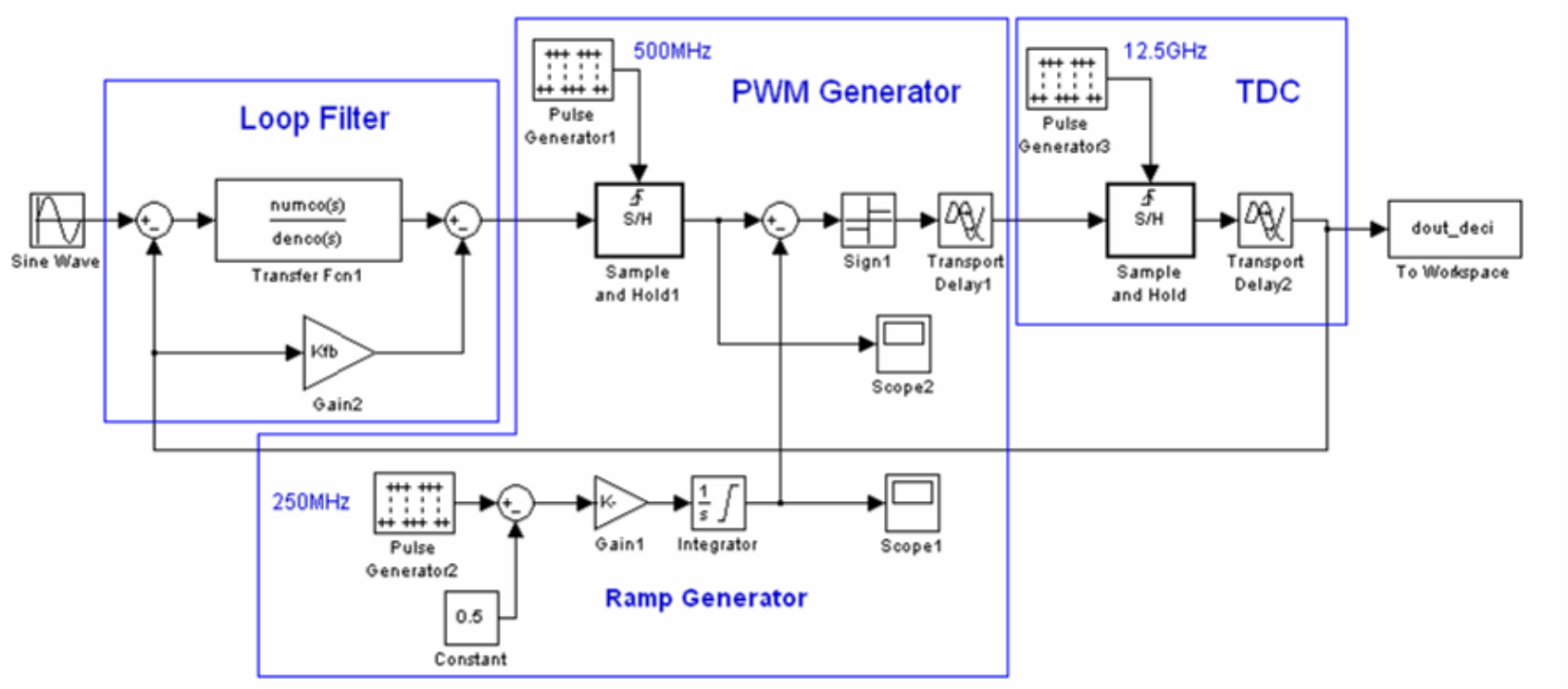
- **PWM + TDC cannot achieve necessary performance**
  - Timing edges are precise to sub-pS level but resolution is limited
  - Typical TDC resolution is about 1 inverter delay (~15pS in 65nm technology)
  - Difficult to achieve good linearity of PWM at this speed
- **Noise shaping is used to overcome limited time resolution of TDC**
  - Time quantization results in quasi-white noise that can be shaped by the loop filter
  - Precise timing edges (standard deviation < 800fS), required for the feedback path, is achieved by using matched delay elements
- **Loop filter serves to suppress the quantization noise introduced by the TDC and the non-linearity of the PWM**

Merits of the Proposed Approach

- **Flash ADC and Multi-level DAC is replaced by PWM Generator & TDC**
- **The TDC is implemented by digital circuits, which takes advantage of technology scaling**
- **Feedback signal is inherently linear and is ultimately limited by timing precision**
- **Reduced sensitivity to clock jitter**

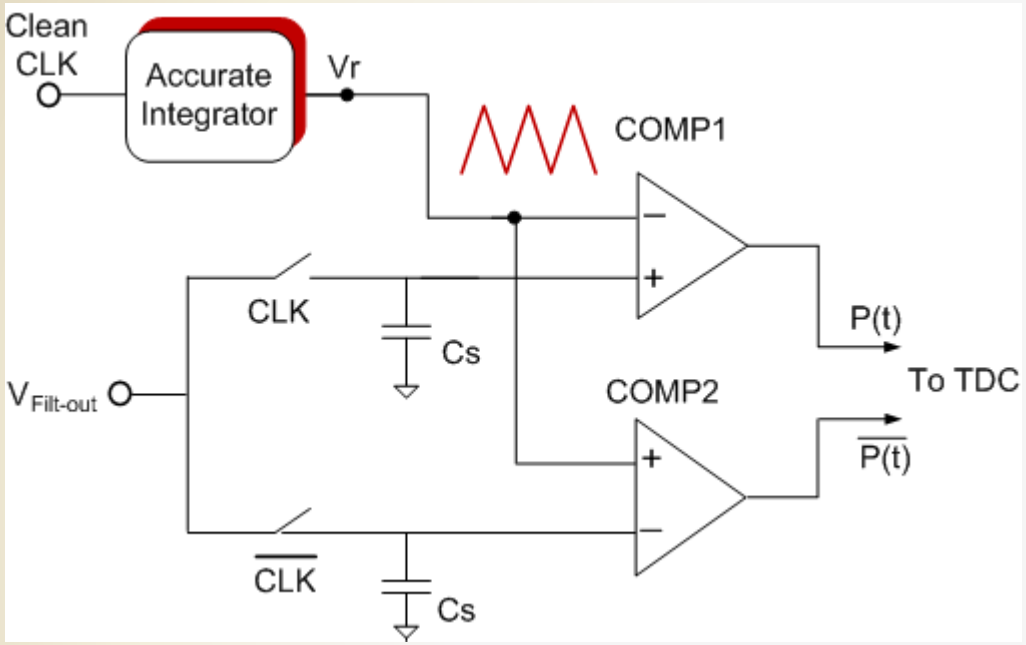
	Multi-bit	Proposed
Low OSR design	☺	☺
Small supply voltage	☹	😐
DAC linearity	☹	☺
Sensitivity to clock jitter	☹	☺

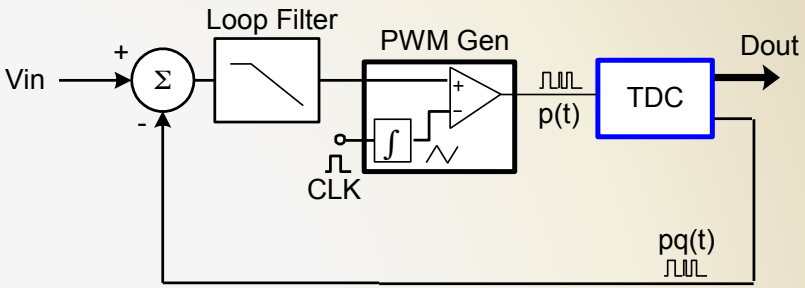
Full System Simulation



- System level design and simulation of the proposed architecture was performed using SIMULINK
- Transistor level simulations were performed using TISPICE, SPECTRE and FINESIM simulators

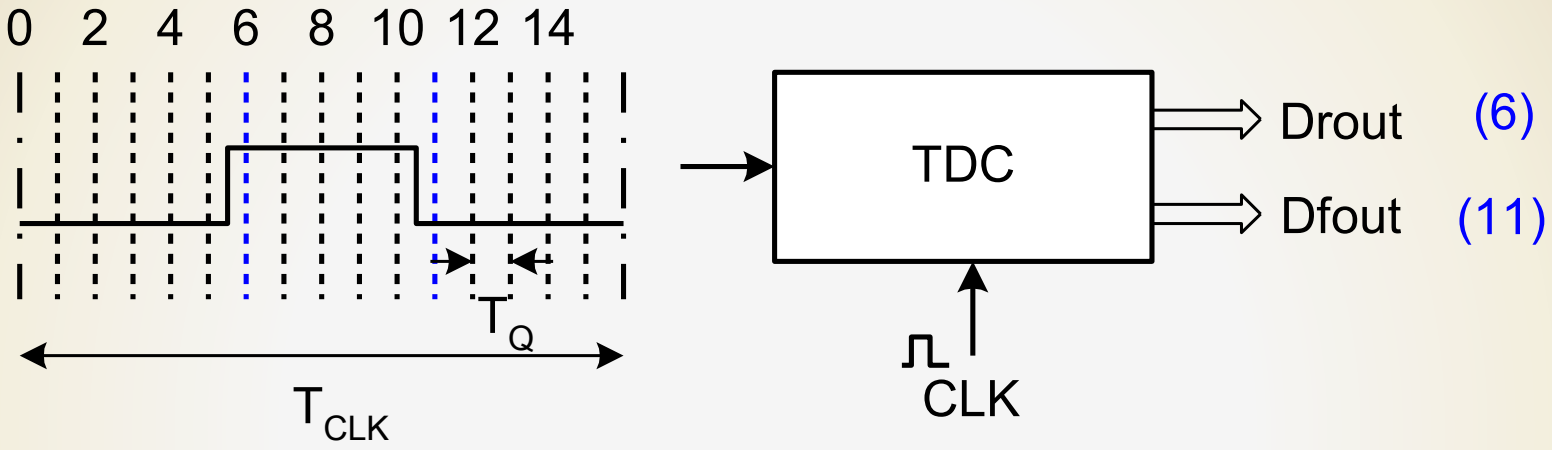
PWM Generator





- PWM signal generated by standard method - comparing signal with triangle waveform
- Double-sampled or “asymmetric sampled” PWM is used to minimize distortion and improve OSR
- Performance is relaxed due to noise shaping

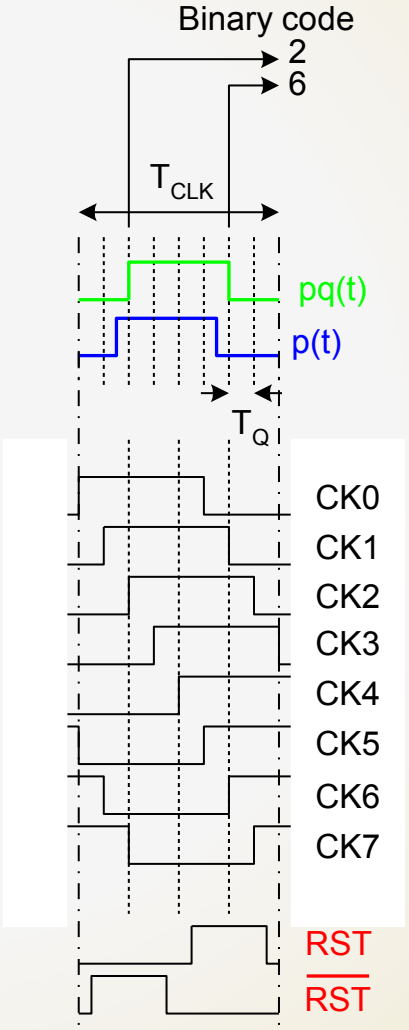
TDC Functionality

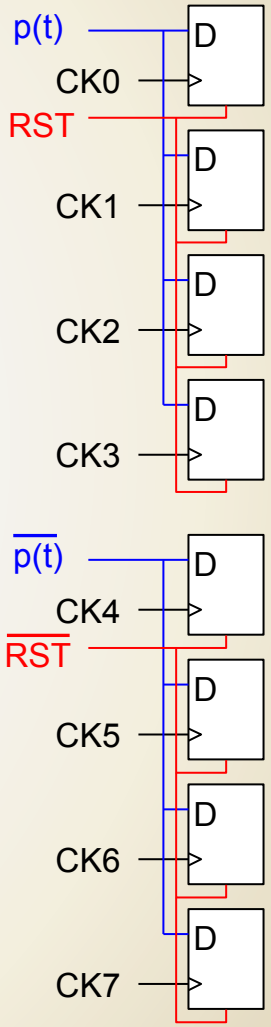


- TDC
  - Converts pulse timing information to digital codes (Drout & Dfout)
  - Drout & Dfout can be used to reconstruct signal in clocked digital domain
  - Also generates a feedback pulse aligned to the timing edges represented by the dotted lines

TDC & Time quantized feedback pulse

- Digital output code
  - CT PWM output p(t) is latched by delayed versions of the clock
  - Flipflop outputs provide "thermometer" coded pulse width
  - D input of the flipflops are driven by p(t) to facilitate easy generation of f/b pulse
- Feedback pulse - pq(t)
  - Must match output code
  - Edges of pq(t) are always aligned to the delayed clock edges

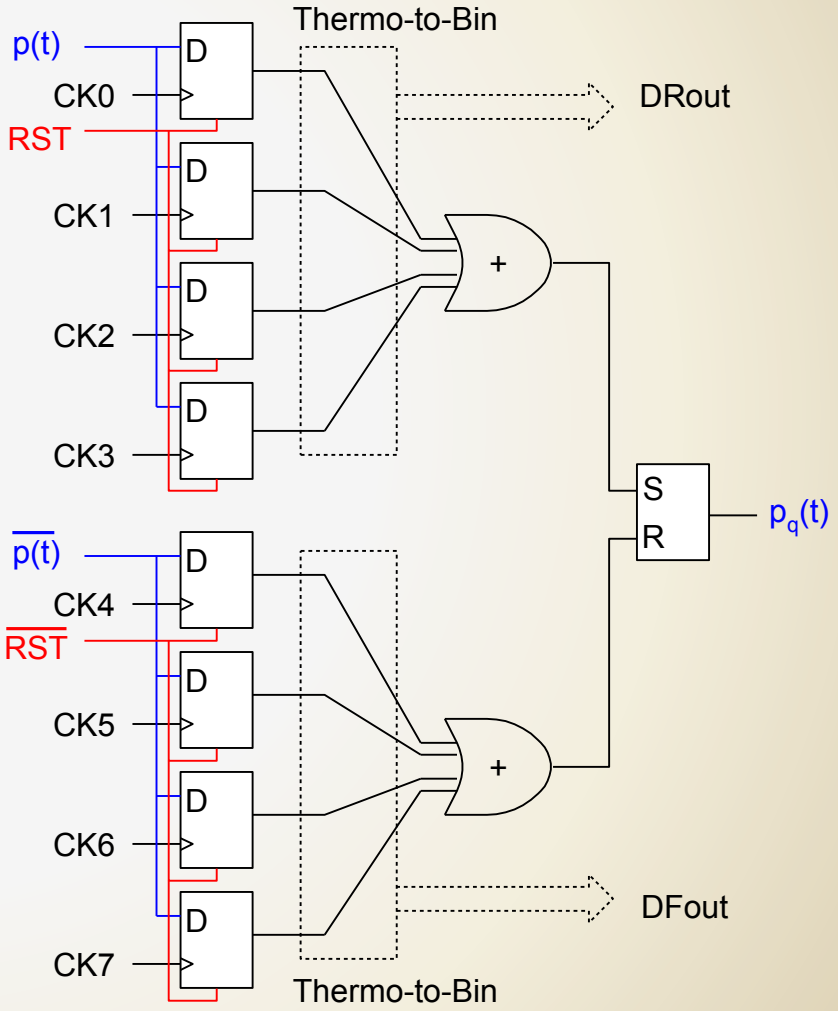




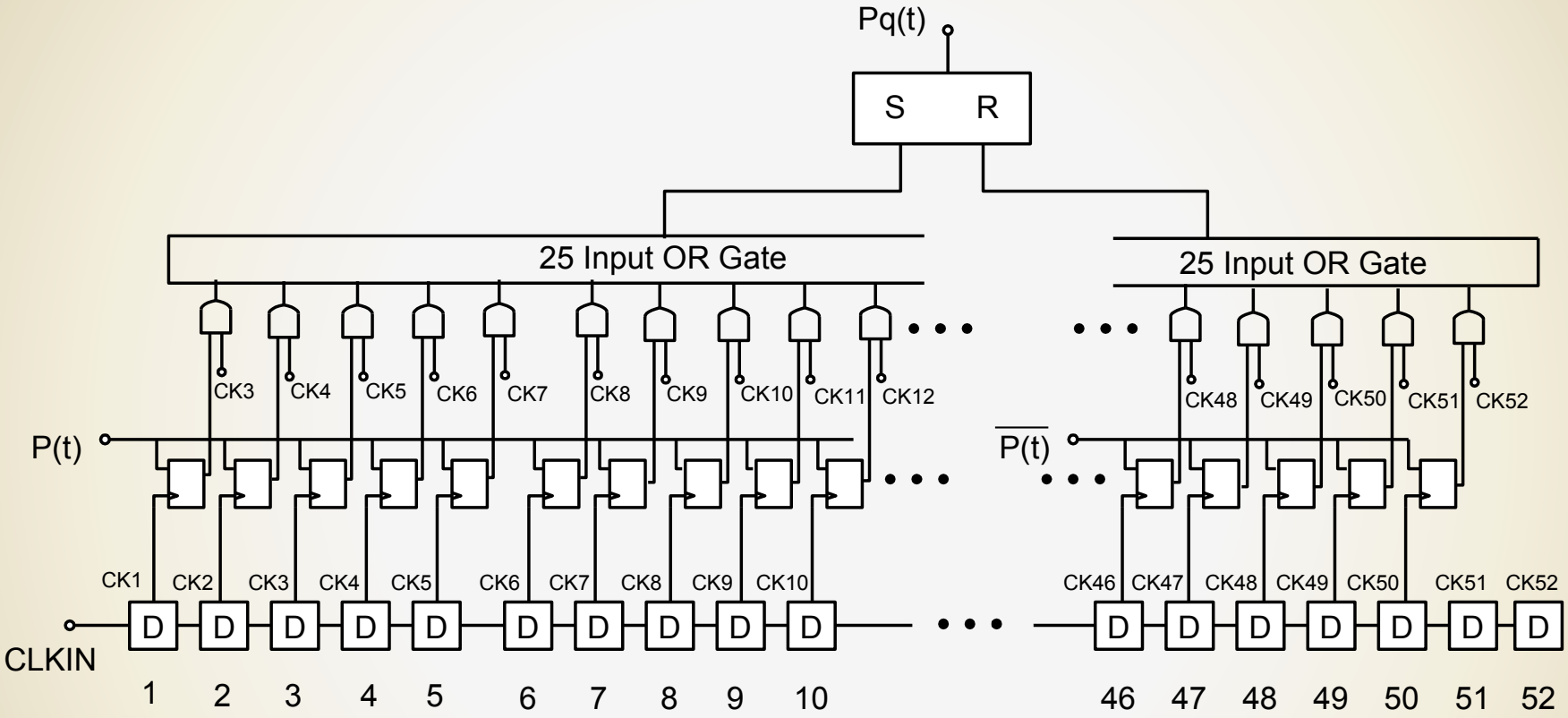
Time quantized pulse generator

- Pq(t) can be generated using a OR gates and SR latch
- Pq(t) turns 'High' when the earliest of CK0-3 goes High after p(t) is High
- Pq(t) turns 'Low' when the earliest of CK4-7 goes High after p(t) is Low

- **Wired-NOR/NAND gate can be used to ensure uniform delay**

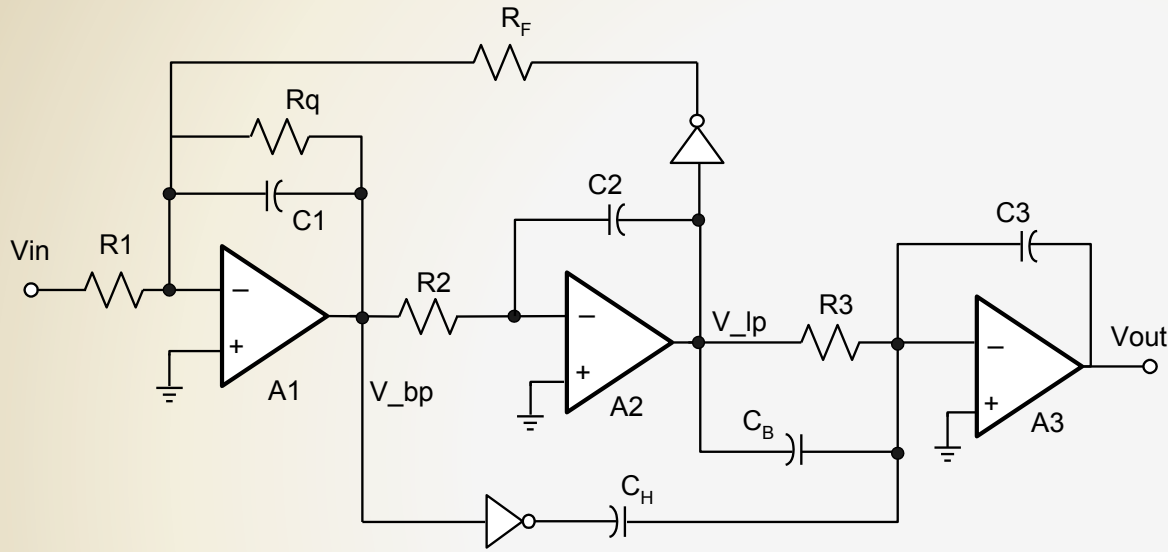


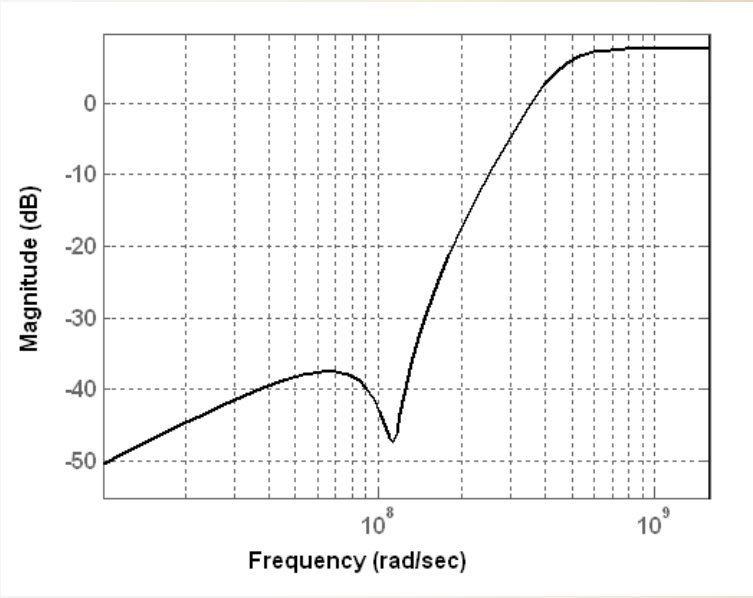
Full TDC Schematics



- 50 levels of time steps are used in the proposed design for 20MHz ADC
- Clock phases are generated using cascade of delay elements that are tuned using a phase detector

Active-RC Topology Loop Filter



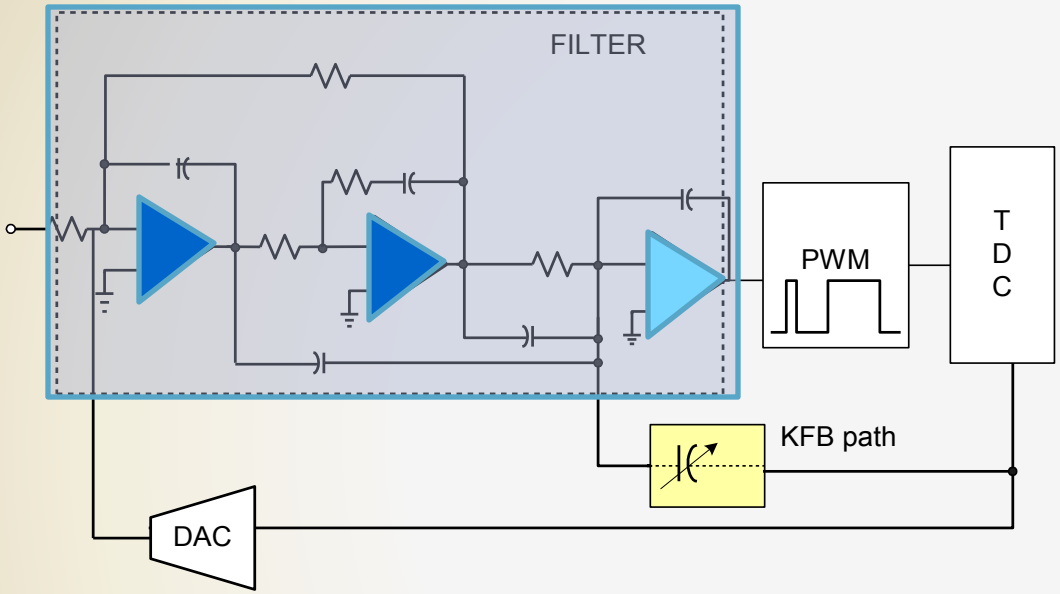


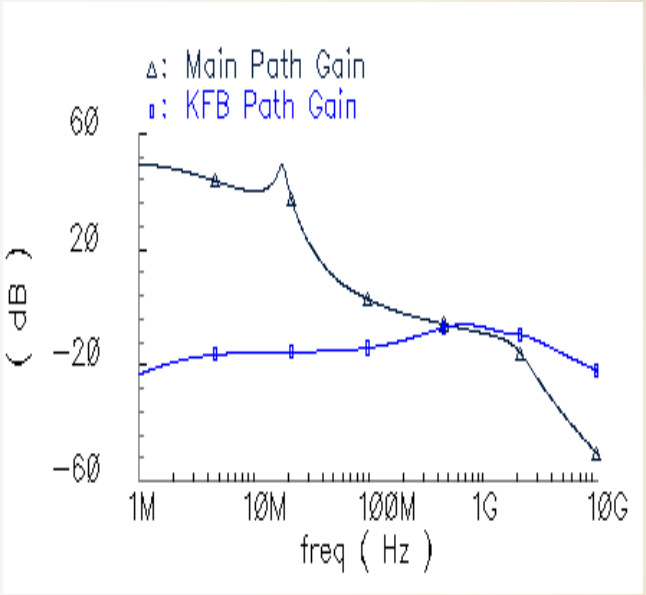
$$H(s) = \frac{Vout(s)}{Vin(s)} = \frac{7.312s^2 + 2.312e17s + 4.223e25}{s(s^2 + 1.414e7s + 1.279e16)}$$

Noise Transfer Function (NTF)

- **The gain of the filter in the signal bandwidth (20MHz) serves to suppress the quantization noise of the TDC**
- **The filter has a minimum inband gain of 37dB**

Mitigating Excess loop delay

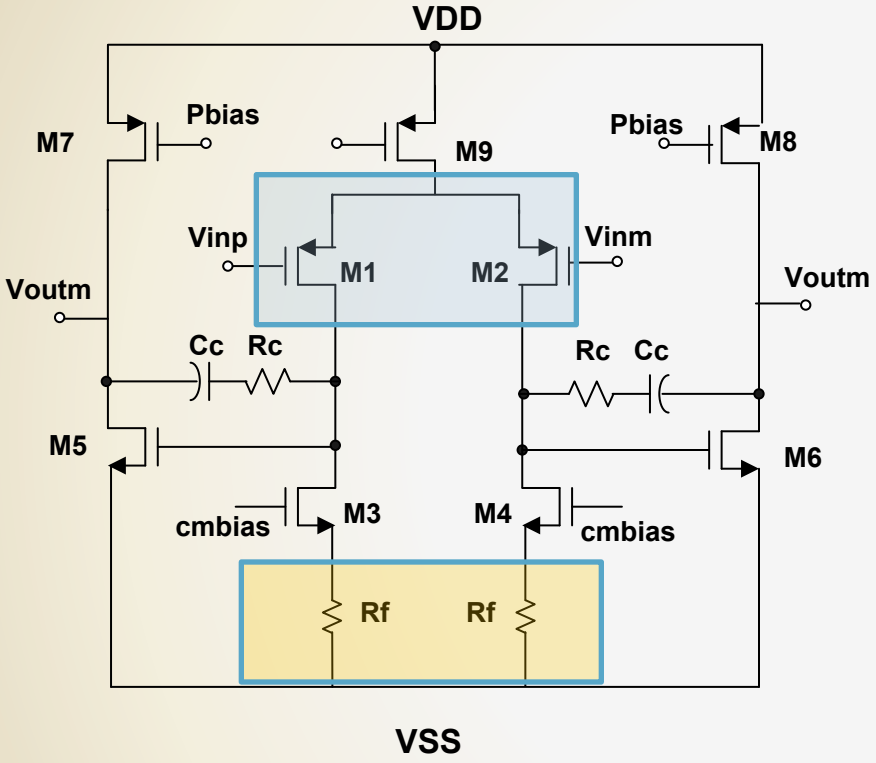




Characterstics	Amplifier 1-2	Amplifier 3
DC Gain	High (>30dB)	Moderate-low (20dB)
Gain-Bandwidth	Moderate (150-250MHz)	High (>500MHz)
Supply Noise Rejection	High (>40dB)	Moderate

KFB provides a 'fast path' through INT3 => *Make AMP3 a minimum phase structure*

Schematic: Amplifier1 / Amplifier2



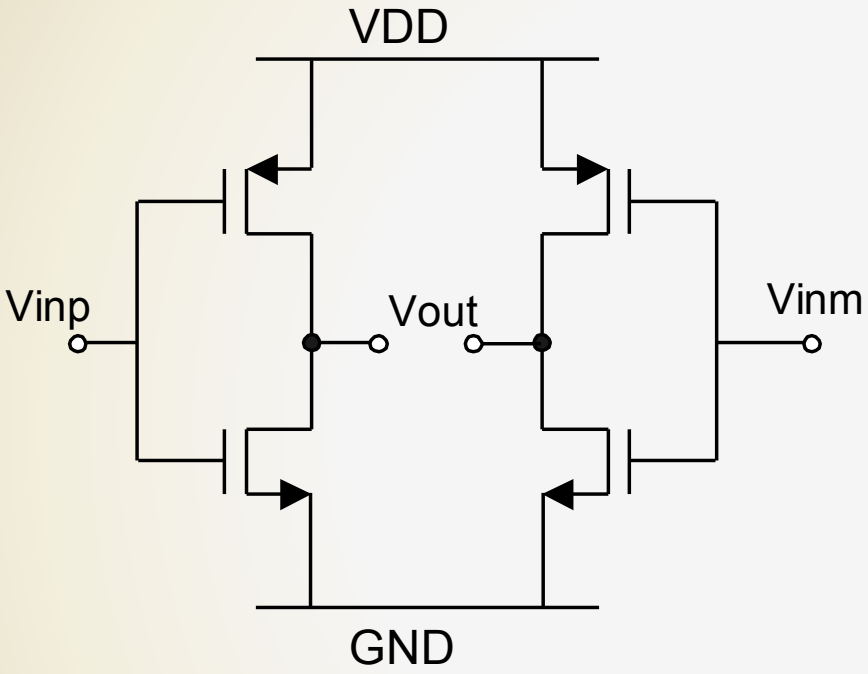
Two Stage 'Typical' configuration

- maximizes gain of the initial stages => Better Q control
- Output pole ~ 4*GBW
- Overall noise limited by input devices
- Rf reduces (degenerate) noise due to NMOS current mirrors

Limitations:

- **Parasitic poles result in additional loop delay/excess phase in the filter (could be > 10 deg at 500MHz)**
- **Limits loop stability and affects the overall performance**

Schematic: Amplifier 3



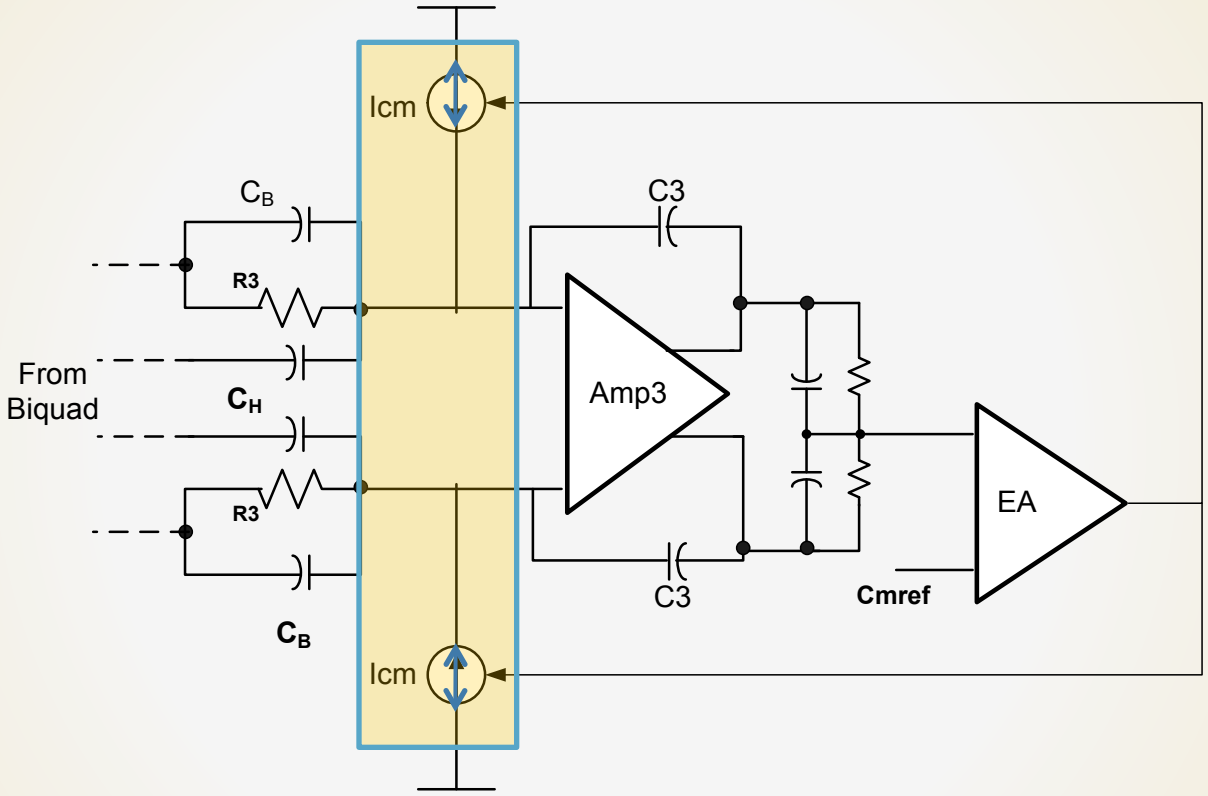
Single Ended Schematic of Amp3

- A simple single stage pseudo-differential 'inverter based' amplifier
- Complementary structure with class A-B action
- CM noise (supply etc) is suppressed by biquad gain of 18dB

Limitations:

- Bias point not accurately controlled + % variation across statistical corner & Temp
- Need for 'Non-conventional' common-mode control

Amplifier 3 Common Mode control

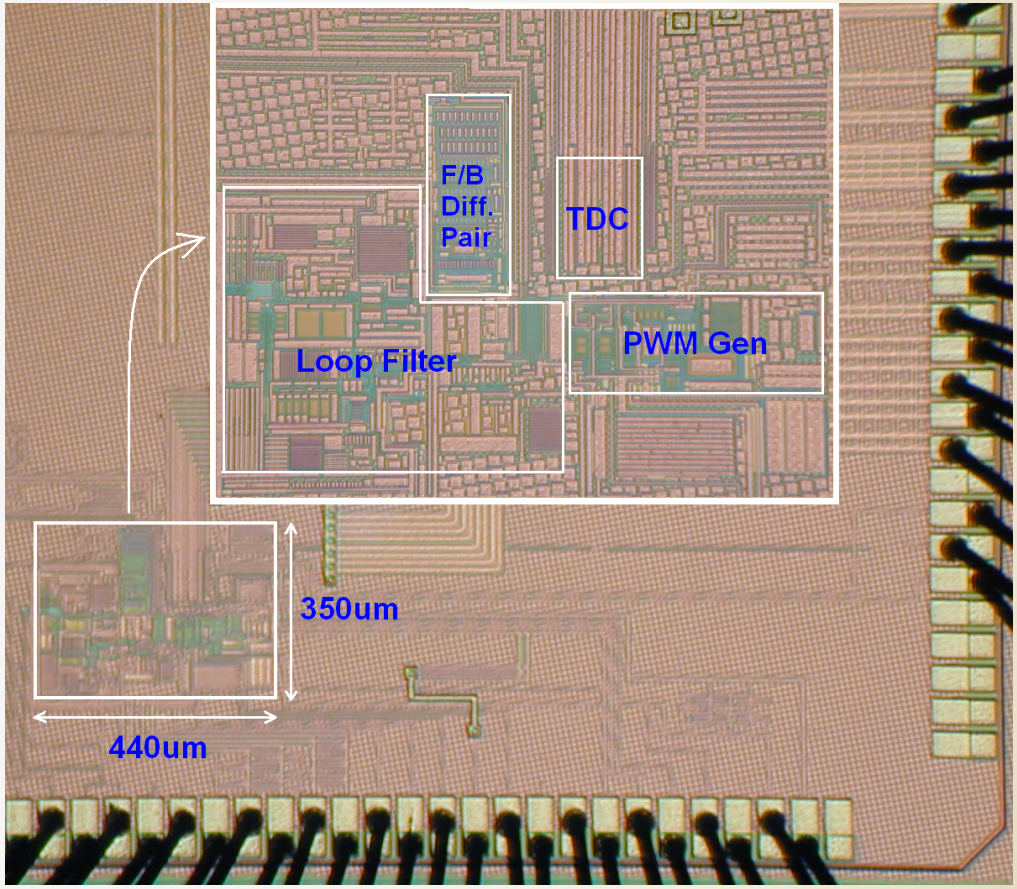


- Current sources at virtual ground control amplifier's common mode

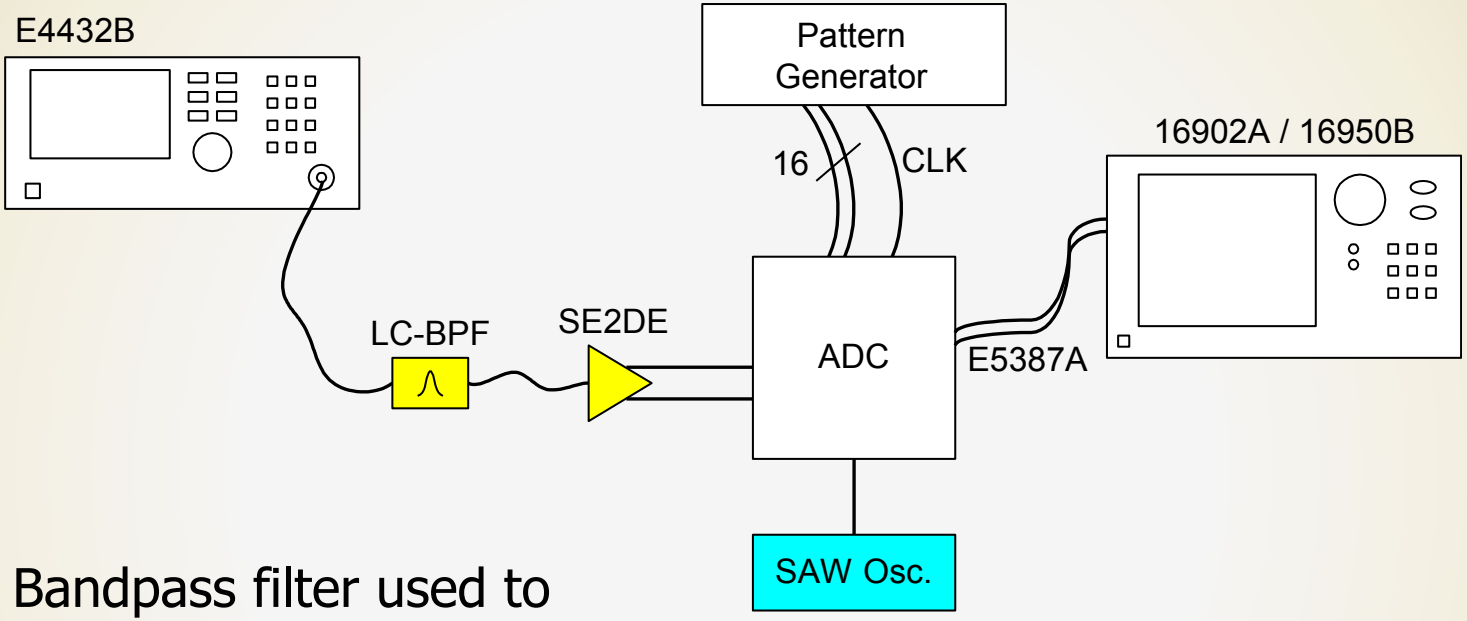
- Icm are: small current source, sized to meet transconductance and noise specifications

Chip Micrograph

- Folded layout to minimize delay in feedback
- Digital approach minimizes area requirement
- Occupies 0.15mm^2



Test Setup



- LC Bandpass filter used to generate a clean input (remove noise and distortion from source)
- SAW Osc. used to generate low jitter clock

- **16950B LVDS input Logic analyzer used to capture data @500MHz**

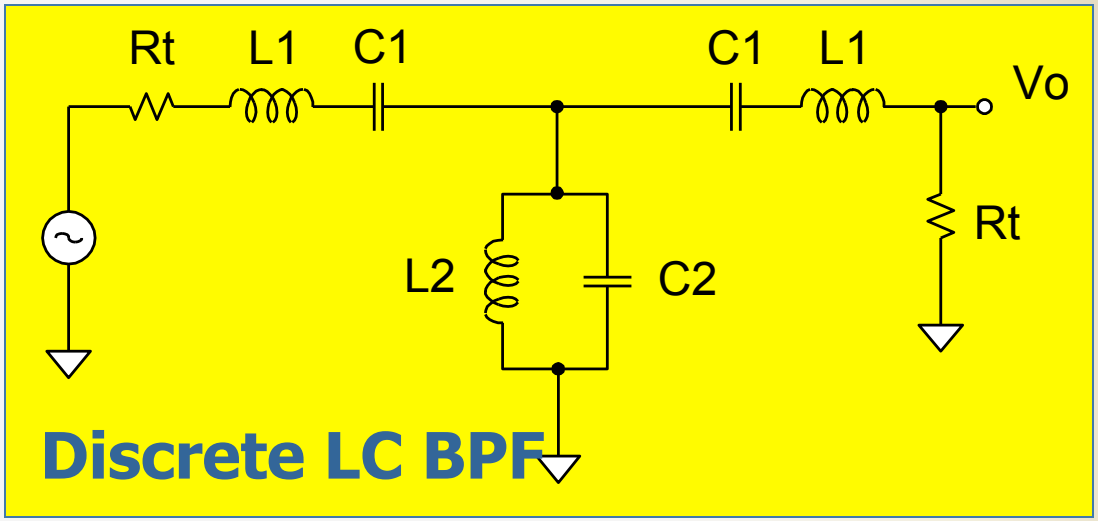
Input Conditioning Filter

Source Performance

- Noise floor = -125dBm/Hz
- THD = -45dB

Required Performance

- Noise < -143dBm/Hz
- THD < -70dB



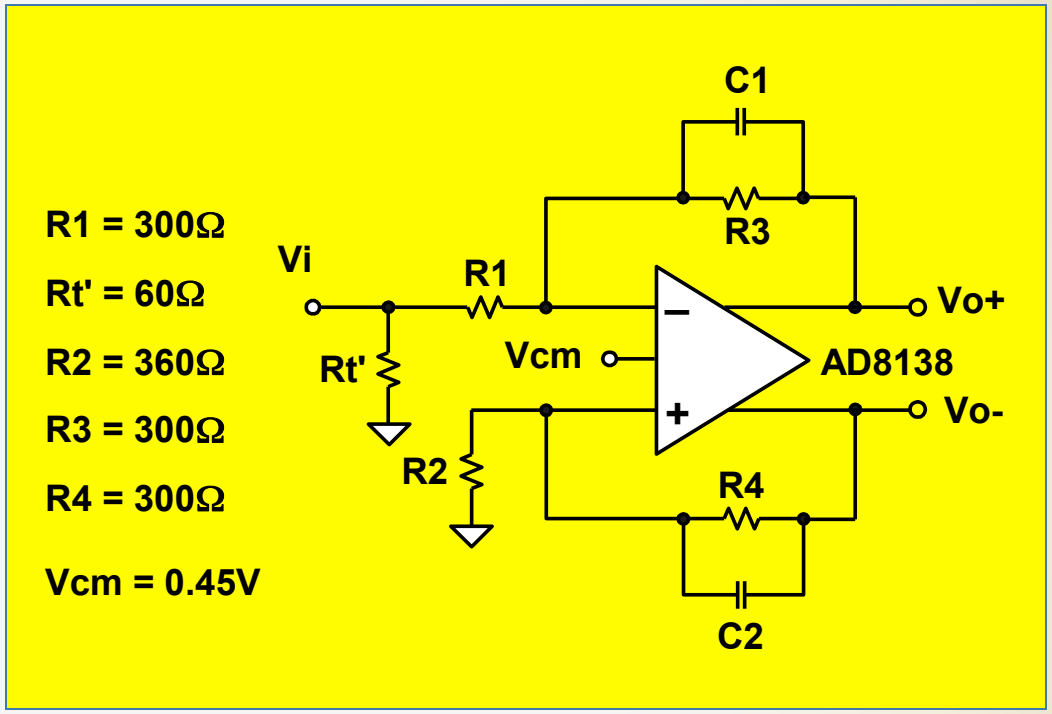
3rd order Chebyshev BPF centered at 4MHz

Performance after filtering

- Noise beyond 150KHz offset < -150dBm/Hz
- Distortion < -75dB

Single-ended to Differential Converter

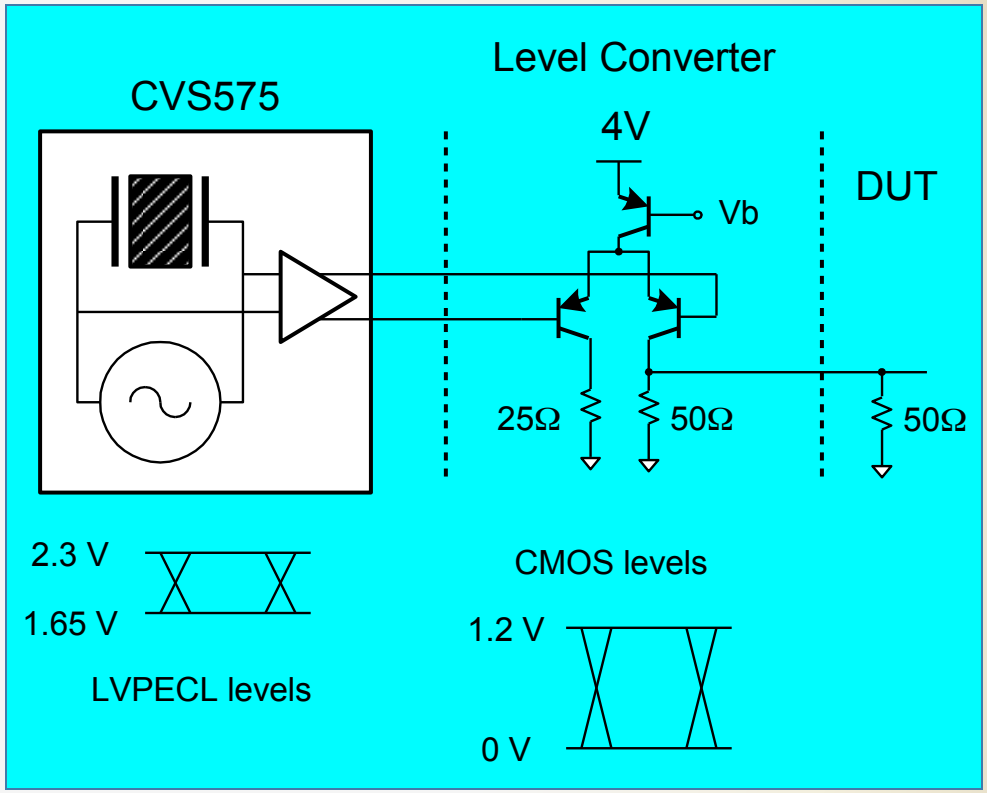
- Differential opamp with CM control
- Input resistance set to 50Ω (Rt=Rt' ||R1)
- R1+Rt' = R2 to eliminate offset
- 1st order RC pole at ~30MHz



- Noise < -146dBm/Hz
- THD < -85dB

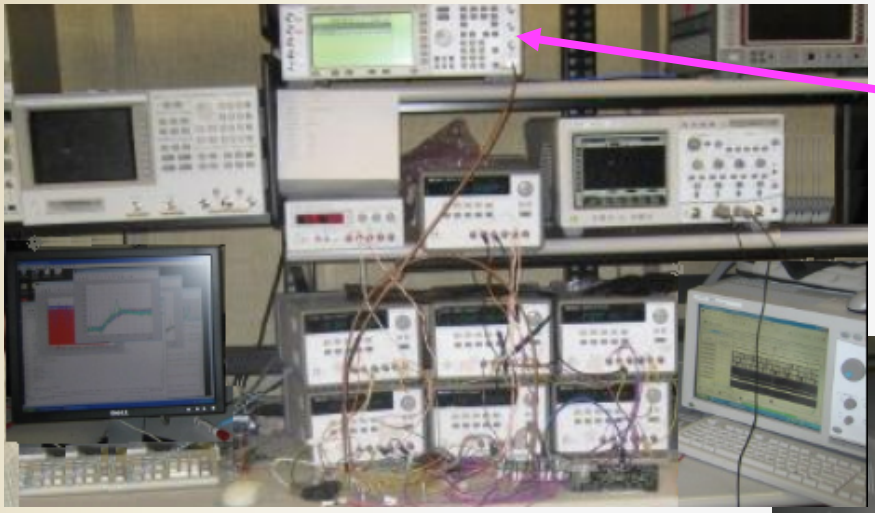
Clock Generation

- Agilent clock generator (E88440) RMS jitter = 20pS
- Need clock jitter < 3pS-rms
- CVS575 SAW Osc. provides low jitter (0.2pS-rms) LVPECL clock
- On-PCB BJT diff.pair converts LVPECL to CMOS levels



Diff pair bias adjusted to provide peak current swing of 50mA

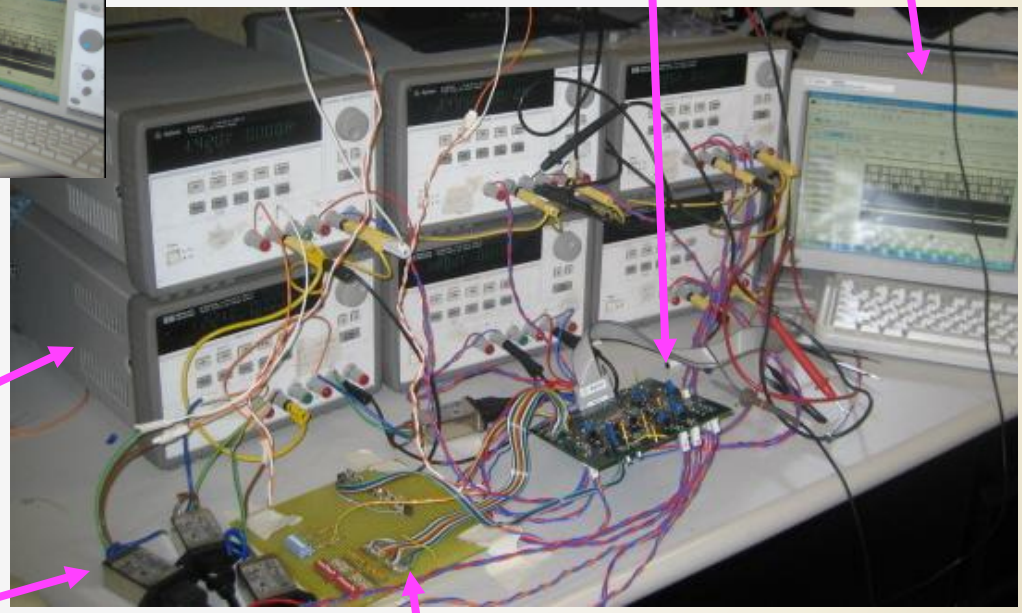
Test Setup Pictures



Signal source

Logic Analyzer

PCB



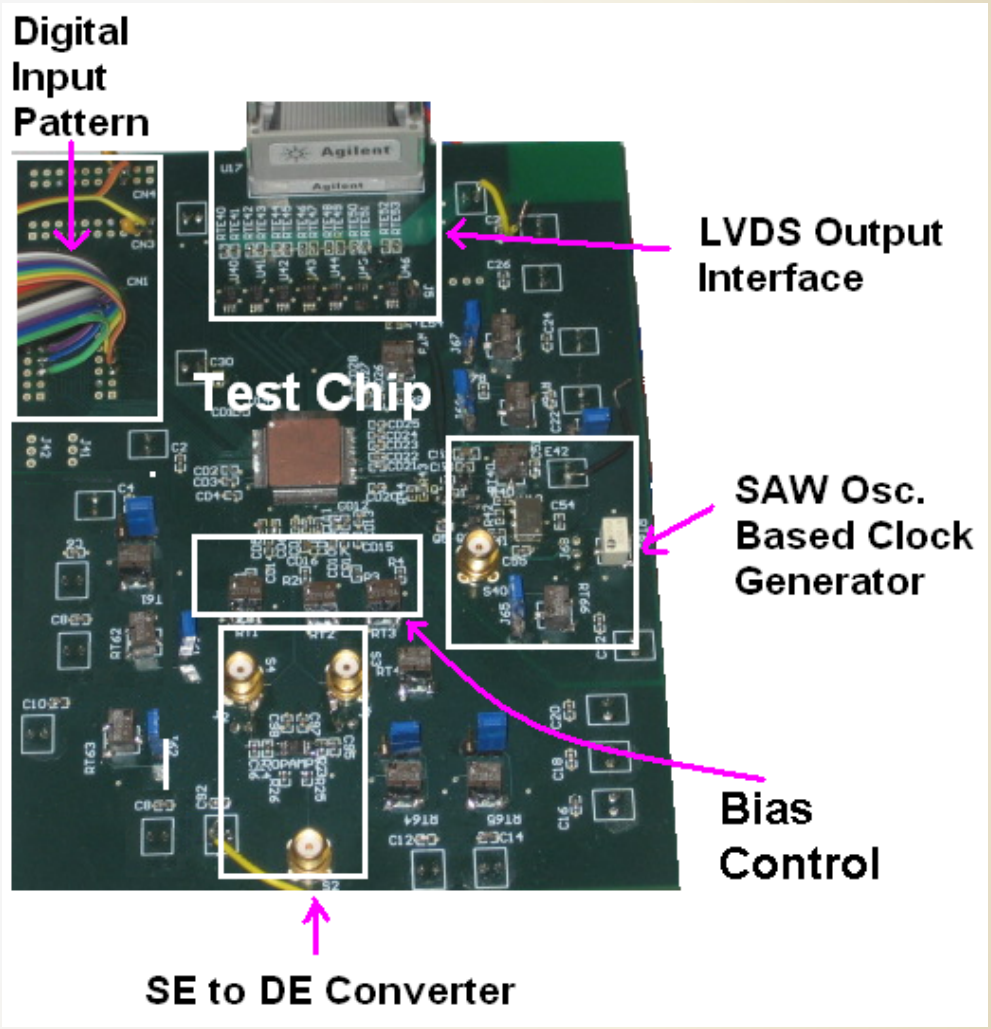
Power supplies

Line filters

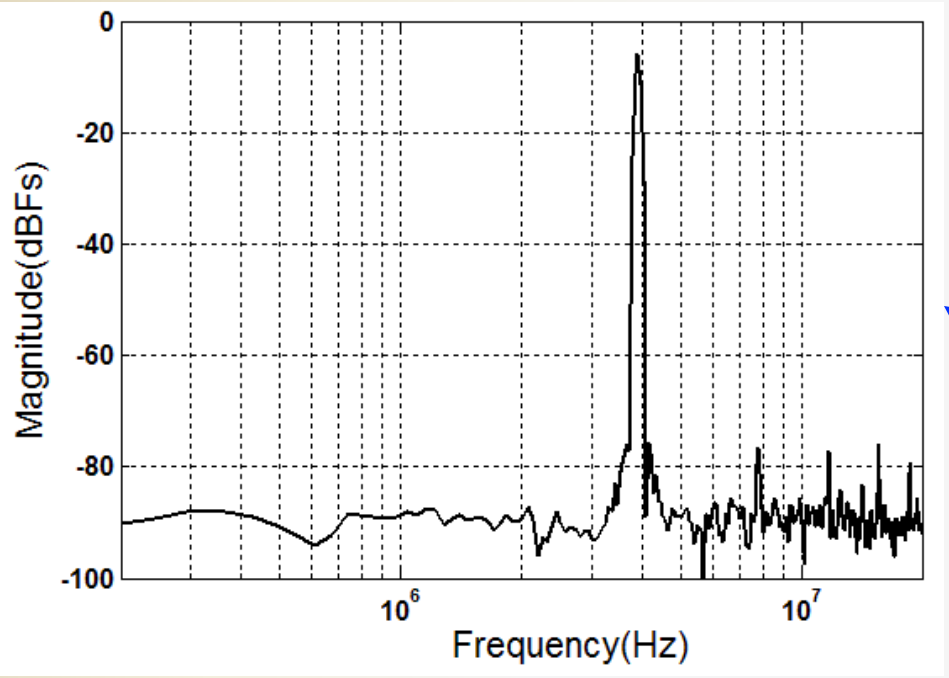
Pattern Generator & LC-BPF

PCB Pictures

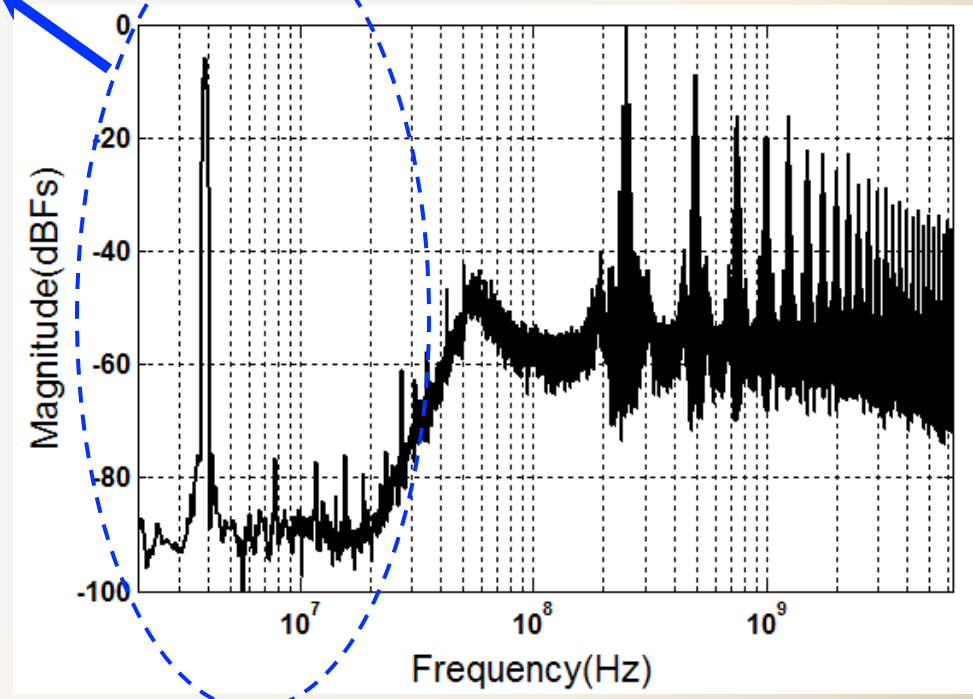
DC Regulators on bottomside of the PCB



Output Spectrum: -5dB Input



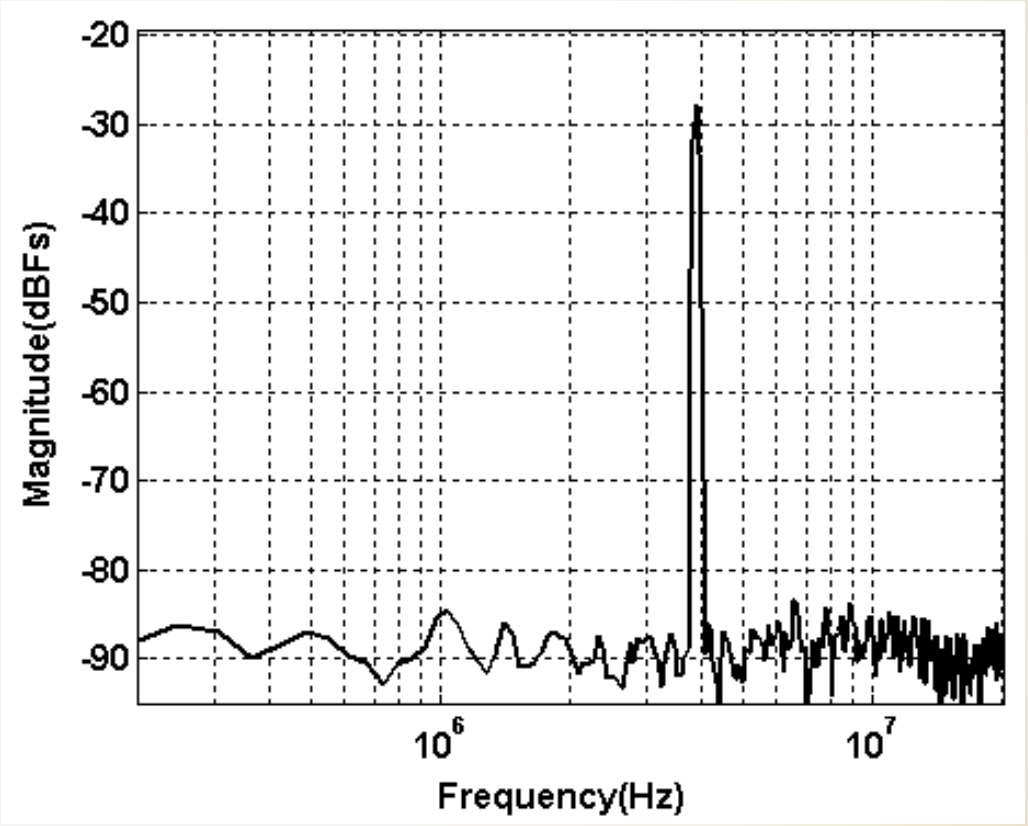
- Output spectrum for -5dB 4MHz Input signal



- **SNR=62dB**
- **THD=65dB**

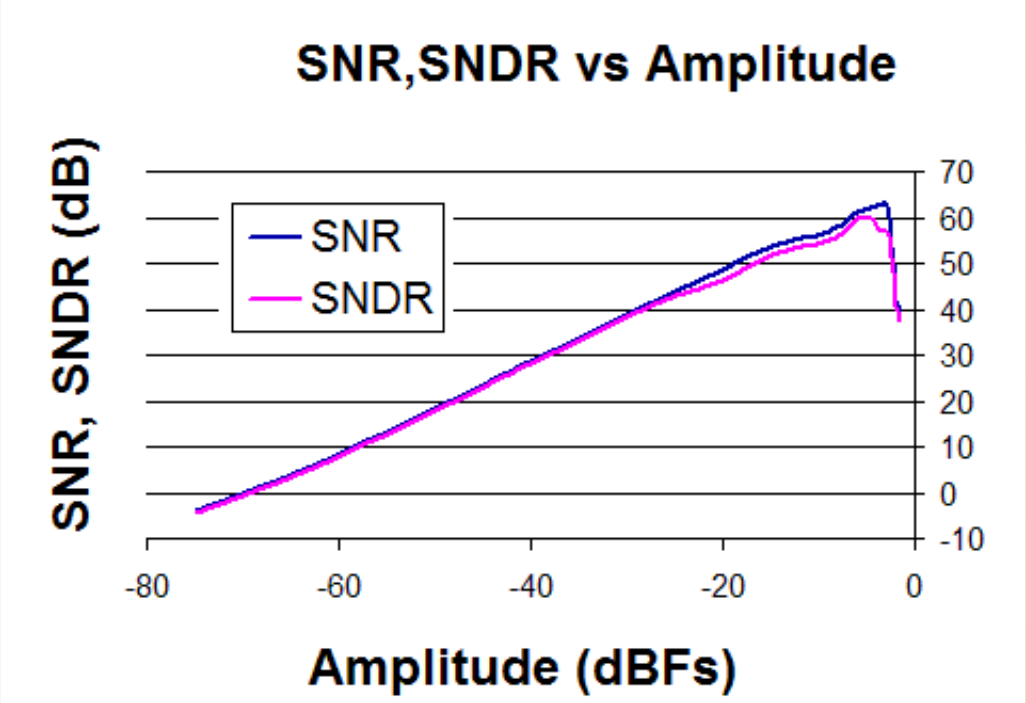
Output Spectrum : -30dB Input

- Output spectrum for -30dB 4MHz Input signal
- SNR=38.6dB
- THD=50.0dB
- Slight increase in noise floor due to loop delay variation with amplitude



Dynamic Range

- DR = 68DB
- Peak SNDR=60dB @ -5dB input
- Peak THD=67dB @ -6dB input



Dynamic Range (DR) is defined as the amplitude range with SNR>0dB

Comparison of 20MHz BW ΔΣ ADCs

	Breems ISSCC 07	Straayer * VLSI 07	Malla ISSCC 08	Proposed ADC
SNDR (dB)	69	55	70	60
Power (mW)	56	38	27.9	10.5
Energy/Conv. (fJ/Step)	595	2058*	270	319
Area (mm^2)	0.5	0.19	1.0	0.15
Output Rate (MSPS)	680	950	420	250

*** Uses VCO based time domain approach**

Conclusions

- Demonstrated the suitability of time-to-digital converter based ADC in silicon
- Sub pico second time edge matching is experimentally proven
- Not just “works around” scaled technology limitations but leverages their strength
- Proposed a ADC solution for nanometric technologies

25MHz Bandwidth (BW) Continuous-Time (CT) Lowpass (LP) ΣΔ Modulator with Time-Domain 3-bit Quantizer and DAC

Cho-Ying Lu, et.al., Sept 2010, JSSC

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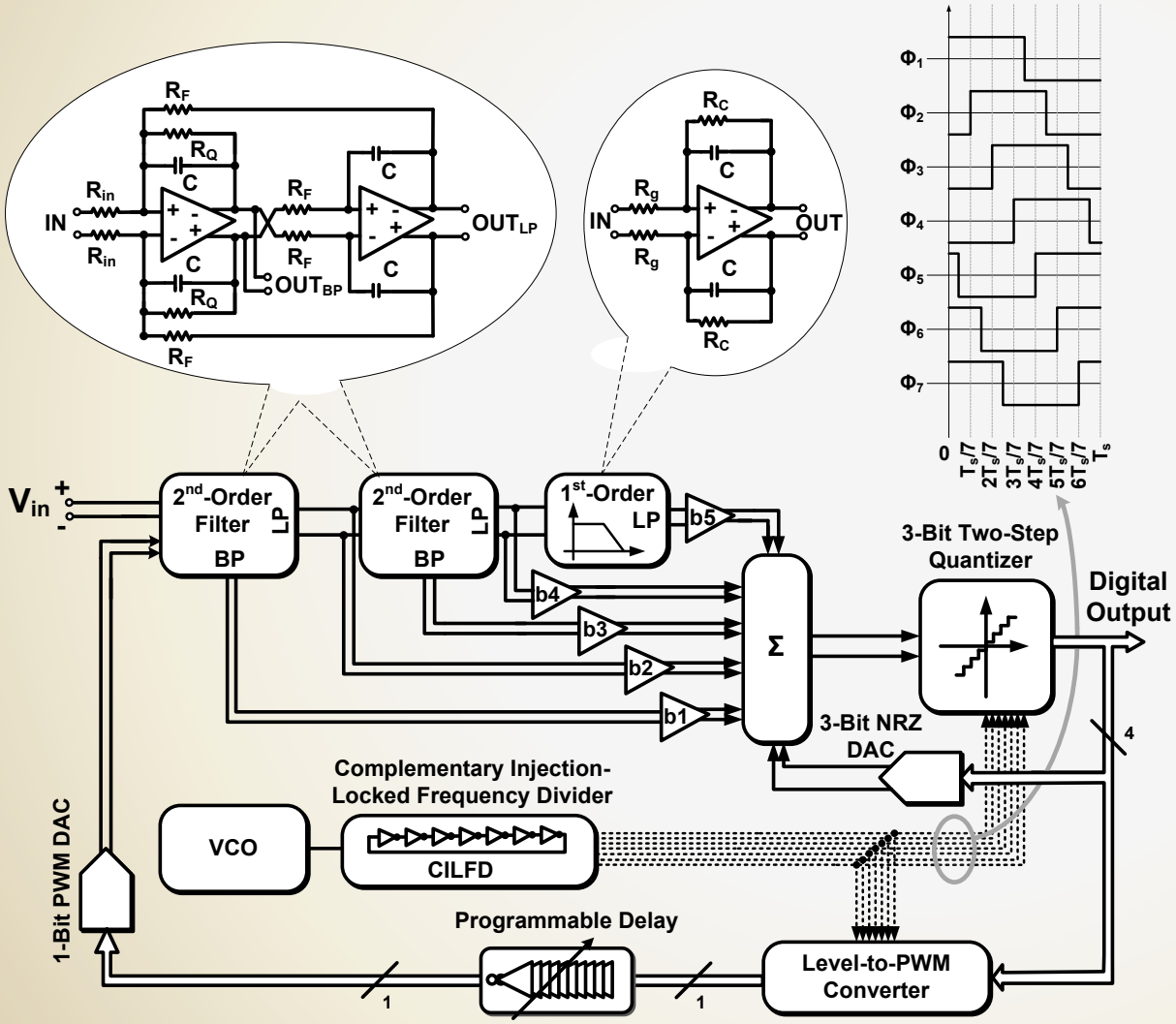
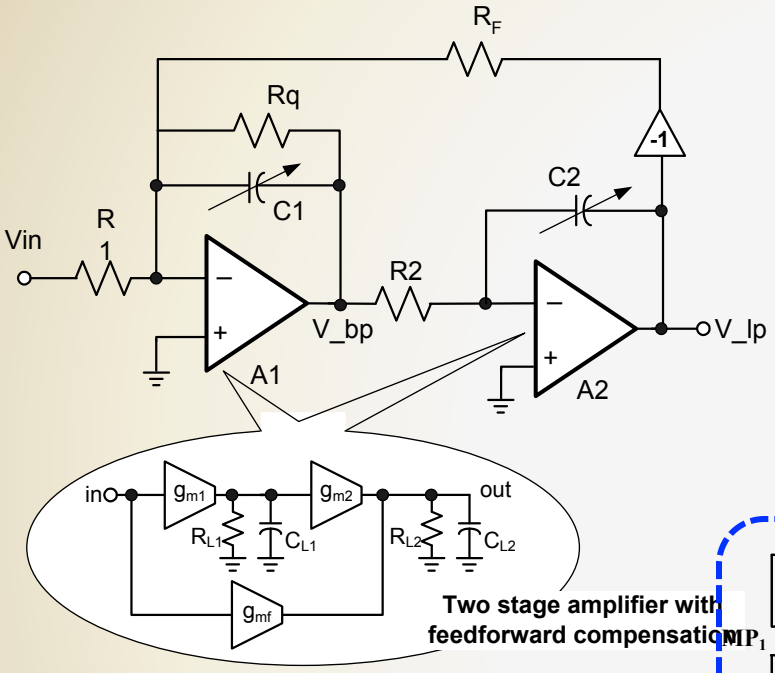
System Architecture



- 5th-order 3-bit feedforward architecture
- Local feedback is to compensate the excess loop delay
- LC-VCO+CILFD are used to generate clean reference clocks

Biquadratic section and OPAMP



Quiescent current ~ 1.0 mA

GBW > 800MHz

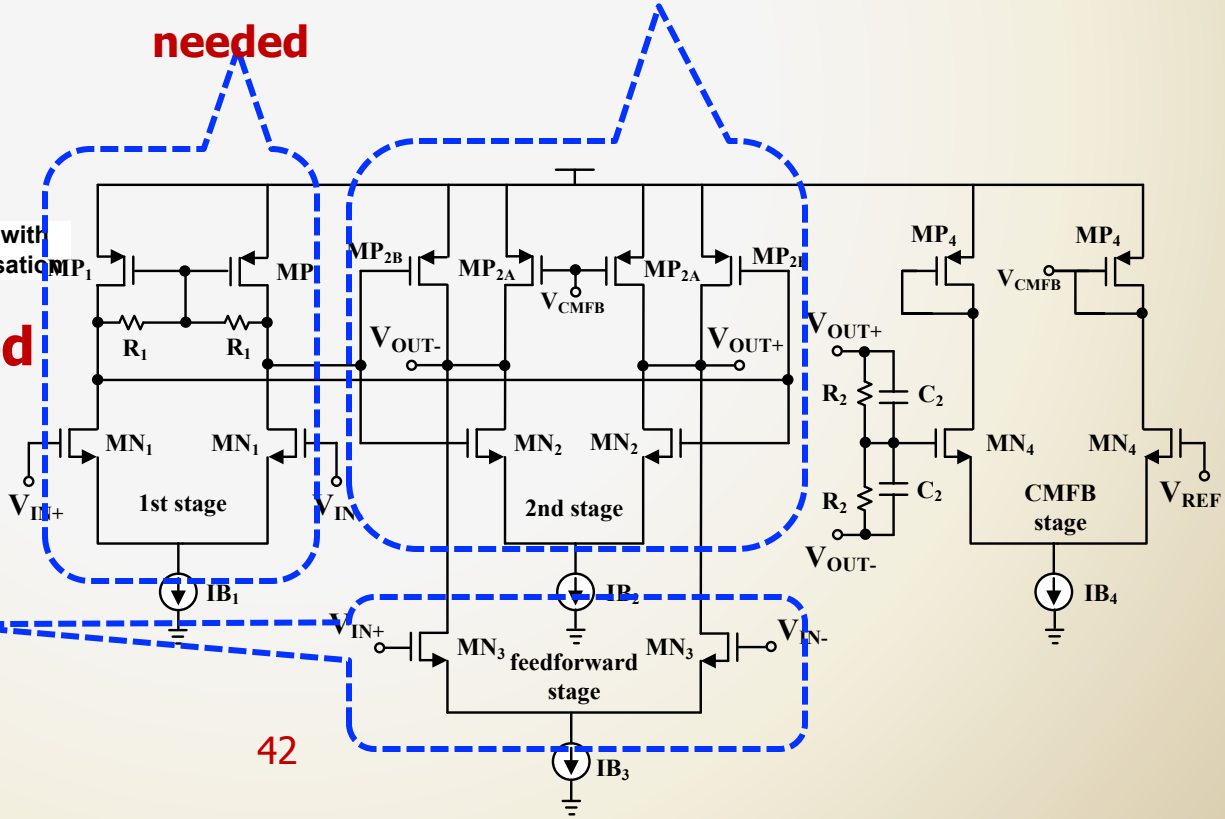
First stage

No extra CMFB needed

Second stage

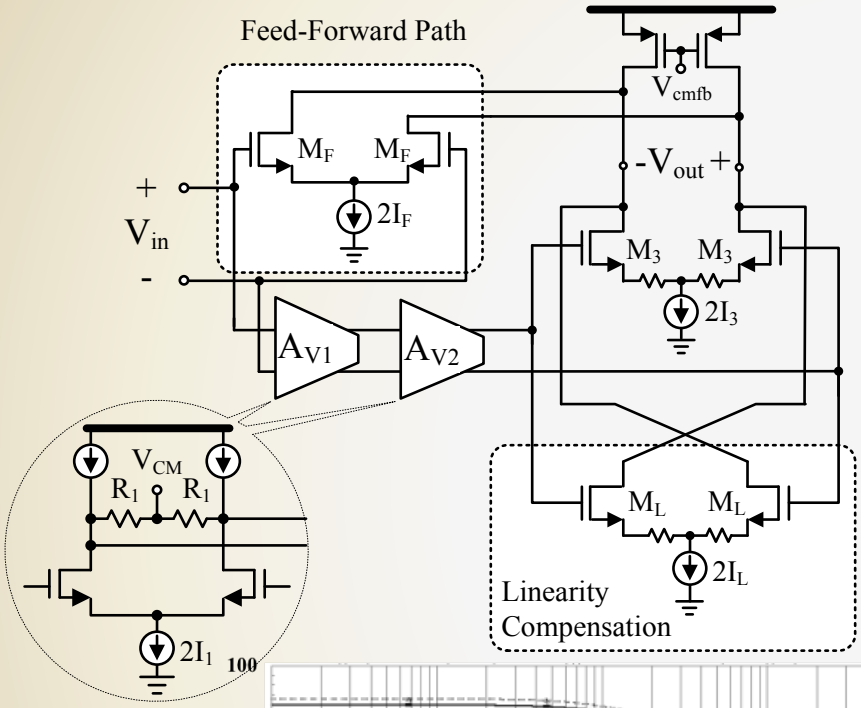
(current re-use)

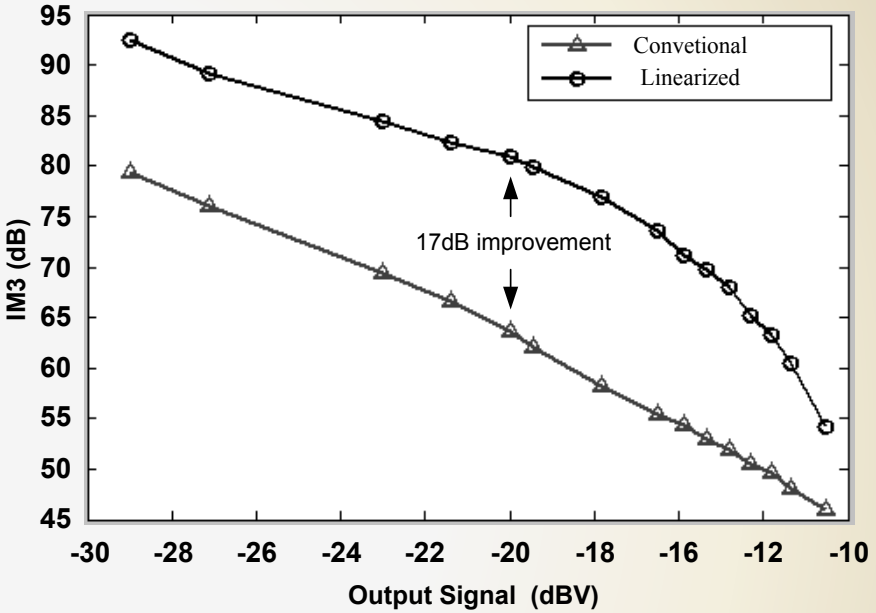
Large resistors are used

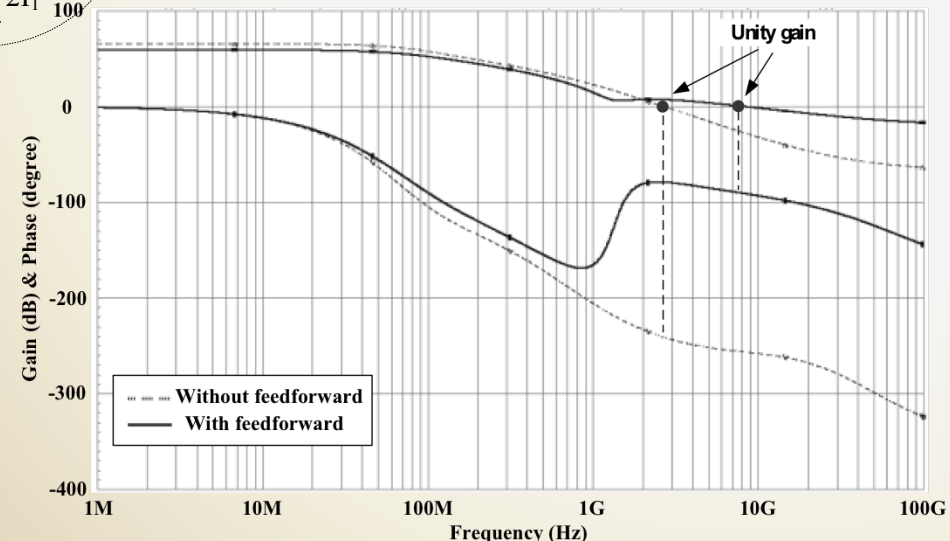


Feed-forward stage

Very linear OPAMP for >100MHz applications

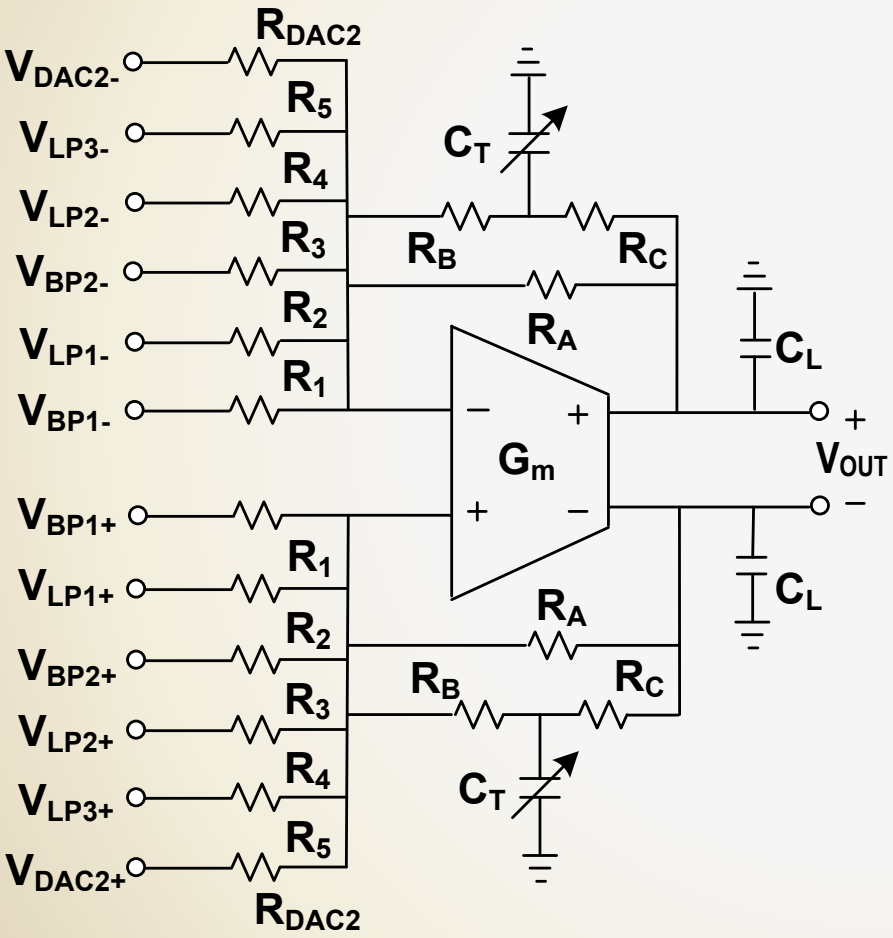






C.-Y. Lu, "A 6th-order 200MHz IF Bandpass Sigma-Delta Modulator With over 68dB SNDR in 10MHz Bandwidth," To be published JSSC

Wide-band Adder with delay compensation



The load resistor is split into 2 pieces and one section replaced by an RC T-network

Rfeedback = Ra||(Rb+Rc) at low frequencies

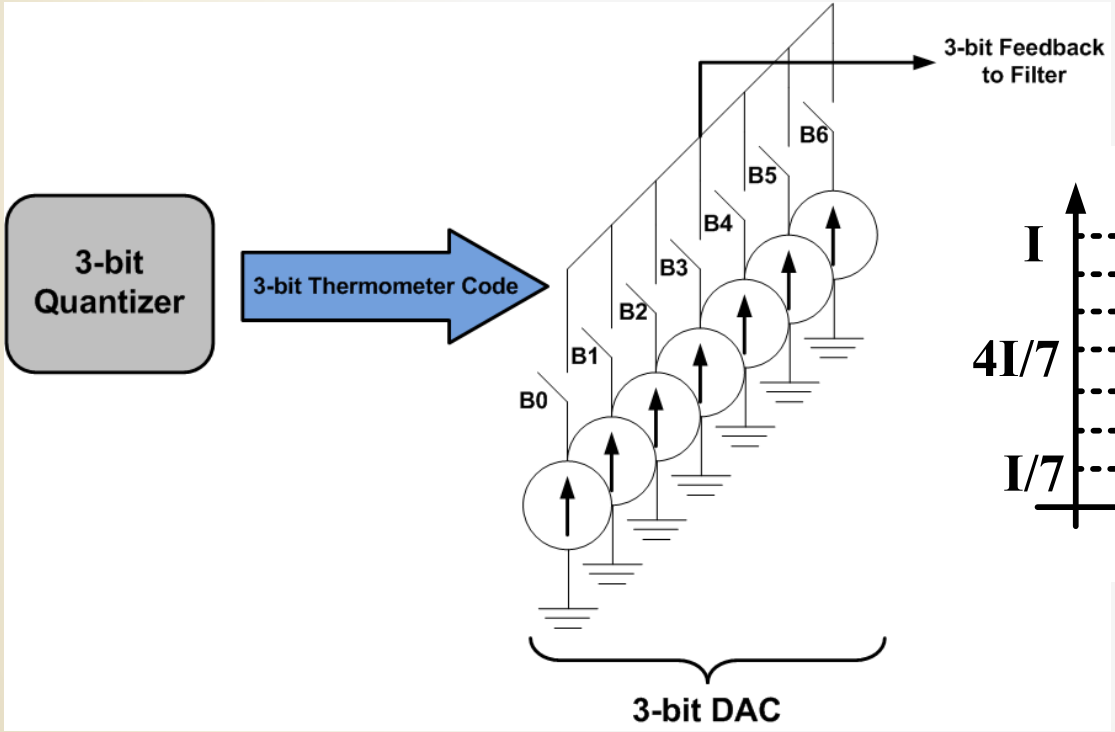
Rfeedback = Ra at low frequencies

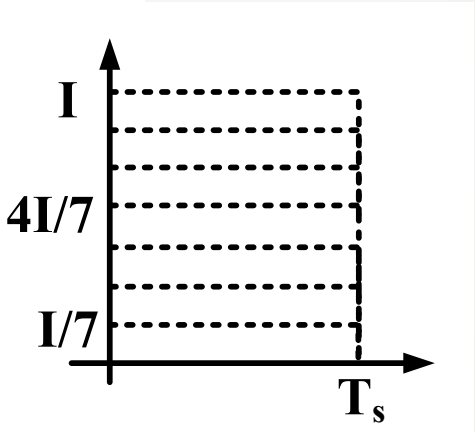
$$\theta(\omega) = \tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_p}\right)$$

$$\tau_{delay} = -\frac{d\theta(\omega)}{d\omega} = -\frac{(\omega_z - \omega_p)(\omega^2 - \omega_z\omega_p)}{(\omega^2 + \omega_z^2)(\omega^2 + \omega_p^2)}$$

Pulse Amplitude Modulation

- Traditional Multi-level Digital Signal





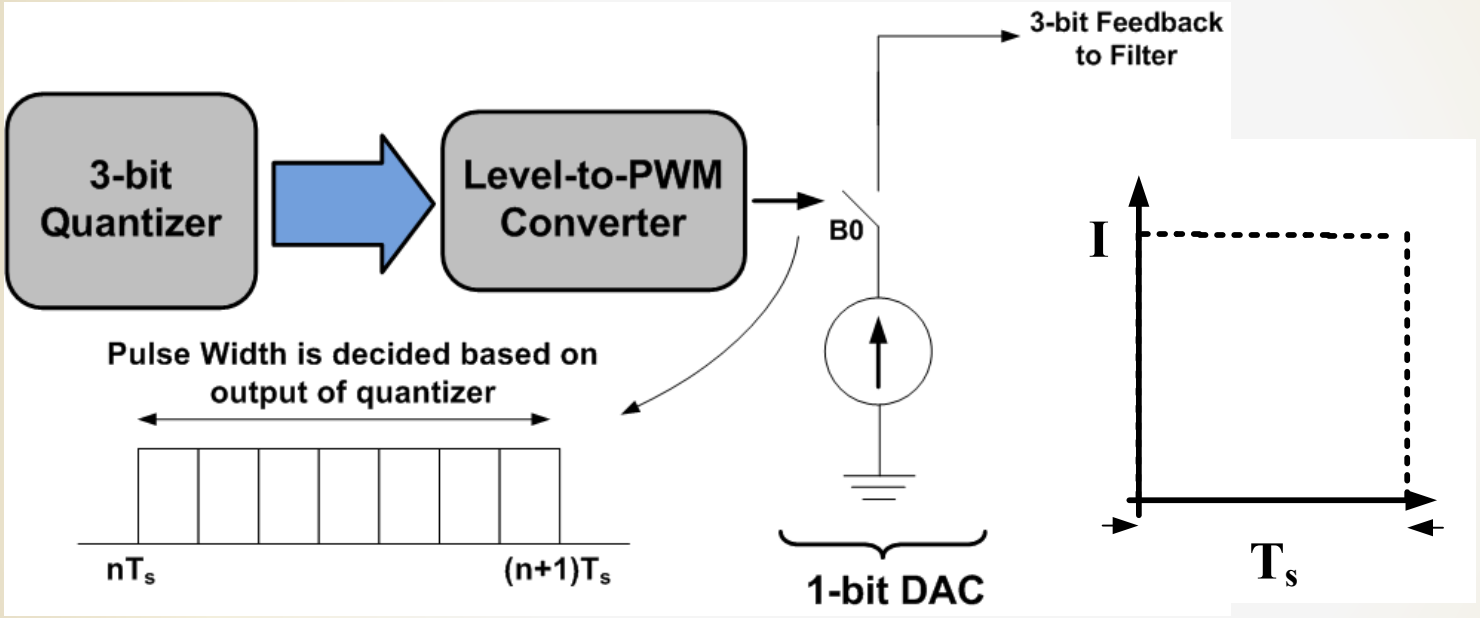
$$Q_{inj} = (\alpha I)T_s$$

where:

$$\alpha = [0, \frac{1}{7}, \frac{2}{7}, ... \ 1]$$

Unit element current mismatch generates DAC non-linearity.

Time-Domain Pulse Width Modulation



$$Q_{inj} = I(\alpha T_s)$$

where:

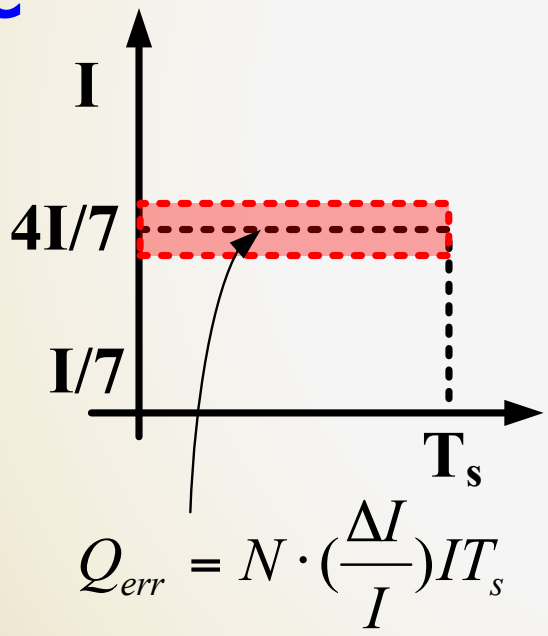
$$\alpha = [0, \frac{1}{7}, \frac{2}{7}, \ldots. 1]$$

Only inherently linear 1-level DAC achieve multi-bit feedback

Systematic (Nonlinearity) errors

- Error Charge from Device Mismatch

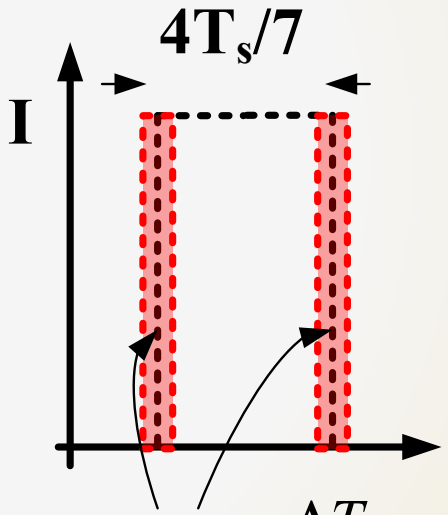
Conventional Multi-Level DAC



$$Q_{err} = N \cdot (\frac{\Delta I}{I}) I T_s$$

Current errors accumulate

1-level PWM DAC

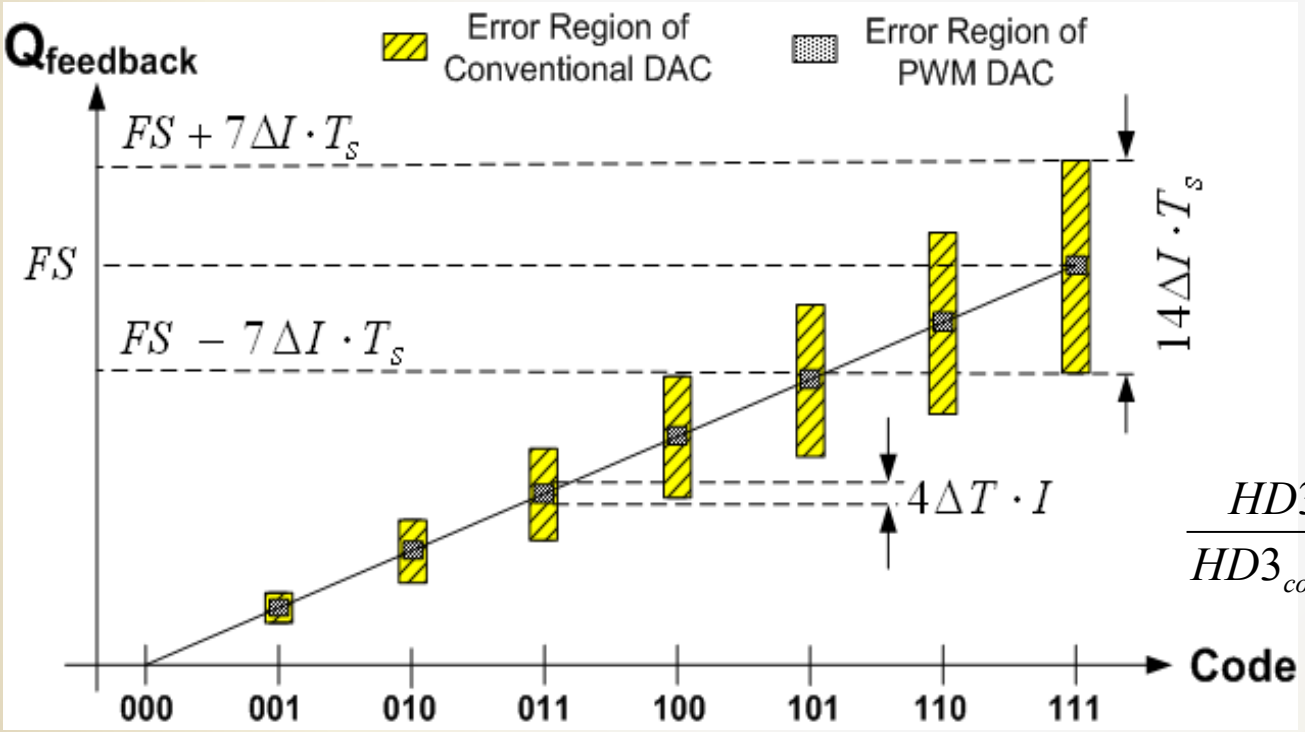


$$Q_{err} = 2 \cdot (\frac{\Delta T}{T}) I T_s$$

Timing errors at the pulse edges

INL, DNL and Linearity

- Robustness to device mismatch
  - only affect the edges of the pulse



$$\delta_{\%I} = \frac{\Delta I}{I} = 0.5\%$$

$$\delta_{\%T} = \frac{\Delta T}{T} = 0.16\%$$

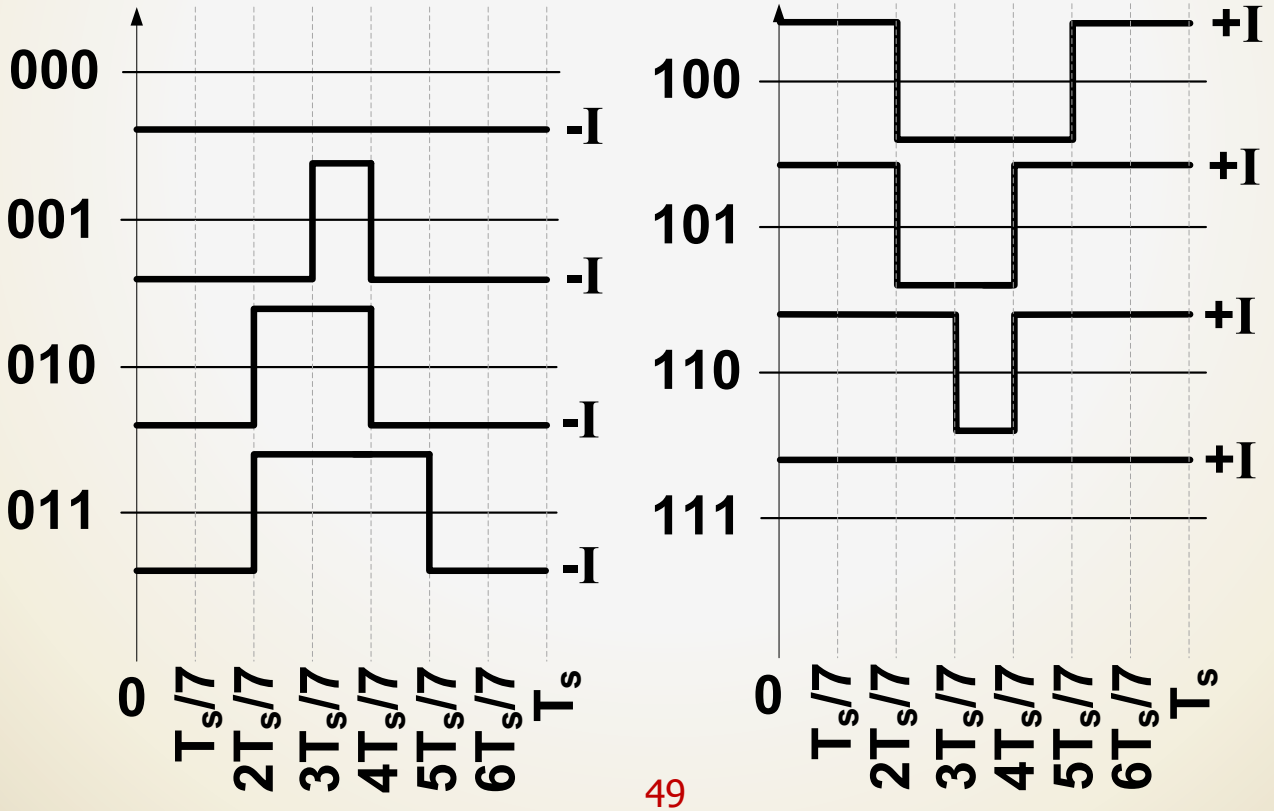
$$\frac{HD3_{PWM}}{HD3_{conventional}} \cong \left(\sqrt{\frac{2}{7}}\right)\left(\frac{\delta_{\%T} = 0.16\%}{\delta_{\%I} = 0.5\%}\right)$$

PWM Linearity could be >10dB better!

Time-Domain Pulse Width Modulation

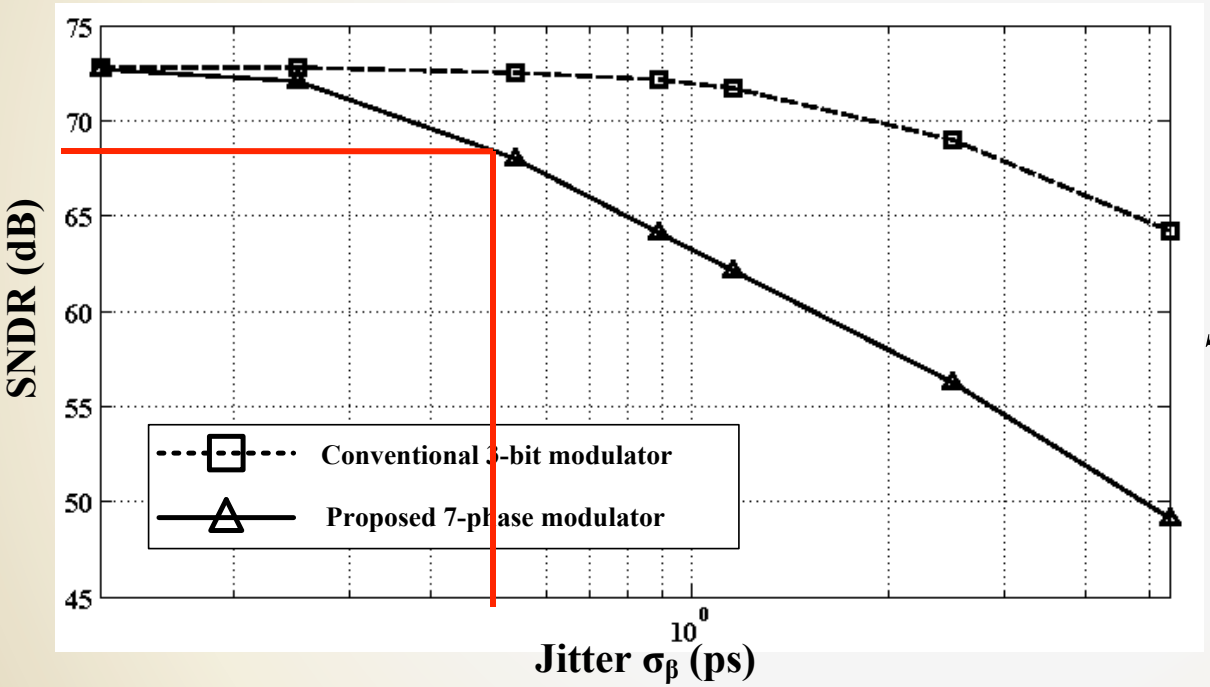
- Pulse Arrangement
  - To ease the design of interface circuitry between quantizer and level-to-PWM converter

$$SJNR_{peak} = 10\,log_{10}\left(\frac{T_s^2 \cdot OSR}{2 \cdot \sigma_y^2 \cdot \sigma_\beta^2}\right)$$



Jitter Comparison

- Sensitivity to Jitter Noise: 400 MHz clock frequency
  - More transitions in one sampling period

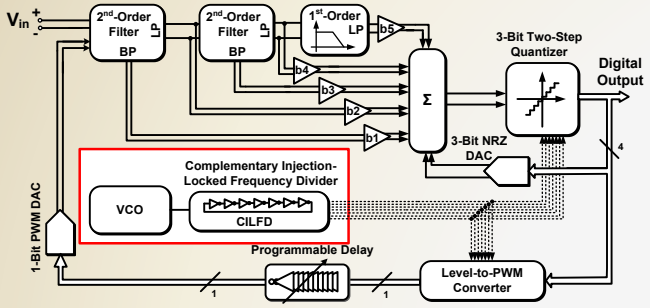


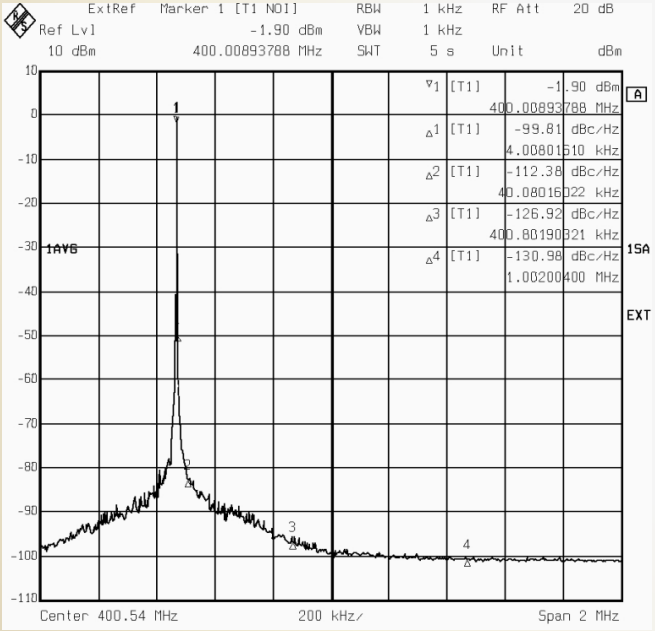
$$SJNR_{peak} = 10\,log_{10}\left(\frac{T_s^2 \cdot OSR}{2 \cdot \sigma_y^2 \cdot \sigma_\beta^2}\right)$$

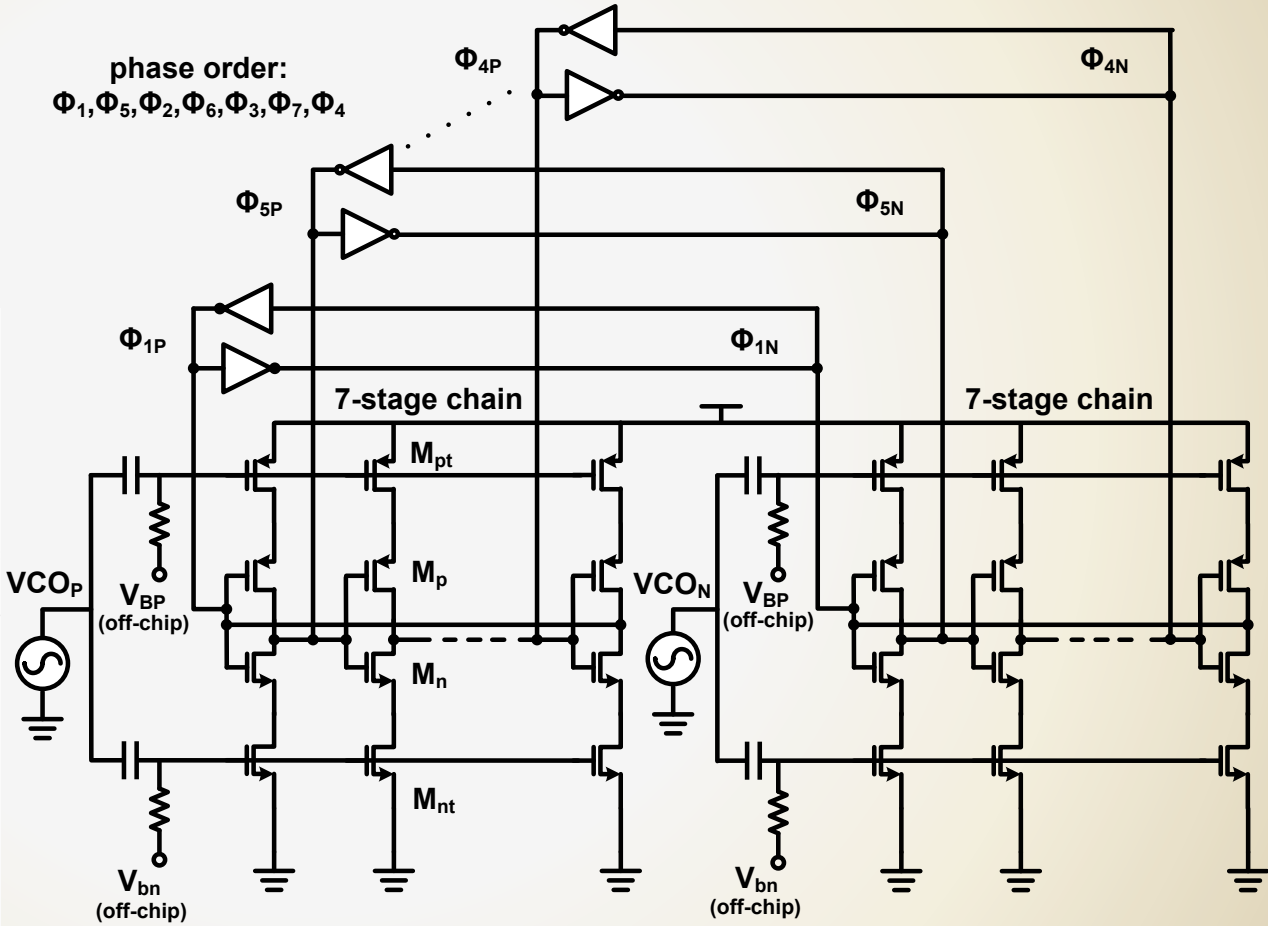
Worst case for the PWM case: Jitter at both edges is uncorrelated

More sensitive to jitter => Require low-jitter Clock (< 0.5ps)

LC-VCO + CILFD



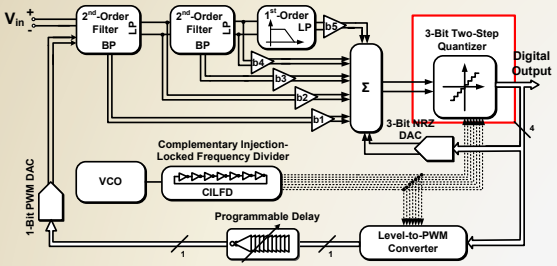




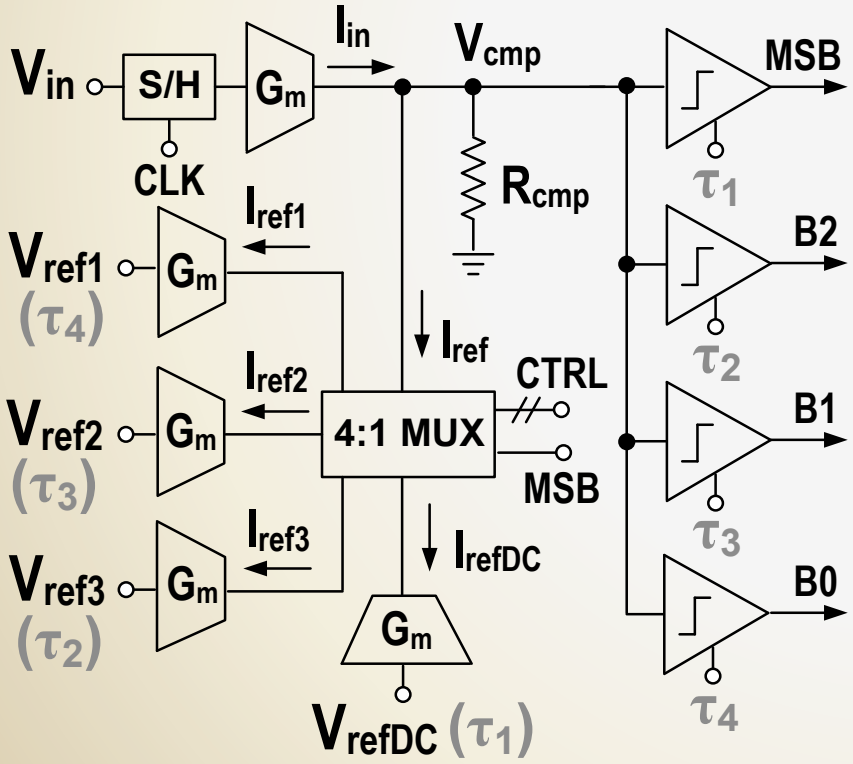
- Phase noise of VCO is -119dBc/Hz @ 1MHz
- CILFD phase noise is -136dBc/Hz @ 1MHz

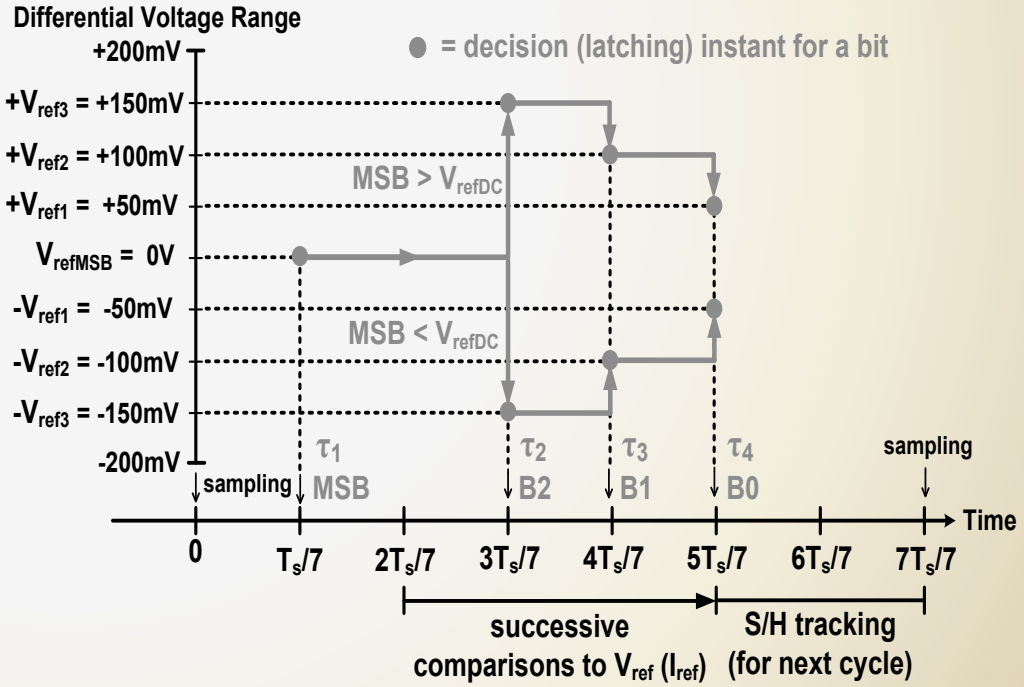
Jitter between phases is highly correlated

Proposed 3-bit Two-Step Quantizer

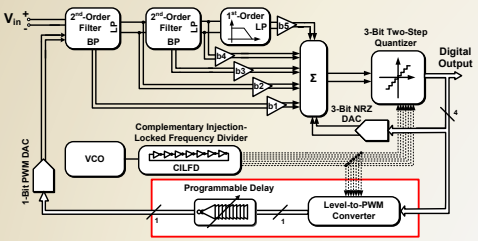


- The output is composed by **1 MSB + 3LSB**
- The MSB is determined first

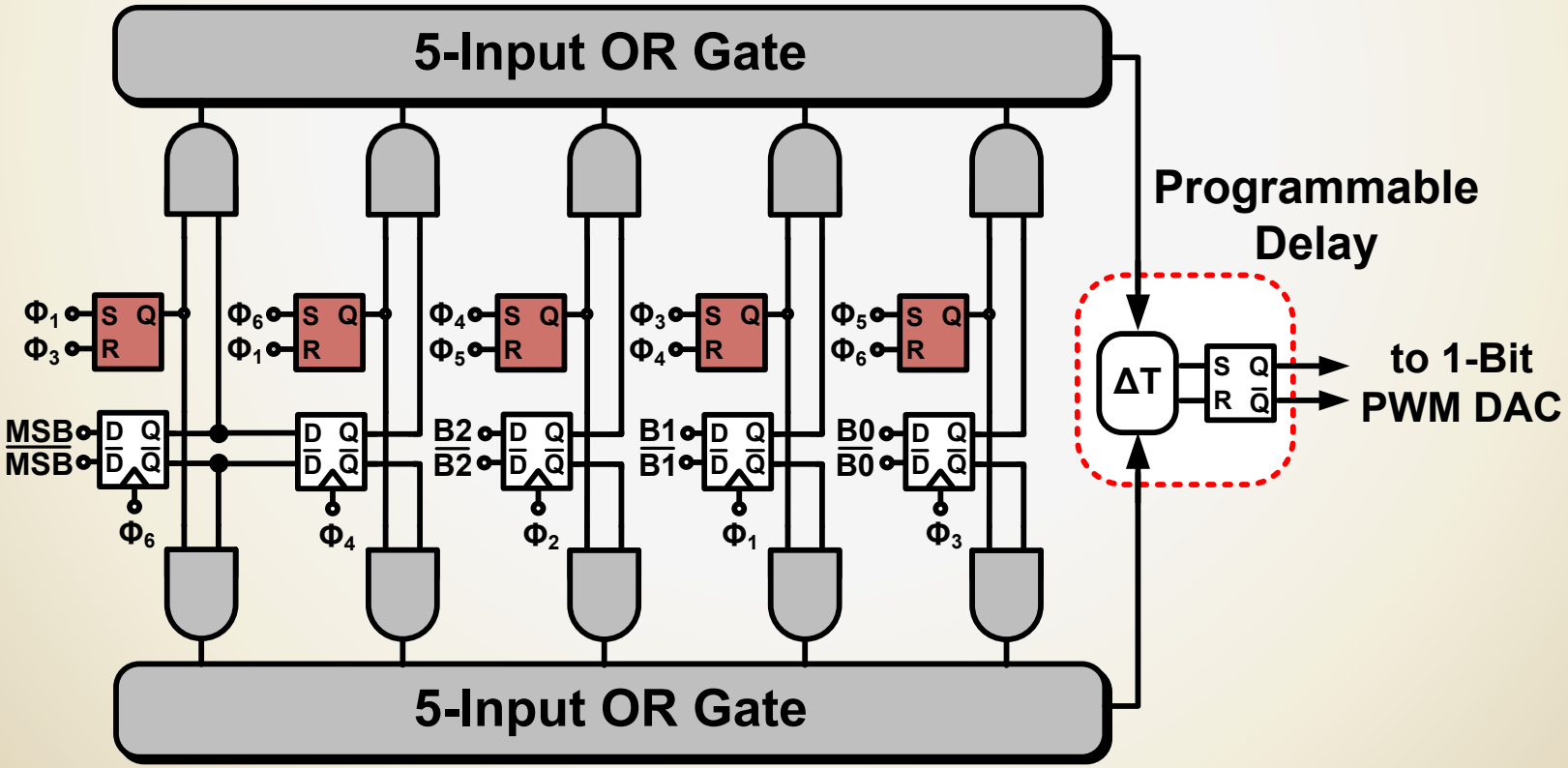




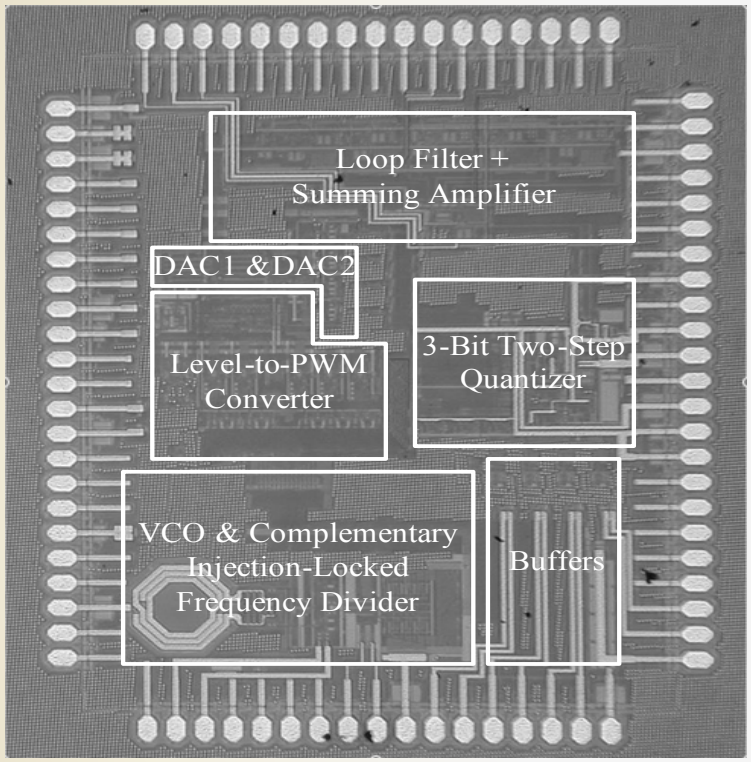
Proposed Level-to-PWM Converter

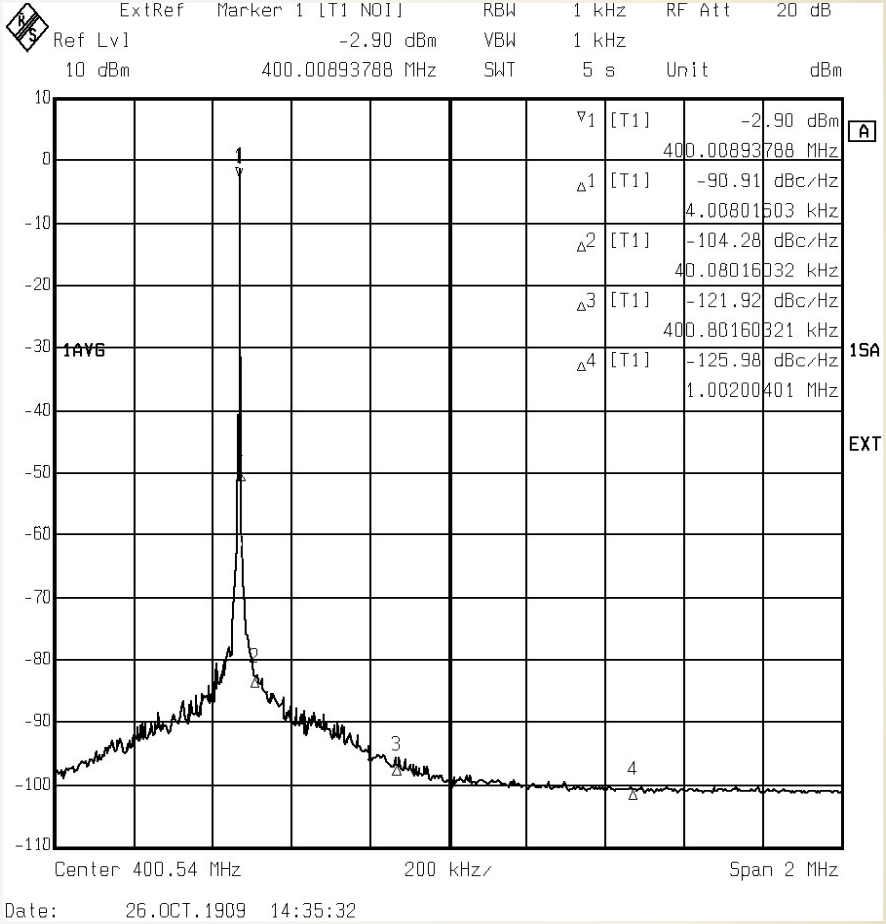


- SR latches generate the pulses
- AND gates + OR gates decide the required pulses
- Programmable Delay is used to minimize excess loop delay



Chip Microphotograph & Clock Jitter





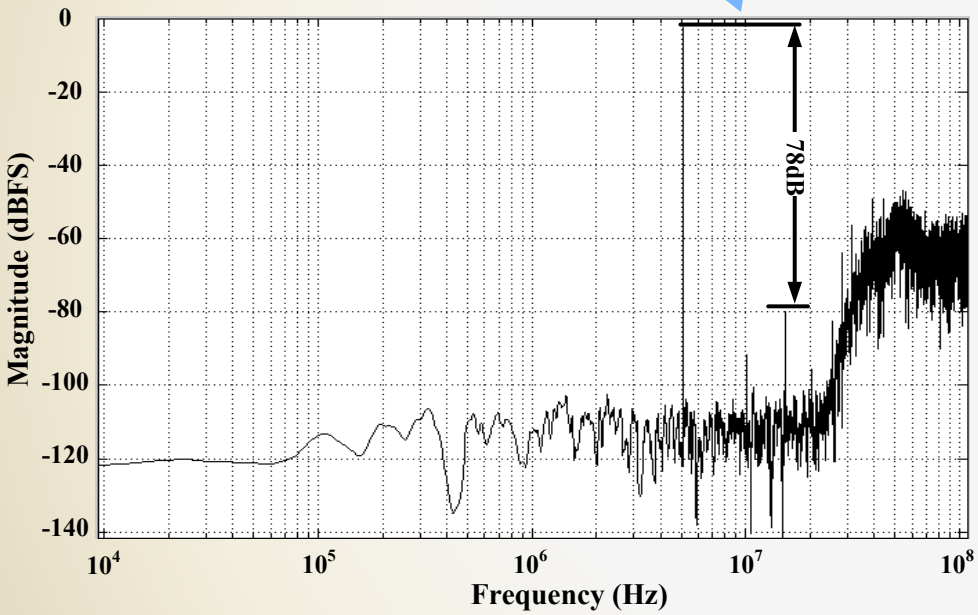
Core area = 2.6mm²

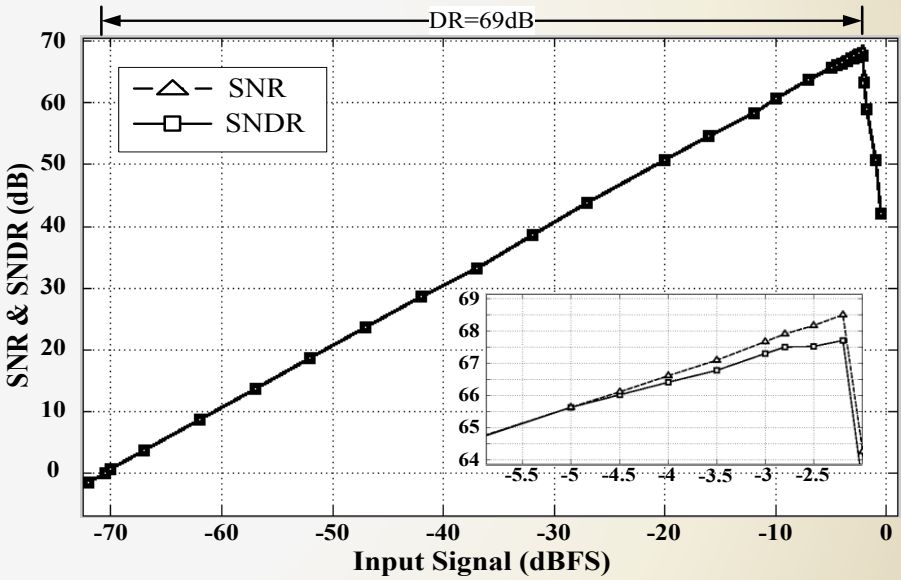
RMS jitter= 0.27ps
=> SJNR > 75dB

Measurement Result – SNDR & SFDR

- Output Spectrum of the Modulator

-2.2dBFS @ 5.08MHz



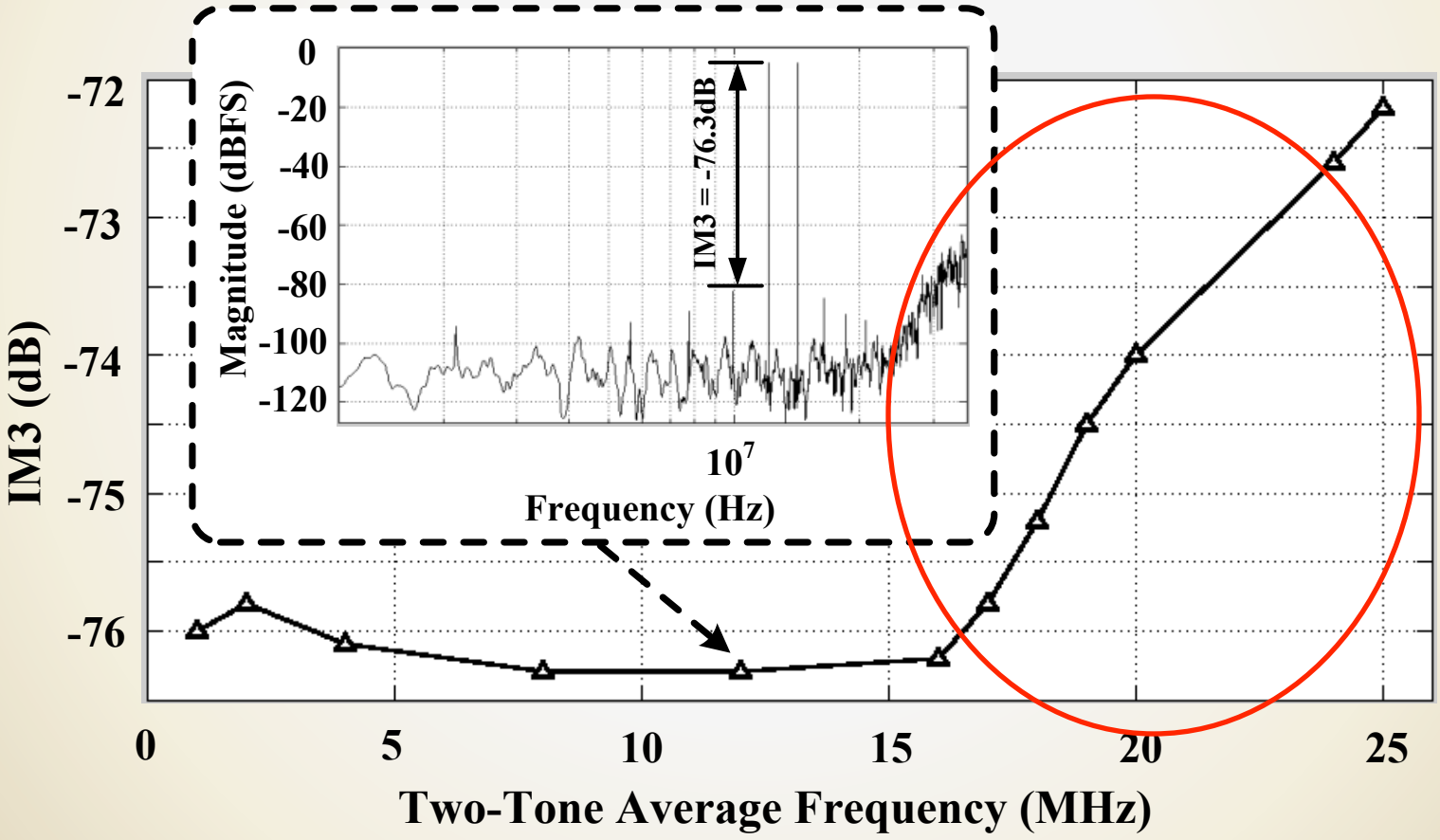


- **Peak SNR= 68.5dB @25MHz BW**
- **Peak SNDR= 67.7dB @25MHz BW**
- **SFDR=78dB**

55

Signal to Distortion Ratio

- Two tones with 2MHz apart and -2dBFS overall power

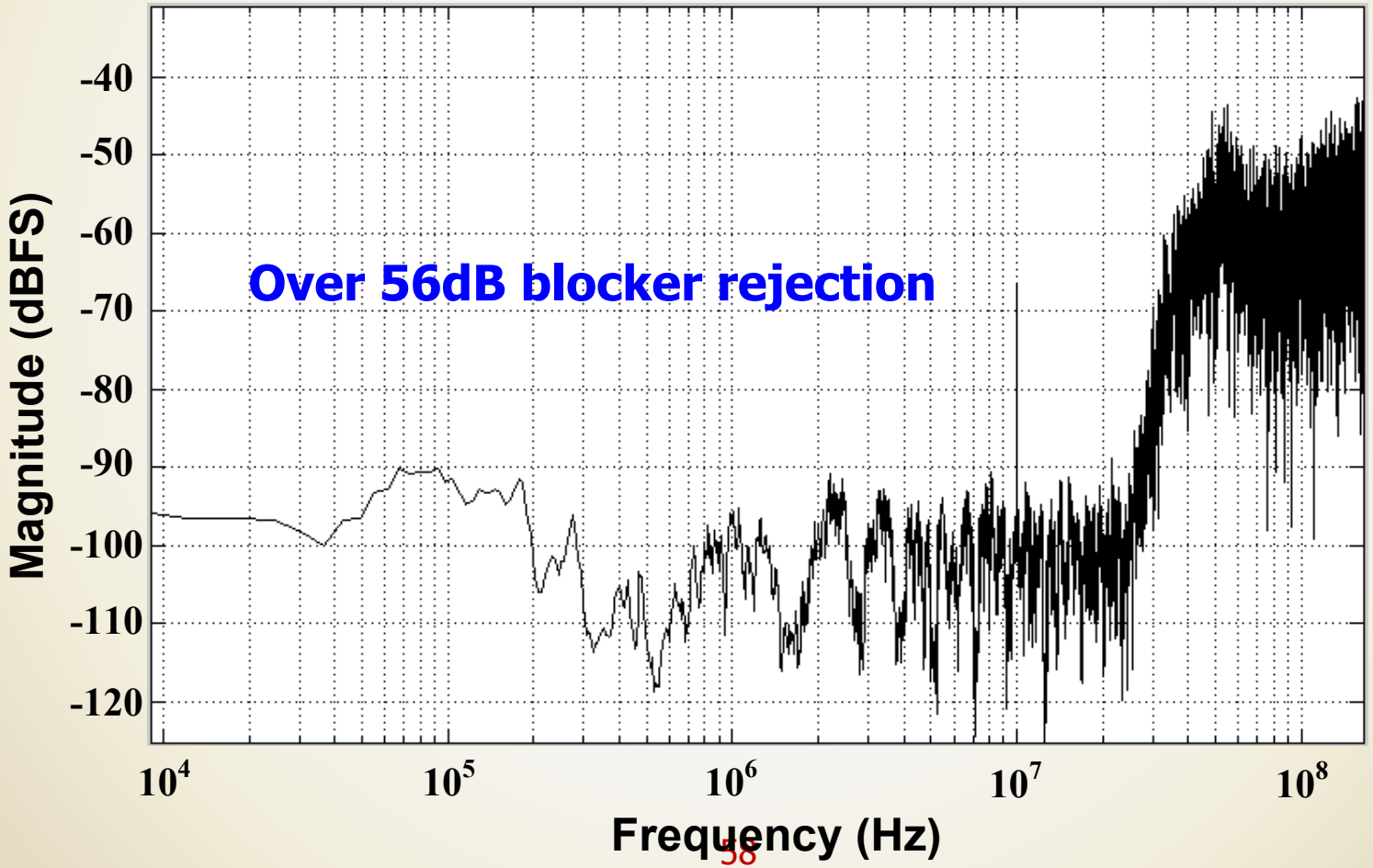


Overall Performance

Technology	Jazz 0.18µm CMOS
Power Supply	1.8V
Clock Frequency	400MHz
Bandwidth	25MHz
Peak SNR / SNDR* @ 25MHz Bandwidth	68.5dB / 67.7dB
SFDR	78dB
IM3 (-5dBFS per tone)	< -72dB
Dynamic Range	69dB
Power Consumption	48mW
Area without pads &ESD protection	2.6mm^2

Aliasing Test: -10dBFS tone at 390MHz

- Two tones with 2MHz apart at 10 MHz offset from Clock frequency and -10dBFS overall power



Comparison with Reported Works

A 25MHz Bandwidth 5th-Order Continuous-Time Lowpass Sigma-Delta Modulator With 67.7dB SNDR Using Time-Domain Quantization and Feedback, C.Y. Lu, et.al., *Sept 2010, IEEE J. Solid-State Circuits*.

Reference	Technology	F_s	BW	Filter Order	Peak SNDR	Power	FoM (fJ/bit)
JSSC 2008	130nm CMOS	950MHz	10MHz	2	72dB	40mW*	500
ISSCC-2008	180nm CMOS	640MHz	10MHz	5	82dB	100mW†	487
ISSCC-2009	65nm CMOS	250MHz	20MHz	3	60dB	10.5mW†	319
ISSCC-2007	90nm CMOS	340MHz	20MHz	4	69dB	56mW#	608
ISSCC-2008	90nm CMOS	420MHz	20MHz	4	70dB	28mW†	271Δ
JSSC 2006	130nm CMOS	640MHz	20MHz	3	74dB	20mW†	122
This work	**180nm CMOS**	**400MHz**	**25MHz**	**5**	**67.7dB**	**44mW†**	**444†**

*** Includes clock generation circuitry.**
† For modulator circuitry only.
 # Includes digital calibration of RC spread & noise cancellation filter.
Δ Discrete-time modulator (would require anti-aliasing filter for comparable blocker rejection).

Conclusions

- A 5^{th}-order LP CT ΣΔ modulator with time-domain 3-bit quantizer and DAC was designed
- The jitter effect and device mismatch issue are analyzed and considered in the design
- By employing the proposed time-domain PWM digital signal, the timing **mismatch issue is minimized**
- Better jitter tolerance if jitter is correlated in all clock phases
- Measured **67.7dB peak SNDR** @ 25MHz BW and **< -72dB IM3**.
- Over 55dB blocker rejection