Fundamentals of Continuous-Time ΣΔ Modulators

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Outline

- Fundamentals of Sigma-Delta Modulators
  - Noise and Signal Transfer Function
  - Error Function
  - Blockers tolerance
- System Limitations
  - Linear Range
  - Stability
  - Clock Jitter
- Building blocks
  - Filter issues
  - Quantizer
  - DAC issues
  - Clock Generation
- Conclusions

State of the art

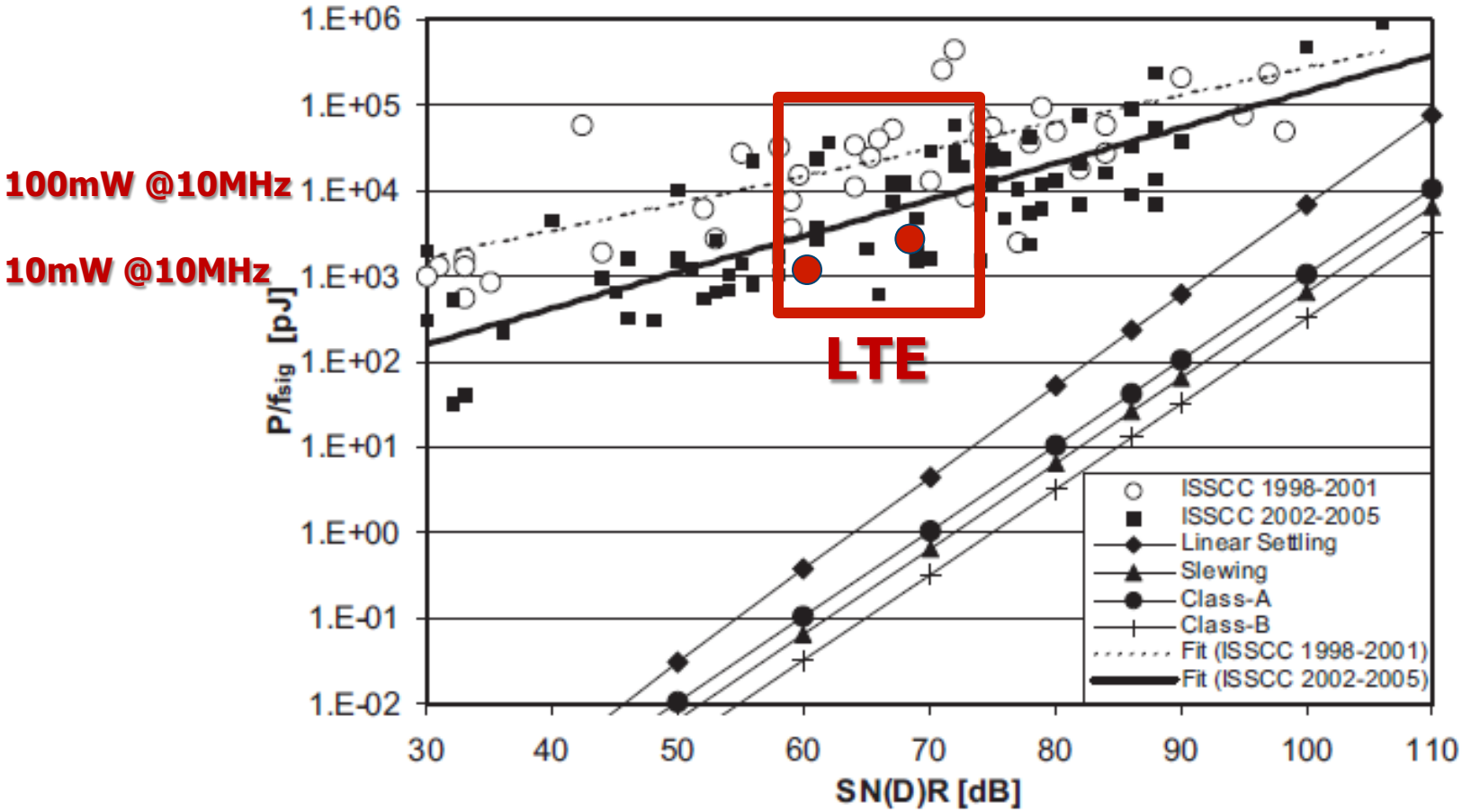


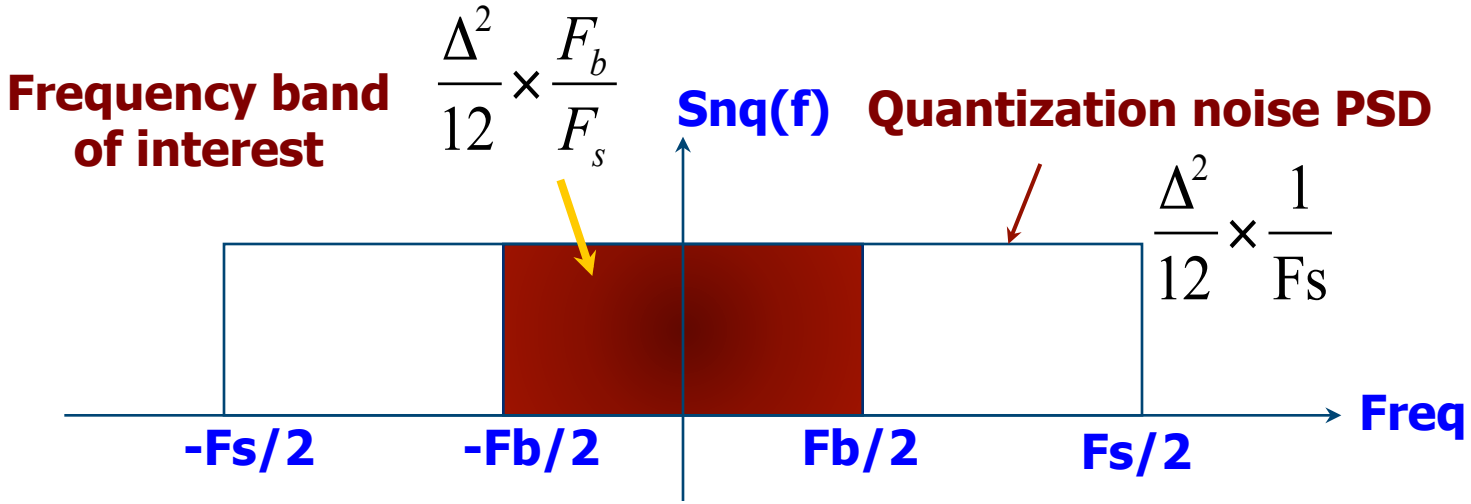
Fig. 2. Experimental ADC data and fundamental asymptotes for analog circuits containing a single amplifier and capacitor.

Nyquist-Rate and Oversampled A/D Conversion

- According to the ratio of sample frequency and Nyquist sample rate, A/D converters can be classified as,
  - Nyquist-rate A/D converter
  - Oversampled A/D converter
- For a Nyquist-rate A/D converter, the sample frequency is at, or slightly higher than, Nyquist sample rate of the input signal.
- For an oversampled A/D converter, the sample frequency (F_S) is much higher than the Nyquist sample rate ($F_{nyquist}$). The ratio of $M=Fs/F_{nyquist}$ is the oversample ratio (OSR).

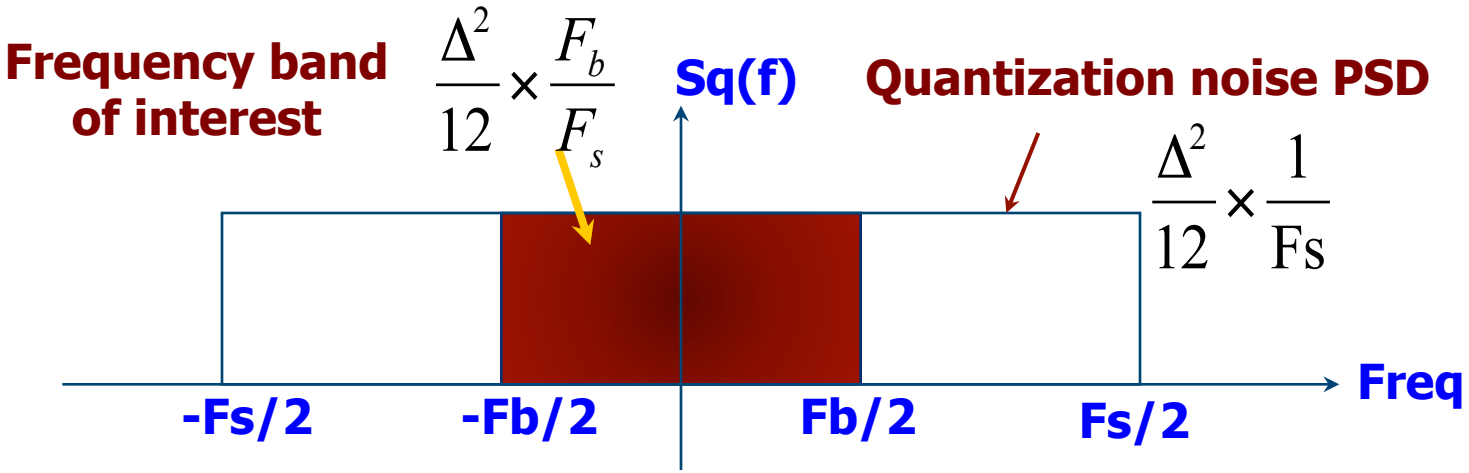
Nyquist-Rate and Oversampled A/D Conversion

- One direct benefit of oversampled ADC is that the quantization noise is M (M is the oversample ratio) times less than its Nyquist counterpart.
- Every time we double the sample frequency, the effective resolution increases with 3 dB (0.5 bit).



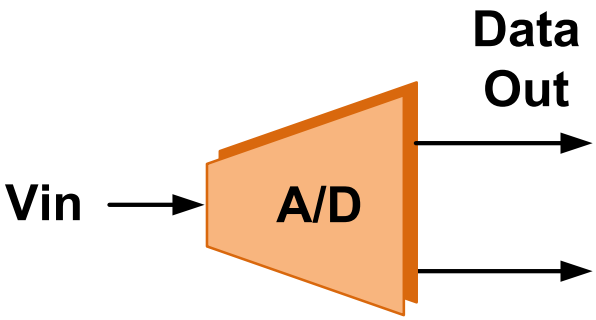
The quantization noise outside of the frequency of interest should be filtered out by post digital filtering.

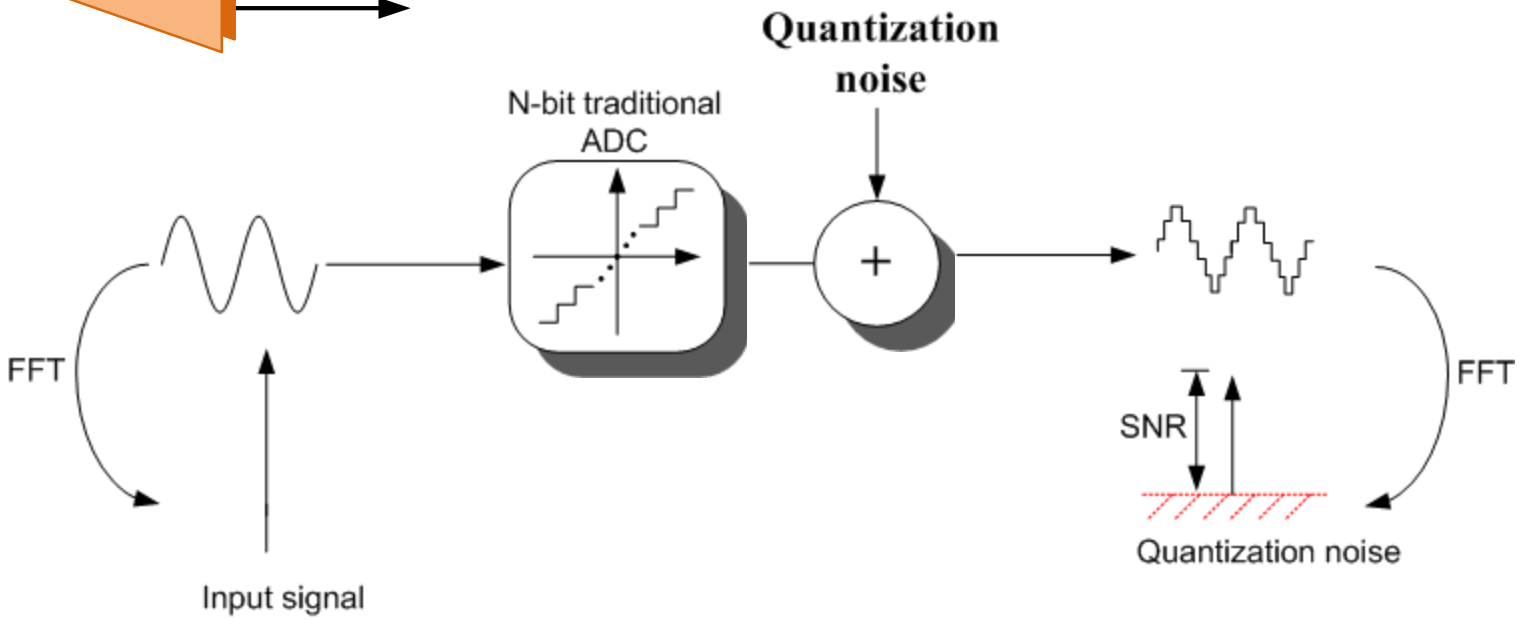
Nyquist-Rate and Oversampled A/D Conversion



- Reducing signal bandwidth decrease the integrated in-band noise level by 3 dB
- Increasing the oversampling ratio Fs/2Fb by factor of 4 increases the resolution by 6dB or equivalently 1 dB.
- **Changing the sampling frequency by a factor of 100 increases the SQNR by only 20 dB.**
  - **Very expensive: too much effort for additional 3.3 bits**
  - **Can we do better than this?**

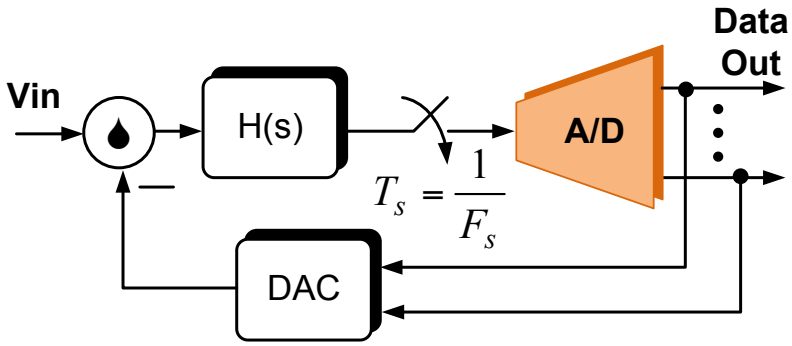
Conventional (Nyquist) ADC

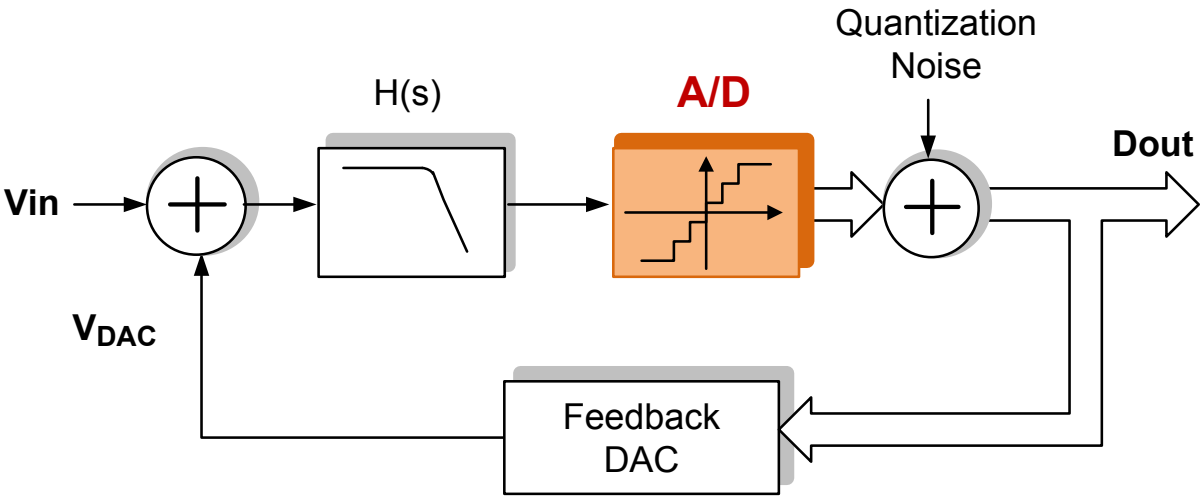


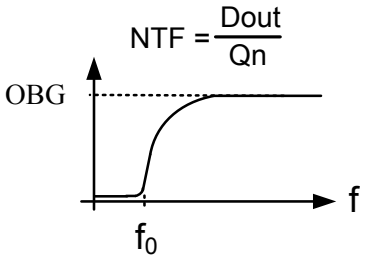


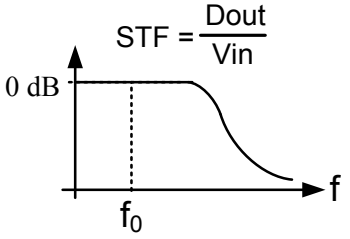
SQNR=6.02*n+1.76

Basic concept in ΣΔ Modulators







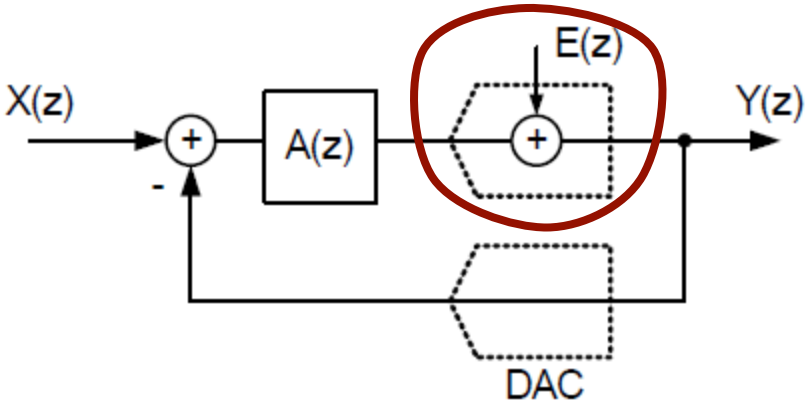


$$STF = \frac{H(s)}{1 + H(s)}$$

$$NTF = \frac{1}{1 + H(s)}$$

Identify the noise and signal and use Feedback to shape the noise!

Original ADC + noise



$$Y(z) = E(z) + A(z)X(z) - A(z)Y(z)$$

$$= E(z)\frac{1}{1+A(z)} + X(z)\frac{A(z)}{1+A(z)}$$

$$= E(z)\underbrace{H_E(z)}_{\substack{\text{Noise Transfer Function}}} + X(z)\underbrace{H_X(z)}_{\substack{\text{Signal Transfer Function}}}$$

$$Y(z) = E(z)\underbrace{\frac{1}{1+A(z)}}_{\substack{\text{Noise Transfer Function}}} + X(z)\underbrace{\frac{A(z)}{1+A(z)}}_{\substack{\text{Signal Transfer Function}}}$$

Objective

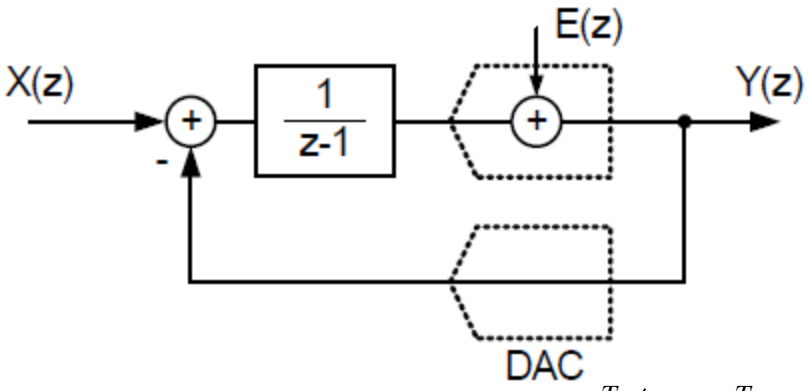
- Want to make STF unity in the signal frequency band
- Want to make NTF "small" in the signal frequency band

If the frequency band of interest is around DC (0…f_B) we achieve this by making |A(z)| >>1 at low frequencies

- Means that NTF is <<1
- Mans that STF ≅ 1

The assumption is that the DAC can do much better than the original ADC; is this realistic? Free lunch?

Oversampled A/D Conversion (Double check Mason's rule)



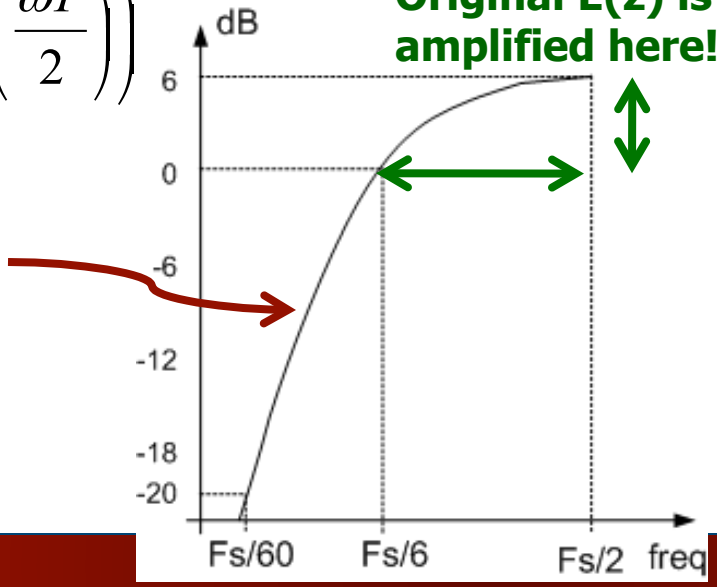
$$Y(z) = E(z)\frac{1}{1+\frac{1}{z-1}} + X(z)\frac{\frac{1}{z-1}}{1+\frac{1}{z-1}}$$
$$= E(z)\left(1-z^{-1}\right) + X(z)z^{-1}$$

Check the input-output trajectories
Original E(z) is shaped by NTF

$$H_e(z) = 1 - Z^{-1} = 1 - e^{-j\omega T} = e^{-j\frac{\omega T}{2}}\left(e^{+j\frac{\omega T}{2}} - e^{-j\frac{\omega T}{2}}\right)$$

$$H_e(z) = e^{-j\frac{\omega T}{2}}\left(2j\sin\left(\frac{\omega T}{2}\right)\right)$$

$$\left|H_e(z)\right| = 2\sin\left(\frac{\omega T}{2}\right)$$



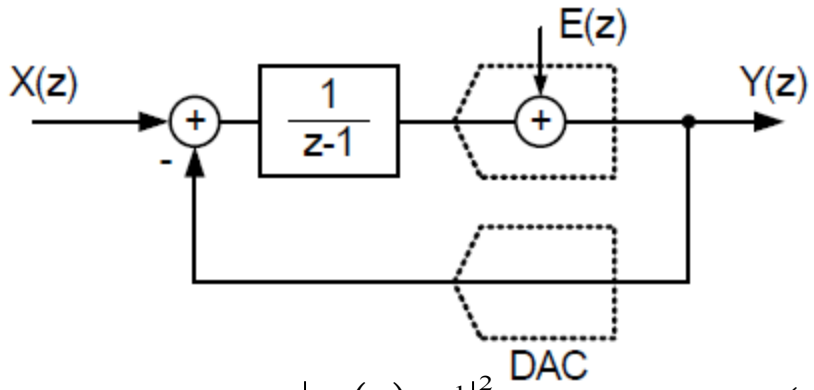
Original E(z) is amplified here!

Spot SQNR

$$SQNR = \left|\frac{X(z)Z^{-1}}{E(z)H_e(z)}\right|^2$$

$$SQNR = \left|\frac{X(z)}{E(z)}\right|^2 * \left|\frac{1}{2\sin\left(\frac{\omega T}{2}\right)}\right|^2$$

Oversampled A/D Conversion



$$SQNR \cong 1.5 * \left(2^N - 1\right)^2 * \left(3 * \frac{OSR^3}{\pi^2}\right)$$

$$SQNR \cong 1.76 + 6.02 * N - 5.2 + 30 * log(OSR)\ \ dB$$

$$SQNR = \frac{\left|X(z)Z^{-1}\right|^2}{\left|\int_0^{f_b} (E(z)H_e(z))^2\, df\right|} = \frac{|X(z)|^2}{\left|E(z)\int_0^{f_b} (H_e(z))^2\, df\right|}$$

$$SQNR = \left|\frac{X(z)}{E(z)}\right|^2 * \left|\frac{1}{\int_0^{f_b} \left(2\sin\left(\frac{\omega T}{2}\right)\right)^2 df}\right|$$

If fb << fs, then

$$SQNR \cong \frac{\frac{1}{2}\left|\left(\frac{2^N - 1}{2}\right)\left(\Delta V_q\right)\right|^2}{\frac{\Delta V_q^{\,2}}{12} * \frac{2}{f_S}} * \left|\frac{6 * \left(\frac{f_S}{2f_b}\right)^3}{\pi^2 * f_S}\right|$$

$$SQNR \cong 1.5 * \left(2^N - 1\right)^2 * \left(3 * \frac{OSR^3}{\pi^2}\right)$$

Signal to Quantization Noise Ratio (SQNR)

- N=number of bits
- OSR=fs/2fb
- SQNR improves by 30dB when OSR increases by 10
- Or 9dB SQNR improvement when doubling OSR

Oversampled A/D Conversion

Typical spectrum for a 2nd order system

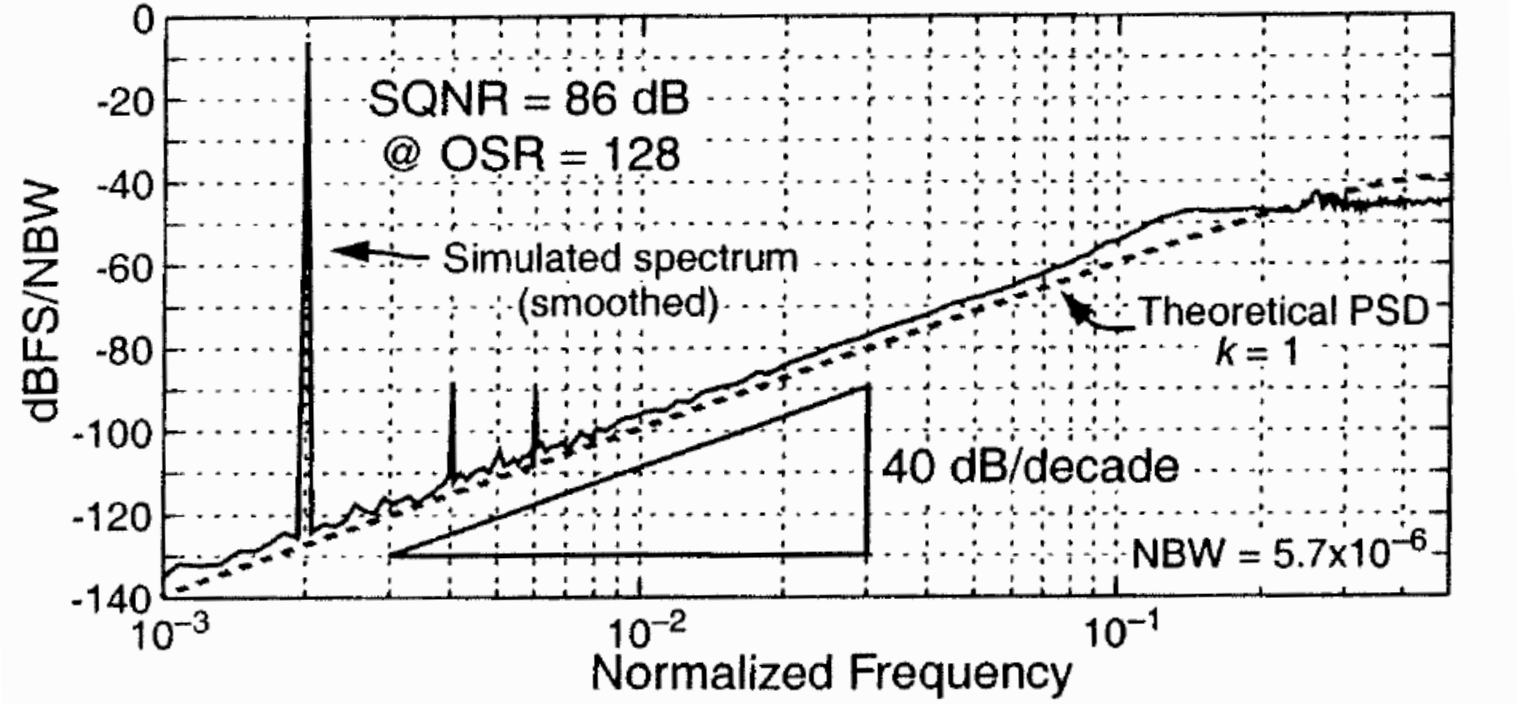
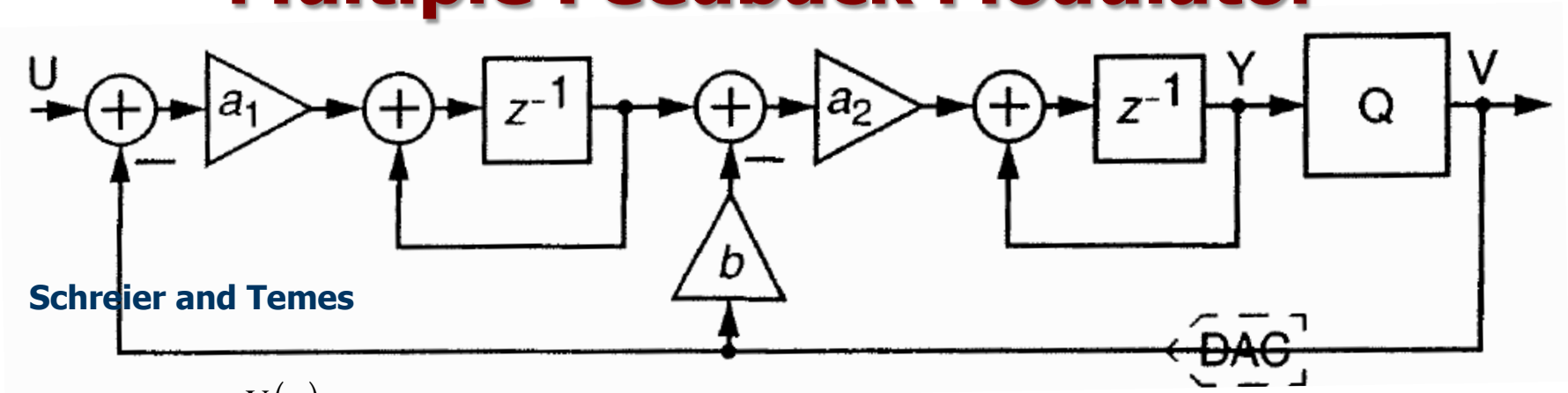


Figure 3.6: Output spectrum of MOD2 with a –6-dBFS sine-wave input.

Understanding Delta-Sigma Data Converters, Schreier and Temes

Linearized Model: 2nd order Multiple Feedback Modulator

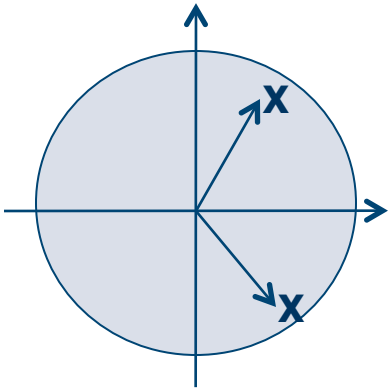


Schreier and Temes

STF

$$\frac{V(z)}{U(z)} = \frac{a_1 a_2}{(z-1)^2 + (z-1)ba_2 + a_1 a_2} = \frac{a_1 a_2}{z^2 - (2 - ba_2)z + (1 + a_1 a_2 - ba_2)}$$

$$\frac{V(z)}{U(z)} = \frac{a_1 a_2}{z^2 - (2r\cos(\omega_0 T))z + (1 - r^2)} = \frac{a_1 a_2}{(z - re^{j\omega_0 T})(z - re^{-j\omega_0 T})}$$



NTF

$$NTF = \frac{V(z)}{E(z)} = \frac{(z-1)^2}{(z-1)^2 + (z-1)ba_2 z + a_1 a_2}$$

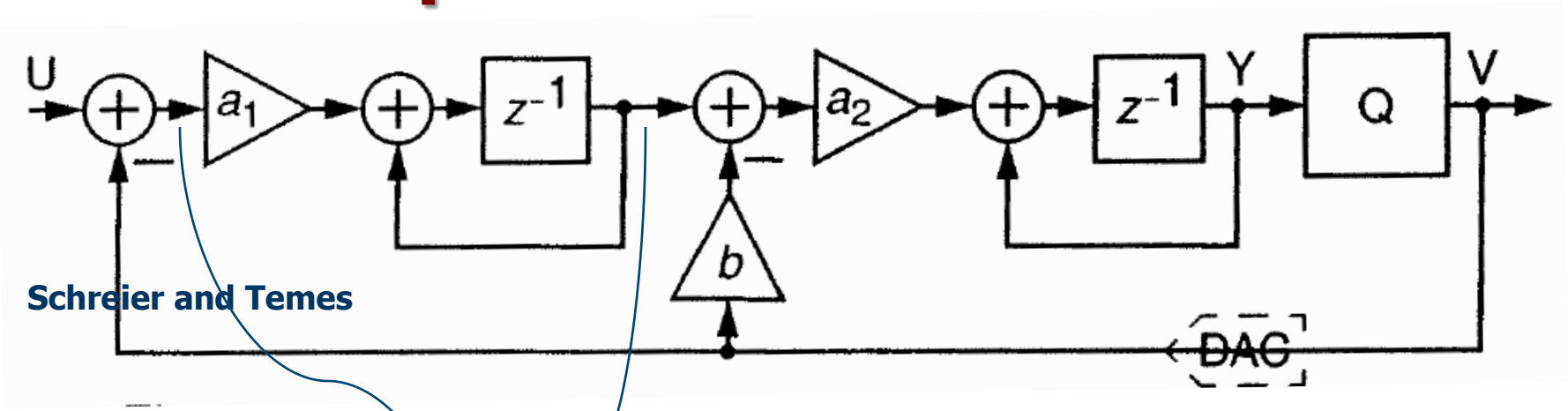
Under the conditions $a_1a_2=1$ and $a_2b=2$, then

$$V(z) = z^{-2}U(z) + (1 - z^{-1})^2 E(z)$$

$$U(z) - V(z) = (1 - z^{-2})U(z) - (1 - z^{-1})^2 E(z)$$

This is the real signal at the filter's input: THINK ABOUT IT!

Linearized Model: 2nd order Multiple Feedback Modulator



STF and NTF are definitely not enough to design a robust system!

$$V(z) = z^{-2}U(z) + \left(1 - z^{-1}\right)^2 E(z)$$

At the input of the first amplifier we have:

$$U(z) - V(z) = \left\{1 - z^{-2}\right\}U(z) - \left(1 - z^{-1}\right)^2 E(z)$$

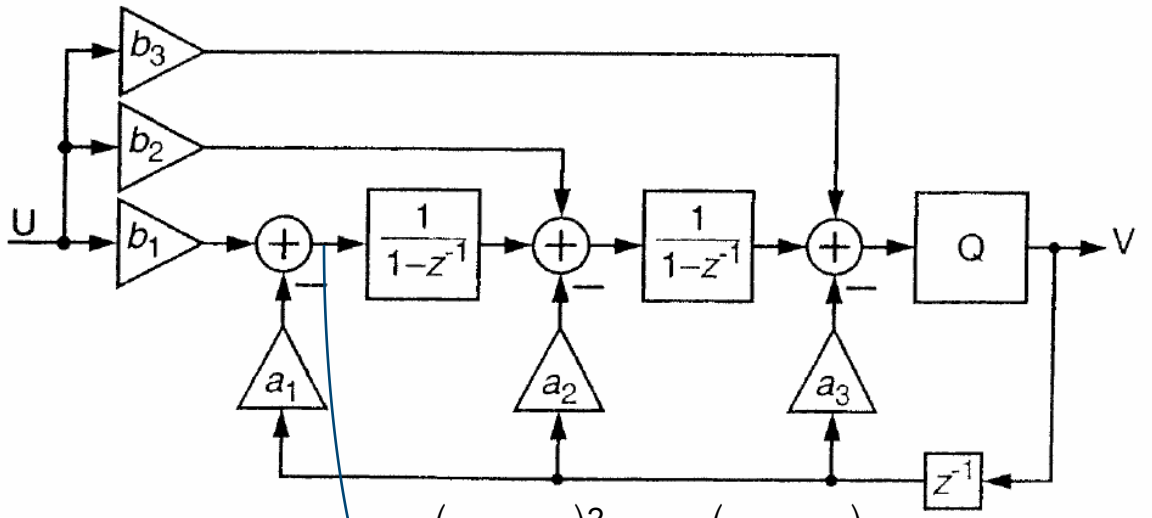
Small for inband signals but what about the blockers?

At the output of the first integrator we have (saturation?)

$$\frac{\left\{V(z) - U(z)\right\}z^{-1}a_1}{1 - z^{-1}} = \left\{1 + z^{-1}\right\}z^{-1}a_1 U(z) - \left(1 - z^{-1}\right)z^{-1}a_1 E(z)$$

If a1>0.5, hence the in-band output of the 1st integrator is > than the input !

2nd order Multiple Feedback Modulator



Schreier and Temes

$$STF = \frac{V(z)}{U(z)} = \frac{b_3\left(1-Z^{-1}\right)^2 + b_2\left(1-Z^{-1}\right) + b_1}{\left(1-Z^{-1}\right)^2 + a_3 Z^{-1}\left(1-Z^{-1}\right)^2 + a_2 Z^{-1}\left(1-Z^{-1}\right) + a_1 Z^{-1}}$$

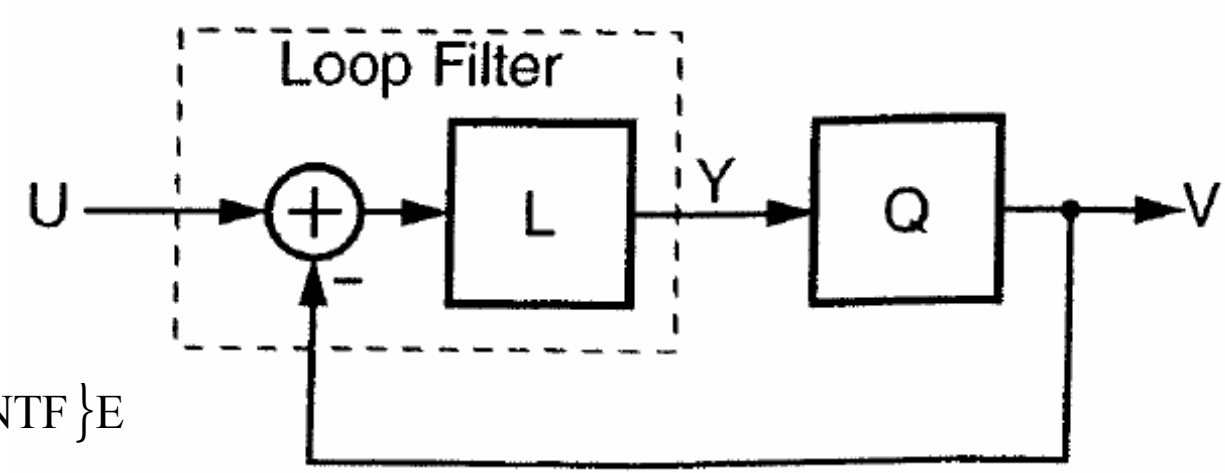
$$STF = \frac{V(z)}{U(z)} = b_3\left(1-Z^{-1}\right)^2 + b_2\left(1-Z^{-1}\right) + b_1$$

$$NTF = \frac{V(z)}{E(z)} = \left(1-Z^{-1}\right)^2$$

a1 = a2=1
a3 = 0

Amplifier input $Ve(z) = \left\{-b_2\left(1-Z^{-1}\right) - b_3\left(1-Z^{-1}\right)^2\right\}U(z) - \left(1-Z^{-1}\right)^2 E(z)$

Generic model for the Feed-forward Modulator



$$V = \{STF\}U + \{NTF\}E$$

$$V = \left\{\frac{L}{1+L}\right\}U + \left\{\frac{1}{1+L}\right\}E$$

$$V_e = U - V = \left\{\frac{1}{1+L}\right\}U - \left\{\frac{1}{1+L}\right\}E = \frac{U-E}{1+L}$$

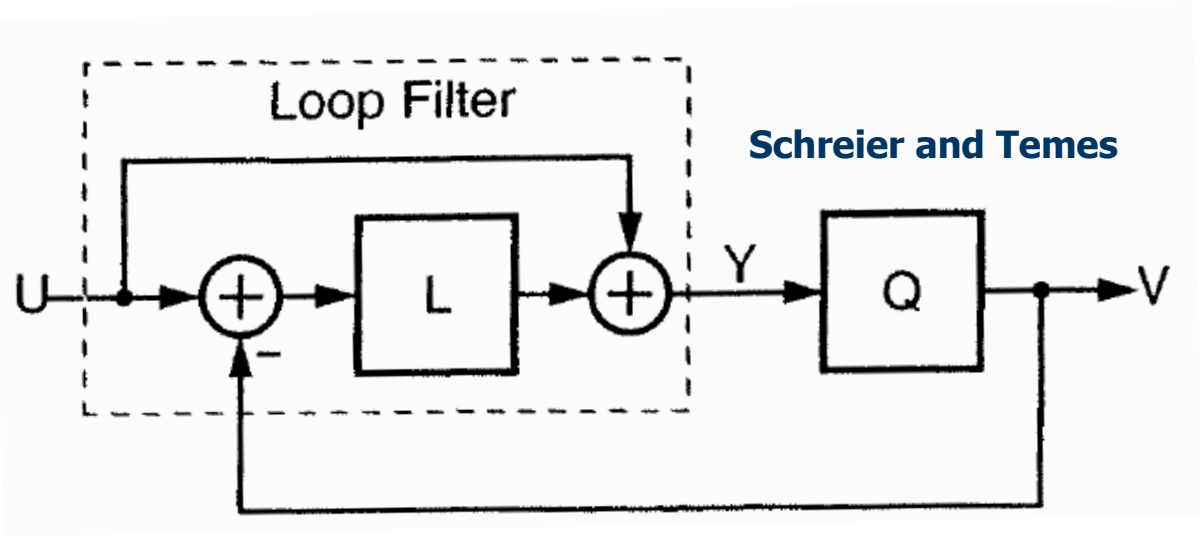
$$Y = V_e L = \left\{\frac{L}{1+L}\right\}\{U-E\}$$

Be sure that |1+L|>0 for all frequencies; e.g. phase at the unity frequency

Very good for inband signals, but some issues for out of band signals specially if NTF>1 at high frequencies

Little chance of overloading at the quantizer input

Generic model for the Feed-forward Modulator



$$V = U + \left\{\frac{1}{1+L}\right\}E$$

Very good STF but it is not very relevant in practice

$$V_e = U - V = -\left\{\frac{1}{1+L}\right\}E$$

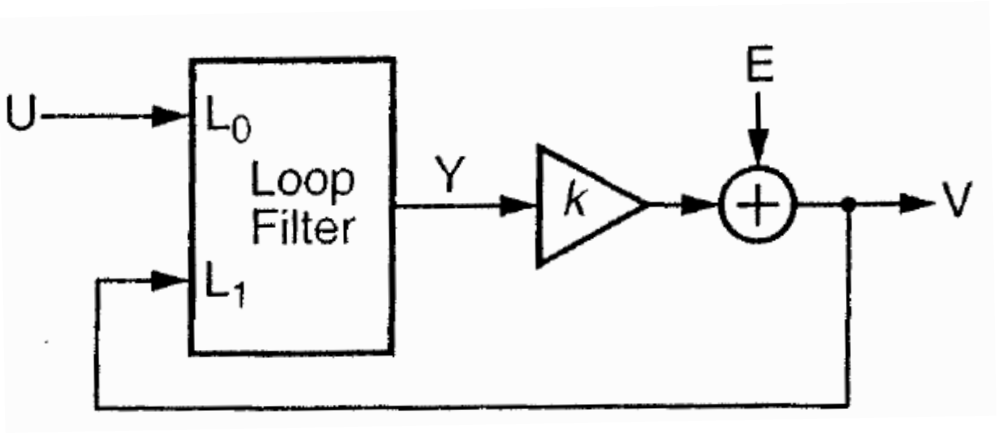
Excellent for both in-band and out-of-band blockers; minor issues if NTF>1 at high frequencies

$$Y = U + V_e L = U - \left\{\frac{L}{1+L}\right\}E$$

Little chance of overloading at the quantizer input

But.. What about aliasing of HF signals? After Y we have the quantizer (S/H)!

Generic model for a Hybrid Modulator



$$V = \left\{\frac{L_0 k}{1+L_1 k}\right\}U + \left\{\frac{1}{1+L_1 k}\right\}E$$

$$Error\ Signal = V - E$$

$$= \left\{\frac{L_0 k}{1+L_1 k}\right\}U - \left\{\frac{L_1 k}{1+L_1 k}\right\}E$$

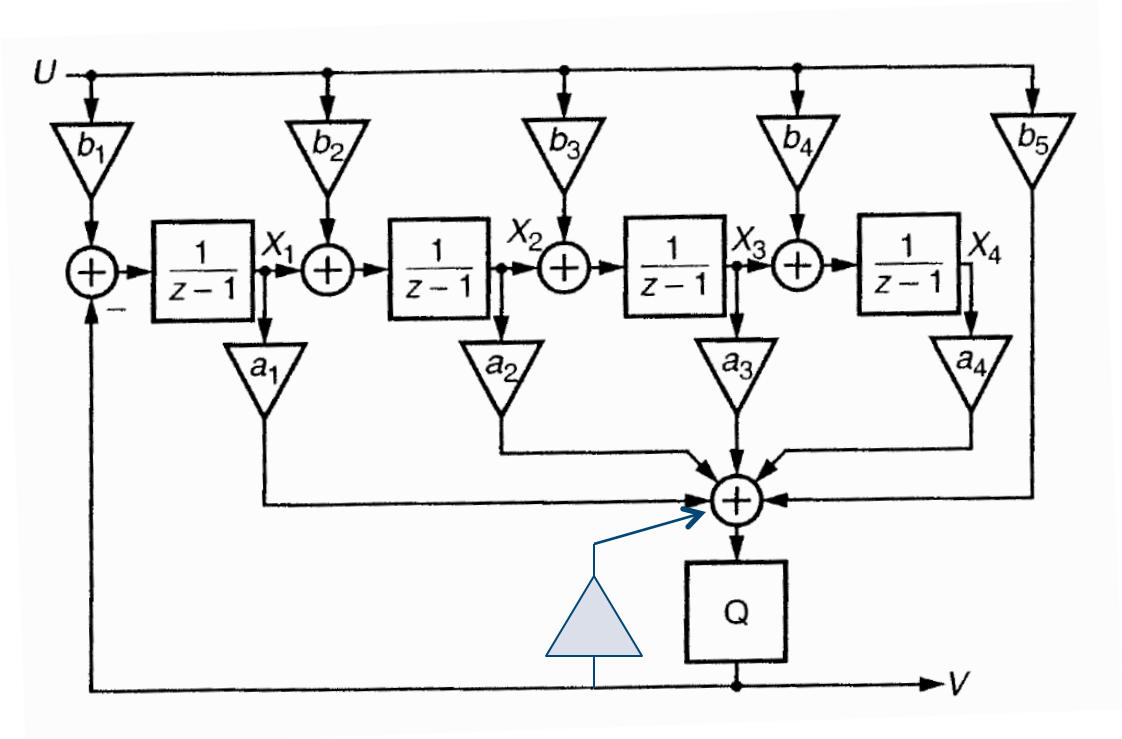
(HIGH) Risk of excessive signal at the internal nodes

You have to analyze case by case; hard to make general conclusions

Once you define Lo and L1 and the topology you must analyze how L1*V and Lo*U affect the signal swing at every internal node

Inband SNR is a strong function of Lok

High-order Feedforward Modulator based on Integrators

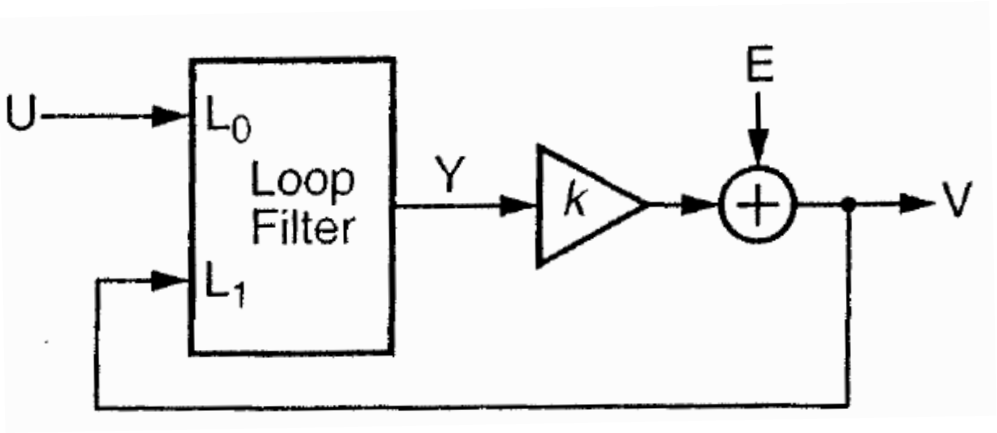


This architecture is very popular in CT modulators

No problem with non-touching loops nor with trajectories non-touching loops

A major issue is the frequency response of the adder

Generic model for a Hybrid Modulator



$$V = \left\{\frac{L_0 k}{1+L_1 k}\right\} U + \left\{\frac{1}{1+L_1 k}\right\} E$$

$$\text{ErrorSignal} = V - E = \left\{\frac{L_0 k}{1+L_1 k}\right\} U - \left\{\frac{L_1 k}{1+L_1 k}\right\} E$$

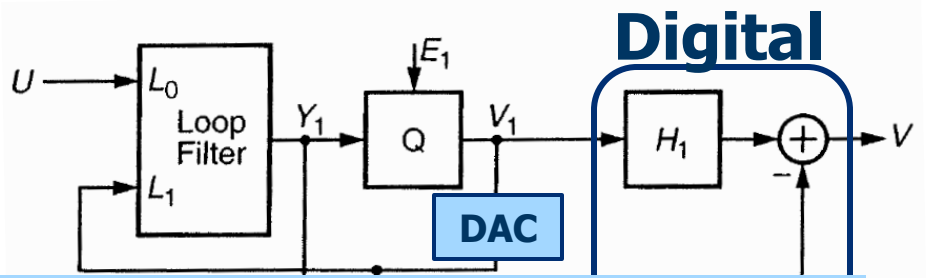
(HIGH) Risk of excessive signal at the internal nodes

You have to analyze case by case; hard to make general conclusions

Once you define Lo and L1 and the topology, you must analyze how L1*V and Lo*U affects the signal swing in every node

Inband SNR is a strong function of Lok

Fundamentals on MASH architectures



Quite relevant topology: Notice that the auxiliary ADC processes the quantization error E1 What about E2?

Any other option?

$$V(z) = H_1(z)V_1 - H_2(z)V_2$$

$$V_1(z) = STF_1(z)U + NTF_1(z)E_1$$

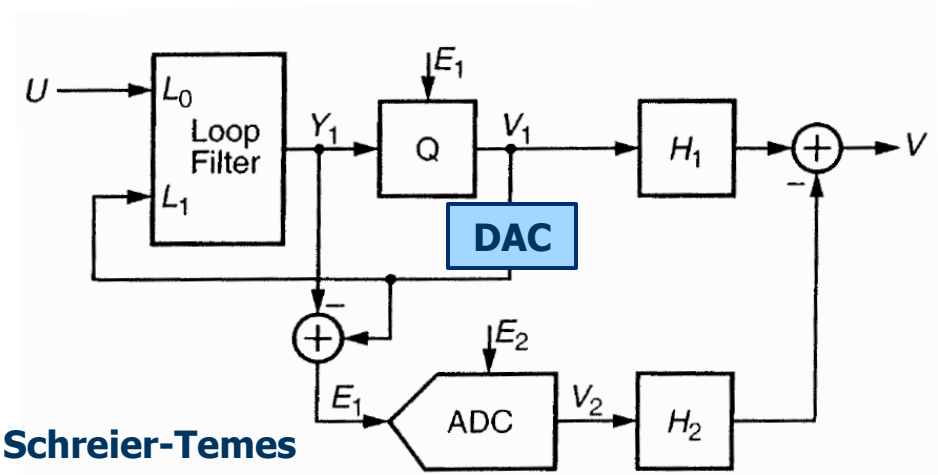
$$V_2(z) = STF_2(z)E_1 + NTF_2(z)E_2$$

Then

$$V(z) = H_1\{STF_1 * U + NTF_1 * E_1\} - H_2\{STF_2 * E_1 + NTF_2 * E_2\}$$

$$V(z) = \{H_1 * STF_1\}U + \{H_1 * NTF_1 - H_2 * STF_2\}E_1 - \{H_2 * NTF_2\}E_2$$

Fundamentals on MASH architectures



Schreier-Temes

Figure 4.22: The L-0 cascade (Leslie-Singh) structure.

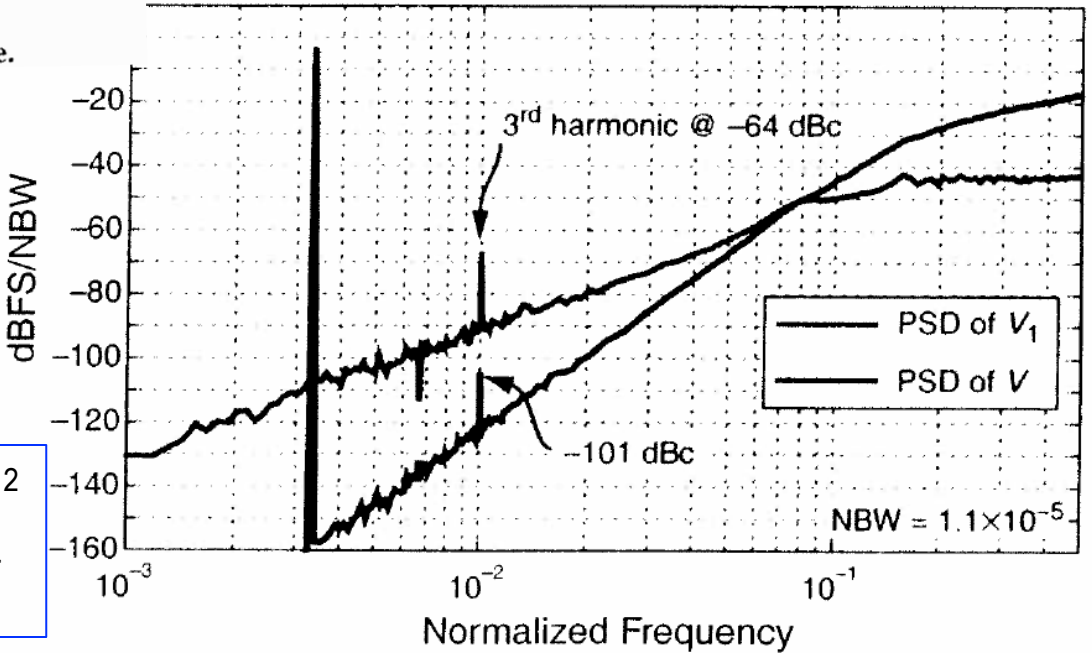
Analog Intensive MASH topology

$$If \quad H_1 * NTF_1 - H_2 * STF_2 = 0$$

$$Then$$

$$V(z) = \{H_1 * STF_1\}U - \{H_2 * NTF_2\}E_2$$

$$SQNR = \left\{\frac{E_1}{E_2}\right\}^2 \left\{\frac{STF_2}{NTF_2}\right\}^2 \left\{\frac{STF_1 * U}{NTF_1 * E_1}\right\}^2$$



Sigma-Delta Modulators Design Issues

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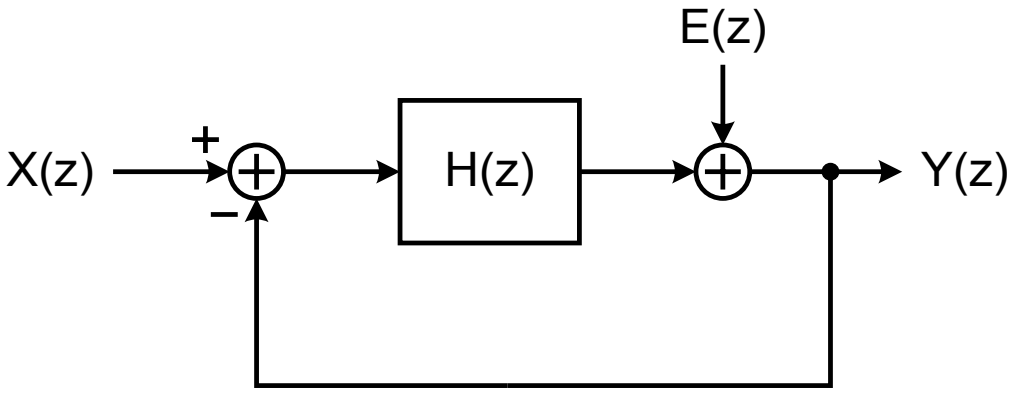
Part 1.2

Linearized Discrete-Time Model



$$H(z)=\frac{z^{-1}}{1-z^{-1}}$$

$$Y(z)=H(z)\cdot[X(z)-Y(z)]+E(z)$$

$$\Rightarrow Y(z)=\frac{H(z)}{1+H(z)}\cdot X(z)+\frac{1}{1+H(z)}\cdot E(z)$$

$$\Rightarrow Y(z)=z^{-1}\cdot X(z)+\left(1-z^{-1}\right)\cdot E(z)$$

Signal Transfer Function:

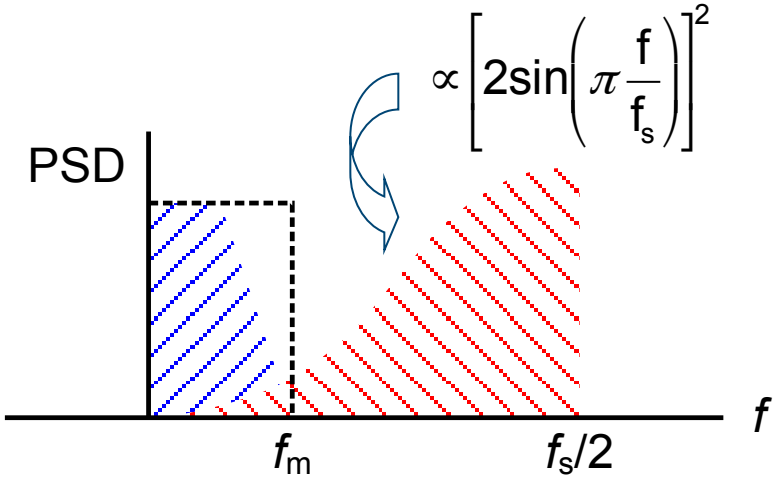
$$STF=\frac{Y(z)}{X(z)}=z^{-1}\leftarrow \text{Delay}$$

Noise Transfer Function:

$$NTF=\frac{Y(z)}{E(z)}=1-z^{-1}\leftarrow \text{HP}$$

Caveat: E(z) may be correlated with X(z) – not "white".

1st-Order Noise Shaping



$$N_e^2 = \int_0^{f_m} \frac{\Delta^2}{12} \cdot \frac{1}{f_s/2} \cdot |NTF|^2 \, df$$

$$= \frac{\Delta^2}{12} \cdot \frac{1}{f_s/2} \cdot \int_0^{f_m} \left[2\sin\left(\pi \frac{f}{f_s}\right)\right]^2 df$$

$$\approx \frac{\Delta^2}{12} \cdot \frac{1}{f_s/2} \cdot \int_0^{f_m} \left[2\pi \frac{f}{f_s}\right]^2 df$$

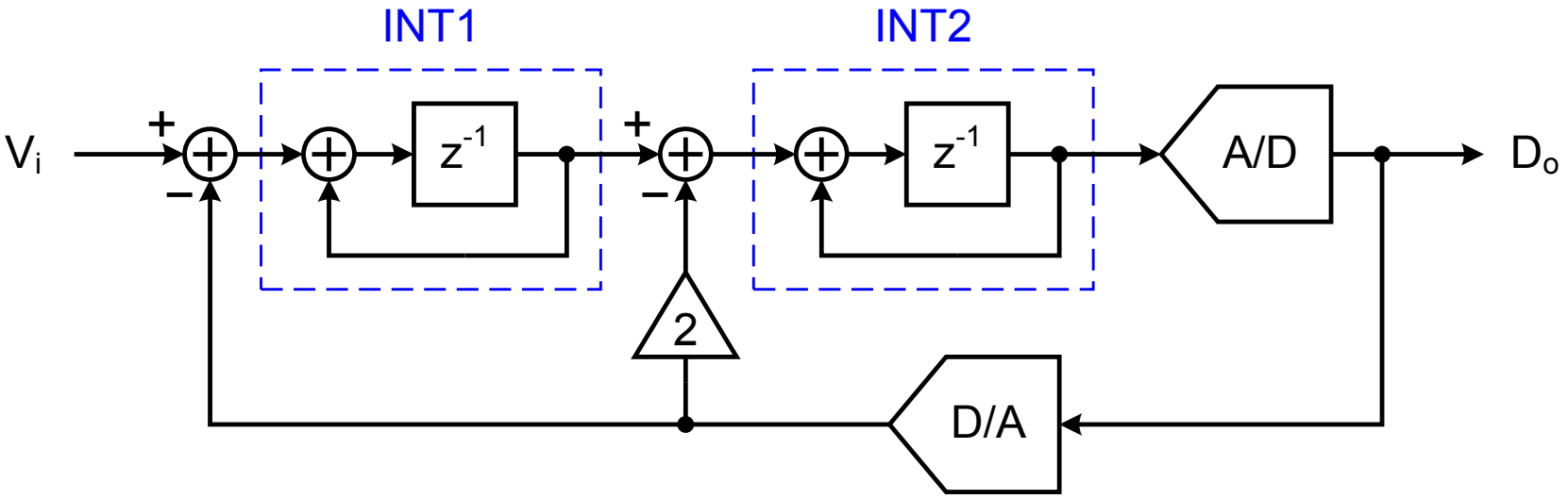
$$= \frac{\Delta^2}{12} \cdot \left(\frac{2f_m}{f_s}\right)^3 \cdot \frac{\pi^2}{3}$$

In-band quantization noise :

$$N_e^2 \approx \frac{\Delta^2}{12} \cdot \frac{\pi^2}{3OSR^3}$$

Doubling OSR increases SQNR by 9 dB (1.5 bit/oct).

2nd-Order ΣΔ Modulator



Signal Transfer Function:

$$STF = z^{-2}$$

Noise Transfer Function:

$$NTF = \left(1 - z^{-1}\right)^2$$

In-band quantization noise:

$$N_e^2 \approx \frac{\Delta^2}{12} \cdot \frac{\pi^4}{5M^5}$$

Doubling OSR (M) increases SQNR by 15 dB (2.5 bit/oct).

Generalization (Lth-Order Noise Shaping)

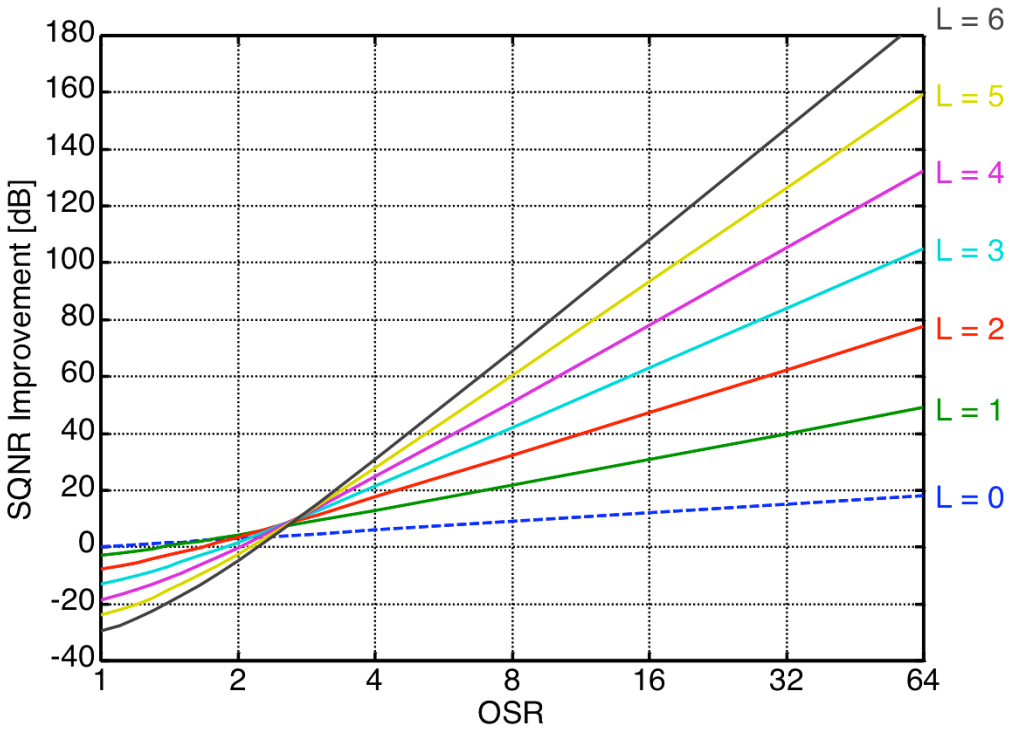
Modulator transfer function :

$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^{L} E(z)$$

In-band quantization noise :

$$N_e^2 \approx \frac{\Delta^2}{12} \cdot \frac{\pi^{2L}}{(2L+1) \cdot OSR^{2L+1}}$$

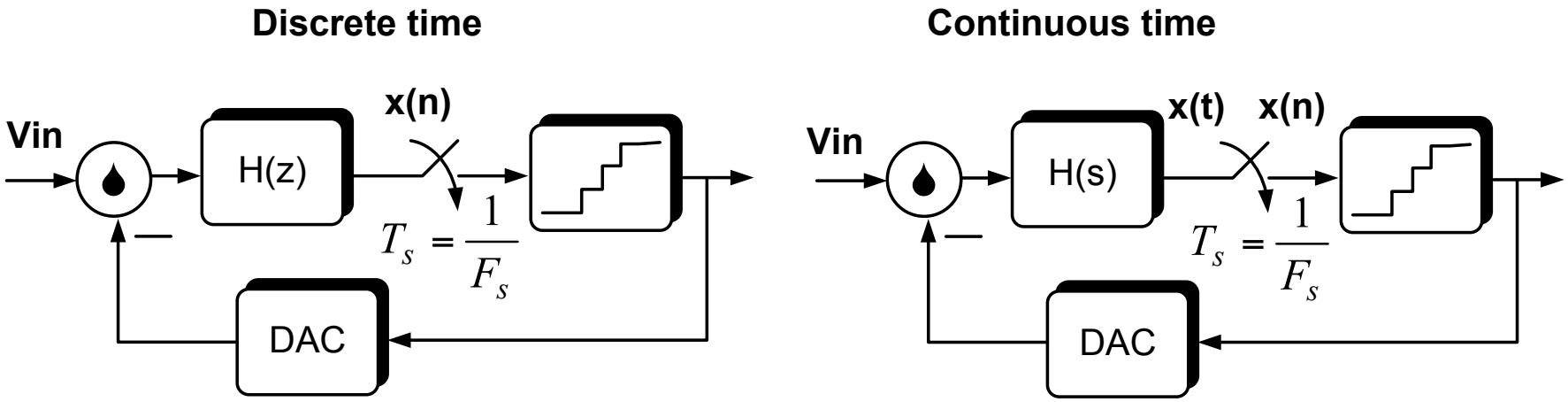
$$SQNR = \left(\frac{3}{2}\right)\left(2^{N} - 1\right)^2 \left(\frac{(2L+1) \cdot OSR^{2L+1}}{\pi^{2L}}\right)$$



- Doubling OSR (M) increases SQNR by (6L+3) dB, or (L+0.5) bit.
- Potential instability for 3rd- and higher-order single-loop ΣΔ modulators.

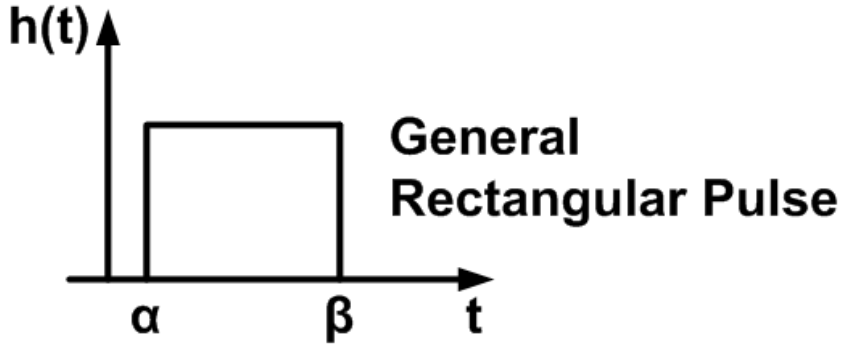
$$SQNR(dB) = 6.02N + 1.76 + (2L+1)10\log_{10} OSR - 10\log_{10}\frac{\pi^{2L}}{2L+1}$$

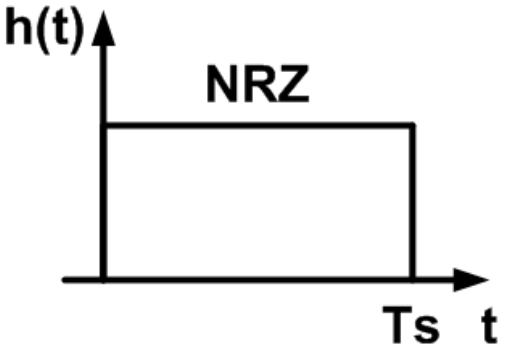
Equivalence of Continuous-Time & Discrete-Time ΣΔ

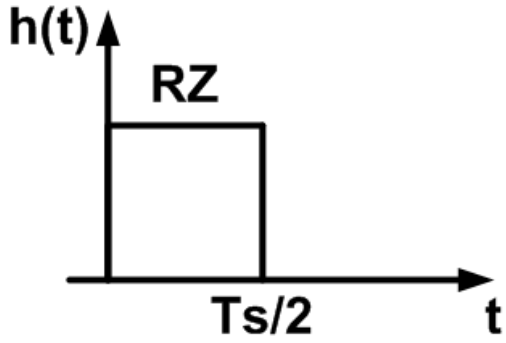


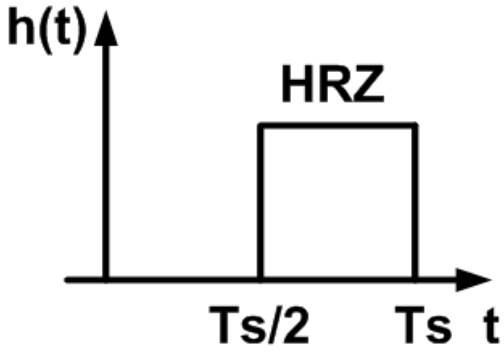
- The key feature of the ΣΔ modulator is the noise shaping (NTF)
- To achieve equivalence between a continuous-time and discrete-time implementations, **Loop Gain should have the same properties**
- How can we realize the same NTF using continuous-time and discrete-time loop filters ?
  - **The NTF is mainly determined by the transient response of the loop filter and the feedback DAC !**

Types of Feedback DAC with Rectangular





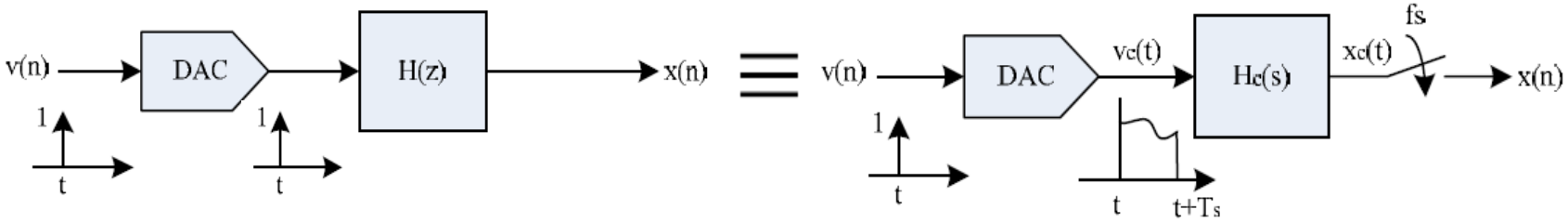




NRZ: Easy to design

RZD: More tolerant to excess loop delay

Impulse Invariant Transformation

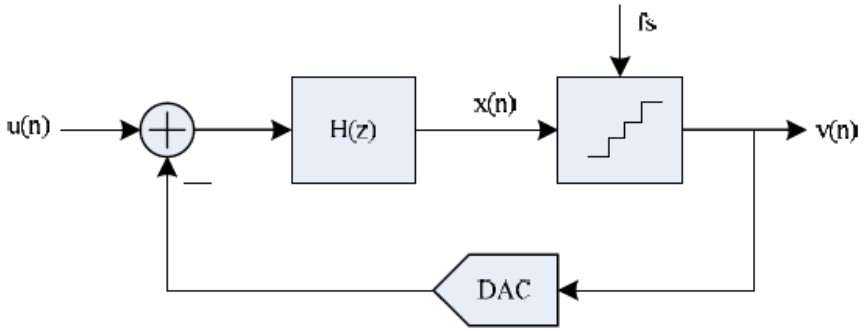


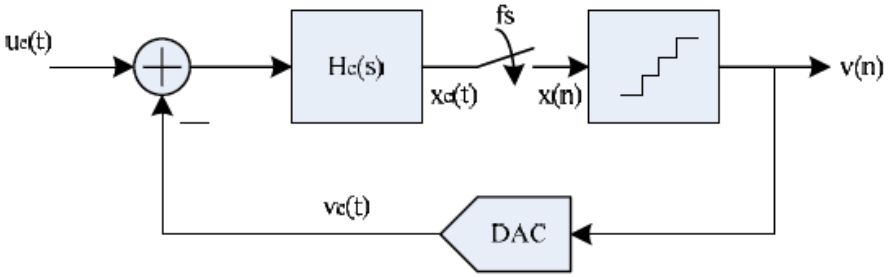
$$Z^{-1}\{H(z)\} = L^{-1}\{H_{dac}(s)H_c(s)\}\,|_{t=nT_s}$$

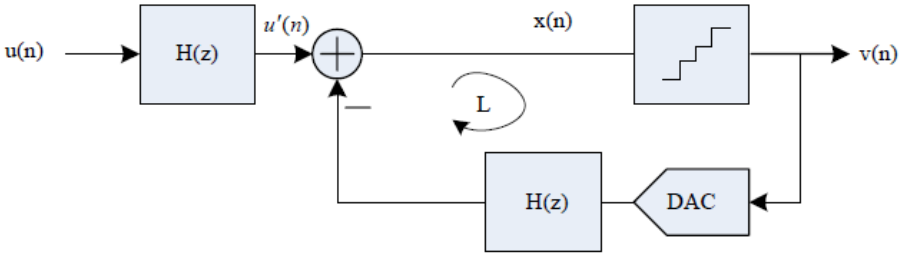
$$h(n) = [h_{dac}(t) * h_c(t)]\,|_{t=nT_s} = \int_{-\infty}^{\infty} h_{dac}(\tau)h_c(t-\tau)d\tau\,|_{t=nT_s}$$

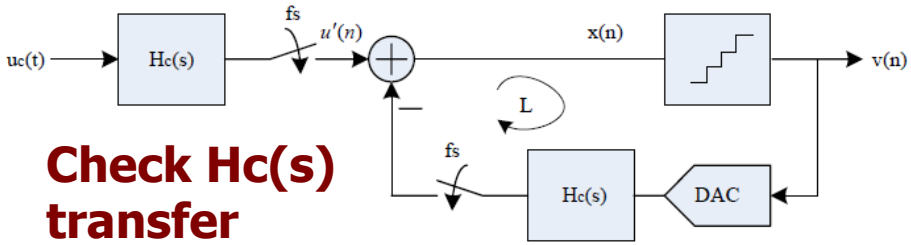
Transformations can be easily applied by decomposing the original DT (Z-domain) loop filter into partial fractions and use S-domain equivalences for the Z-domain poles to get the CT loop filter.

"Inherent Anti-aliasing" for narrow-band applications







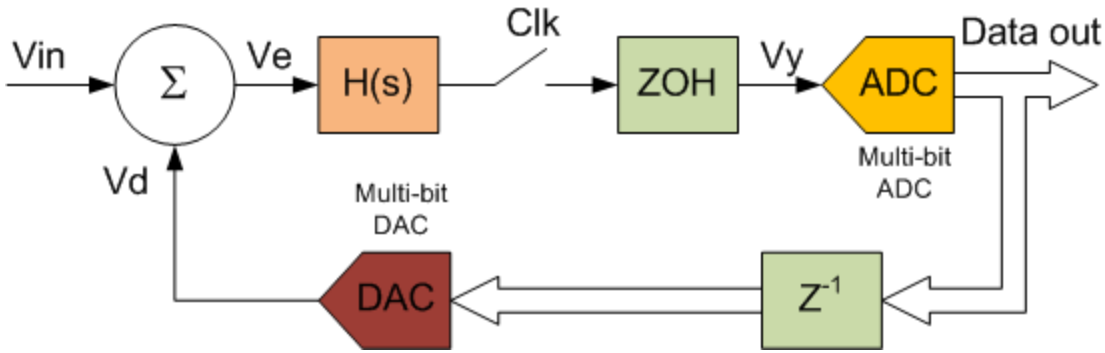


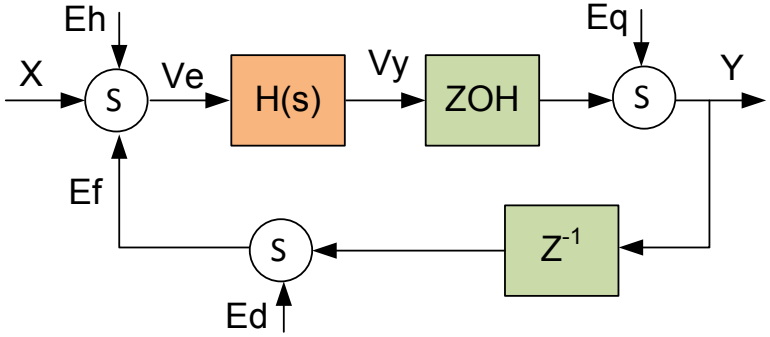
Check Hc(s) transfer function!

Hc(s) has a low-frequency gain over 40 dB, with a -3dB frequency equal to ADC bandwidth and unity gain frequency between 5-10 times higher

Oversampled A/D Conversion: Feedforward architecture

- Eq stands for the quantization noise
- Ed stands for DAC non-idealities (jitter + thermal noise)
- Filter's thermal noise is accounted in Eh





- The modulator's output becomes

$$Y = STF * (X + E_d + E_h) + NTF * E_q$$

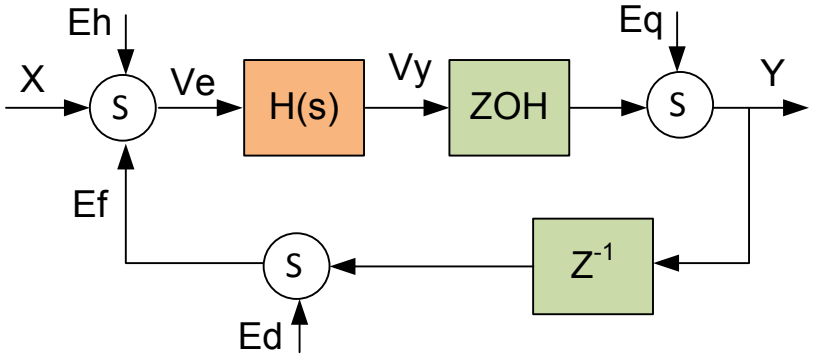
$$STF = \frac{H(s) * ZOH(s)}{1 + H(s) * ZOH(s) * Z^{-1}}$$

- The error signal (Filter's input) is

$$V_e = NTF * \{H(s)\,ZOH(X + E_d + E_h) + Z^{-1} * E_q\}$$

$$NTF = \frac{1}{1 + H(s) * ZOH(s) * Z^{-1}}$$

Oversampled A/D Conversion
Feed-forward configuration



$$STF = \frac{H(s)*ZOH(s)}{1+H(s)*ZOH(s)*Z^{-1}}$$

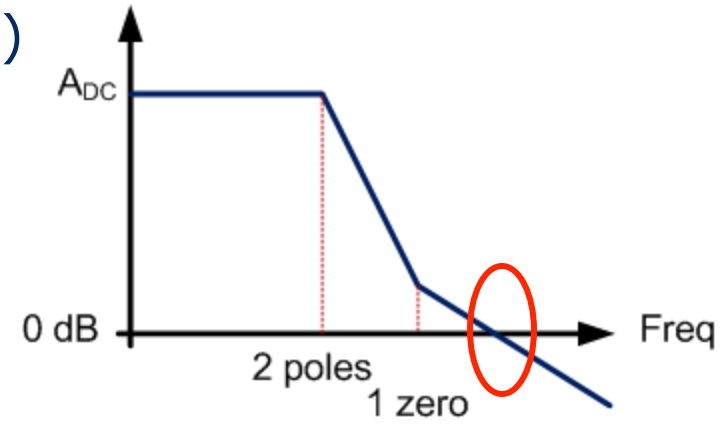
$$NTF = \frac{1}{1+H(s)*ZOH(s)*Z^{-1}}$$

- The system parameters are defined as

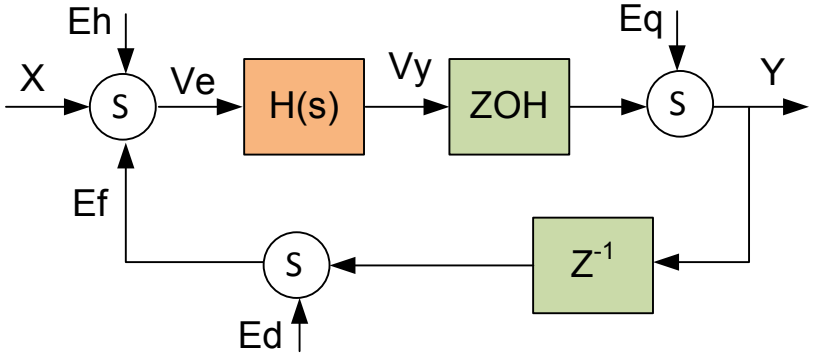
$$Z = e^{j\omega T_S}$$

$$ZOH(z) = T_S * sinc\left(\frac{\omega T_S}{2}\right)$$

- The lowpass transfer function H(s) provides large loop gain (Noise shaping)
  - DC gain >>0 dB
  - Enough phase margin at 0 dB gain
  - **Z is a complex number (phase)**
  - **Loop stability is fundamental**



Oversampled A/D Conversion
Feed-forward configuration

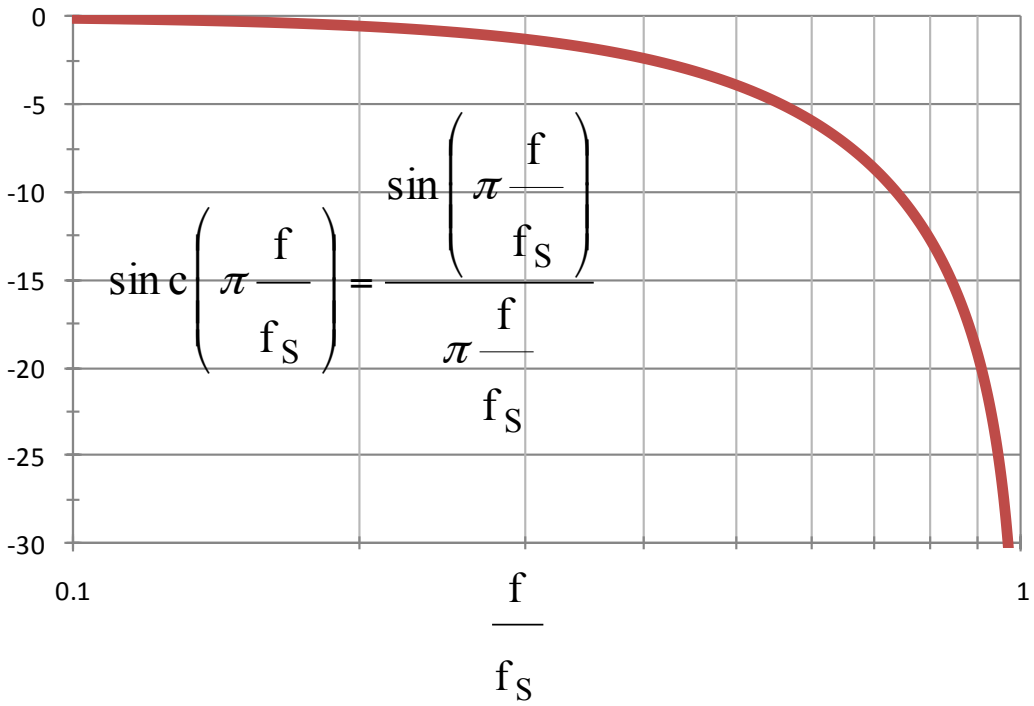


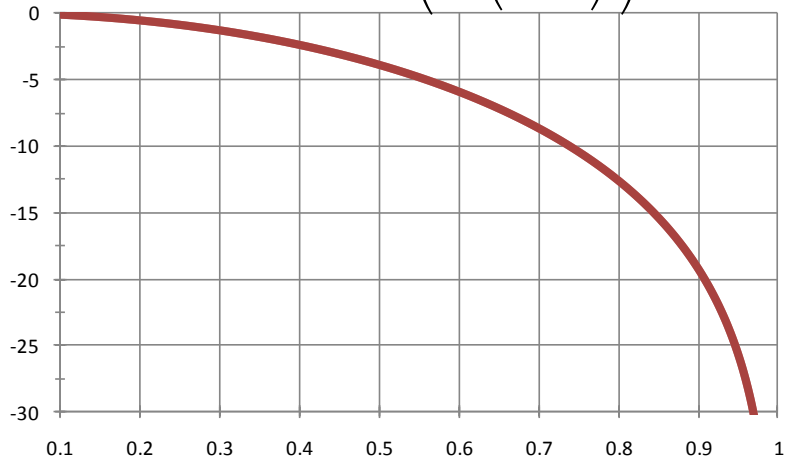
$$Z = e^{j\omega T_S}$$

$$ZOH(z) = T_S * sin\,c\left(\frac{\omega T_S}{2}\right)$$

- Notice that

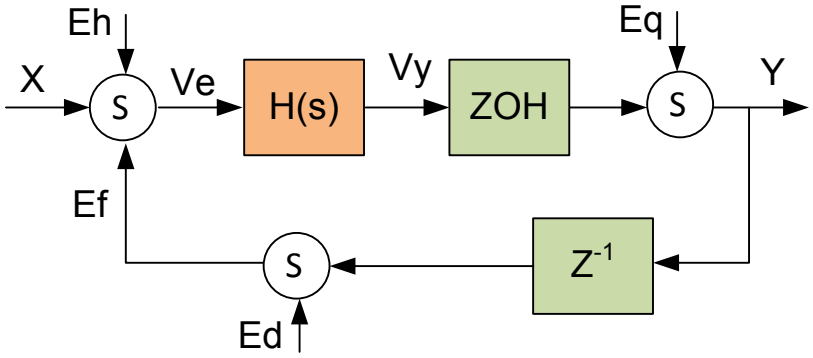
$$ZOH(f) = \sin c\left(\pi\left(\frac{f}{f_S}\right)\right)$$





Oversampled A/D Conversion

Use Mason's rule again!



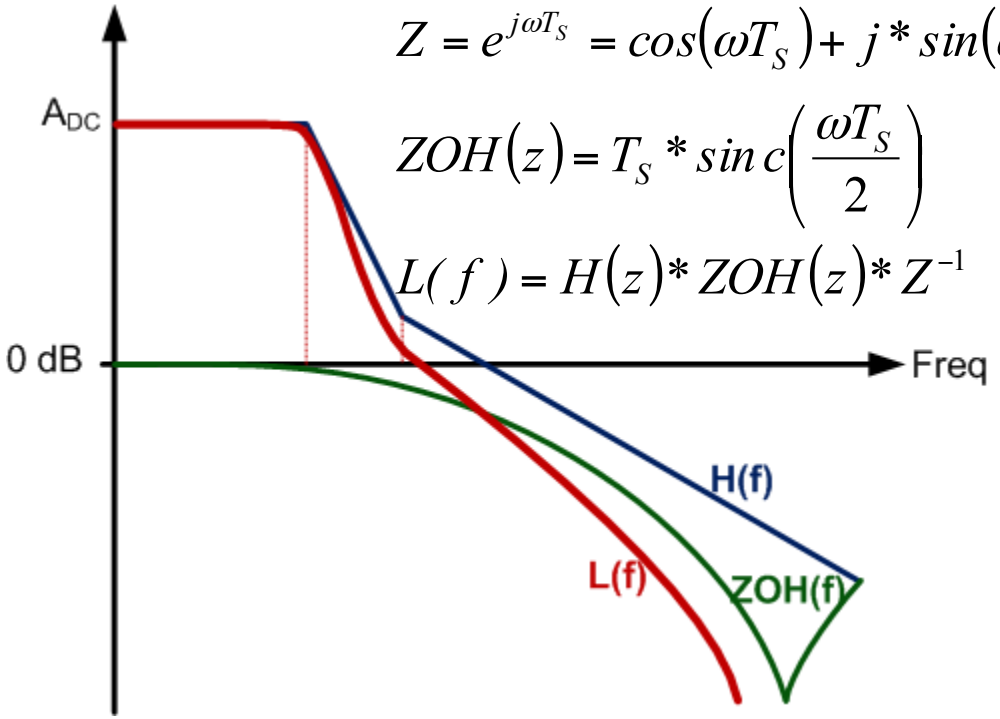
$$STF = \frac{L(f)*Z}{1+L(f)}$$

$$NTF = \frac{1}{1+L(f)}$$

$$Z = e^{j\omega T_S} = cos(\omega T_S) + j*sin(\omega T_S)$$

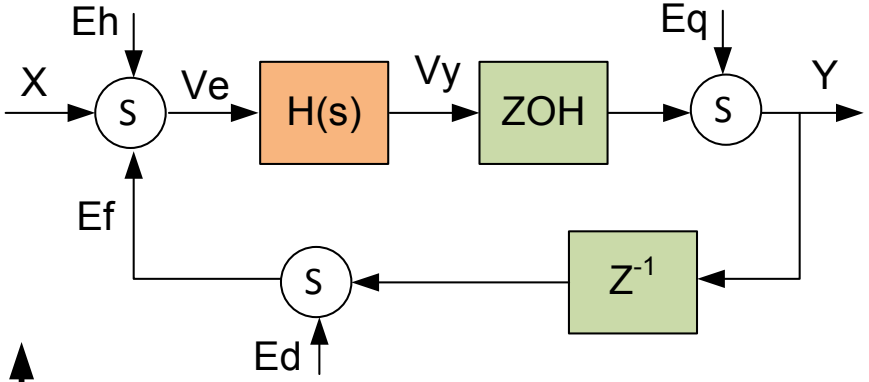
$$ZOH(z) = T_S * sinc\left(\frac{\omega T_S}{2}\right)$$

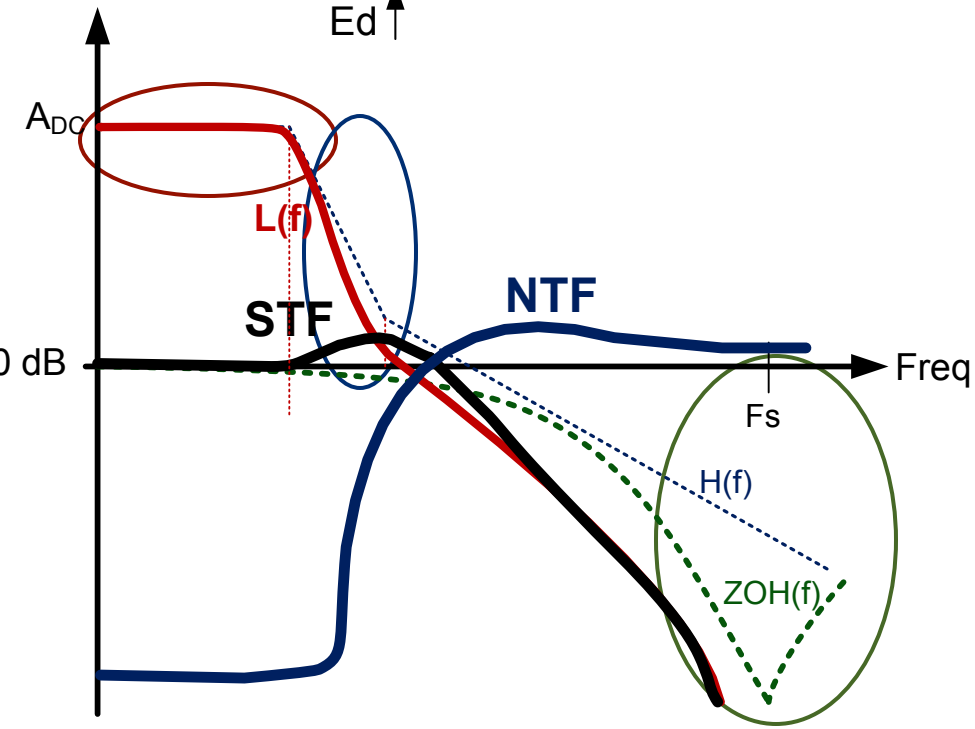
$$L(f) = H(z)*ZOH(z)*Z^{-1}$$



- **L(f)** is defined as the loop gain
- Phase of **L(f)** is quite important for stability
- Z is quite relevant for phase of L(f)

Continuous-Time ΣΔ Modulators





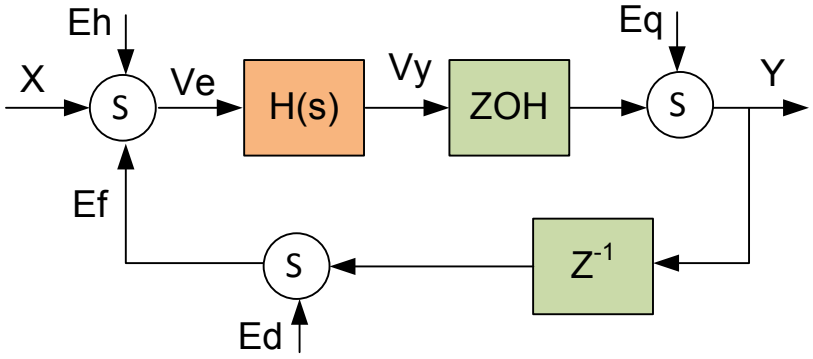
- **For in-band frequencies STF is determined by H(f)**
- **At medium-high frequencies, the blocker rejection is limited (LTE)**
- **Peaking if phase of L(f) phase margin is not enough**
- **At high-frequencies, the anti-alias is mainly provided by the sinc function rather than by the filter**

$$STF = \frac{L(f)*Z}{1+L(f)}$$

$$NTF = \frac{1}{1+L(f)}$$

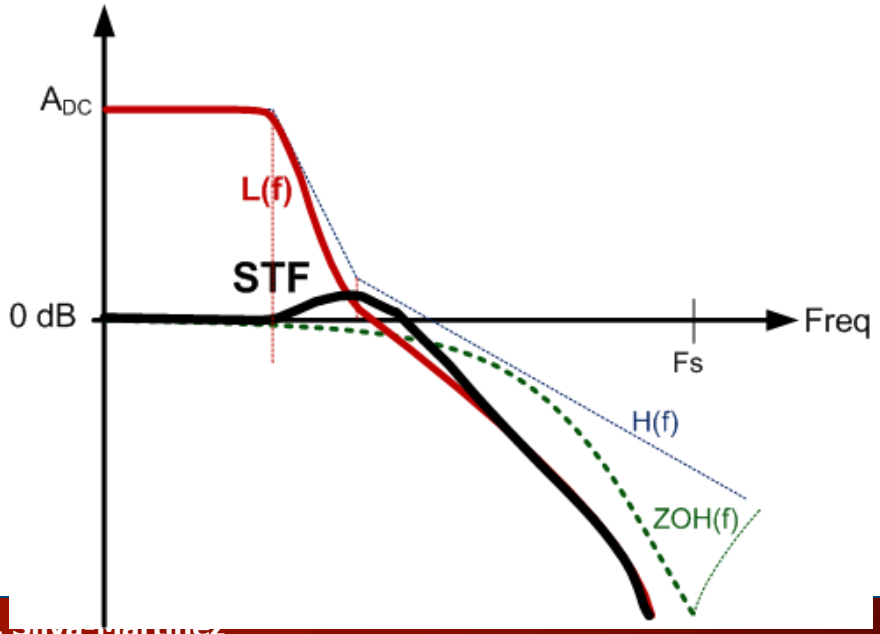
Oversampled A/D Conversion

- **Remarks on DAC non-idealities. Same analysis apply to the input referred filter's noise**



$$Y_{DAC} = STF * E_d$$

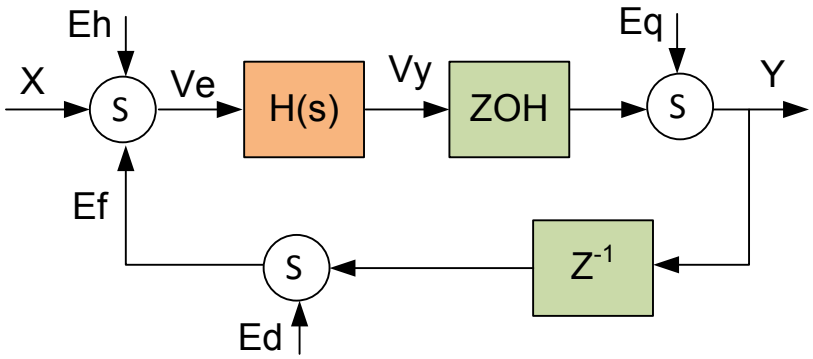
$$STF = \frac{H(s)*ZOH(s)}{1+H(s)*ZOH(s)*Z^{-1}}$$



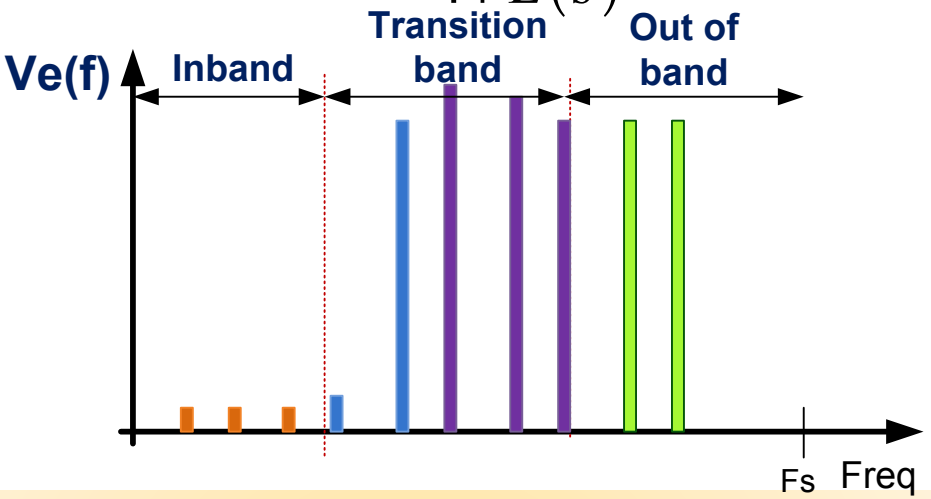
- **DAC non-idealities are reflected at the ADC output similarly to the signal**
- **Baseband noise can be directly mapped to ADC input (Ed and Eh)**
- **Non-linearities in DAC that translate HF noise into baseband affects directly SQNR**
- **DAC is an extremely critical component**

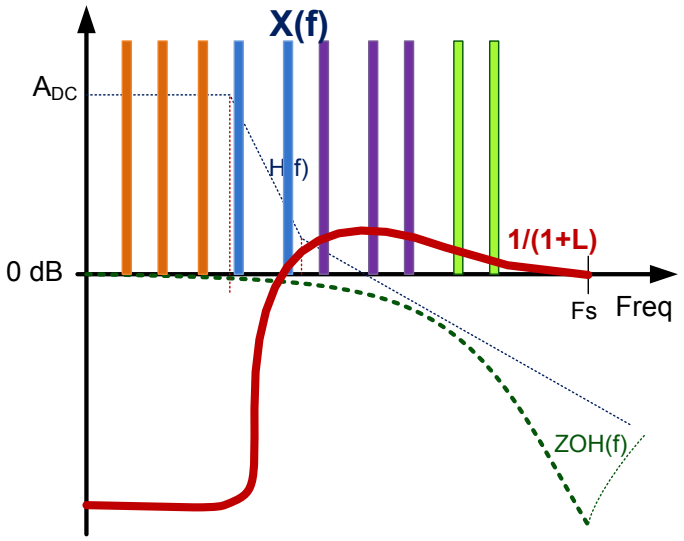
Oversampled A/D Conversion

➢ Remarks on Filter's operation: Filter's input



$$V_e = \frac{X + E_d + E_h + Z^{-1} * E_q}{1 + L(s)}$$

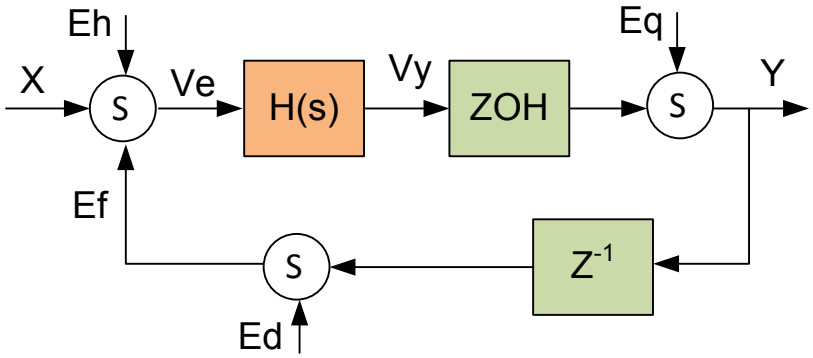




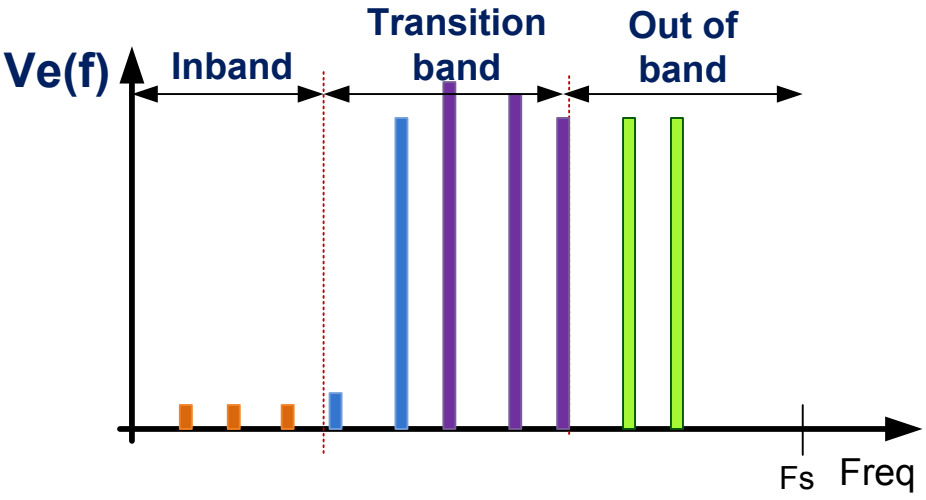
- For the single feedback loop architectures, the inband signal is usually very small: Nice property but…
- Transition band is more critical for filter's linearity (neighbor channels); is this bad? Could be worse and it is!
- Medium and high frequency 1/(1+L) gain could be around 2-10 dB!
- Filter must be designed for out-of-band blockers!

Oversampled A/D Conversion

Remarks on Filter's operation: Filter's input

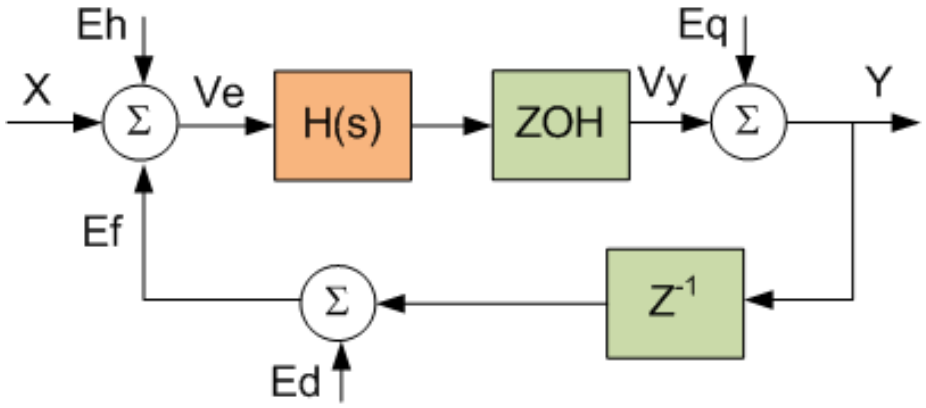


$$V_e = \frac{X + E_d + E_h}{1 + L(s)} + NTF * Z^{-1} * E_q$$



- Ef is an out-of-phase replica of the X+Ef+Eh if L(f)>>1
- When loop gain reduces, the loop is less effective and all HF input signals appear at filter input
- Filter must be very linear at HF to minimize signal intermodulation distortions
- Filter must be designed for the blockers
- Blocker tolerance is a major issue in broadband applications (WiMAX)

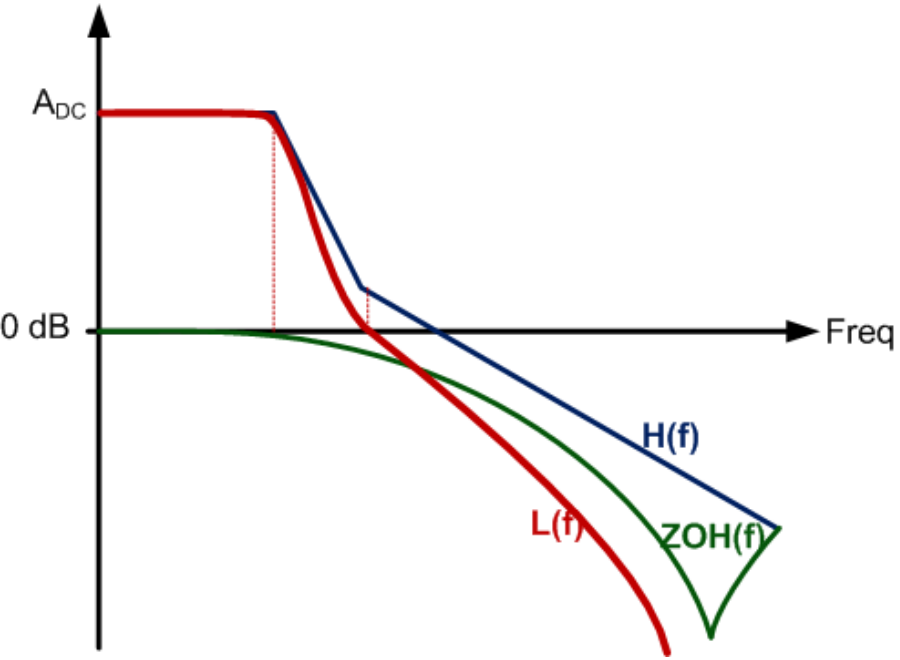
Continuous-Time ΣΔ Modulators

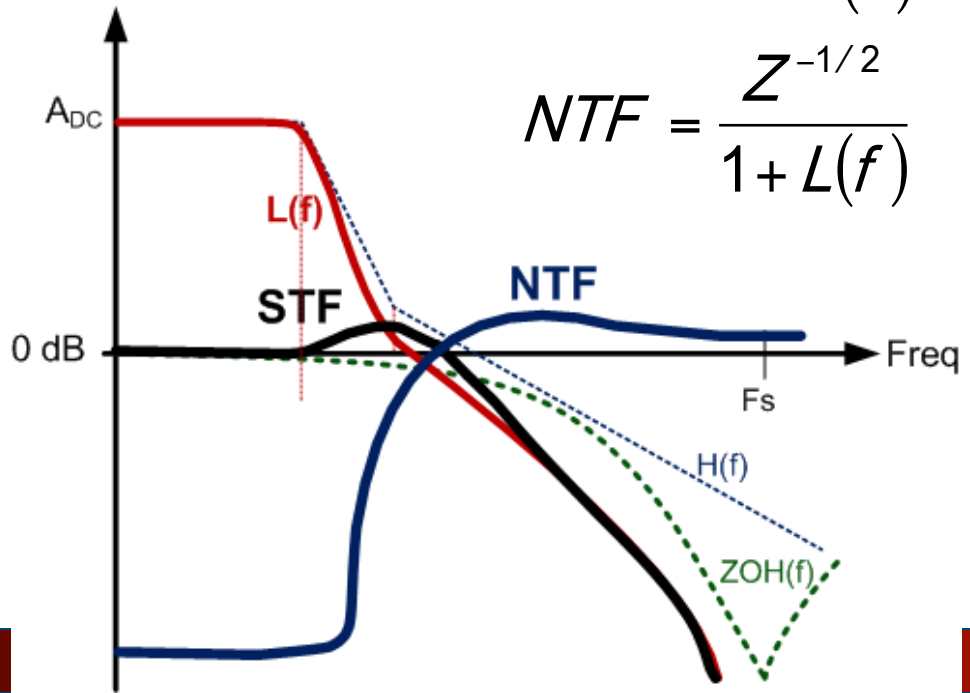


- **This is a realistic model**
- Check the phase of the loop at the unity gain frequency!

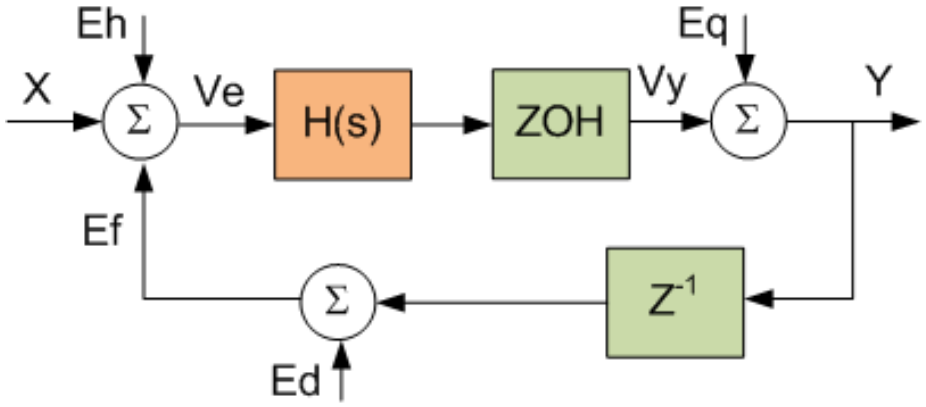
$$STF = \frac{L(f)^* Z}{1+L(f)}$$

$$NTF = \frac{Z^{-1/2}}{1+L(f)}$$

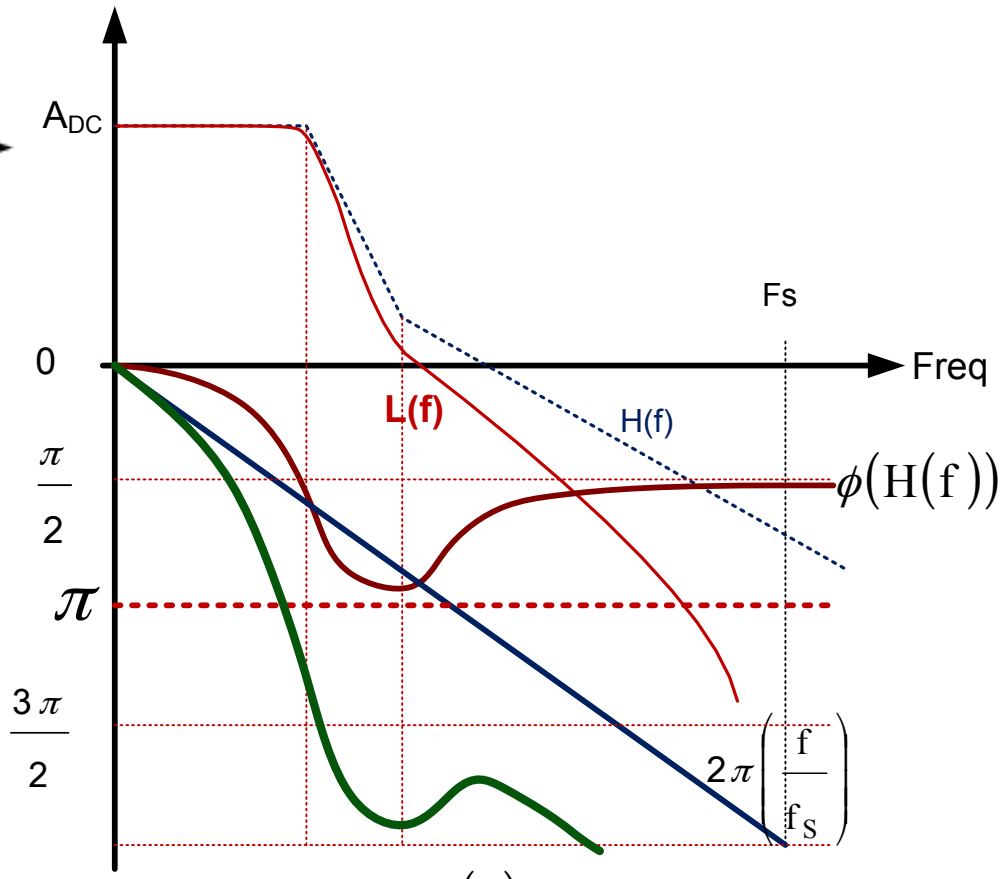




Stability Issues: ΣΔ Modulators



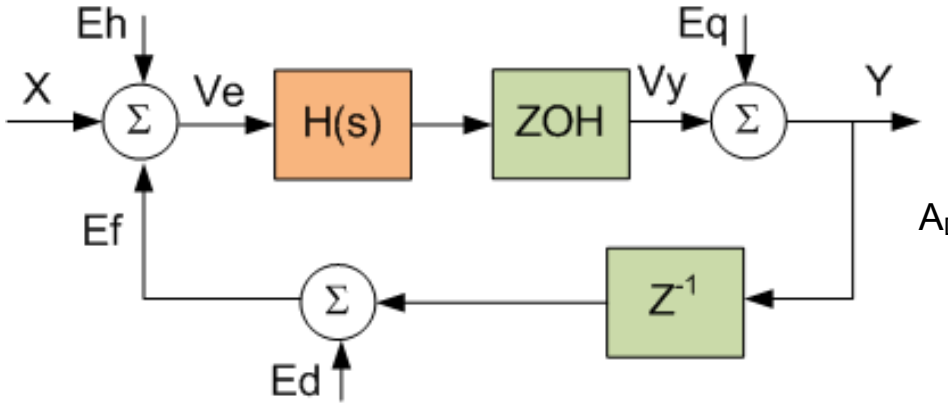
- Check the phase contribution of the **filter** and the **delay element!**
- Check the **phase of the loop** at the unity gain frequency!
- Can you stabilize the loop employing the conventional filter design approach?
- **Additional parasitic poles!**



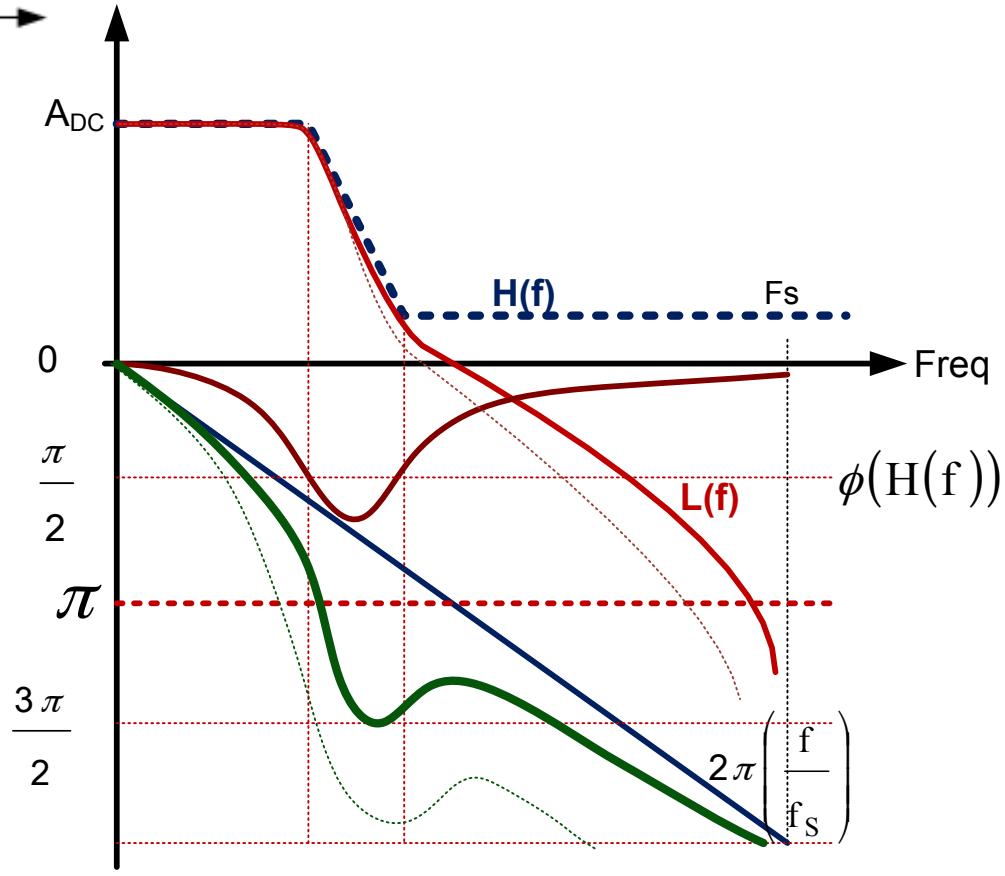
$$STF = \frac{L(f)^* Z}{1+L(f)}$$

$$NTF = \frac{Z^{-1/2}}{1+L(f)}$$

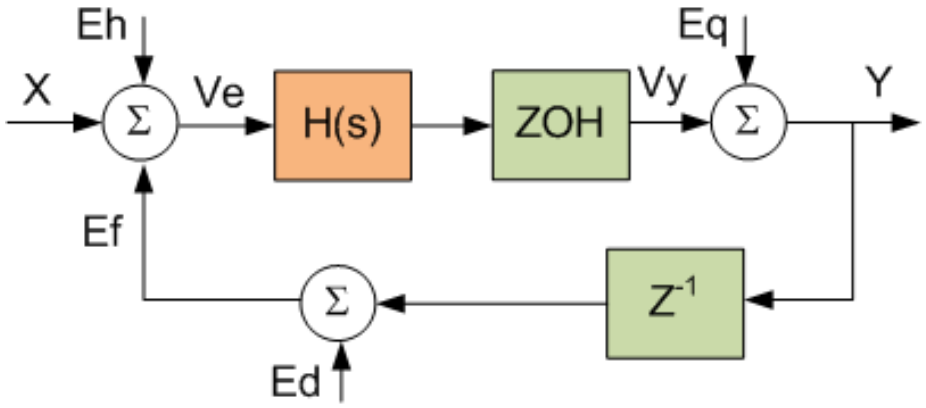
Stability Issues: ΣΔ Modulators



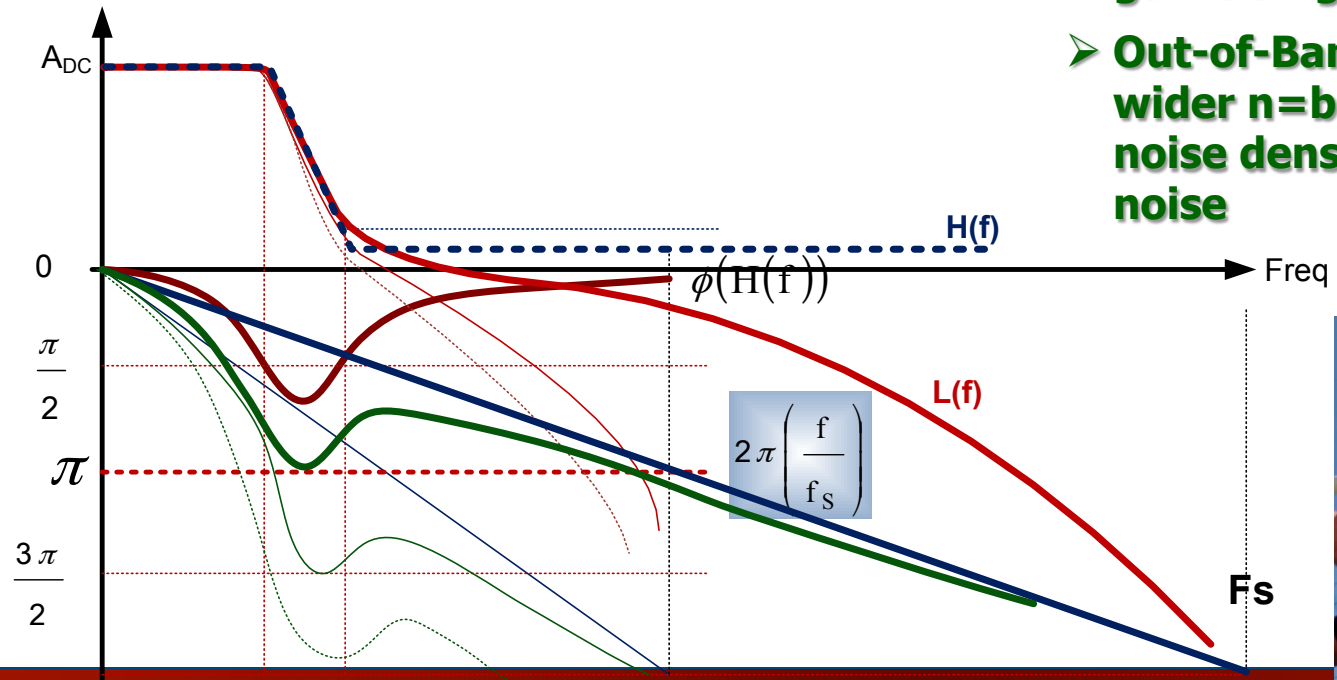
- **With a filter with 2 zeros (finite gain at high frequency)**
  - **Hard to stabilize the loop if the unity gain frequency is close to Fs/2! (Very Low OSR)**
  - **Notice that the delay element add -180 degrees at f=Fs/2**
  - **If the loop unity gain frequency is not beyond f=Fs/4, then maximum phase contribution due to the delay element is <-90 degrees**



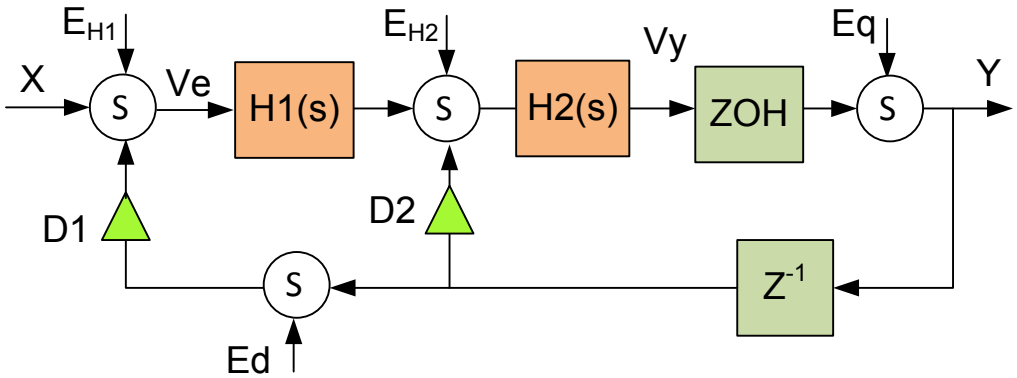
Stability Issues: ΣΔ Modulators



- Not very difficult to stabilize the loop if the unity gain frequency is below Fs/4! (not very Low OSR); e.g. around 100Mhz if clock frequency is 400MHz
- Notice that larger oversampling ratio allow you to reduce the filter gain at high-frequency
- Out-of-Band noise is distributed in wider n=bandwidth, hence smaller noise density but same integrated noise



Oversampled A/D Conversion Multiple Feedback architecture



This architecture presents several interesting properties, but be careful with its drawbacks!

- Eq stands for the quantization noise
- Ed stands for DAC non-idealities (jitter + thermal noise)
- Filter's thermal noise is accounted in EH1,2
- D1,2 are the DAC coefficients

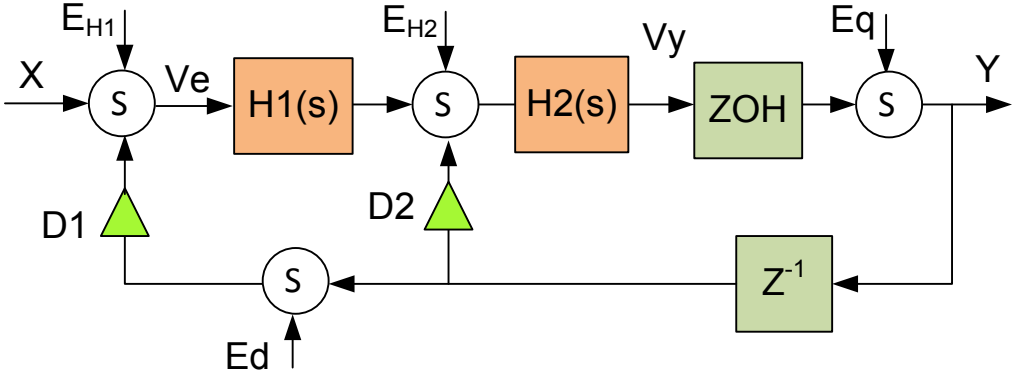
$$Y = STF*\left(X + E_d + E_{H1}\right) + NTF*E_q + STF2*E_{H1}$$

$$STF = \frac{H_1(s)*H_2(s)*ZOH}{1+\left\{D1*H_1(s)+D2\right\}*\left\{H_2(s)*ZOH*Z^{-1}\right\}}$$

$$NTF = \frac{ZOH}{1+\left\{D1*H_1(s)+D2\right\}*\left\{H_2(s)*ZOH*Z^{-1}\right\}}$$

$$STF2 = \frac{H_2(s)*ZOH}{1+\left\{D1*H_1(s)+D2\right\}*\left\{H_2(s)*ZOH*Z^{-1}\right\}}$$

Oversampled A/D Conversion Feedback architecture



$$Y = STF*\left(X + E_d + E_{H1}\right) + NTF * E_q + STF2 * E_{H2}$$

$$STF = \frac{H_1(s)*H_2(s)*ZOH}{1+\left\{D1*H_1(s)+D2\right\}*\left\{H_2(s)*ZOH*Z^{-1}\right\}}$$

$$NTF = \frac{ZOH}{1+\left\{D1*H_1(s)+D2\right\}*\left\{H_2(s)*ZOH*Z^{-1}\right\}}$$

$$STF2 = \frac{H_2(s)*ZOH}{1+\left\{D1*H_1(s)+D2\right\}*\left\{H_2(s)*ZOH*Z^{-1}\right\}}$$

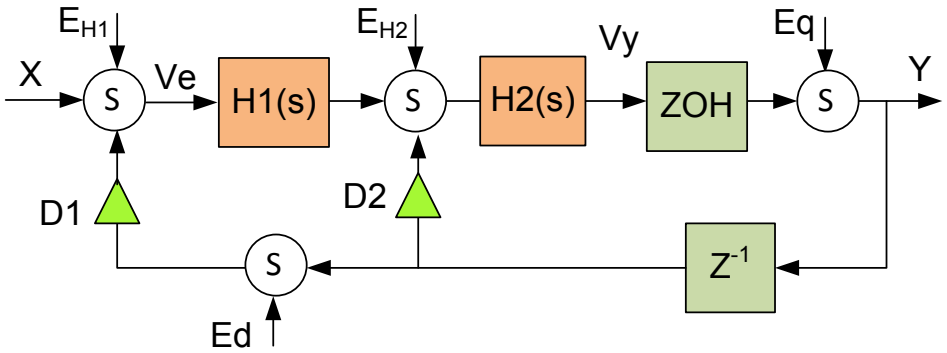
- **Notice that in-band STF is still approximately unity (1/D1 if D1H1>>D2) up to the unity gain frequency**
- **The error signal becomes:**

$$V_e = \frac{\left(X + E_d + E_{H1}\right)\left(1 + D2*H_2(s)*ZOH*Z^{-1}\right)}{1+\left\{D1*H_1(s)+D2\right\}*\left\{H_2(s)*ZOH*Z^{-1}\right\}} + NTF*Z^{-1}*\left(H_2(s)*E_{H2} + E_q\right)$$

- **In-band signal level at Ve is approximately obtained as**

$$V_e \cong \frac{\left(X + E_d + E_{H1}\right)*D2 + E_{H2}}{D1*H_1(s)+D2} + \frac{E_q}{\left\{D1*H_1(s)+D2\right\}*\left\{H_2(s)\right\}}$$

Oversampled A/D Conversion Feedback architecture

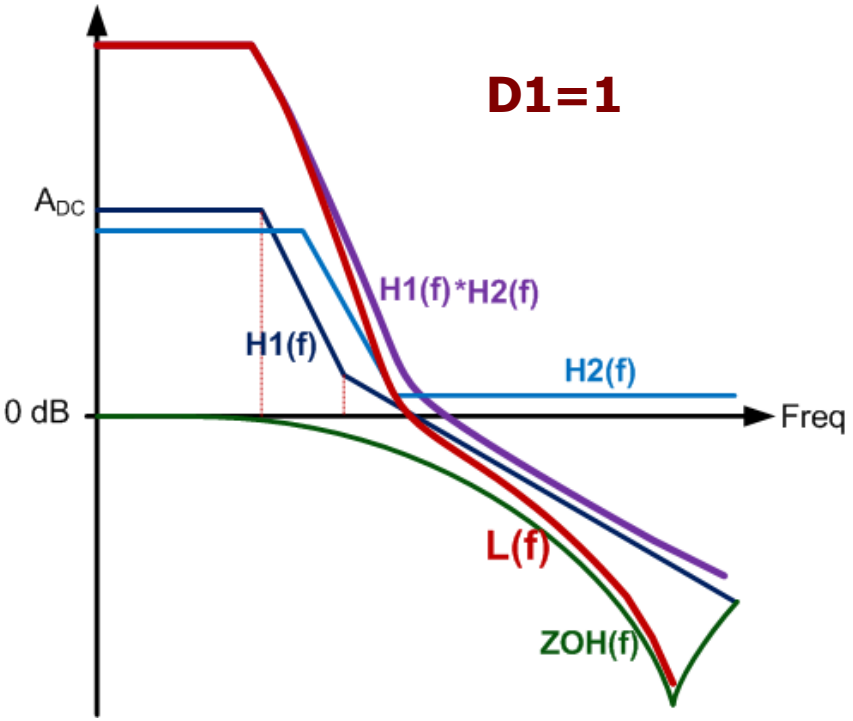


$$Y = STF*\left(X + E_d + E_{H1}\right) + NTF*E_q + STF2*E_{H2}$$

$$STF = \frac{H_1(s)*H_2(s)*ZOH}{1+L(f)}$$

$$NTF = \frac{ZOH}{1+L(f)}$$

$$STF2 = \frac{H_2(s)*ZOH}{1+L(f)}$$

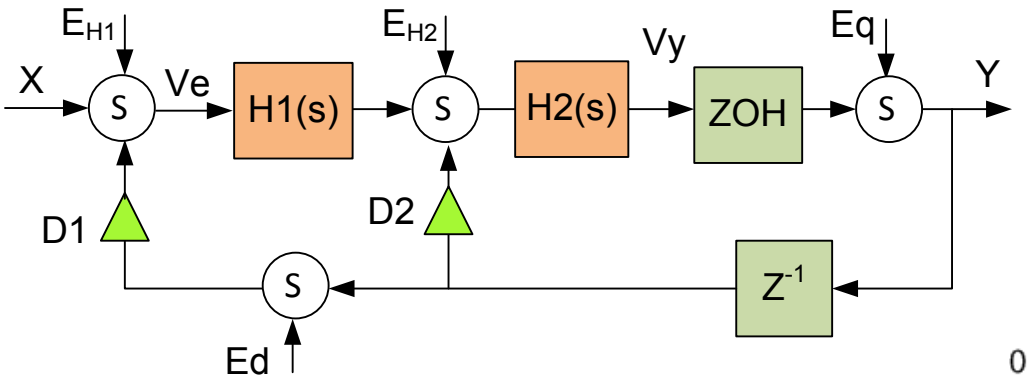


$$L(f) = \left\{D1*H_1(s) + D2\right\}*\left\{H_2(s)*ZOH*Z^{-1}\right\}$$

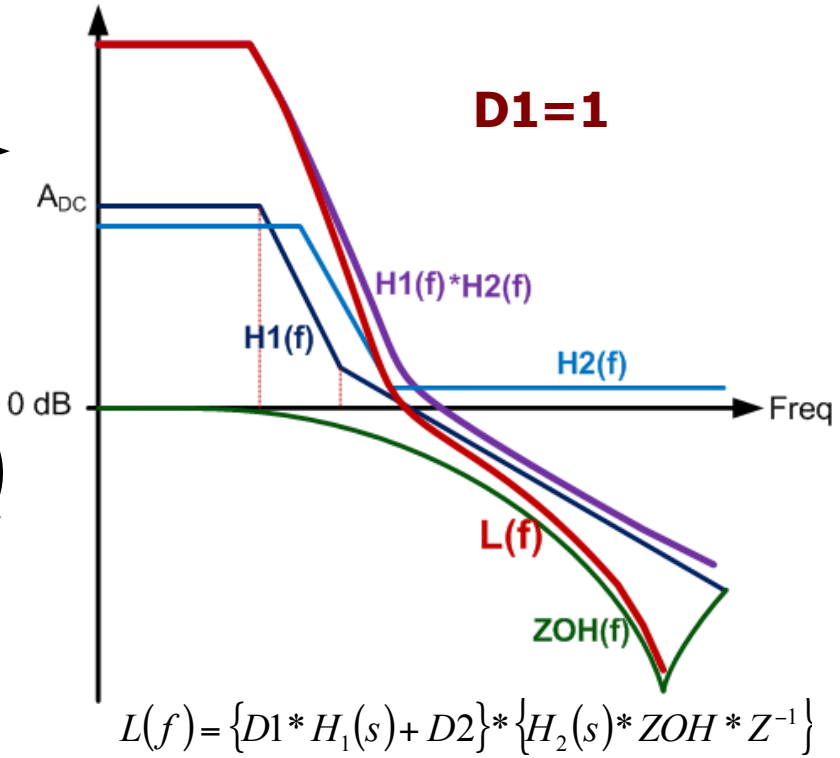
- Out of band STF is quite small; excellent for blockers rejection
- NTF follows the ZOH at very high frequencies, Minimizing the alias issue
- For STF2, again, the ZOH helps, but..
- The ZOH is excellent filter around f=fs

The ZOH provides -4 dB attenuation at f=0.5fs and -20 dB at f=0.9fs

Oversampled A/D Conversion Feedback architecture



$$V_{e1} = \frac{(X + E_d + E_{H1})(1 + D2 * H_2(s) * ZOH * Z^{-1})}{1 + L(f)}$$



$$L(f) = \{D1 * H_1(s) + D2\} * \{H_2(s) * ZOH * Z^{-1}\}$$

- For in-band signals apparently is fine:

$$V_{e1} \cong \frac{(X + E_d + E_{H1})D2}{D1 * H_1(s) + D2}$$

- At the output of H1(s) we get

$$V_{H1-out} \cong \left(\frac{D2}{D1}\right)(X + E_d + E_{H1})$$

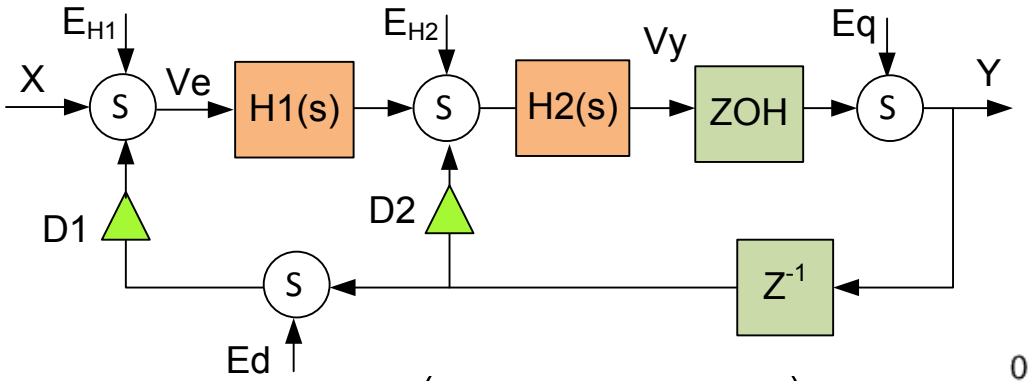
- This signal could be excessive for H2

- For out-band signals:

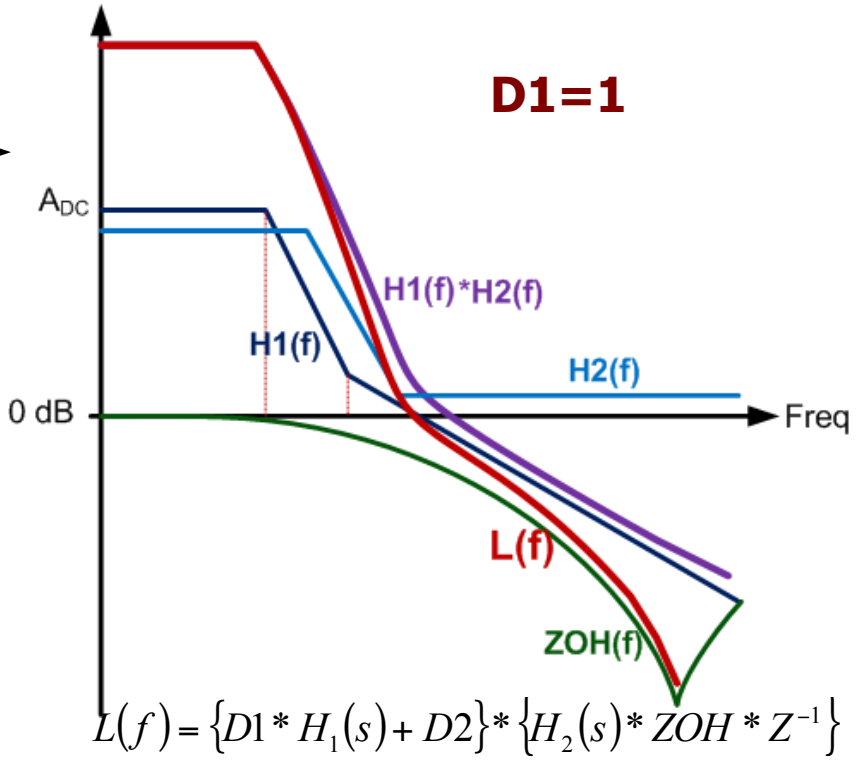
$$V_{e1} = (X + E_d + E_{H1})(1 + D2 * H_2(s) * ZOH * Z^{-1})$$

- Most of the blockers and HF noise sources are present at H1 input

Oversampled A/D Conversion Feedback architecture



$$V_{e2} = \frac{ZOH * Z^{-1} * \left(H_2(s) * E_{H2} + E_q\right)}{1 + L(f)}$$



$$L(f) = \{D1 * H_1(s) + D2\} * \{H_2(s) * ZOH * Z^{-1}\}$$

- For in-band signals:

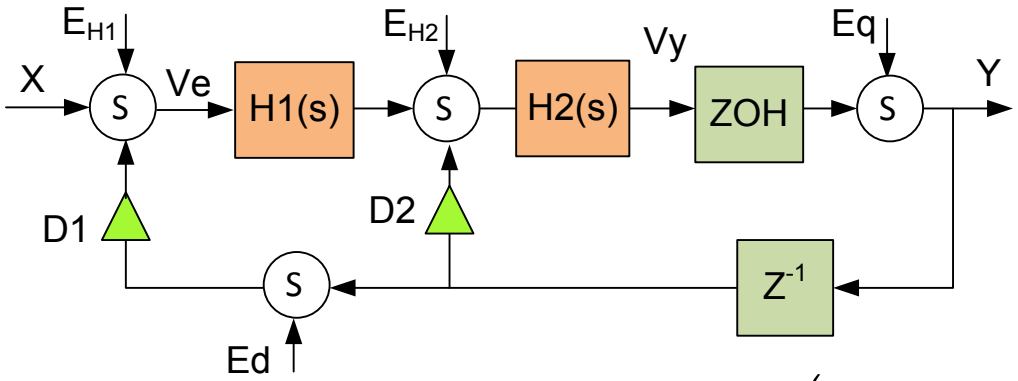
$$V_{e2} = \frac{E_{H2}}{H_1(s)} + \frac{E_q}{H_1(s) * H_2(s)}$$

- At medium and HF only the ZOH helps

$$V_{e2} = ZOH * \left(H_2(s) * E_{H2} + E_q\right)$$

- **Looks like E_{H2} and E_q are not the main issue in this topology**

Oversampled A/D Conversion Multiple Feedback architecture



This linear model is probably more appropriated for the feedback architecture!

ZOH does not affect the numerator of NTF

$$Y = STF*(X + E_d + E_{H1}) + NTF*E_q + STF2*E_{H2}$$

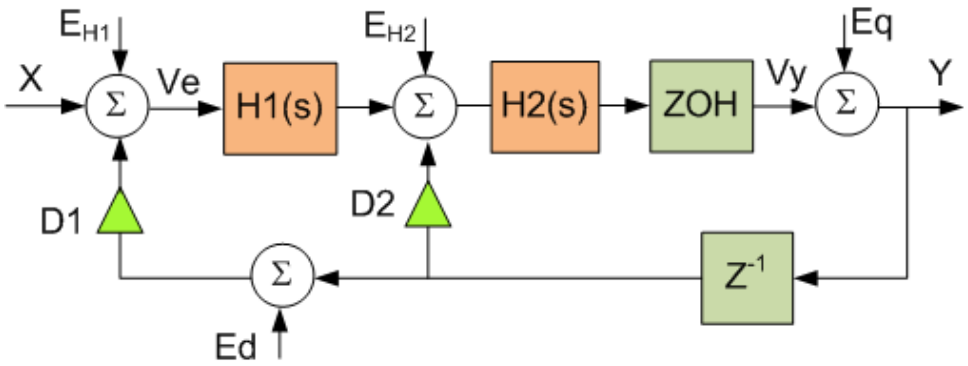
- Eq stands for the quantization noise
- Ed stands for DAC non-idealities (jitter + thermal noise)
- Filter's thermal noise is accounted in EH1,2
- D1,2 are the DAC coefficients

$$STF = \frac{H_1(s)*H_2(s)*ZOH}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}}$$

$$NTF = \frac{1}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}}$$

$$STF2 = \frac{H_2(s)*ZOH}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}}$$

Oversampled A/D Conversion Feedback architecture



$$Y = STF*(X + E_d + E_{H1}) + NTF*E_q + STF2*E_{H2}$$

$$STF = \frac{H_1(s)*H_2(s)*ZOH}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}}$$

$$NTF = \frac{1}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}}$$

$$STF2 = \frac{H_2(s)*ZOH}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}}$$

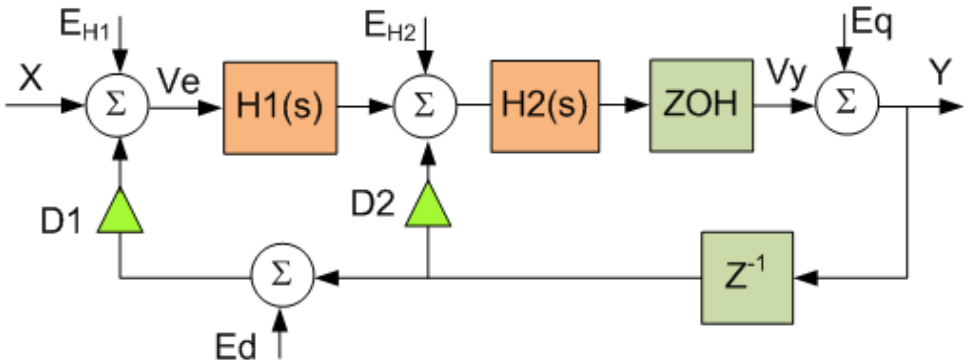
- **Notice that in-band STF is still approximately unity (1/D1 if D1H1>>D2) up to the unity gain frequency; D1 is usually set as 1**
- **The error signal becomes:**

$$V_e = \frac{(X + E_d + E_{H1})(1 + D2*H_2(s)*ZOH*Z^{-1})}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}} + NTF*Z^{-1}*(H_2(s)*ZOH*E_{H2} + E_q)$$

- **In-band signal level at Ve is approximately obtained as**

$$V_e \cong \frac{(X + E_d + E_{H1})*D2 + E_{H2}}{D1*H_1(s)+D2} + \frac{E_q}{\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH\}}$$

Oversampled A/D Conversion Feedback architecture

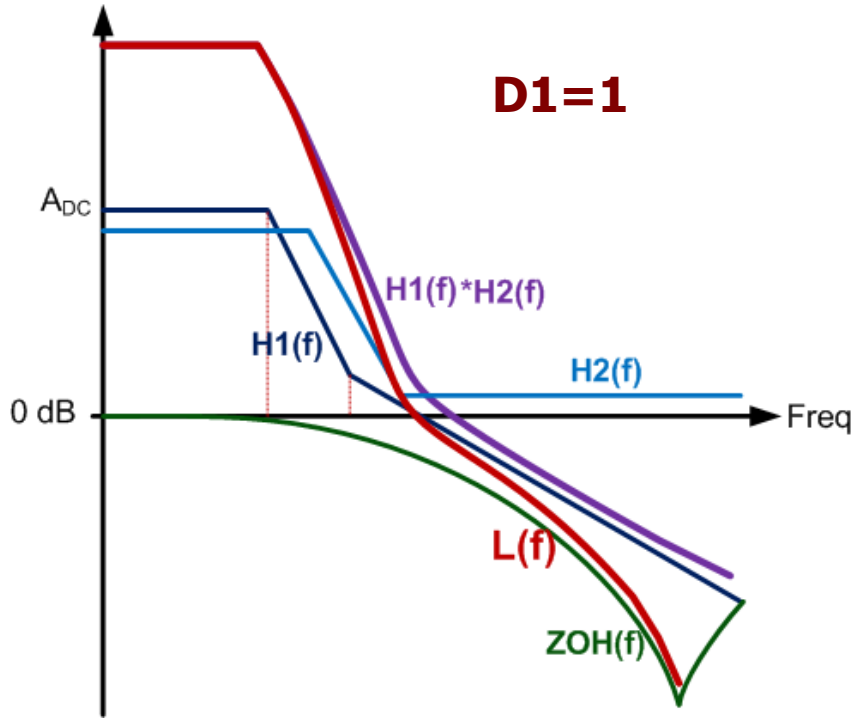


$$Y = STF*(X + E_d + E_{H1}) + NTF*E_q + STF2*E_{H2}$$

$$STF = \frac{H_1(s)*H_2(s)*ZOH}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}}$$

$$NTF = \frac{1}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}}$$

$$STF2 = \frac{H_2(s)*ZOH}{1+\{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}}$$

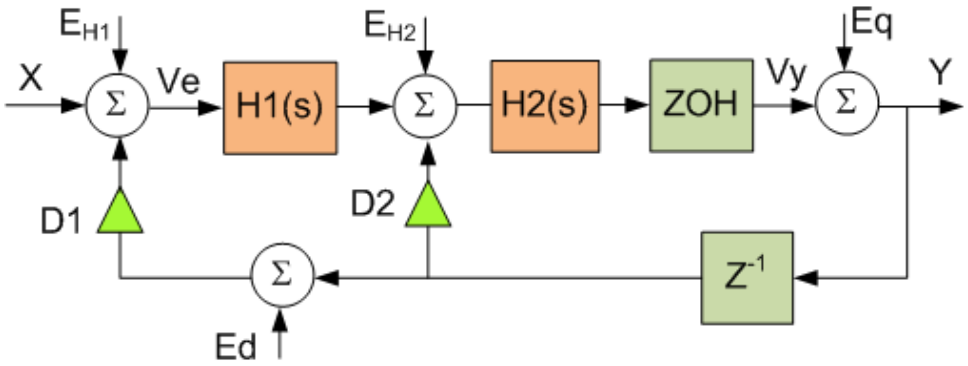


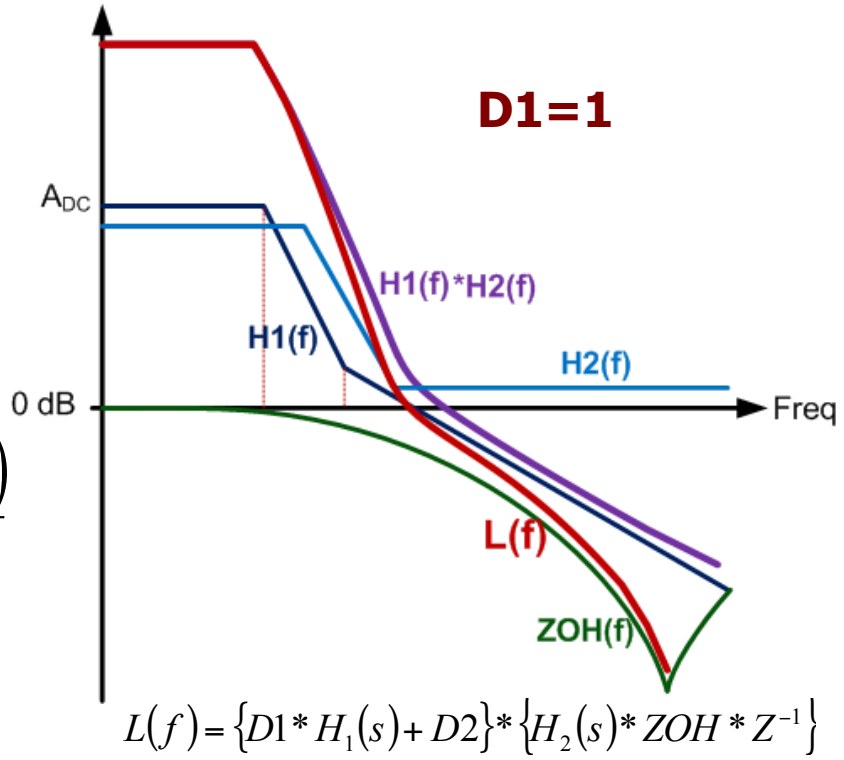
$$L(f) = \{D1*H_1(s)+D2\}*\{H_2(s)*ZOH*Z^{-1}\}$$

- Out of band STF is quite small; excellent for blockers rejection
- NTF does not follows the ZOH at very high frequencies
- For STF2, again, the ZOH helps, but..
- The ZOH is excellent around f=fs

The ZOH provides -4 dB attenuation at f=0.5fs and -20 dB at f=0.9fs

Oversampled A/D Conversion Feedback architecture





$$V_{e1} = \frac{(X + E_d + E_{H1})(1 + D2 * H_2(s) * ZOH * Z^{-1})}{1 + L(f)}$$

$$L(f) = \{D1 * H_1(s) + D2\} * \{H_2(s) * ZOH * Z^{-1}\}$$

- For in-band signals apparently is fine if D2 is not very large

$$V_{e1} \cong \frac{(X + E_d + E_{H1})D2}{D1 * H_1(s) + D2}$$

- At the output of H1(s) we get

$$V_{H1-out} \cong \left(\frac{D2}{D1}\right)(X + E_d + E_{H1})$$

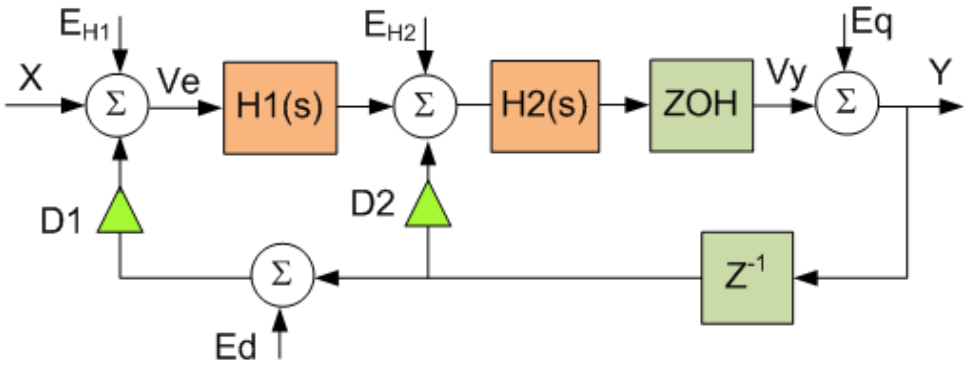
- This signal could be excessive for H2

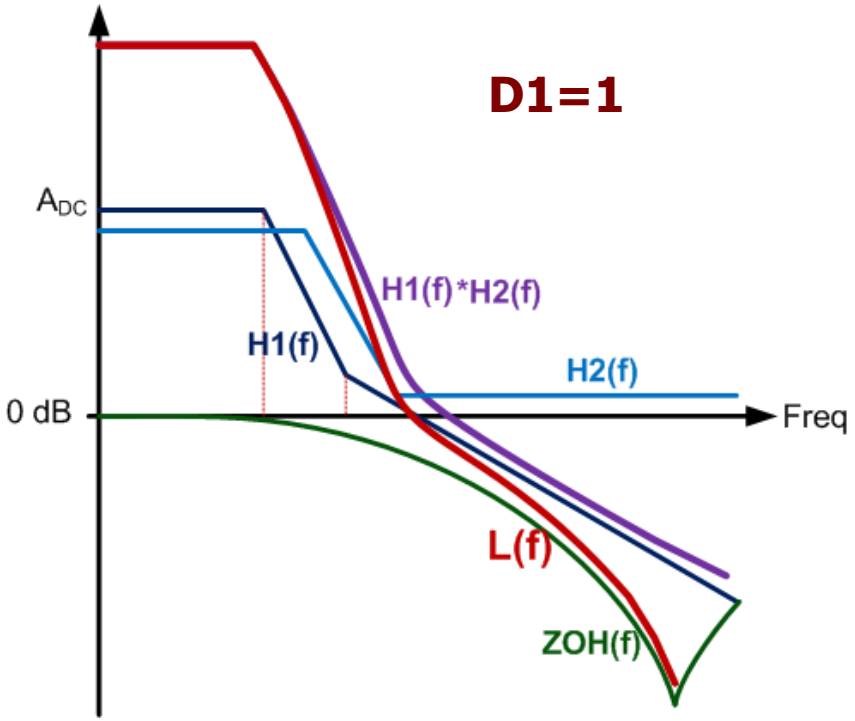
- For out-band signals:

$$V_{e1} \cong (X + E_d + E_{H1})(1 + D2 * H_2(s) * ZOH * Z^{-1})$$

- Most of the blockers and HF noise sources are present at H1 input

Oversampled A/D Conversion Feedback architecture





$$V_{e2} = \frac{Z^{-1} * \left(H_2(s) * ZOH * E_{H2} + E_q\right)}{1 + L(f)}$$

$$L(f) = \left\{D1 * H_1(s) + D2\right\} * \left\{H_2(s) * ZOH * Z^{-1}\right\}$$

- For in-band signals:

$$V_{e2} = \frac{E_{H2}}{H_1(s)} + \frac{E_q}{H_1(s) * H_2(s)}$$

- At medium and HF only the ZOH helps

$$V_{e2} = ZOH * H_2(s) * E_{H2} + E_q$$

- **Looks like E_{H2} and E_q are not the main issue in this topology**

CT ΔΣ ADC Non-idealities

DAC Non-idealities

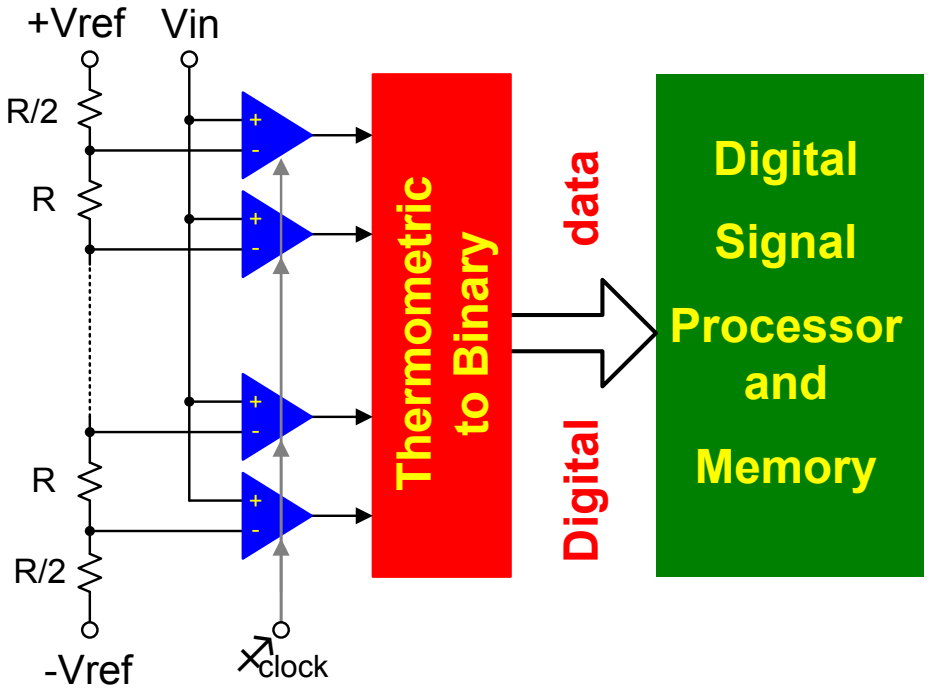
- **Excess loop delay** : Constant delay between ideal and implemented DAC feedback pulse
  - Decision time required by quantizer affecting latches used for synchronizing DAC inputs
  - Finite response time of DAC to its clock and inputs
  - Excess Loop Delay can be incorporated: $Z^{-1} \rightarrow Z^{-1+\Delta}$

- **Inter-symbol interference** : Finite slew rate of DAC outputs with unequal rise and fall times
  - Additional noise and tones fold into baseband

- Clock jitter in DAC
- DAC and Filter Non-linearity

} Processed by STF
Not noise-shaped

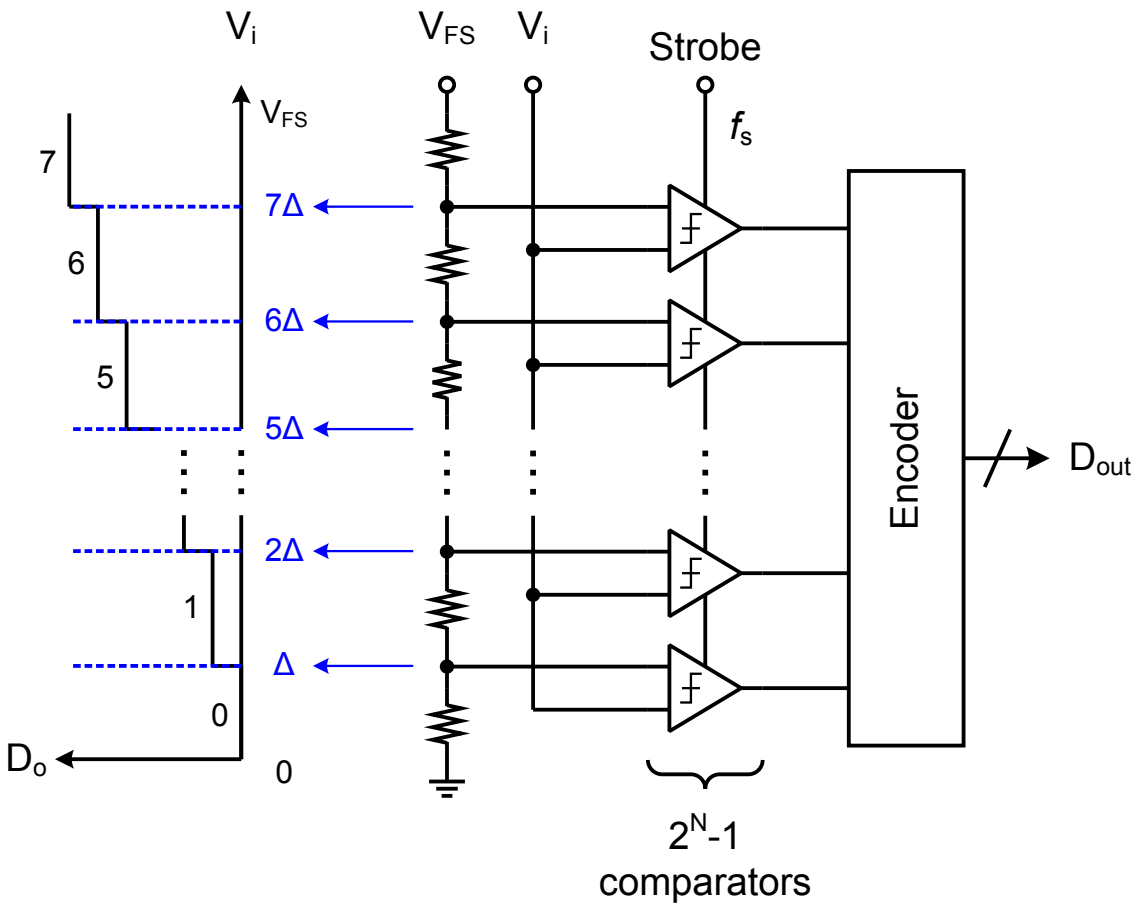
Typical Quantizer: Flash Architecture



- S/H operates at clock rate
- Huge input capacitance if N>6
  - Kick back noise
- Requires a precise low-impedance resistive ladder:
  - Power-accuracy-Speed tradeoff
- Limited by comparator
  - Speed and accuracy
  - Offset voltage
- Hard to improve its resolution

State of the art: ~ 2.4 GS/s 6 bits resolution

Flash Based Quantizer Architecture



- Reference ladder consists of 2^N equal size resistors
- Input is compared to 2^N-1 reference voltages.
- Massive parallelism
- Fastest ADC architecture
- Latency = 1T = $1/f_s$
- Throughput = f_s
- Complexity = 2^N

ADC Input Capacitance

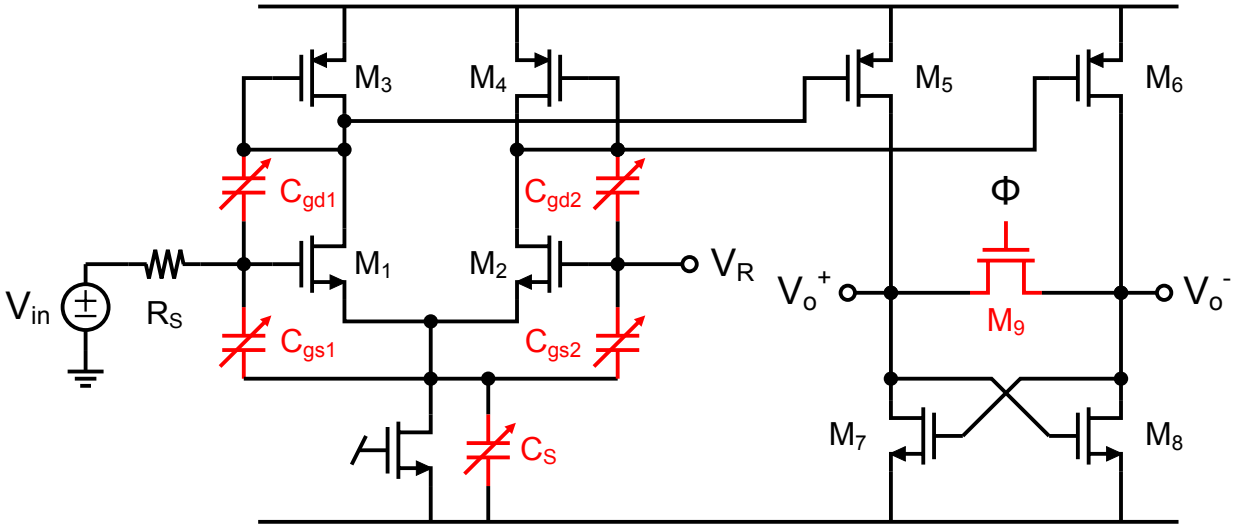
$$\sigma^2(V_{T0}) = \frac{A_{VT0}^{\ 2}}{WL} \qquad C_g = 10\,fF/\mu m^2$$

- **N = 6 bits → 63 comparators**
- **V_{FS} = 1V → 1 LSB = 16mV**
- **σ = LSB/4 → σ = 4mV**
- **A_{VT0} = 10mV·µm → L = 0.24µm, W = 26µm**

N (bits)	# of comp.	C_{in} (pF)
4	15	1
6	63	3.9
8	255	16

- **Small V_{os} leads to large device sizes, hence large area and power.**
- **Large comparator leads to large input capacitance, difficult to drive and difficult to maintain bandwidth.**

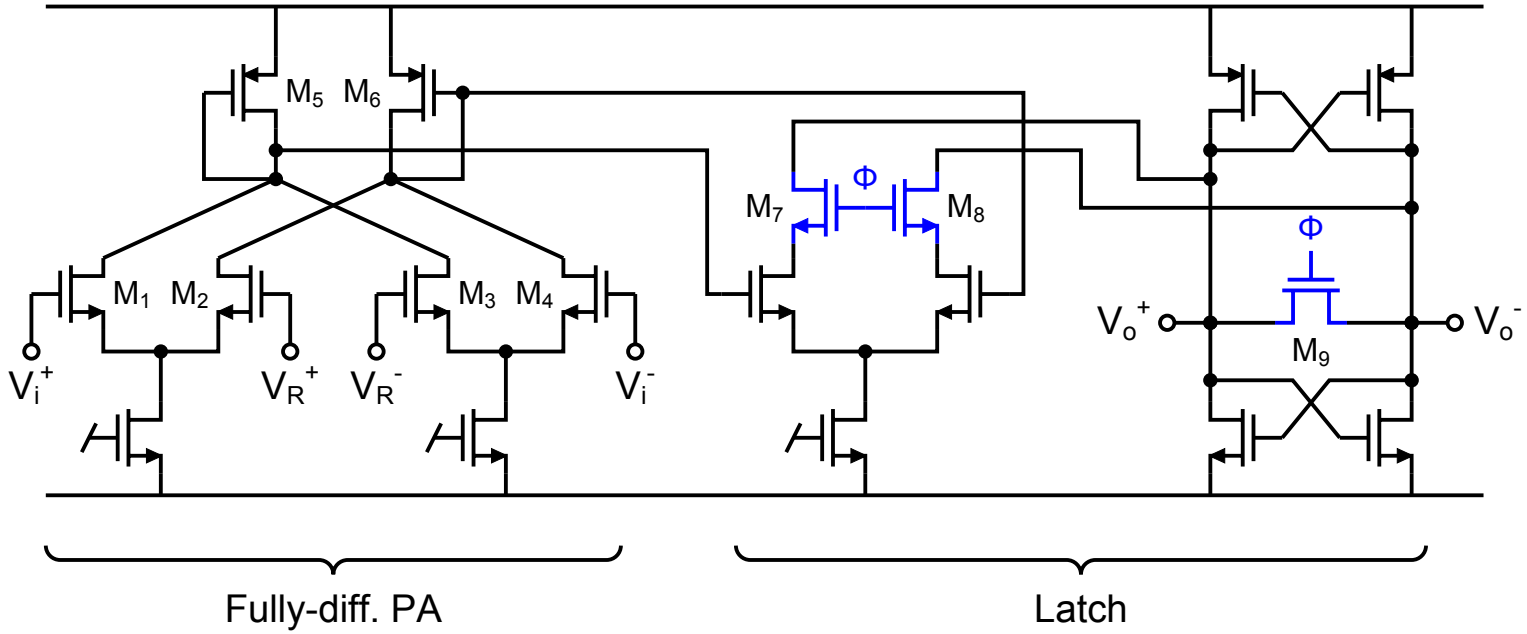
Kick-back noise and coupling capacitors



Φ	Mode
"high"	Track
"low"	Regen.

- Preamp delay and V_{th} of sampling switch (M_9) are both signal-dependent → signal-dependent sampling point (aperture error)
- A major challenge of distributing clock signals across 2^N-1 comparators in flash ADC with minimum clock skew (routing, V_{th} mismatch of M_9)

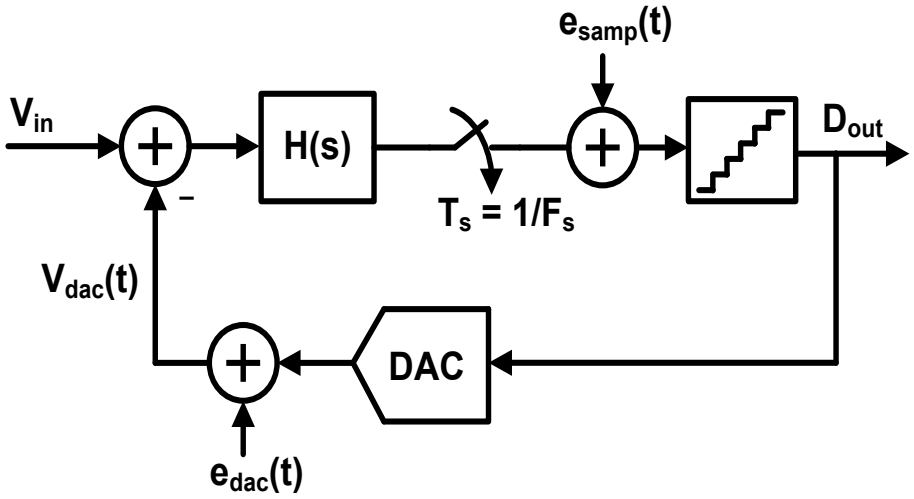
Fully-Differential Comparator



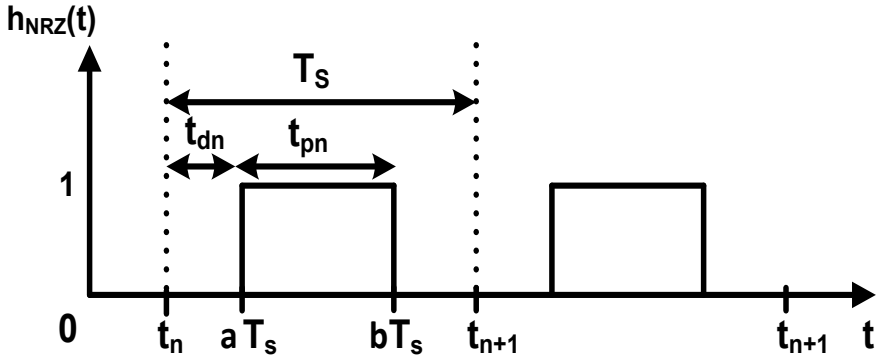
- **Double-balanced, fully-differential preamp**
- **Switches (M_7, M_8) added to stop input propagation during regeneration**
- **Active pull-up PMOS added to the latch**

DAC Non-idealities

Sources of jitter error



Jitter errors in rectangular DAC pulse



$t_{pn} = (b - a)T_S + Dt_{pn}$ ® Pulse-position jitter

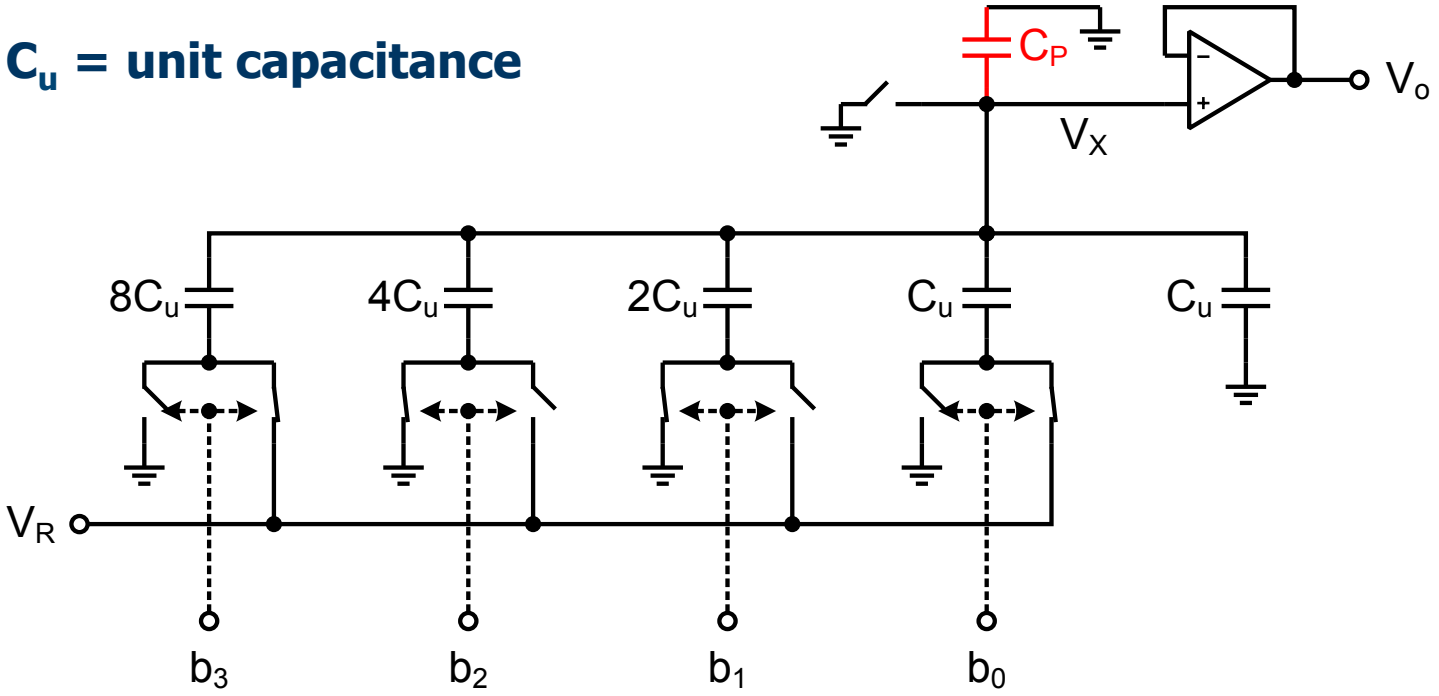
$t_{dn} = aT_S + Dt_{dn}$ ® Pulse-position jitter

- **Pulse-width jitter:** Random variation in charge fed back per clock cycle
  - Wide-band clock phase noise modulates out-of-band ADC inputs and quantization noise to in-band

- **Pulse-position jitter:** Random variation in integration interval of constant charge
  - Amplitude errors due to PP jitter are at least 1st-order noise-shaped

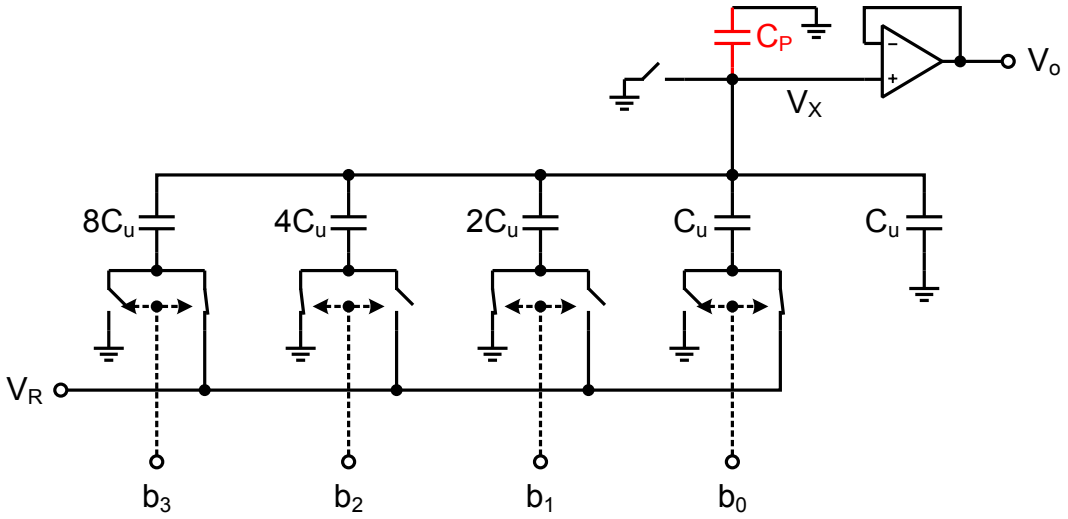
Binary-Weighted CR DAC

C_u = unit capacitance



- Binary-weighted capacitor array → most efficient architecture
- Bottom plate @ V_R with $b_j = 1$ and @ GND with $b_j = 0$

Binary-Weighted C-DAC



$$V_o = \left(\frac{\sum_{j=1}^{N} b_{N-j} \cdot 2^{N-j} C_u}{C_p + C_u + \sum_{j=1}^{N} 2^{N-j} C_u} \right) \cdot V_R$$

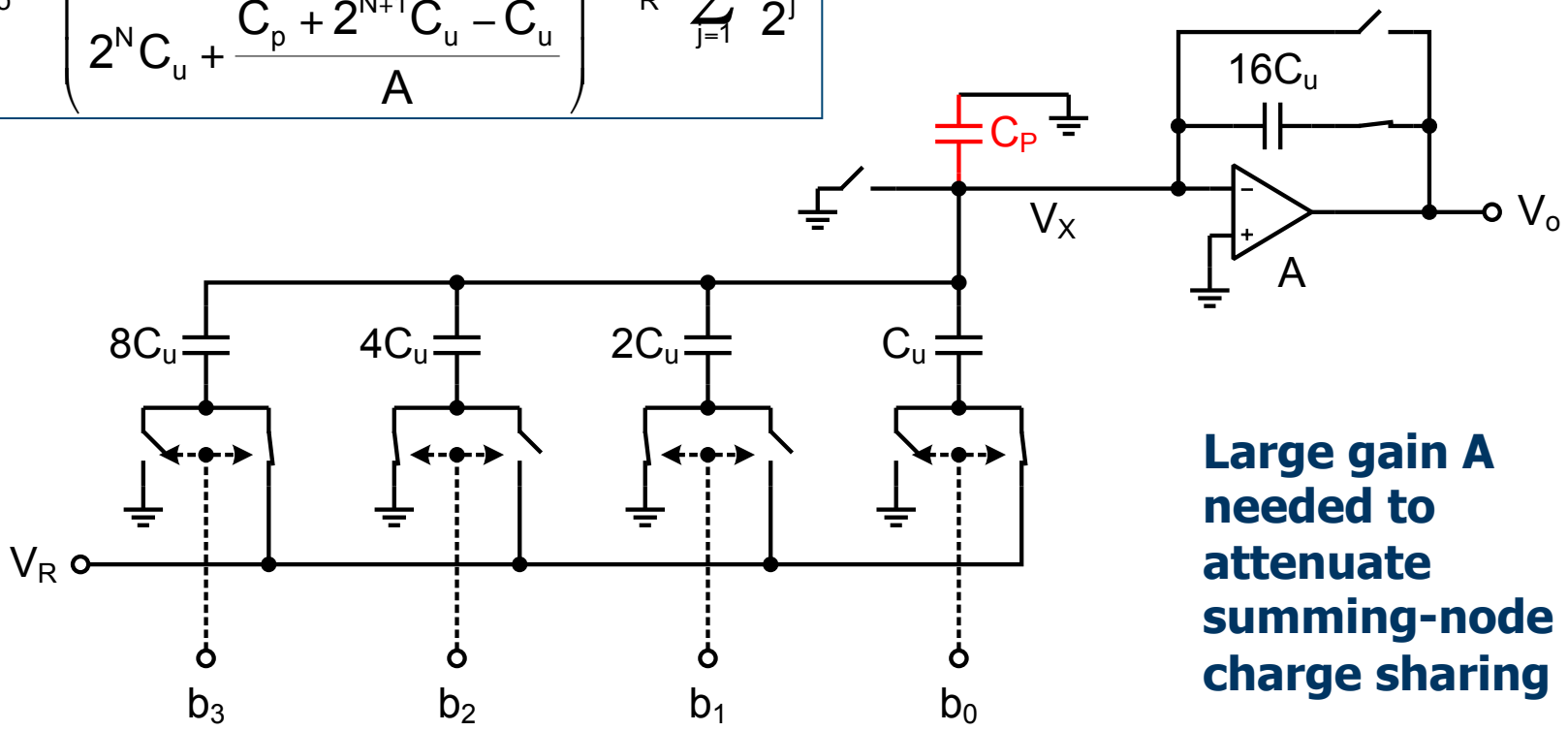
$$= \left(\frac{\sum_{j=1}^{N} b_{N-j} \cdot 2^{N-j} C_u}{C_p + 2^N C_u} \right) \cdot V_R$$

$$V_o = \left(\frac{2^N C_u}{C_p + 2^N C_u} \right) \cdot V_R \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$

- $C_p \rightarrow$ gain error (nonlinearity if C_p is nonlinear)
- INL and DNL limited by capacitor array mismatch

Stray-Insensitive C-DAC

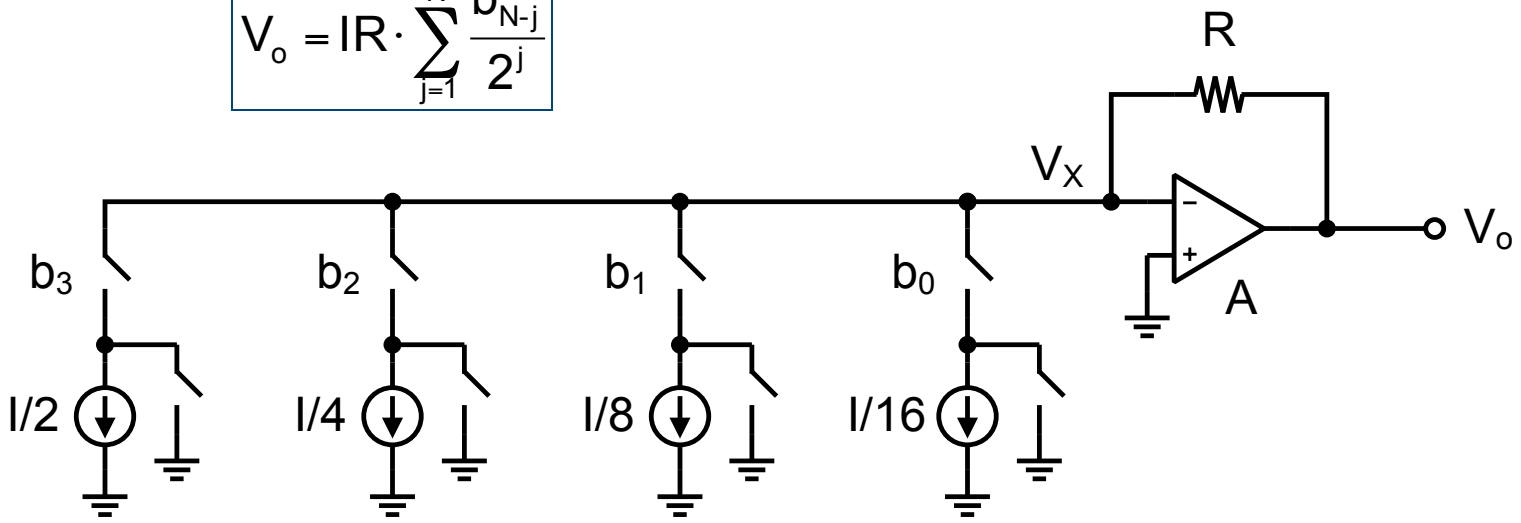
$$V_o = \left(\frac{2^N C_u}{2^N C_u + \frac{C_p + 2^{N+1} C_u - C_u}{A}} \right) \cdot V_R \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$



Large gain A needed to attenuate summing-node charge sharing

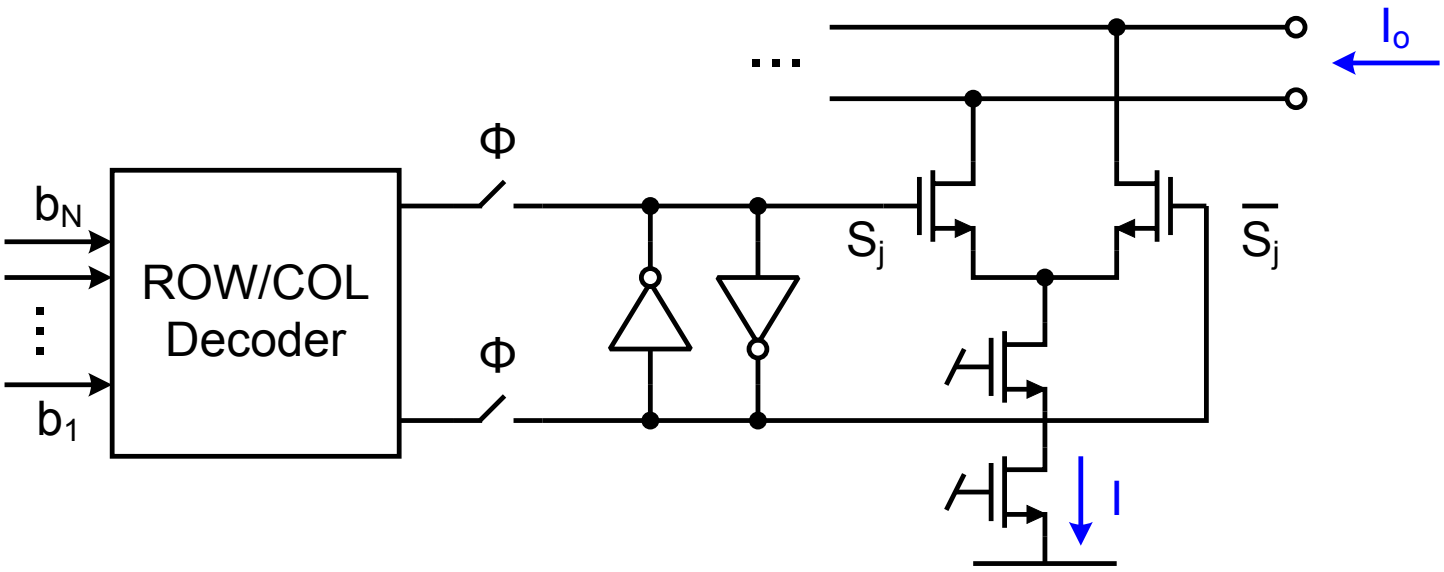
Binary-Weighted Current Steering DAC

$$V_o = IR \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$



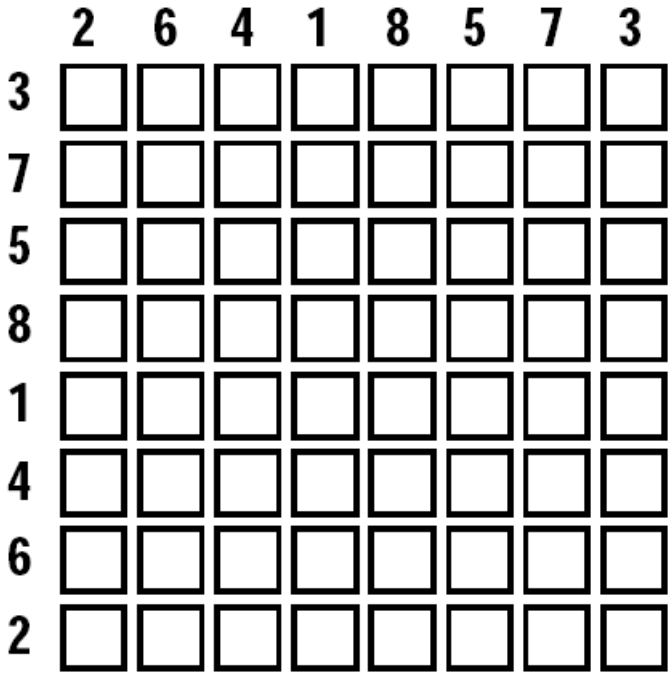
- Current switching is simple and fast.
- V_o depends on R_{out} of current sources without op-amp.
- INL and DNL depend on matching, not inherently monotonic.
- Large component spread (2^{N-1}:1)

Unit Current Cell

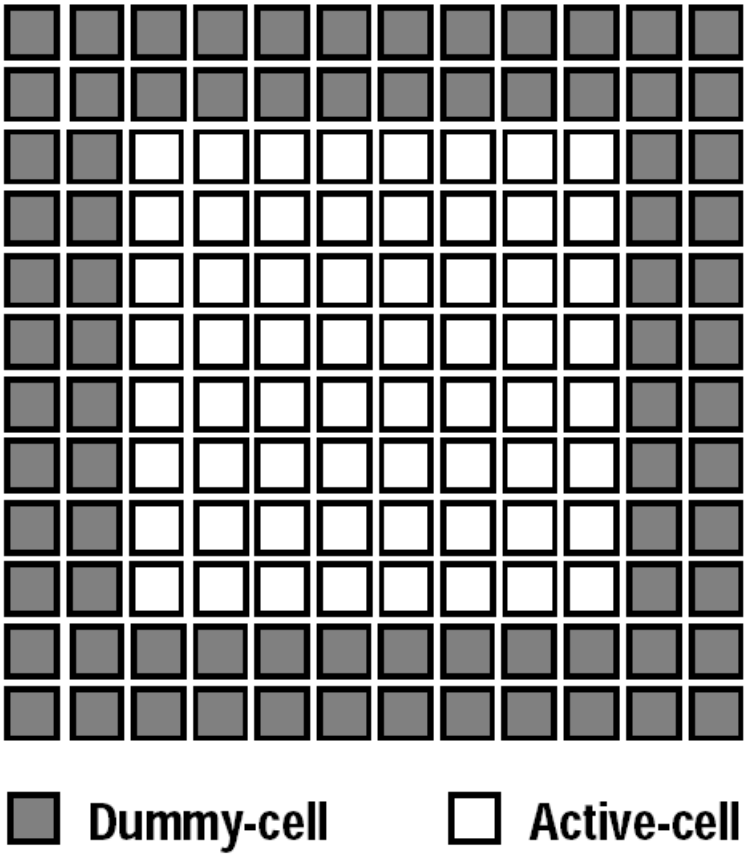


- 2^N current cells typically broken up into a ($2^{N/2}$ X $2^{N/2}$) matrix
- Current source cascoded to improve accuracy
- Coupled inverters improve synchronization of current switches.

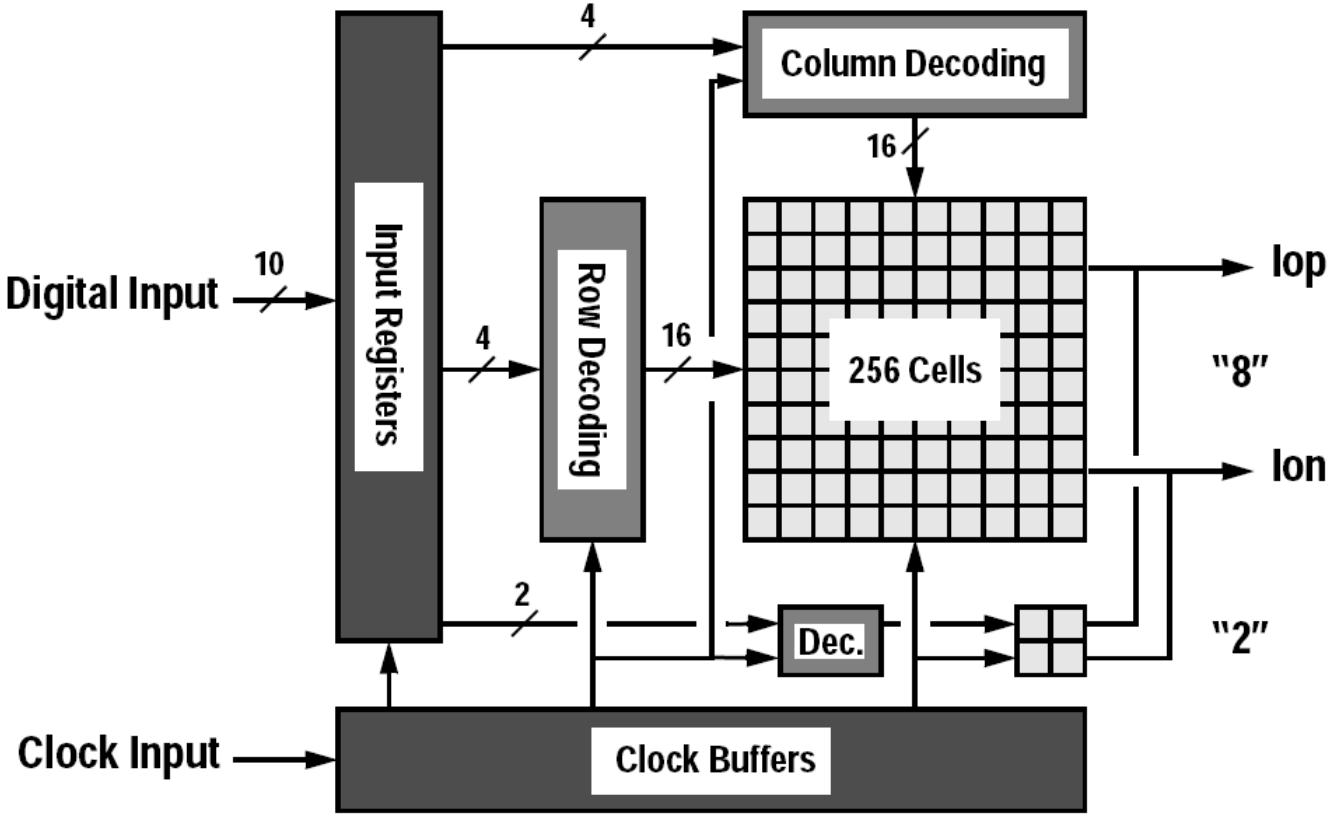
Randomization and Dummies



- Column and row randomization to improve INL



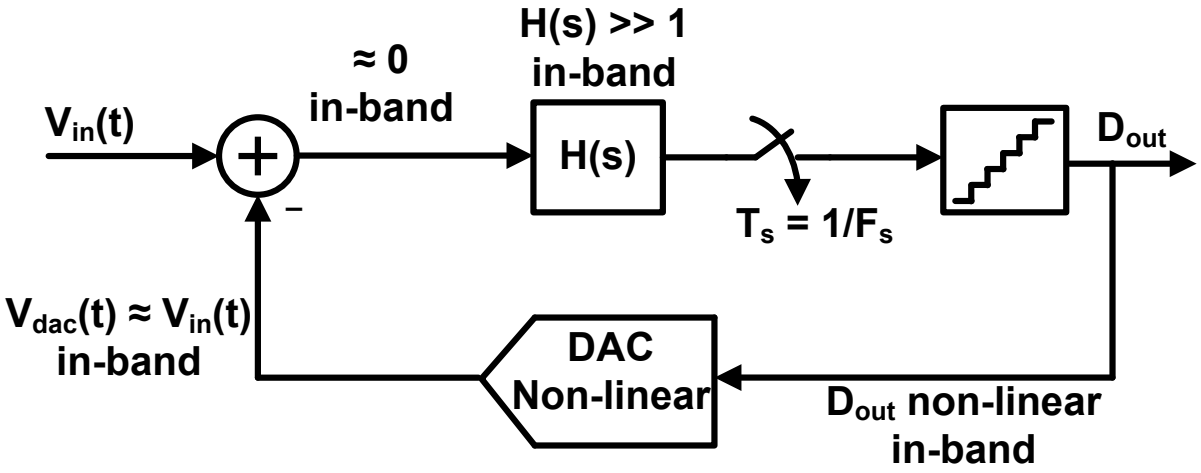
Example: "8+2" Segmented Current DAC



C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2," *IEEE Journal of Solid-State Circuits*, pp. 1948-1958, 1998.

DAC Non-idealities in CT ΔΣ ADCs - 2

Effects of DAC non-linearity



- Non-linearity caused due to mismatch between different output levels of DAC
  - Variation in feedback levels yields signal-dependent feedback charge error directly fed to the modulator input.
- Low resolution feedback DAC requires linearity better than overall modulator

DAC Calibration (Signal-to-Distortion Ratio)

This is a major (hot) research area in multi-bit sigma-delta modulators. Several alternatives have been reported; main trends are:

- Randomize the errors such that the non-linear errors are converted in noise instead of tones that degrades SNDR
  - **Dynamic element matching techniques**
  - **Pseudo Randomizers such as Rotators**
  - **Digital signal processors**
  - **Drawbacks?**
- Calibration
  - **By design using large overdrive voltages and large dimensions**
  - **Pre-calibration of current cells**
  - **Other options?**

Current Cell Design Considerations

Matching considerations

- Sizing of current source transistors

$$W^2 = \frac{1}{2K_p\left(\frac{\sigma_{\Delta I_d}}{I_d}\right)^2}\left[\frac{A_\beta^2}{(V_{gs}-V_t)^2}+\frac{4A_{V_t}^2}{(V_{gs}-V_t)^4}\right]$$

$$L^2 = \frac{K_p}{2I_d\left(\frac{\sigma_{\Delta I_d}}{I_d}\right)^2}\left[A_\beta^2(V_{gs}-V_t)^2+4A_{V_t}^2\right]$$

Output impedance

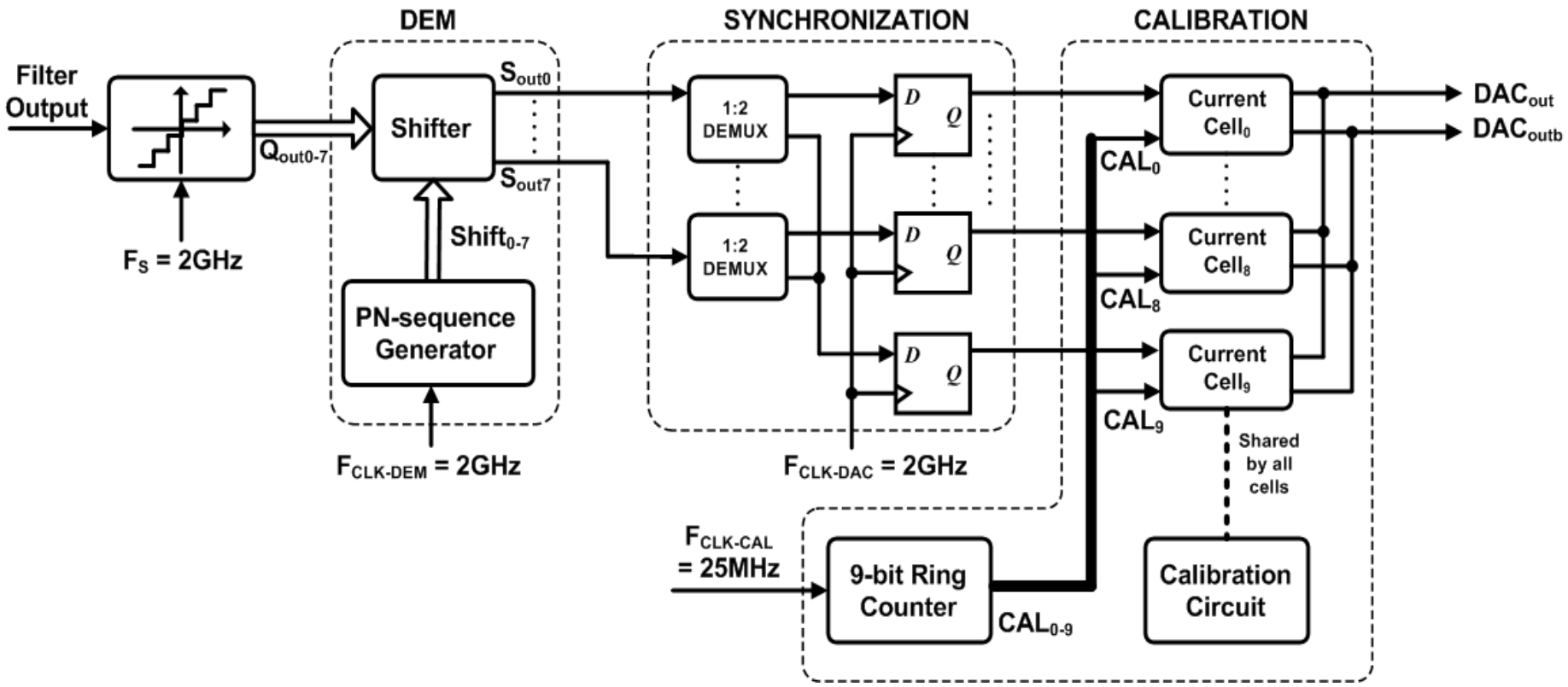
- Greater than 700kΩ over 100MHz signal bandwidth
  - Sufficient for 12-bits static (INL) and dynamic linearity (SFDR)

Trade-off

- Higher overdrive voltage provides better area efficiency at the expense of reduced output swing
- Larger area results in greater parasitic capacitances which limit the speed of operation

DACi	Unit current	(W/L), m=4	Total area, μm²
DAC1-coarse	610uA	203μ/3.84μ	7795
DAC1-fine	35uA	48μ/16μ	7680
DAC2	1.55mA	323μ/2.4μ	6976
DAC3	960uA	255μ/3μ	6885
DAC4	790uA	231μ/3.36μ	6985

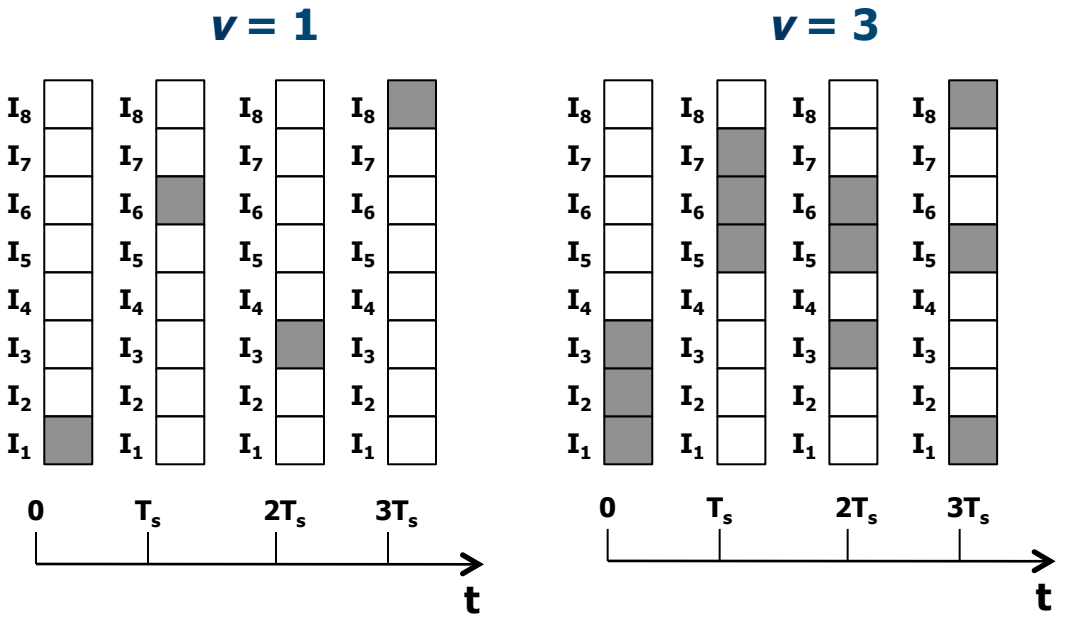
Multi-bit DAC Architecture: DEM

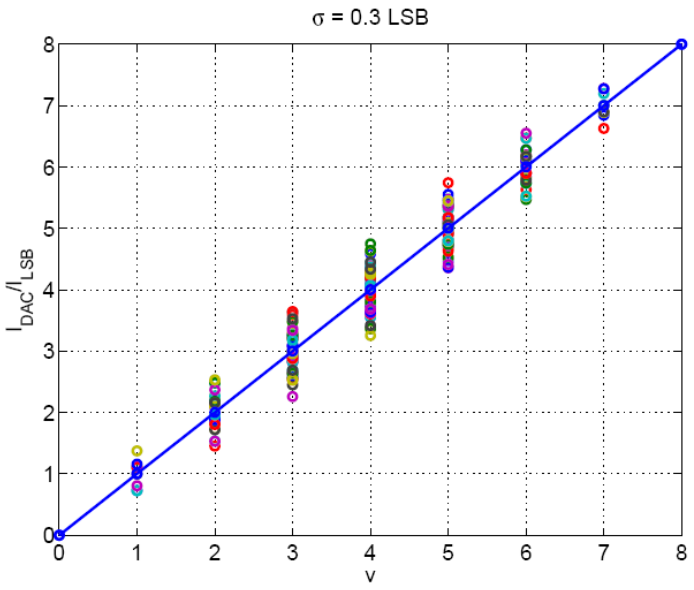


- Dynamic Element Matching (DEM), Self-calibration combined to achieve high linearity
- When DACi is under calibration, demultiplex Datai to dummy current cell

Dynamic Element Matching

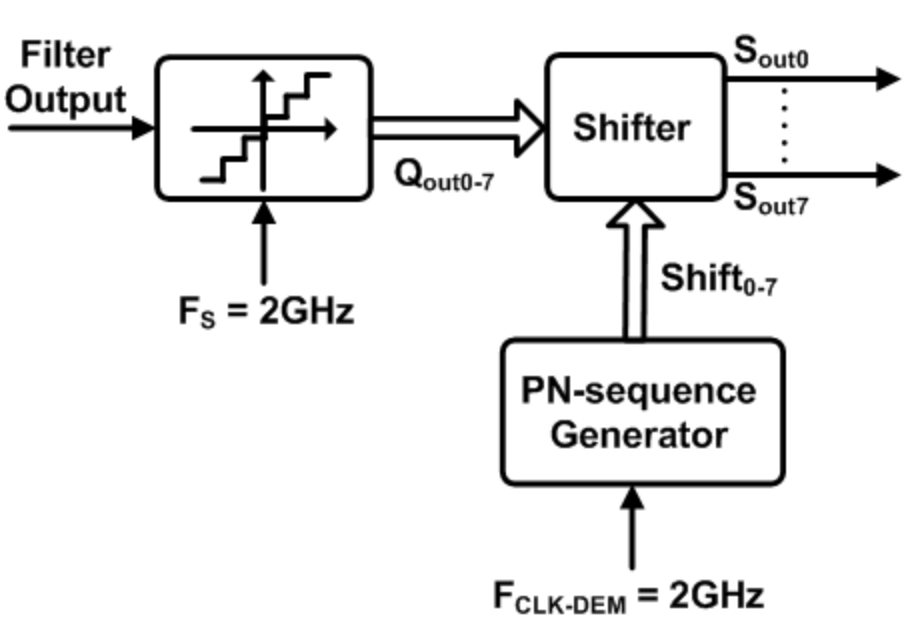
Representing DAC input *v* using a thermometer DAC

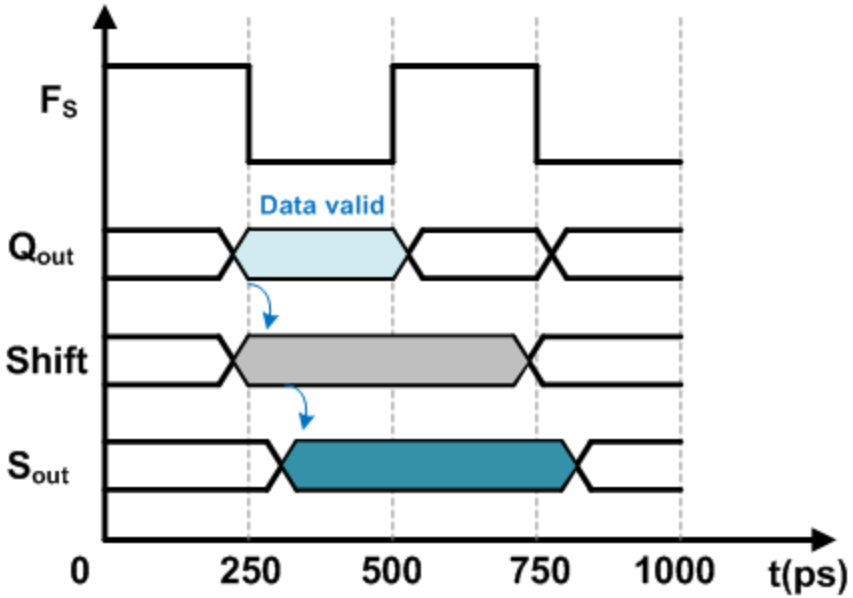




- *v* = 1 can be represented by any one of $I_{1\text{-}8}$
- Averaging all possible combinations produces the ideal output
- Use different combinations to represent a given code
- Errors are randomized

Implementation of DEM Scheme

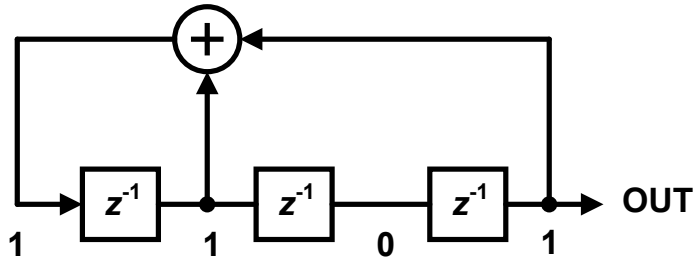




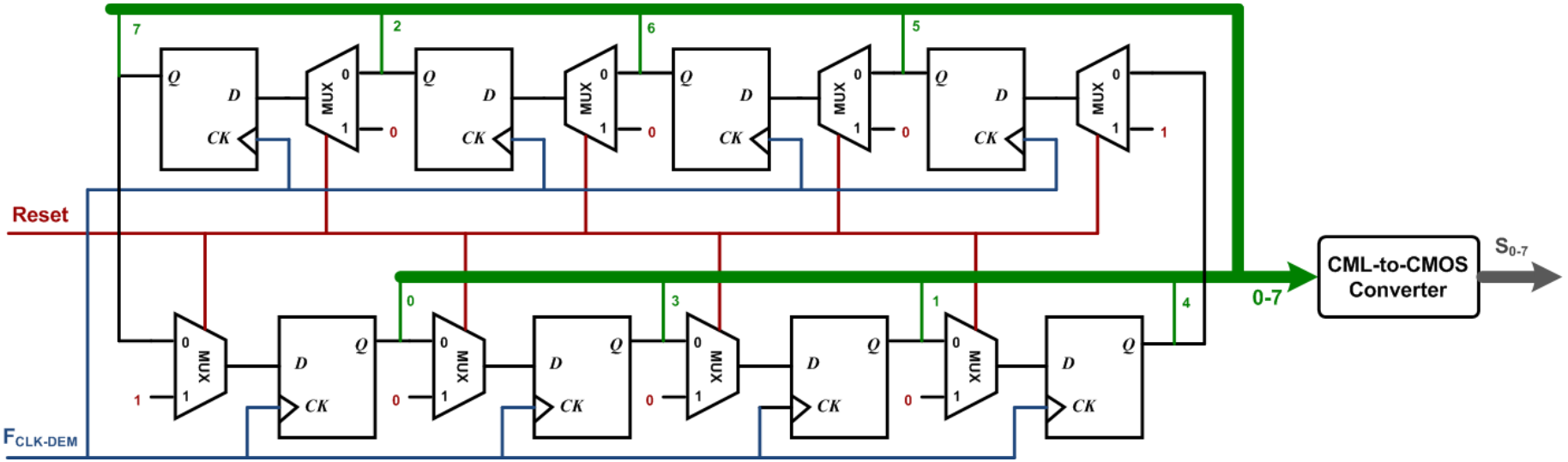
- Shifter performs a Rotate-right shift on its inputs
- PN-sequence generator indicates number of shifts
- DEM is operated at 2GHz to maximize randomization

PN-Sequence Generator

- Generates maximal length sequence based on 3rd-order primitive polynomial

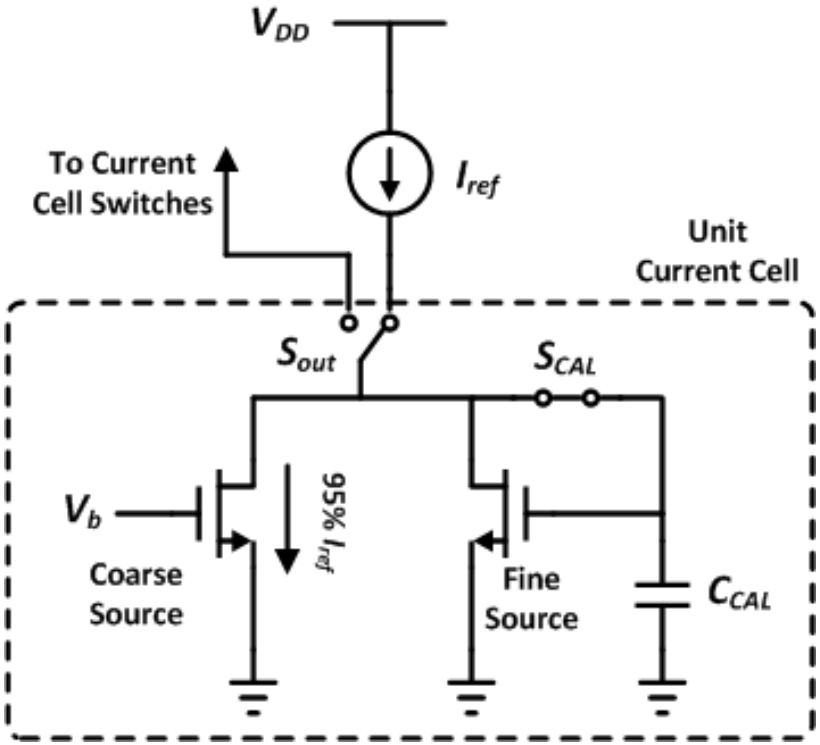


$P(x) = x^3 + x^2 + 1$ State: 1011



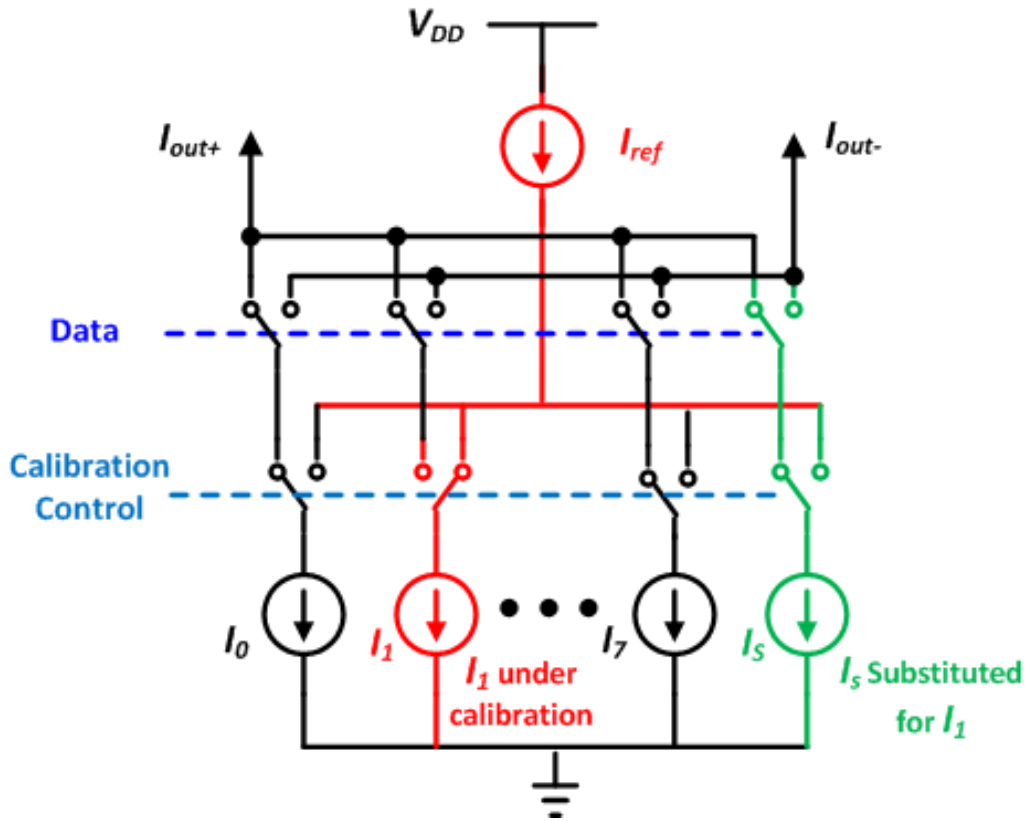
Analog Self-Calibration of Current Sources

Current Calibration Principle



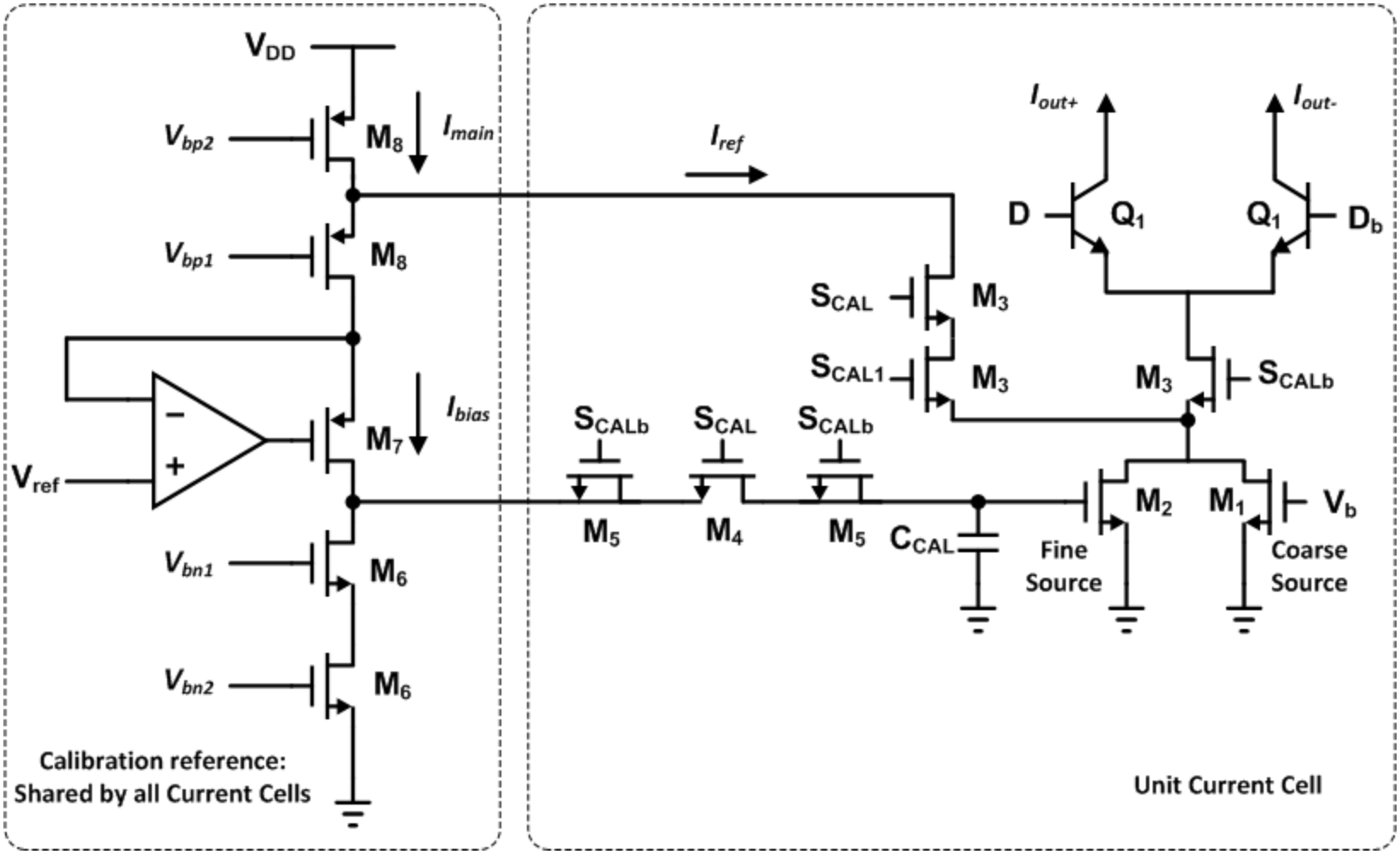
- At the end of a calibration cycle, C_{CAL} attains the correct V_{GS} required to generate I_{ref}

Multi-bit Calibrated DAC

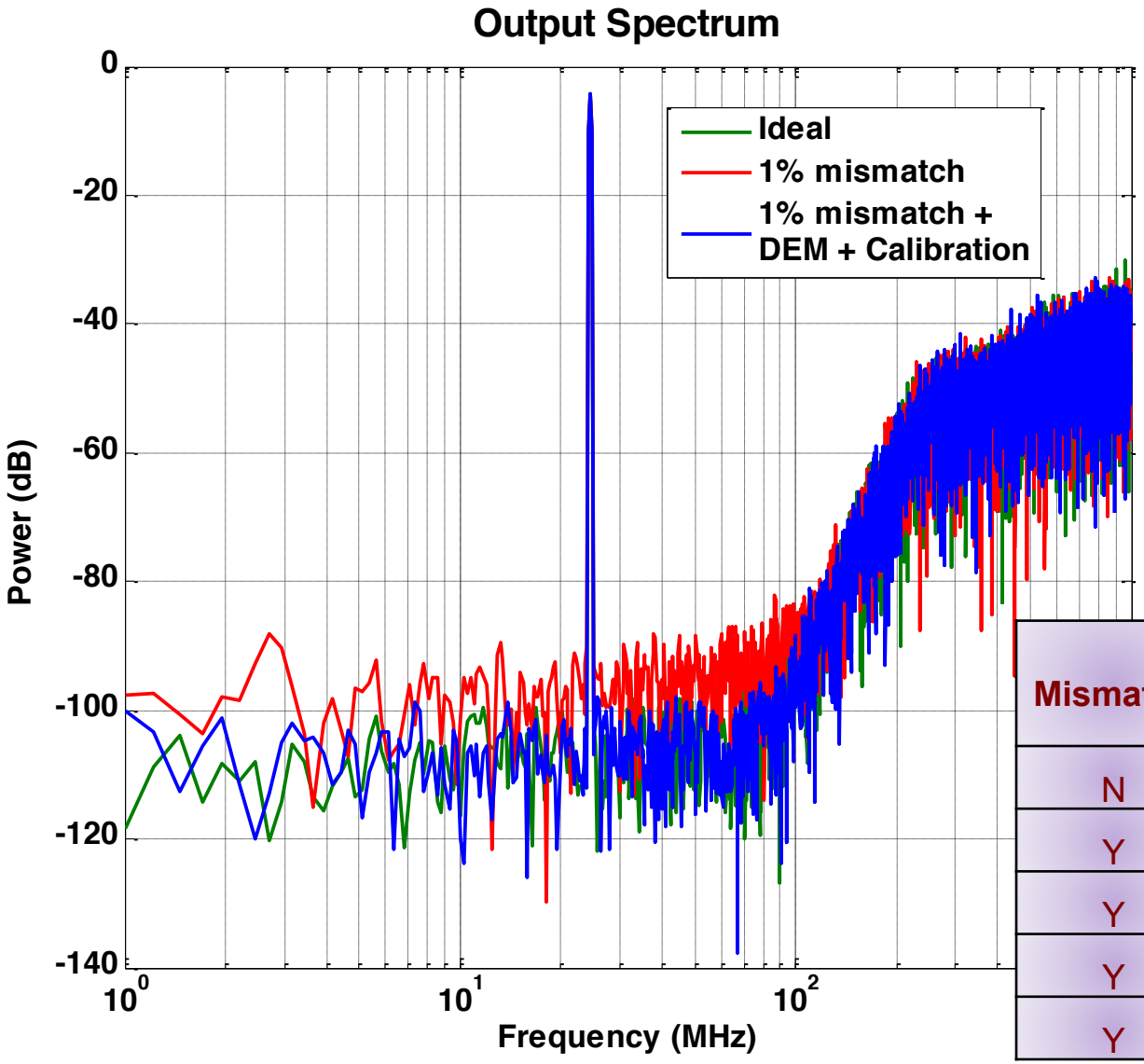


- Calibration control signals generated using a N-bit CMOS Ring Counter
- Extra dummy current cell used to implement continuous background calibration

Current Calibration Circuit



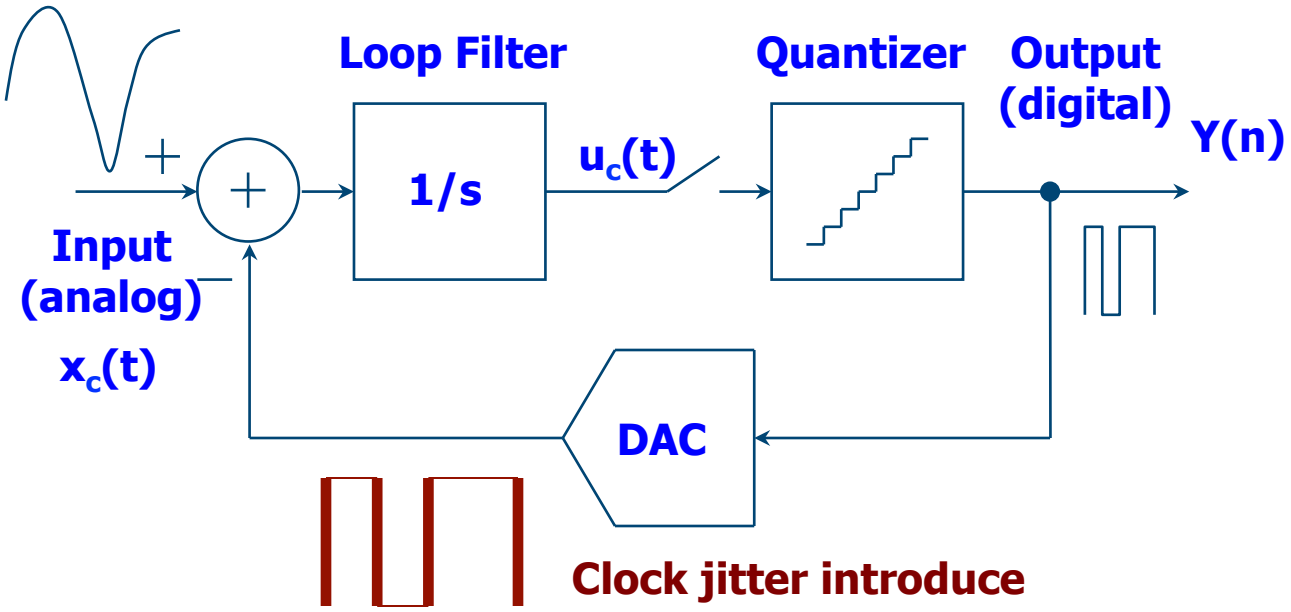
Simulation Results



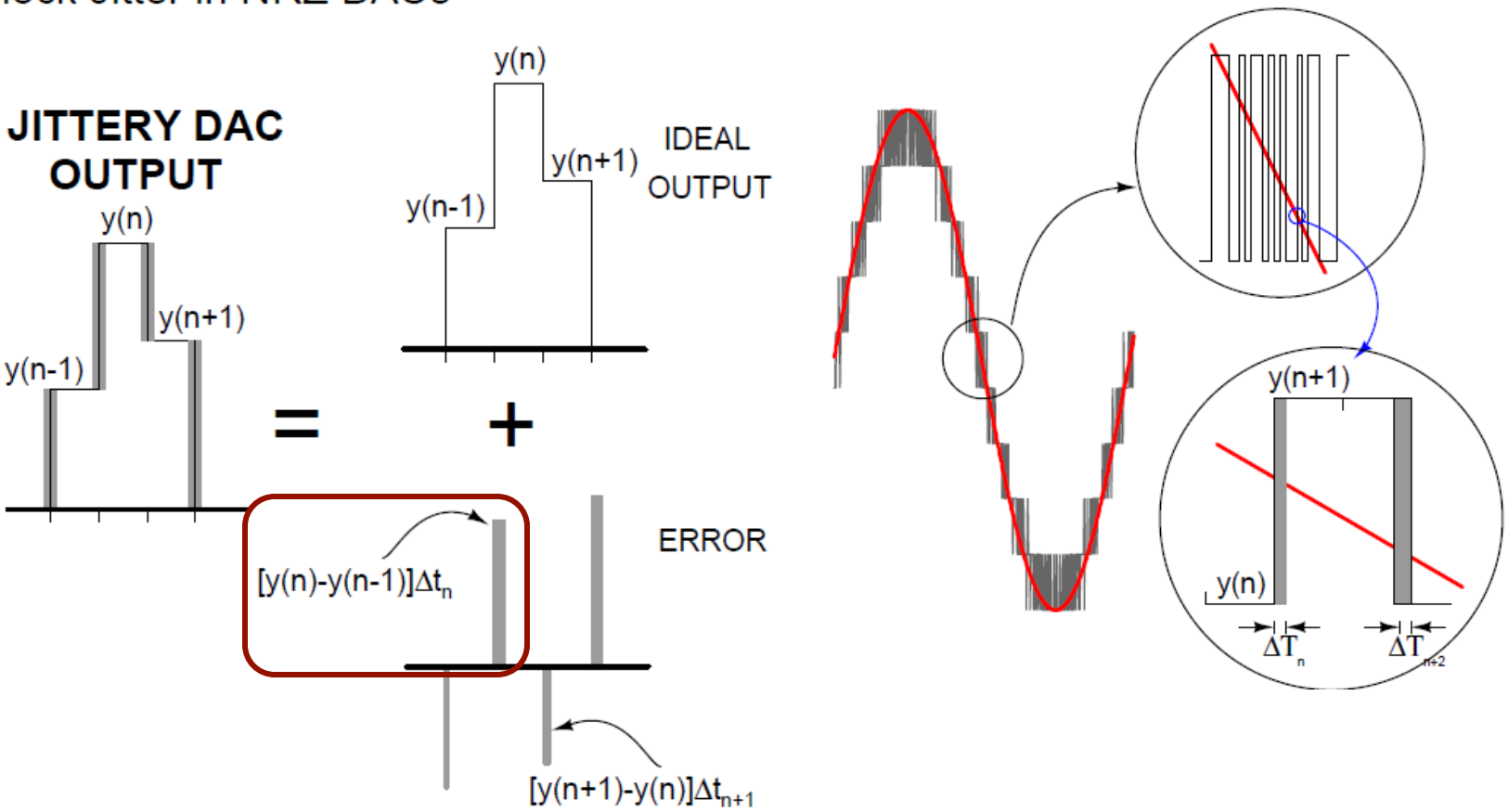
Mismatch	DEM	Self-calibration	SNR (dB)
N	N	N	73.8
Y	N	N	55
Y	Y	N	63.6
Y	N	Y	70
Y	Y	Y	72.7

Clock Jitter Sensitivity (SJNR)

- The effect of clock jitter is present at the input of the quantizer and DAC.
- Jitter induced noise at DAC output is processed according to the NTF, which is a serious problem for continuous-time sigma-delta modulators



Modeling Clock Jitter in NRZ DACs

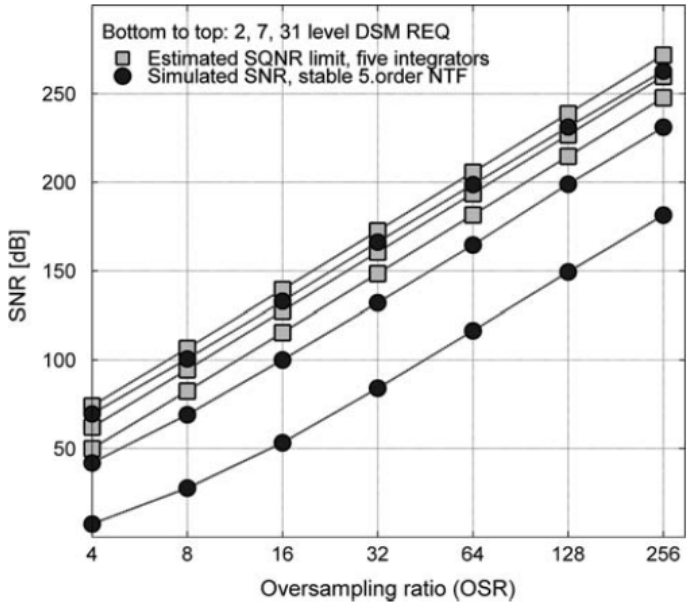


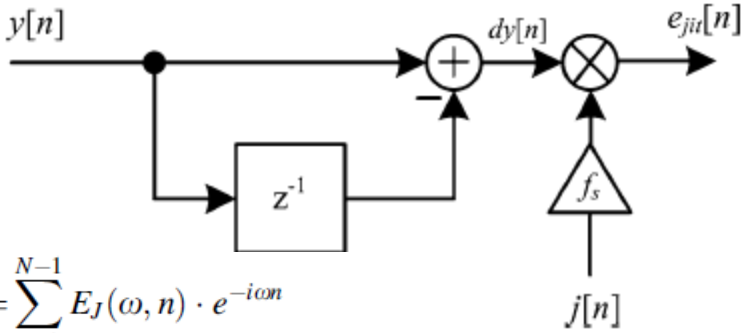
- Error depends on the height & number of transisitions in the DAC output waveform.
- NRZ DACs have a transition height $y(n) - y(n-1)$, one transistion every T_s.
- RZ DACs have a transition height $2y(n)$, two transistions every T_s.
- RZ DACs are MUCH more sensitive to clock jitter !

Analog Integr Circ Sig Process (2010) 62:179–192
DOI 10.1007/s10470-009-9337-3

Review and advances in delta-sigma DAC error estimation based on additive noise modelling

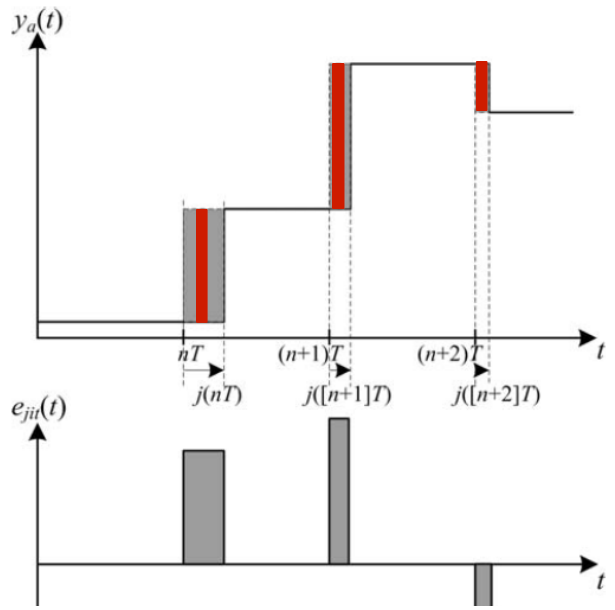
Ivar Løkken · Anders Vinje · Bjørnar Hernes ·
Trond S





$$E_{\text{jit}}(\omega) = \sum_{n=0}^{N-1} E_J(\omega, n) \cdot e^{-i\omega n}$$

$$\approx \frac{1}{T} \sum_{n=0}^{N-1} \left[(y_a[n] - y_a[n-1]) \cdot j[n] \right] \cdot e^{-i\omega n}$$



$$e_{jit}(t) = \sum_{n=0}^{N-1} \left[y_a(nT) - y_a((n-1)T) \cdot \frac{1}{T} \Pi_{j(nT)} \left(nT + \frac{j(nT)}{2} \right) \cdot \text{sign}(j(nT)) \right]. \quad (23)$$

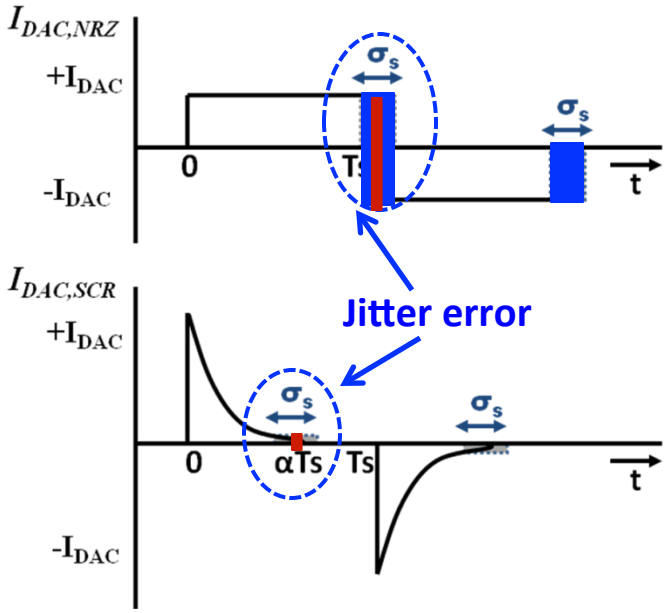
Considering *a single* error pulse on this form, for simplicity denoting its amplitude A and width J, taking the Fourier transform gives the spectrum:

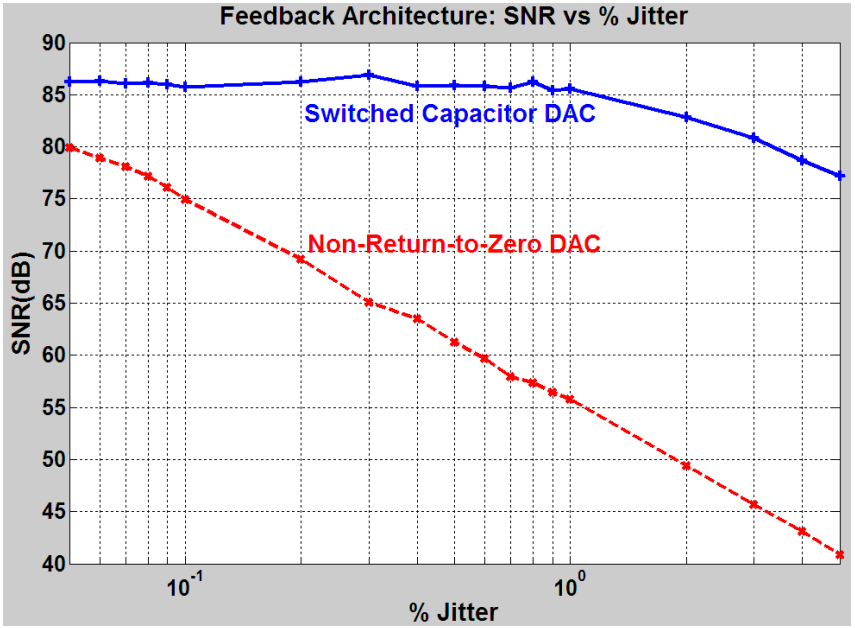
$$\mathrm{E}_J(f) = \int_{t=0}^{J} A \cdot e^{-\mathbf{i} \cdot 2\pi f \cdot t} \Big|_{J \geq 0} = - \int_{t=J}^{0} A \cdot e^{-\mathbf{i} \cdot 2\pi f \cdot t} \Big|_{J < 0}$$

$$= \frac{A \cdot \sin(2\pi J f)}{2\pi f} \cdot e^{-\mathbf{i} \cdot \pi J f}$$

$$= A \cdot J \cdot \sin c(Jf) \cdot e^{-\mathbf{i} \cdot \pi J f}. \quad (24)$$

Jitter Insensitivity of Switched-Capacitor DACs





- So far, SC-DAC is the most jitter tolerant approach
- Quite precise and may not require further calibration procedures

- **Drawbacks of the SC DAC**
- Peak current in the SC-DAC can be as high as 10 time IDAC used in the current mode DAC!
- Very demanding SR for the OPAMP: Power consumption
- Class AB OPAMP may help while dealing with this issue

Clock Jitter Sensitivity (SJNR)

Relationship between jitter and Phase noise: Lets consider a jittered signal

$$cos\left(\omega_o t + \varphi_n\right)$$

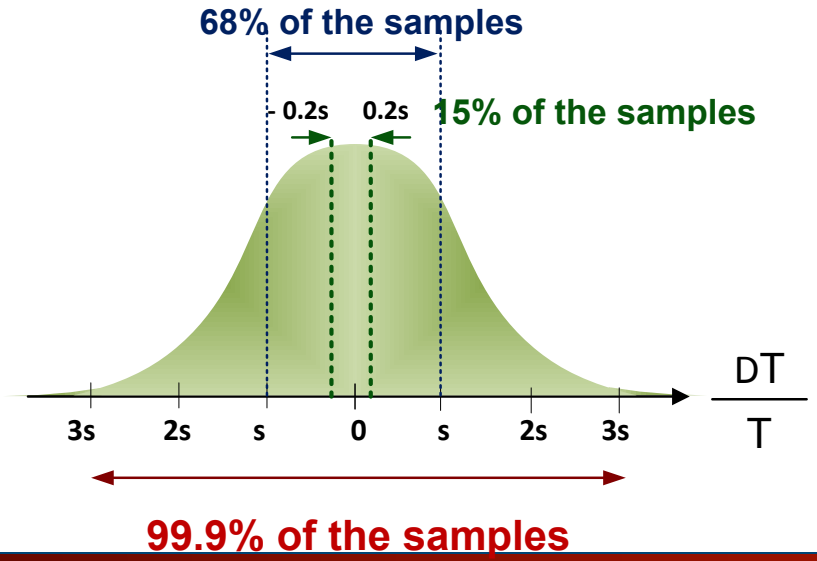
The phase of the noisy signal is then computed as

$$\omega_o\left(t + \frac{\varphi_n}{\omega_o}\right) = \omega_o\left(t + \frac{T * \varphi_n}{2\pi}\right)$$

Therefore, timing error can now be estimated as follows:

$$\frac{\Delta T}{T} = \frac{\varphi_n}{2\pi}$$

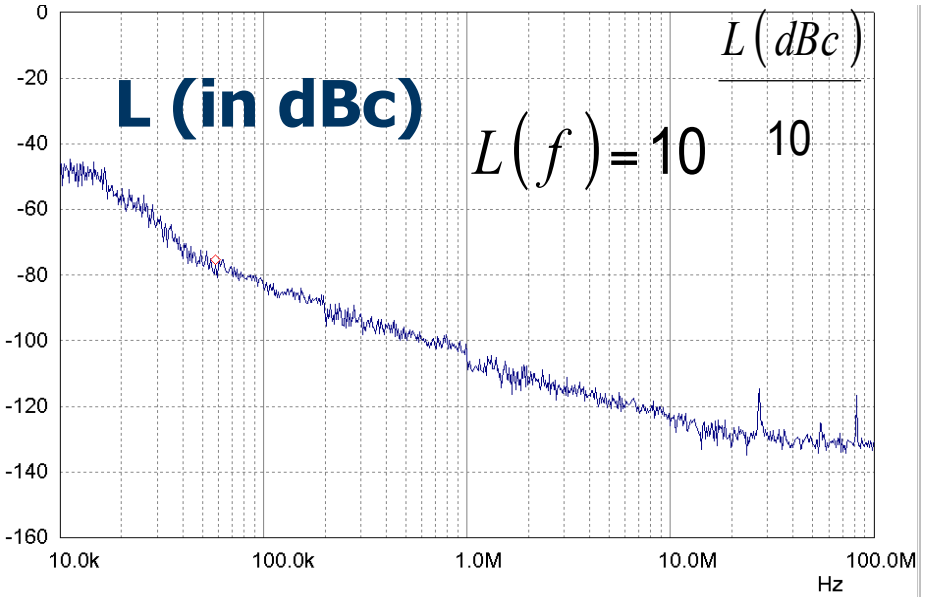
We can find the clock jitter variance employing the eye diagram, and making the following histogram



Clock Jitter Sensitivity (SJNR)

$$cos(\omega_o t + \varphi_n)$$

$$\left(\frac{\Delta T}{T}\right)^2 = \left(\frac{\varphi_n}{2\pi}\right)^2$$



Then

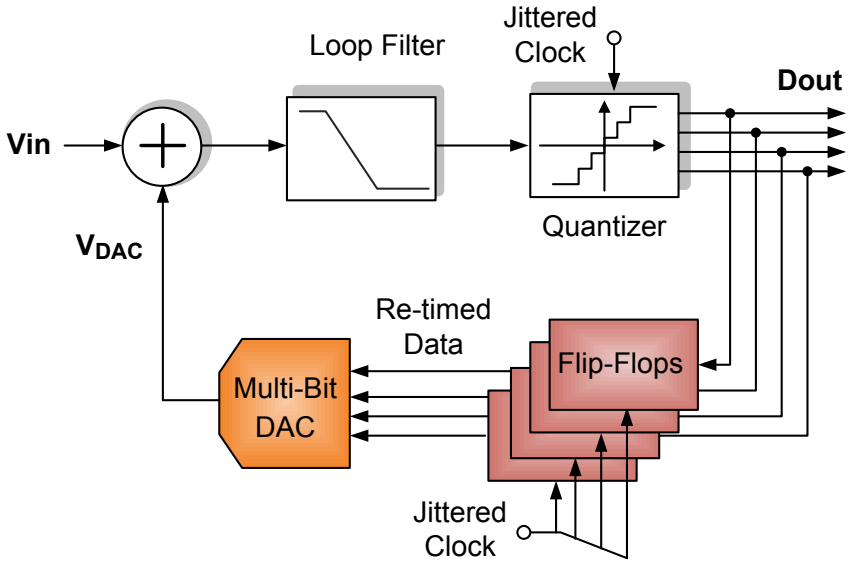
$$RMS\,J_{per} = \left(\frac{T}{2\pi}\right)\sqrt{\int_{-\infty}^{\infty}\phi_n{}^2(f)df}$$

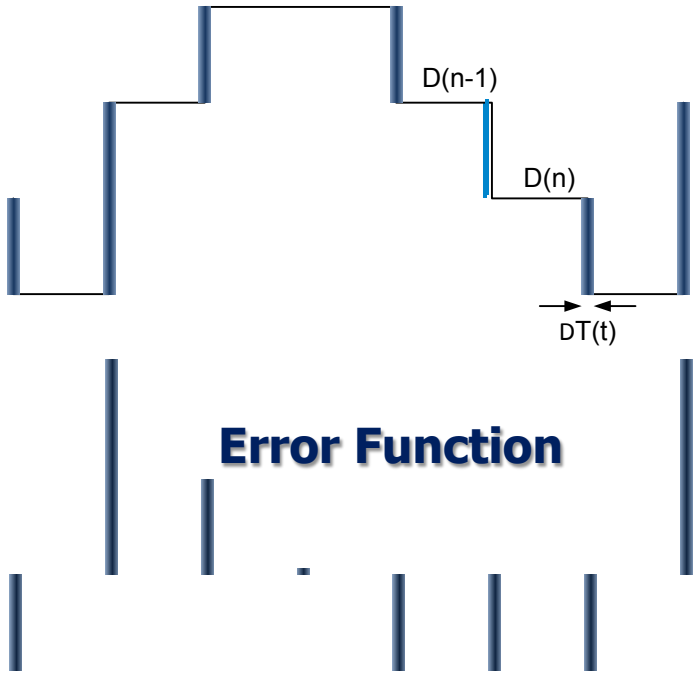
Timing spectrum is correlated with phase noise measured in the spectrum analyzer

RMS value of total jitter

$$RMS\,J_{per} = \left(\frac{T}{2\pi}\right)\sqrt{2\int_{0}^{\infty}(L(f))df}$$

Jitter Issues: High Clock Frequency





The DAC error due to clock jitter:

$$J_{error}(n) = \left(D_{out}(n) - D_{out}(n-1)\right)\left(\frac{\Delta T(t)}{T}\right)$$

In the frequency domain: Differential of Dout convolves with Jn(ω)

$$J_{error}(\omega) = \left[\left(1 - Z^{-1}\right)D_{out}(\omega)\right] \otimes J_n(\omega) = \left[\left(2\sin\left(\frac{\omega T_S}{2}\right)\right)D_{out}(\omega)\right] \otimes J_n(\omega)$$

In-band signal is shaped by $1 - Z^{-1}$, then it is not very critical
Out-of-Band quantization noise and blockers convolve with the clock jitter

Effect of clock jitter and Quantization noise on SNR

$$e_j(n) = \left(V_{out}(n) - V_{out}(n-1)\right)\frac{\Delta t(n)}{T}$$

then

$$E_j(Z) = \left\{\left(1 - Z^{-1}\right)\left(V_{out}(Z)\right)\right\} \otimes \left(J(Z)\right)$$

Or

$$E_j(Z) = \left\{\left(1 - Z^{-1}\right)\left(STF(Z) * V_{in}(Z) + NTF(Z) V_q(Z)\right)\right\} \otimes \left(J(Z)\right)$$

Therefore

$$E_j(Z) = \left\{\left(1 - Z^{-1}\right) STF * V_{in}(Z)\right\} \otimes J(Z) +$$

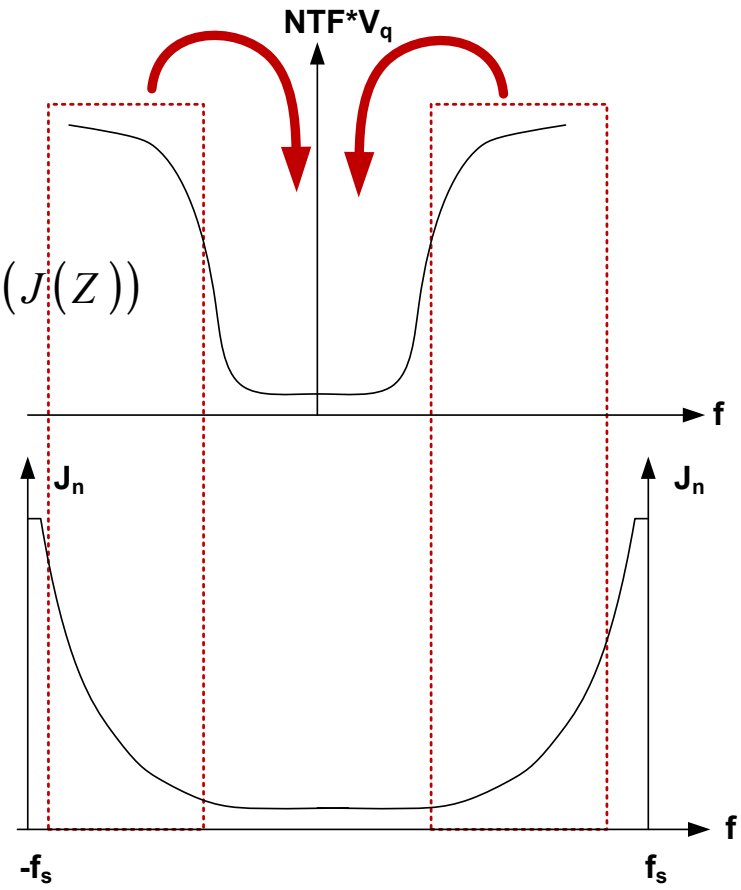
$$+ \left\{\left(1 - Z^{-1}\right) NTF * V_q(Z)\right\} \otimes \left(J(Z)\right)$$

$$\left|1 - Z^{-1}\right| = 2\left|sin\left(\frac{\omega T_s}{2}\right)\right|$$

$$P_{j,S} \cong 2\int_0^{1/2OSR} \left|E_j(Z)\right|^2 d\theta$$

$$P_{j,Q} \cong 2\int_0^{1/2OSR} \left|\left(1 - Z^{-1}\right)\left\{\left(NTF(Z) V_q(Z)\right) \otimes \left(J(Z)\right)\right\}\right|^2 d\theta$$

Quantization noise



Clock Phase Noise

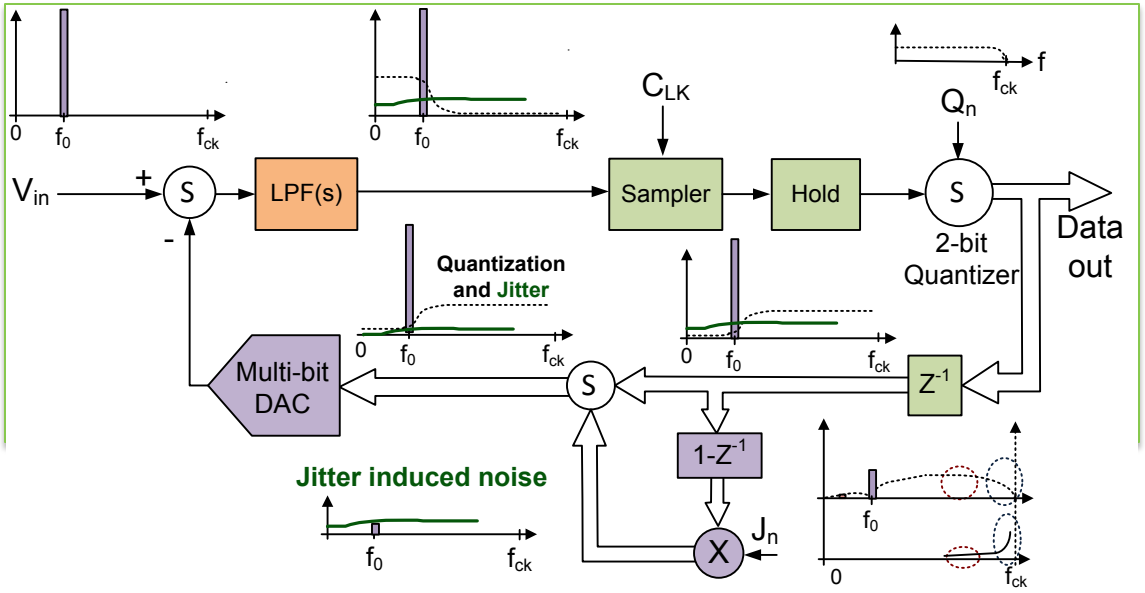
SJNR is function of the convolution of NTF and J(Z)

Continuous-Time BP-ΣΔ ADC: Jitter effects

$$SJNR_{NRZ} \cong 60\,dB \Rightarrow$$

$$\left(\frac{OSR * P_{in}}{4}\right)\left(\frac{T_s}{\sigma_j}\right)^2 > 1$$

$$\sigma_j \approx< 10^{-3} T_s$$



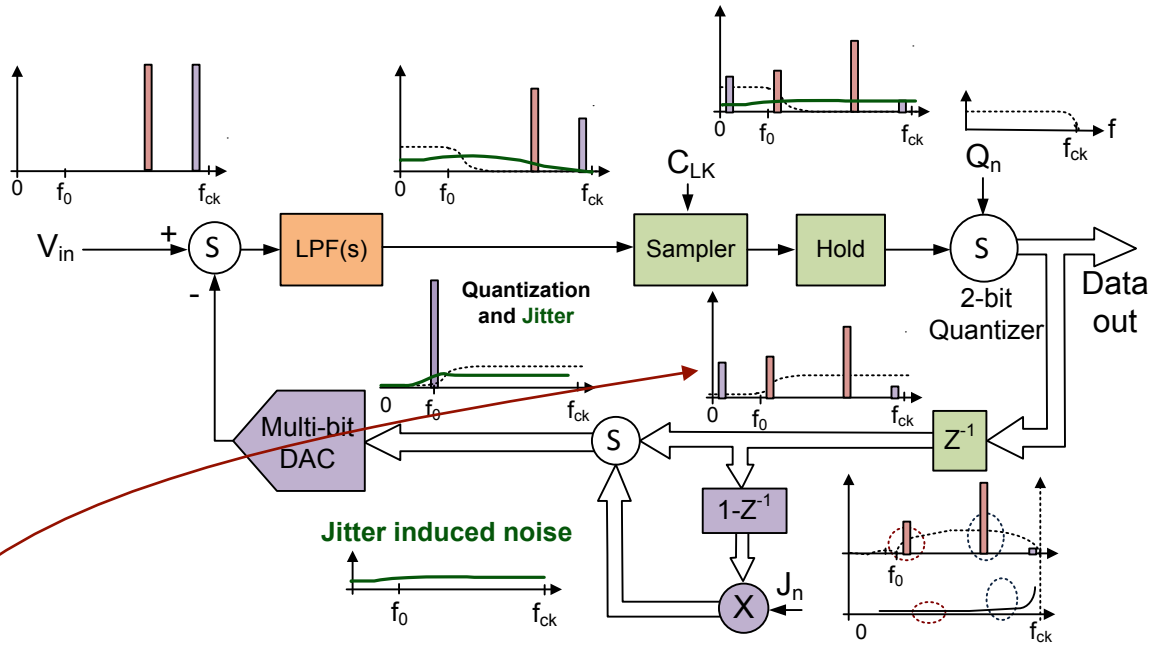
In absence of blockers, assuming white jitter, the jitter induced noise has been usually approximated as:

$$SJNR_{NRZ} \cong 10\log_{10}\left(\frac{P_{in}}{\int_{BW}\left(J_n^2 \otimes \left(1-Z^{-1}\right)^2 P_{Quantization}\right)df}\right) = 10\log_{10}\left(\frac{OSR * P_{in} * \mathrm{sinc}^2\left(\frac{\omega_o T_s}{2}\right)}{4\left(\frac{\sigma_j}{T_s}\right)^2}\right)$$

Continuous-Time ΣΔ ADC: Jitter & Blockers

RF clock filtering is an effective method to partially overcome this issue!

J Silva et.al., SRC report Dec 2010



- **High frequency blockers convolve with Jn and are folded back in band.**
- **Considering Pblocker and Pquantization**

$$SJNR \cong 10\log_{10}\left(\frac{P_{in}}{\int_{BW}\left(J_n^{\,2}\otimes\left(1-Z^{-1}\right)^2 P_{Quantization}+J_n^{\,2}\otimes\left(1-Z^{-1}\right)^2 P_{Blocker}\right)df}\right)$$

$$= SJNR_{no\ Blocker} - 10\log_{10}\left(1+\frac{\int_{BW}\left(J_n^{\,2}\otimes\left(1-Z^{-1}\right)^2 P_{Blocker}\right)df}{\int_{BW}\left(J_n^{\,2}\otimes\left(1-Z^{-1}\right)^2 P_{Quantization}\right)df}\right)$$

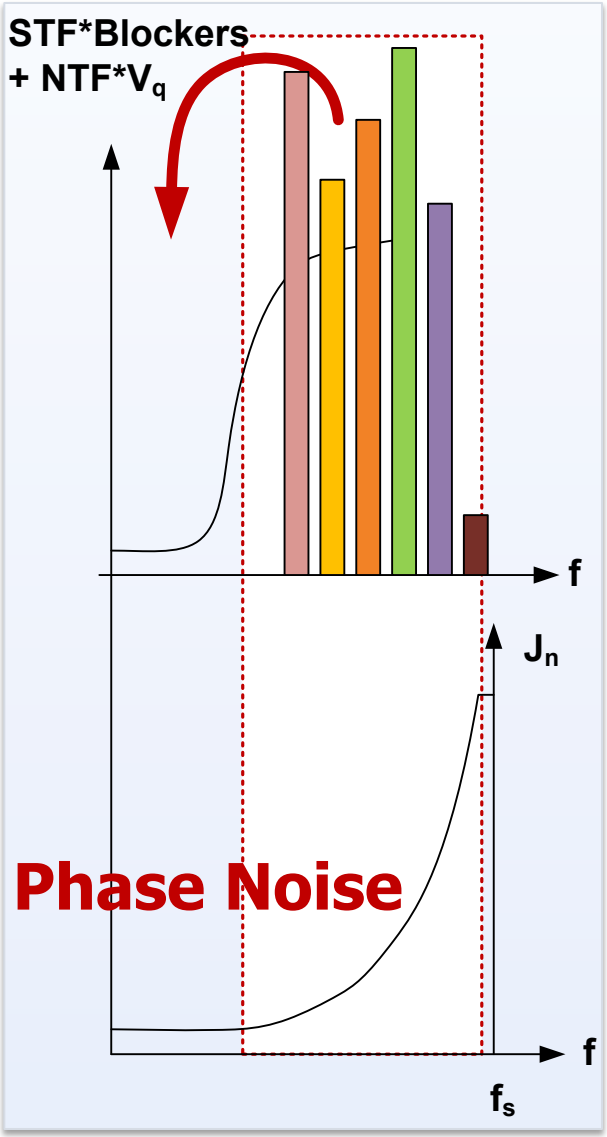
Effect of clock jitter on SNR: Quantization noise +Blockers

$$e_j(n) = \left(V_{out}(n) - V_{out}(n-1)\right)\frac{\Delta t(n)}{T}$$

$$E_j(Z) = \left\{\left(1 - Z^{-1}\right)\left(V_{out}(Z)\right)\right\} \otimes \left(J(Z)\right)$$

$$E_j(Z) = \left\{\left(1 - Z^{-1}\right) STF * V_{in}(Z)\right\} \otimes J(Z) +$$
$$+ \left\{\left(1 - Z^{-1}\right) NTF * V_q(Z)\right\} \otimes \left(J(Z)\right)$$

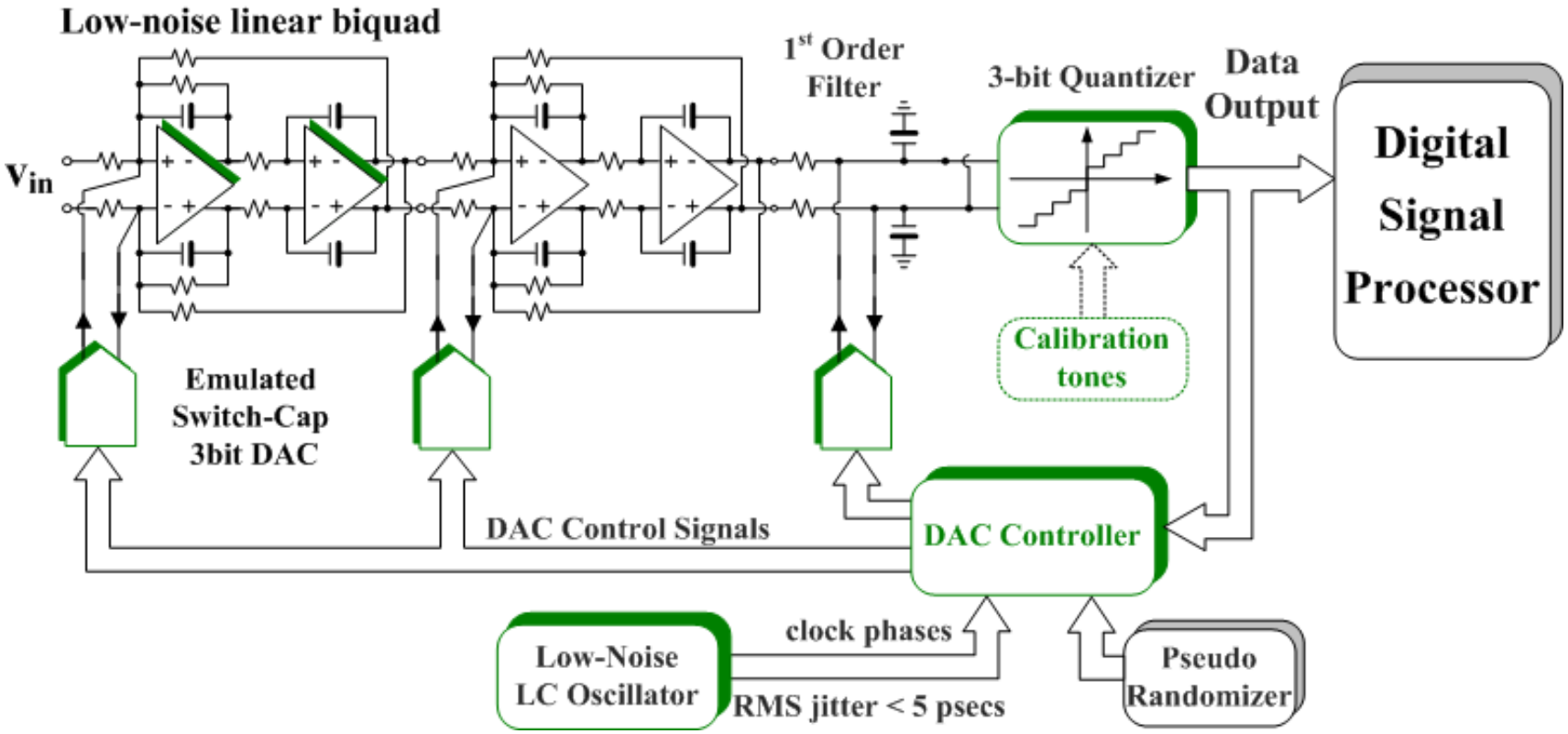
$$P_{j,S} \cong 2\int_0^{1/2OSR} \left|E_j(Z)\right|^2 d\theta$$



Clock Phase Noise

$$P_{j-inband} \cong 2\int_0^{1/2\,OSR} \left|\left(1 - Z^{-1}\right)\left\{\left(STF(\omega)V_{Blockers}(\omega) + NTF(\omega)V_q(\omega)\right) \otimes \left(J(\omega)\right)\right\}\right|^2 d(\omega T_s)$$

A Jitter-Tolerant 12-Bit ΣΔ Modulator

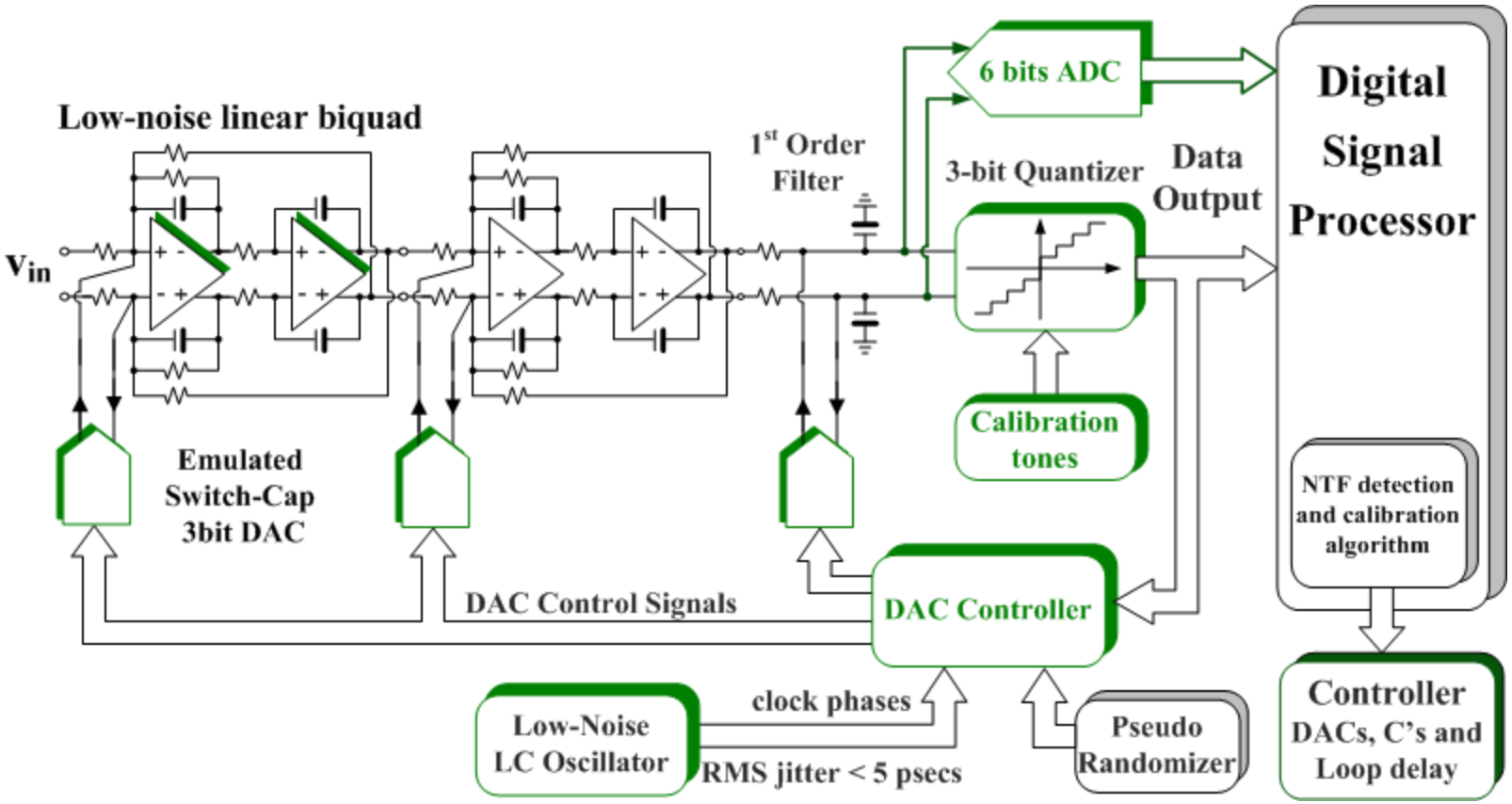


SNR>12 bits, Power < 20mW, BW= 20 MHz, OSR=10

Challenges:

- **Calibration procedure:** NTF will be optimized through the calibration tones
- **Low-sensitivity to clock jitter:** Emulated switched-capacitor DACs
- **Robust against blockers:** Feedback based topology
- **Extremely linear filters:** IM3 @ 20 MHz < 75 dB Full scale

A Jitter-Tolerant 14-Bit ΣΔ Modulator



Main goal: ENOB≥14 bits, SQNR >16 bits, Total power < 50mW, BW= 20 MHz, OSR=10

- **Fully calibrated modulator**
- **Low-sensitivity to clock jitter: clock jitter as high as 10psecs (RMS)**
- **Robust against blockers: 5th-order feedback-based topology**

Design Example: 12-bit, 20MHz CT ΔΣ ADC

System-level Design Considerations

$$SQNR(dB) = 6.02N + 1.76 + (2L+1)10\log_{10} OSR - 10\log_{10}\frac{\pi^{2L}}{2L+1}$$

Design Trade-offs:

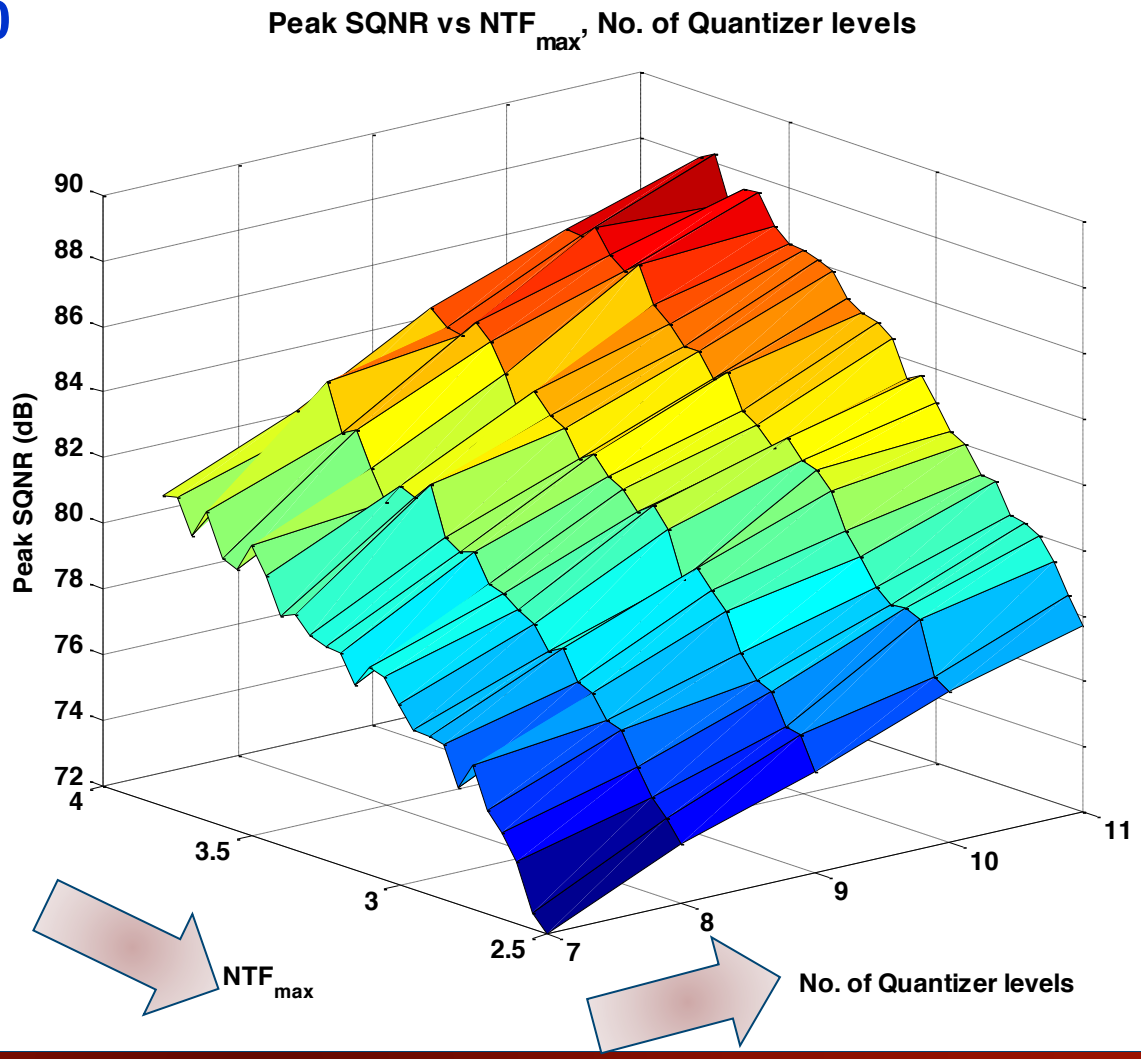
Order of modulator, L	L↑	▪ Reduced stability, ▪ Less robust to PVT variations
Oversampling ratio, OSR	OSR↑	Limited by f_T of technology
Quantizer resolution, N	N↑	▪ **Improved stability** ▪ **Improved clock jitter tolerance** ▪ More power, area in quantizer ▪ **Limited by non-linearity of feedback DAC**
Max. NTF gain, NTF_{max}	NTF_{max} ↑	▪ Reduced stability ▪ More sensitive to clock jitter
Max. stable amplitude, MSA	MSA↑	L↓, N↑, NTF_{max}↓

System-level Optimization

- Order of modulator (L), and OSR set by target SQNR (~80dB) and settling time requirements on 1st integrator stage

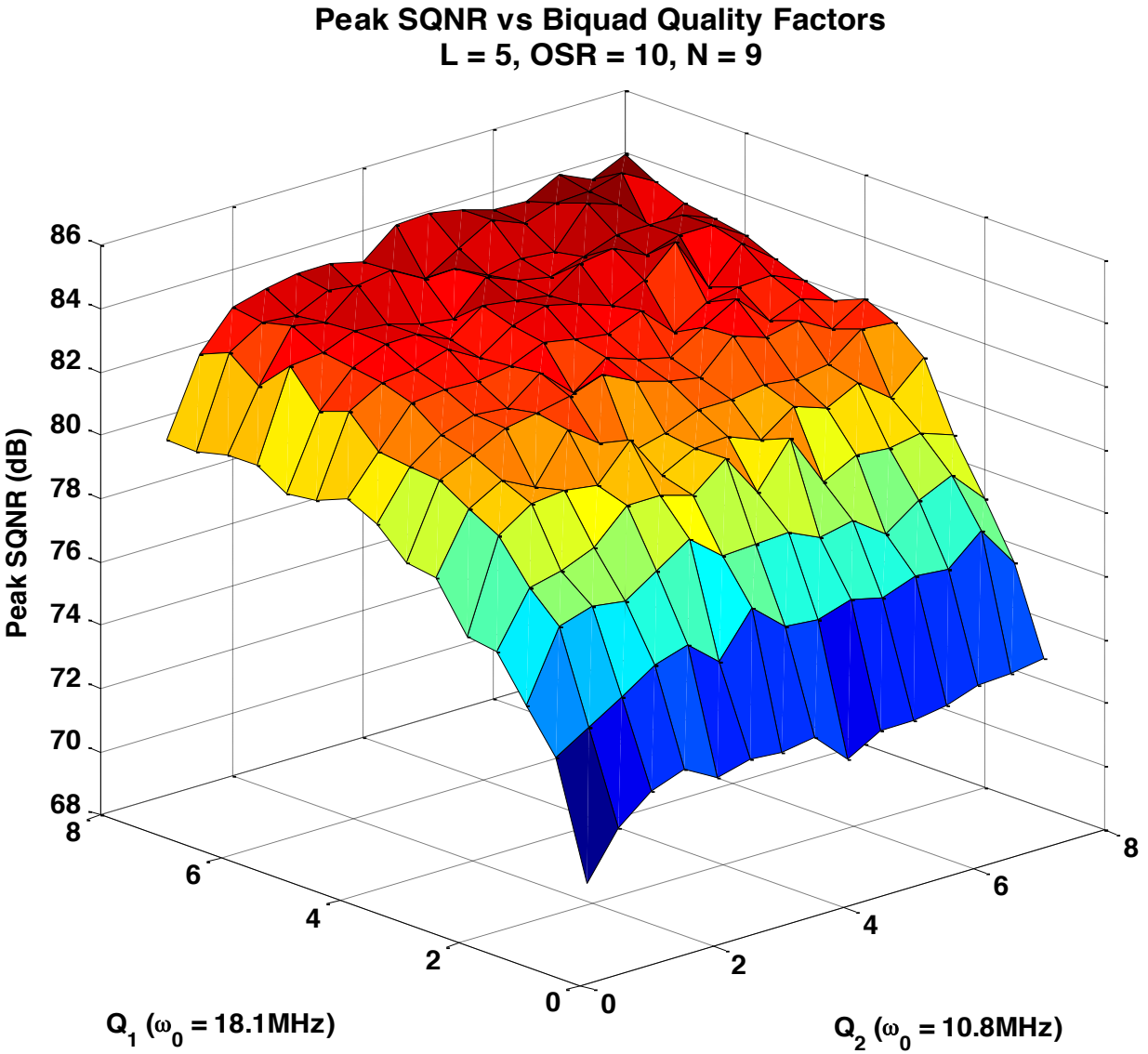
L = 5, OSR = 10

- Order of modulator (L), and OSR set by target SQNR (~80dB)
  - L = 5, OSR = 10
  - A number of tradeoffs involved
- **Just picking values is not a good approach**
- **EDUCATED GUESSES!**



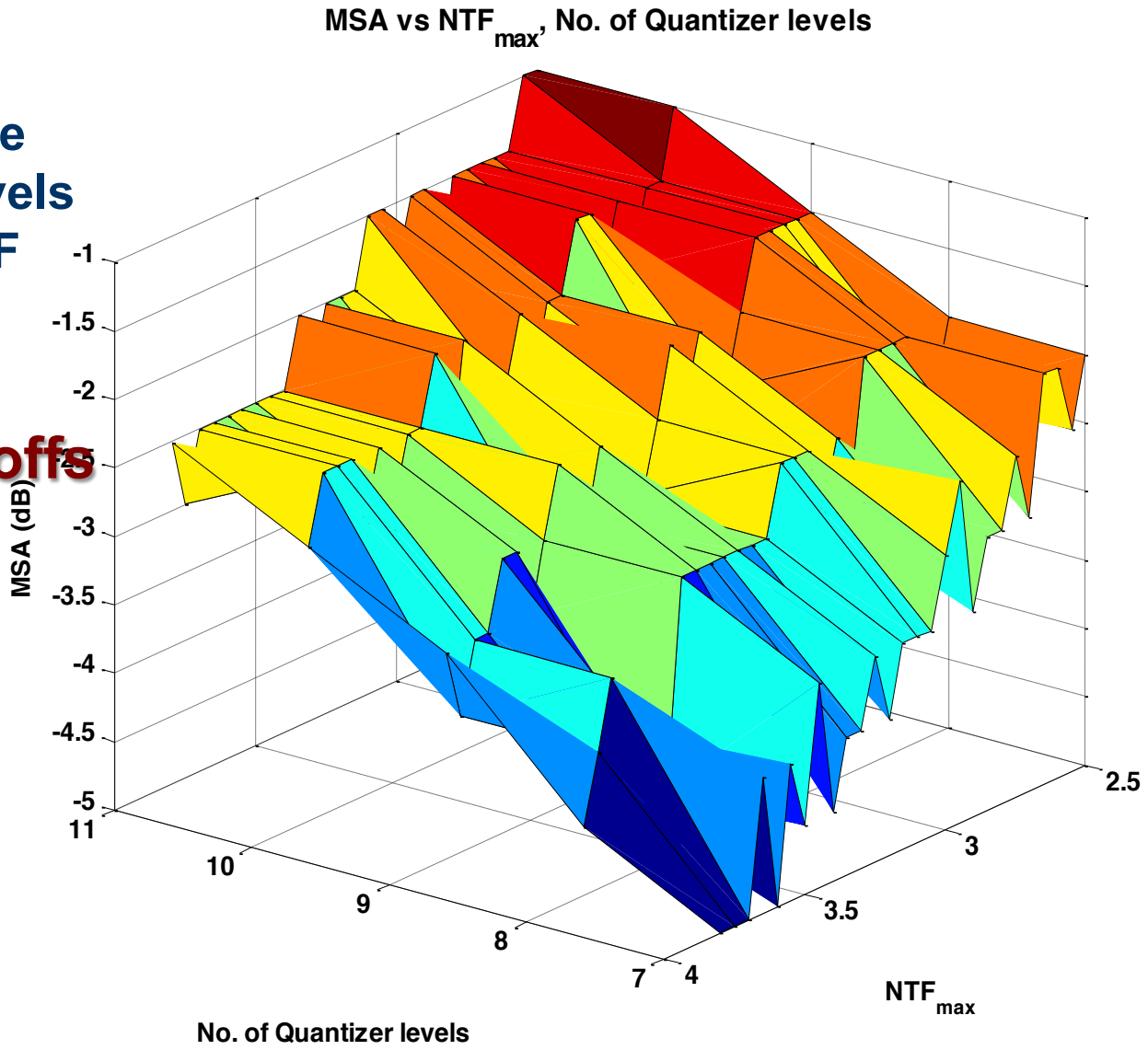
System-level Optimization

- Order of modulator (L), and OSR set by target SQNR (~80dB)
- High-Q filters give you better SQNR (due to picking in the gain; better in-band noise)
- **Implications on filter's signal swing and out-of-band noise?**



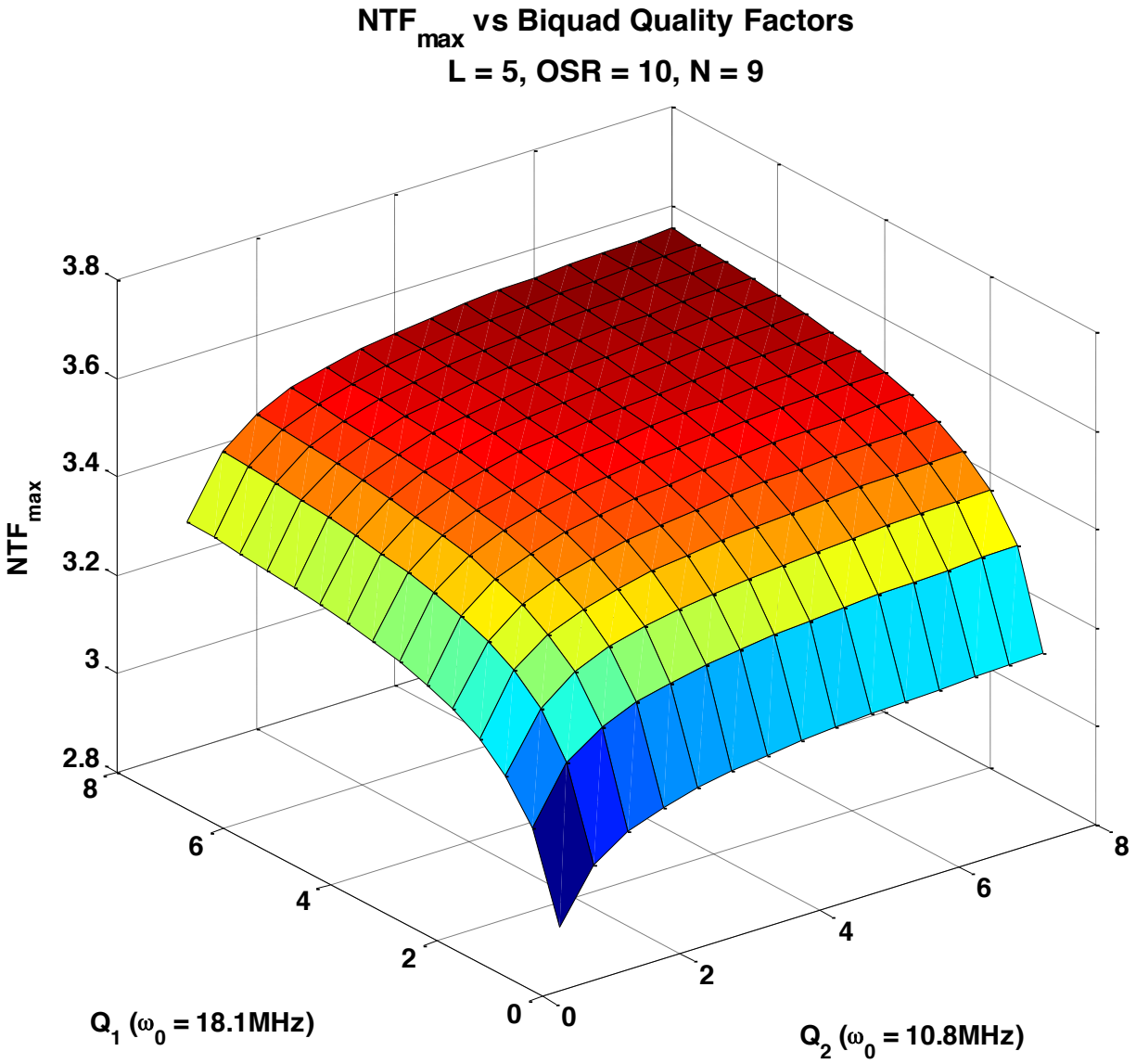
System-level Optimization

- Maximum Signal Amplitude Increase with number of levels and with small NTF values
- Several tradeoffs involved

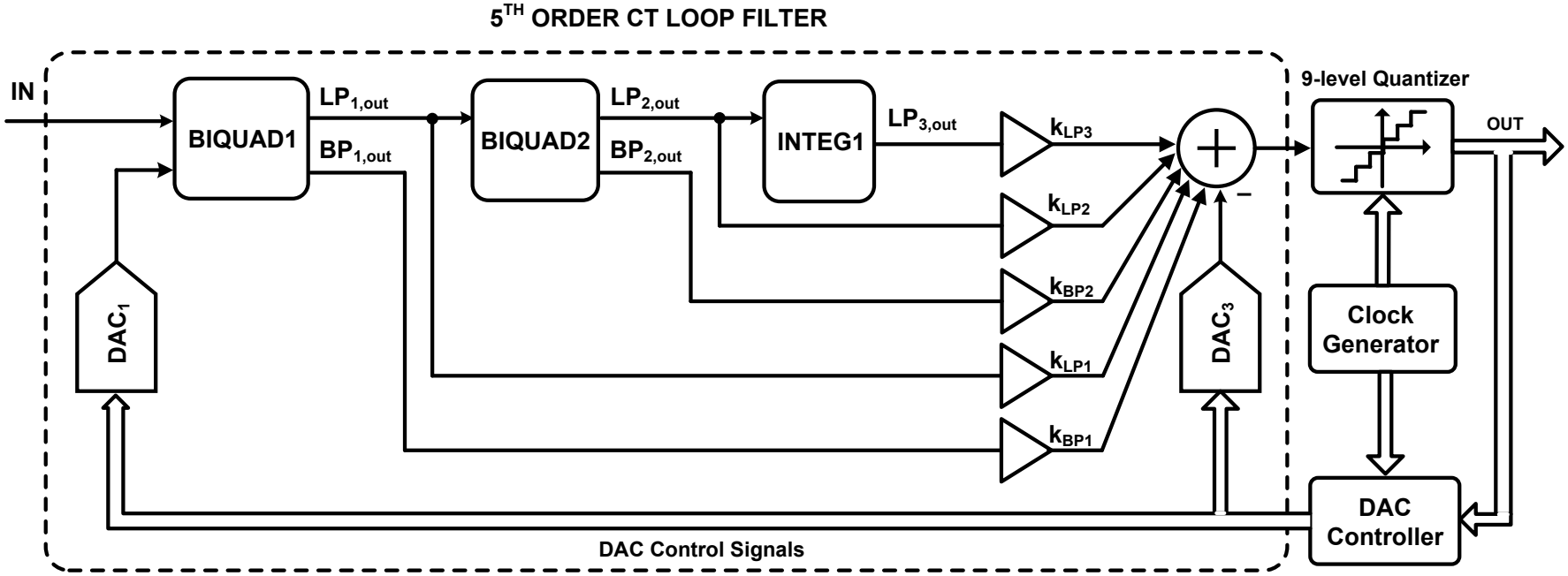


System-level Optimization

- High-Q sections is synonymous of higher NTFmax and better in-band NTF
- However, MSA decreases, then it is unclear if your SQNR is better or not



Loop Filter Design Considerations - 2

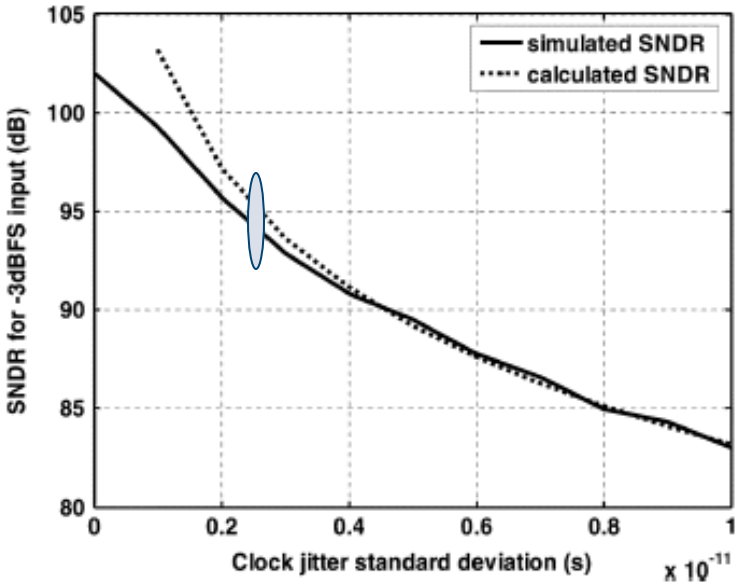


Block	Order	DC Gain dB	Cut-off freq. MHz	Q	IM3 dB	SNR dB
BIQUAD1	2	20	18.4	3	-78	74
BIQUAD2	2	20	10.8	4	-60	60
INTEG1	1	19	3.2	-	-60	60
Filter	5	59	20	-	< -76	72

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 9, SEPTEMBER 2007

A 14 Bit Continuous-Time Delta-Sigma A/D Modulator With 2.5 MHz Signal Bandwidth

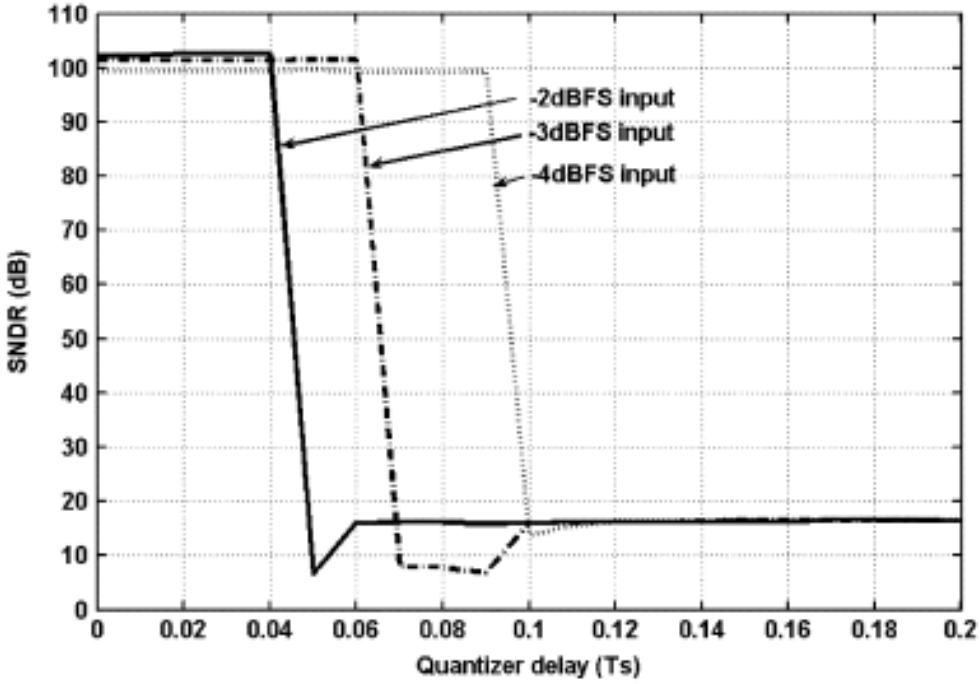
Zhimin Li and Terri S. Fiez, *Fellow, IEEE*

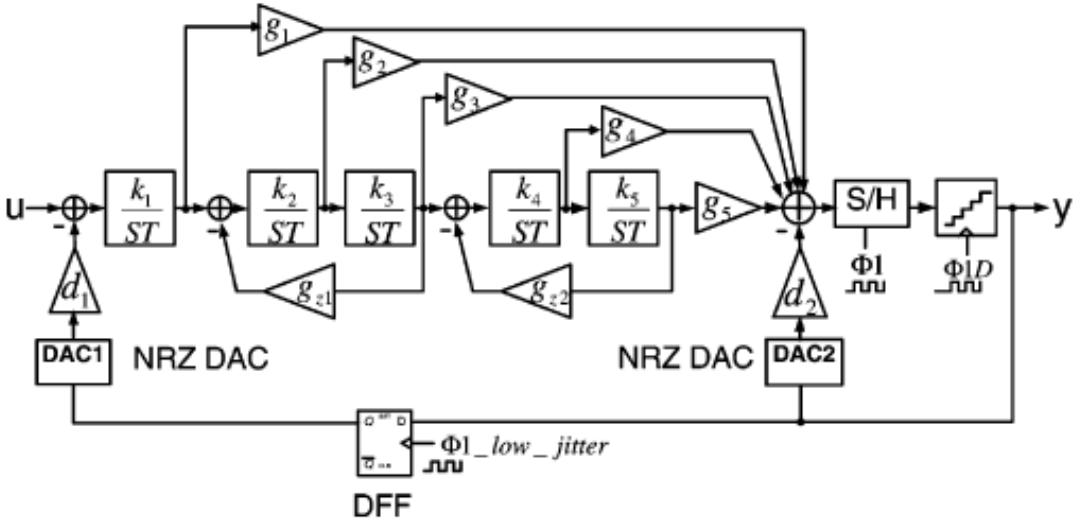


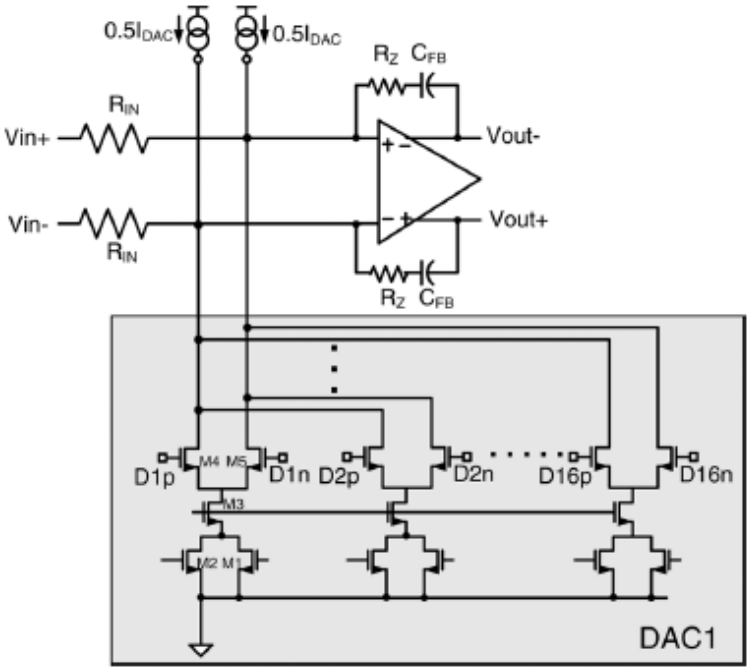
$$\mathrm{SNR}_{\mathrm{jitter}} = \frac{P_s}{P_{\mathrm{jitter}}} = \frac{A^2/2}{\sigma^2 e_{\mathrm{NRZ}}/\mathrm{OSR}} = \frac{\mathrm{OSR}\cdot A^2}{2\sigma^2_{\Delta y,\mathrm{NRZ}}\left(\frac{\sigma_{\Delta_t}}{T}\right)^2}.$$

The resolution of an oversampling $\Delta\Sigma$ A/D modulator is a function of the oversampling ratio (OSR), loop order (L) and the number of quantizer bits (N), as expressed by

$$\mathrm{DR} = \frac{P_s}{P_N} = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N-1)^2\mathrm{OSR}^{2L+1}. \quad (1)$$







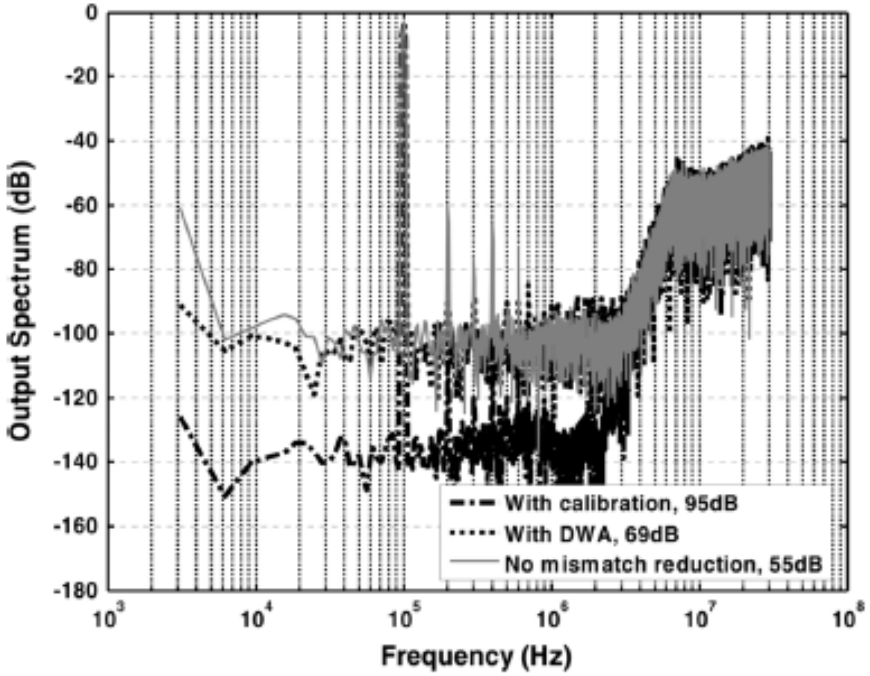
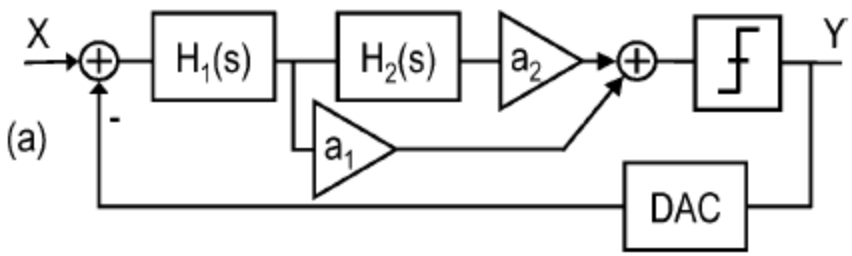


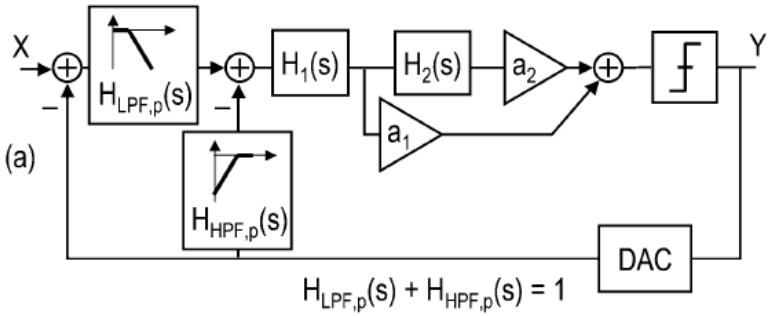
Fig. 5. Output spectrum of the CT modulator for −3 dBFS input.

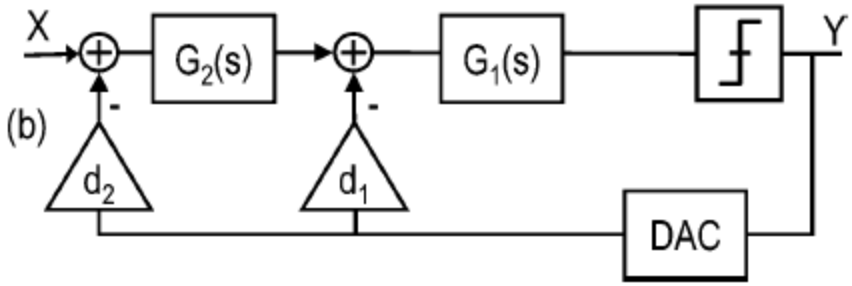
Peak SNDR	80.5dB
Peak SNR	81dB
Peak SFDR	98.4dB
Dynamic range	85dB
Input signal bandwidth	2.5MHz
Clock frequency	60MHz
Oversampling ratio (OSR)	12
Power supply	2.5V
Power consumption	50mW
Die area w/o pads	2.1mm×1.3mm
Die area w/ pads	2.5mm×1.7mm
Fabrication Process	0.25μm 5-metal, mixed/RF CMOS

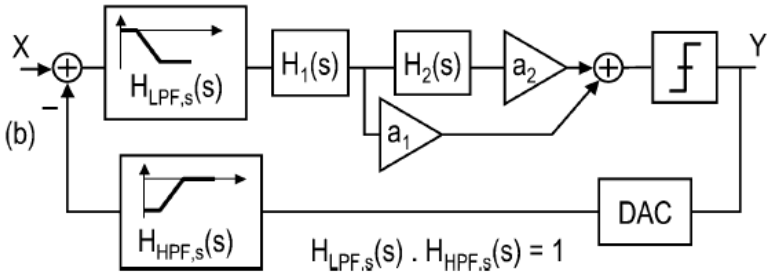
A Continuous-Time ΣΔ ADC With Increased Immunity to Interferers

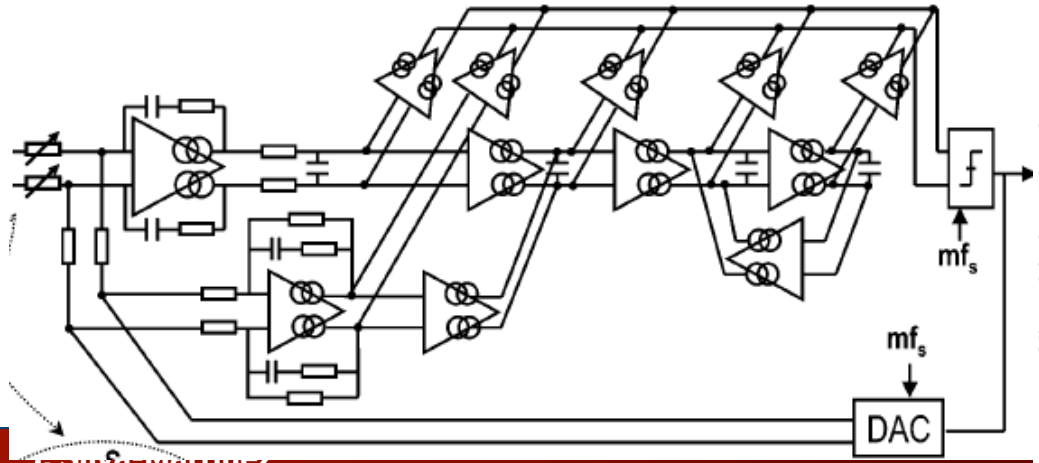
Kathleen Philips, *Member, IEEE*, Peter A. C. M. Nuijten, Raf L. J. Roovers, *Member, IEEE*, Arthur H. M. van Roermund, *Senior Member, IEEE*, Fernando Muñoz Chavero, Macarena Tejero Pallarés, and Antonio Torralba, *Senior Member, IEEE*

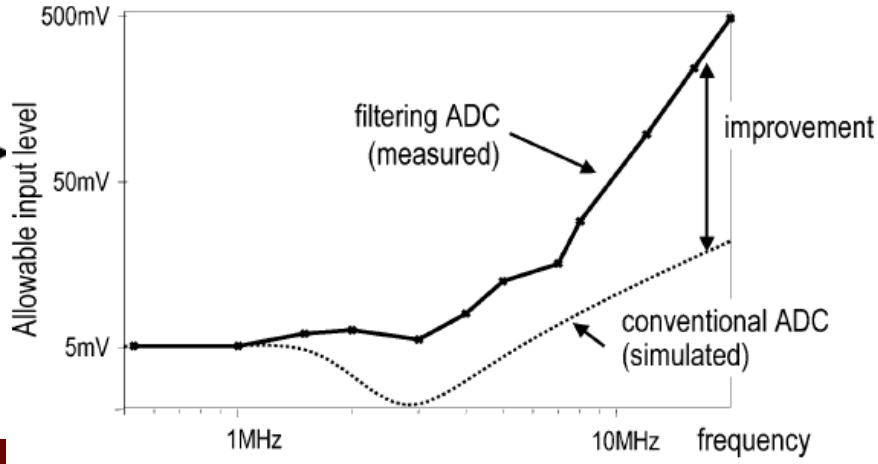






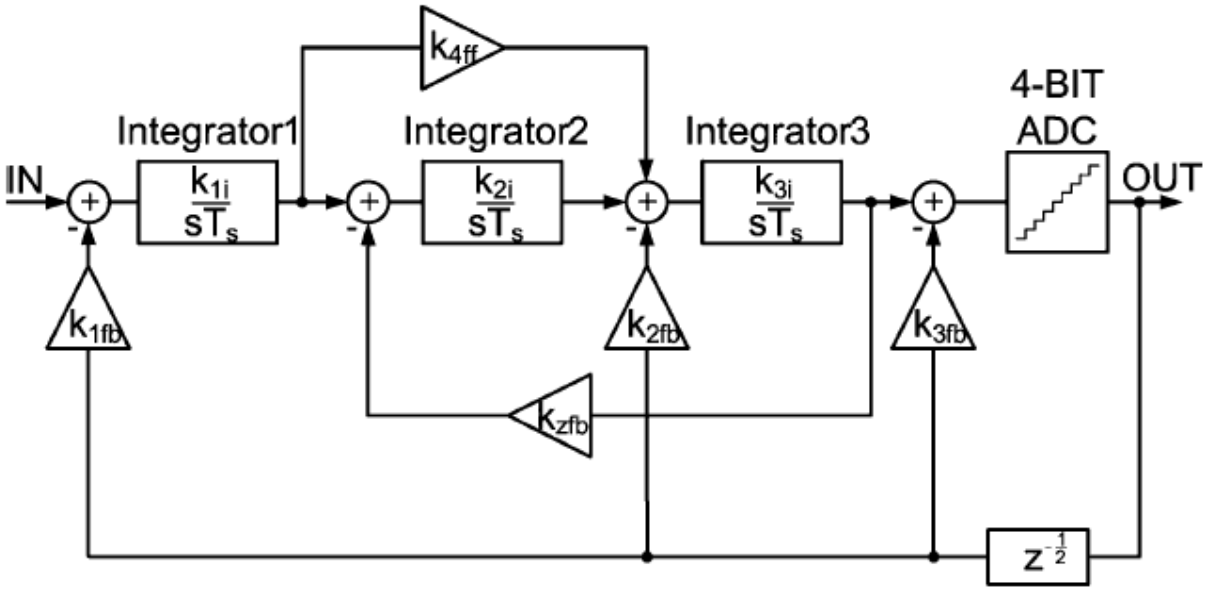


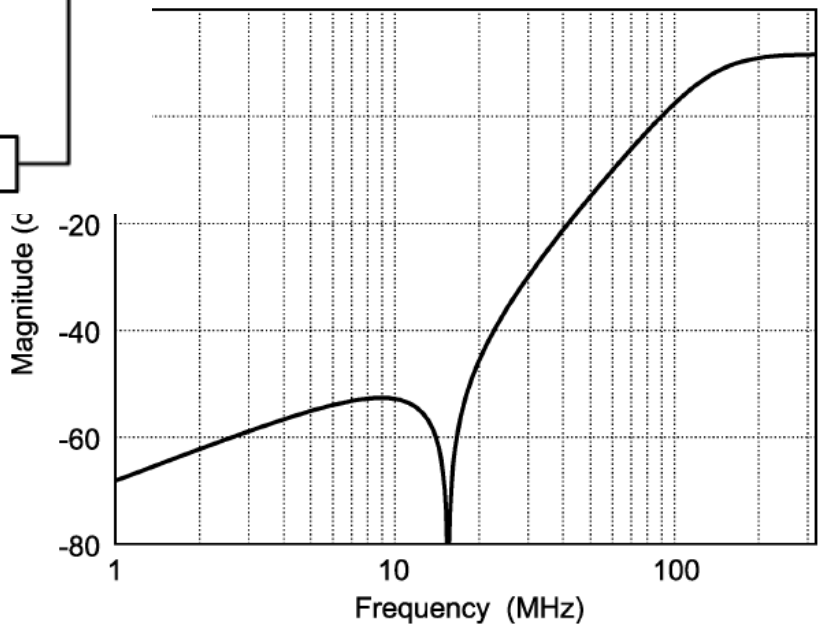


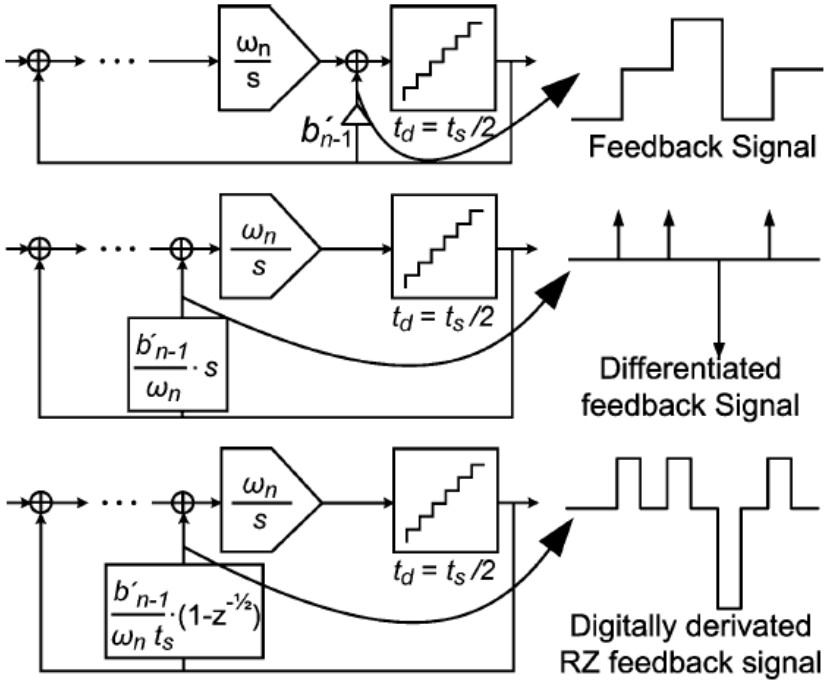


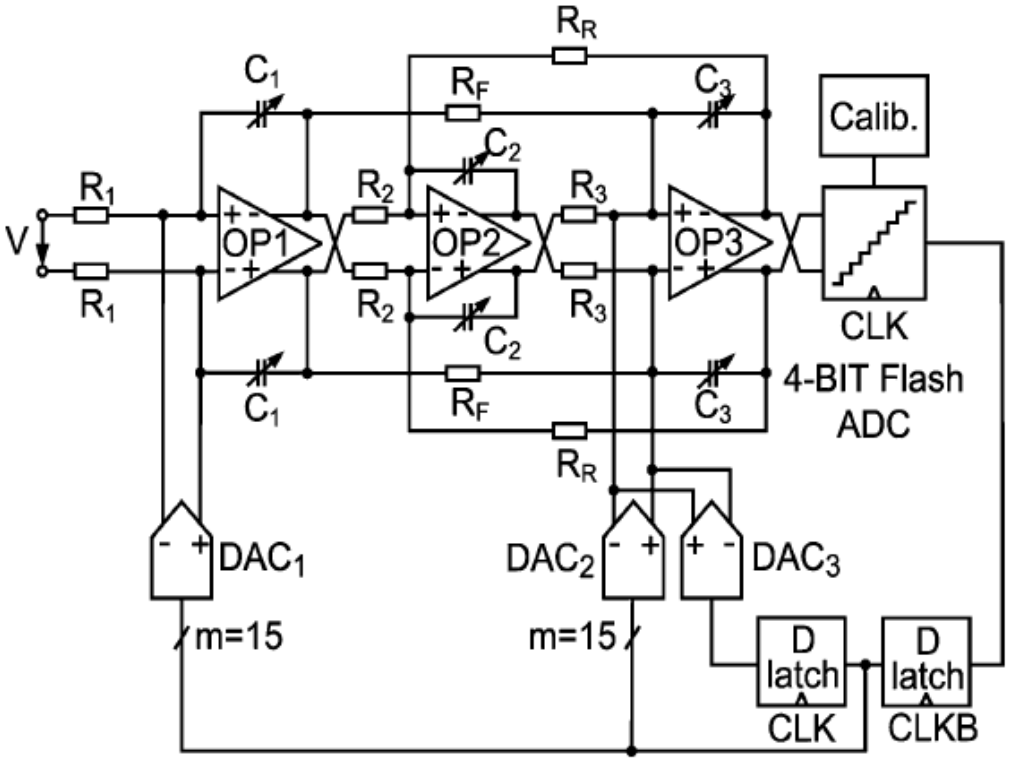
A 20-mW 640-MHz CMOS Continuous-Time ΣΔ ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB

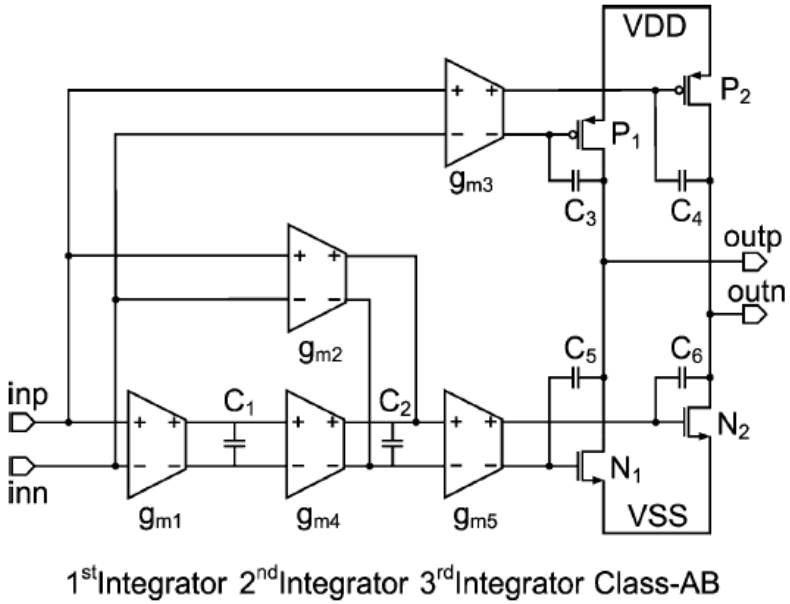
Gerhard Mitteregger, *Member, IEEE*, Christian Ebner, *Member, IEEE*, Stephan Mechnig, *Member, IEEE*, Thomas Blon, *Member, IEEE*, Christophe Holuigue, and Ernesto Romani, *Member, IEEE*

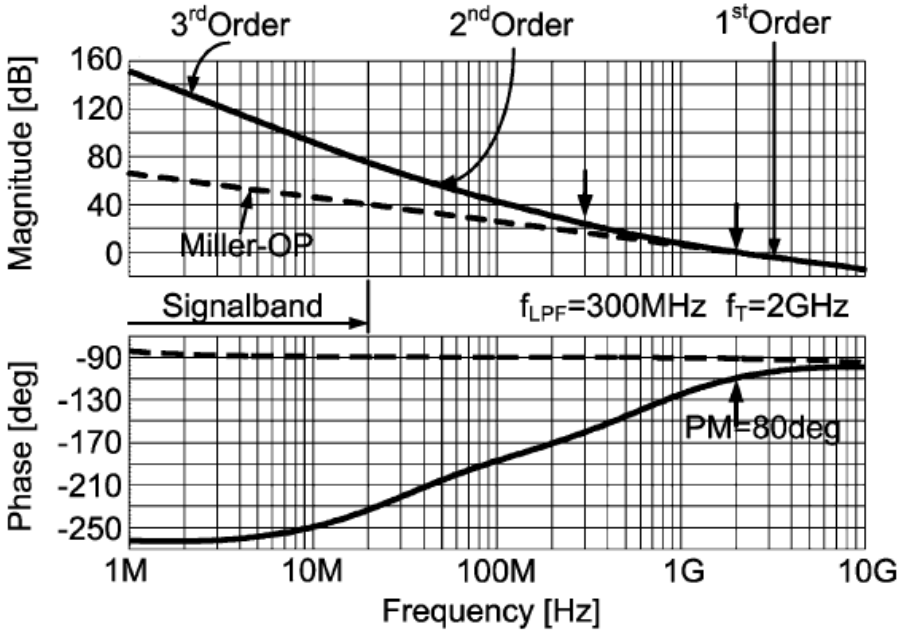





ωn
s
b´n-1
td = ts /2
Feedback Signal
b´n-1 · s
ωn
Differentiated
feedback Signal
b´n-1 (1-z-½)
ωn ts
Digitally derivated
RZ feedback signal


RR
C1
RF
C3
Calib.
C2
R1
R2
R3
V
OP1
OP2
OP3
CLK
4-BIT Flash
ADC
DAC1
DAC2
DAC3
m=15
m=15
D
latch
CLK
CLKB





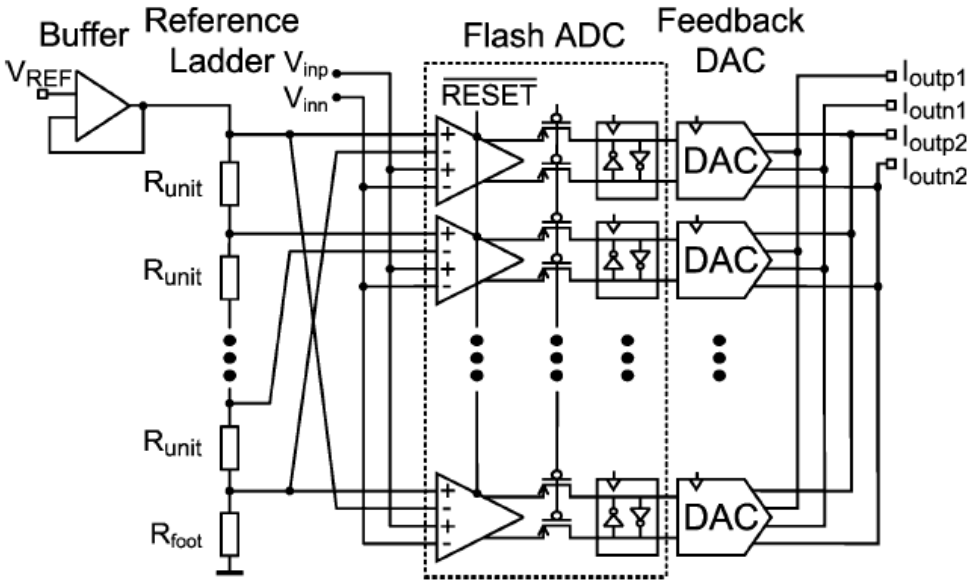


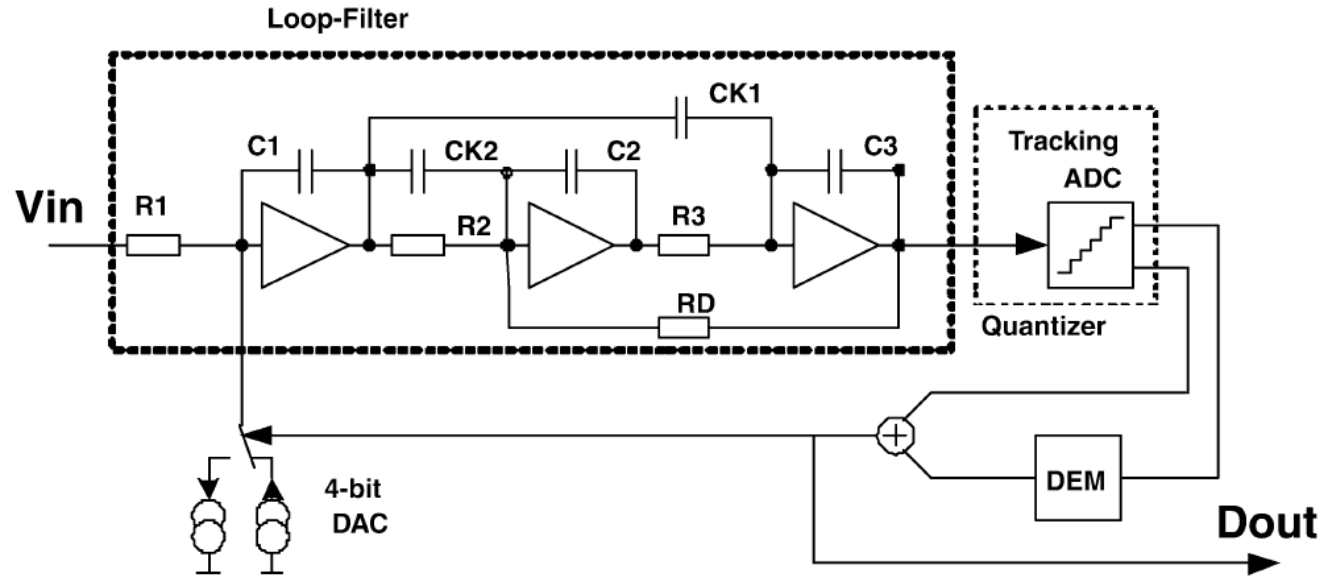
Fig. 10. Four-bit quantizer with 4-bit flash ADC and reference voltage generation plus feedback DAC.

TABLE I
PERFORMANCE SUMMARY

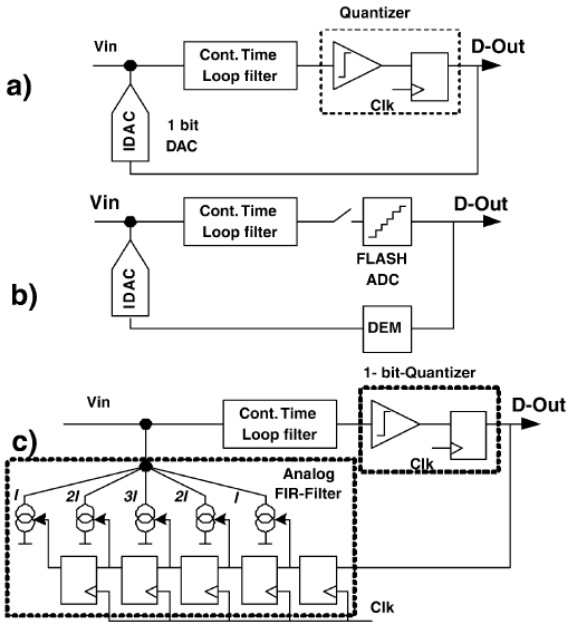
Sampling Frequency		640MHz
Conversion Rate		40MS/s
Input Range		0-20MHz
Peak SNR		76dB
THD		-78dB
Peak SNDR		74dB
ENOB		12
Process		1.2V 130nm 1P8M CMOS
Chip Area		$8.6mm^2$
Power	Modulator	20mW
	Decimator 40MS/s	18mW
	PLL 2.56GHz	12mW
	I/O 1.8V	4mW

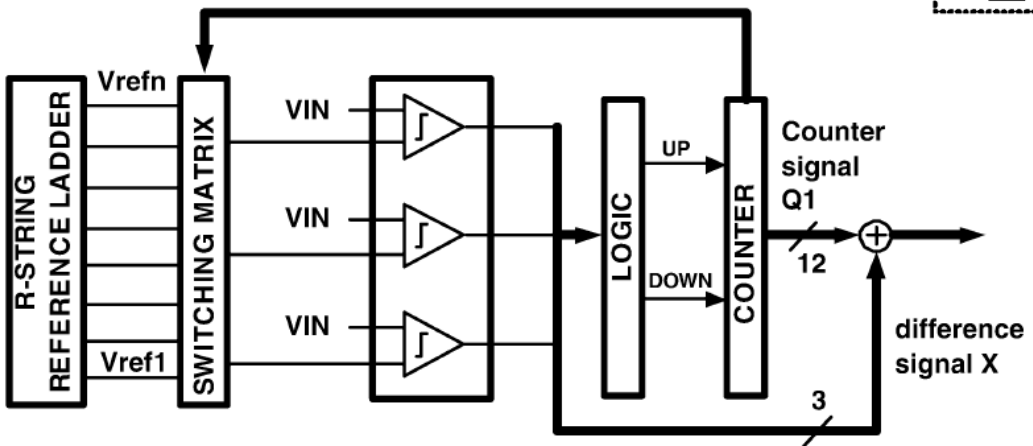
A 3-mW 74-dB SNR 2-MHz Continuous-Time Delta-Sigma ADC With a Tracking ADC Quantizer in 0.13-μm CMOS

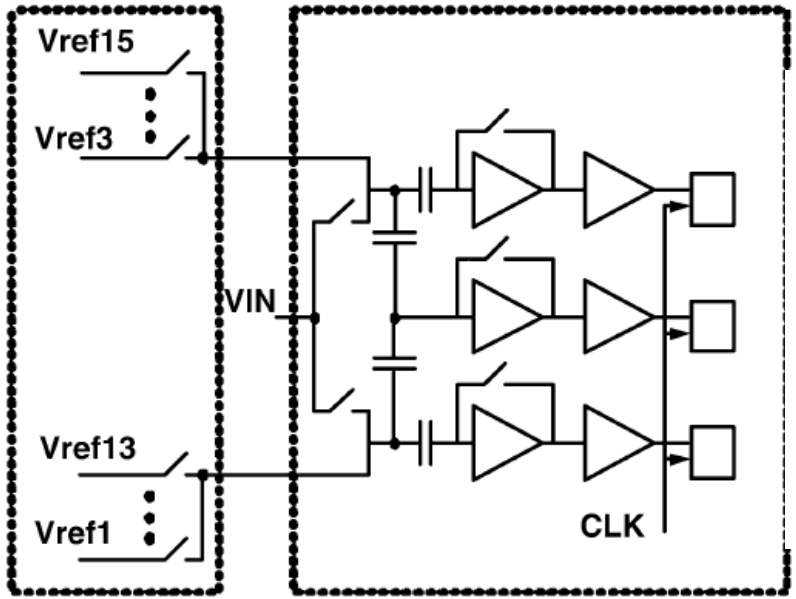
Lukas Dörrer, Franz Kuttner, Patrizia Greco, Patrick Torta, and Thomas Hartig

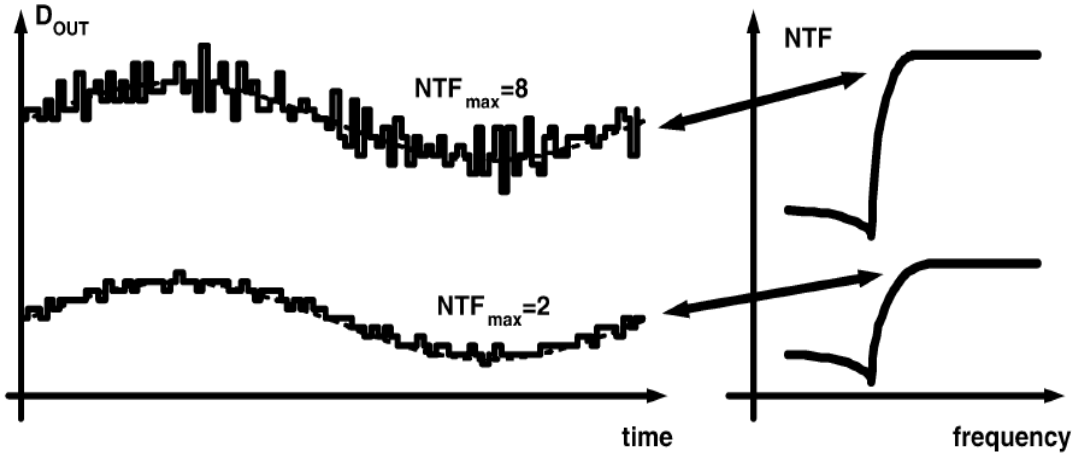


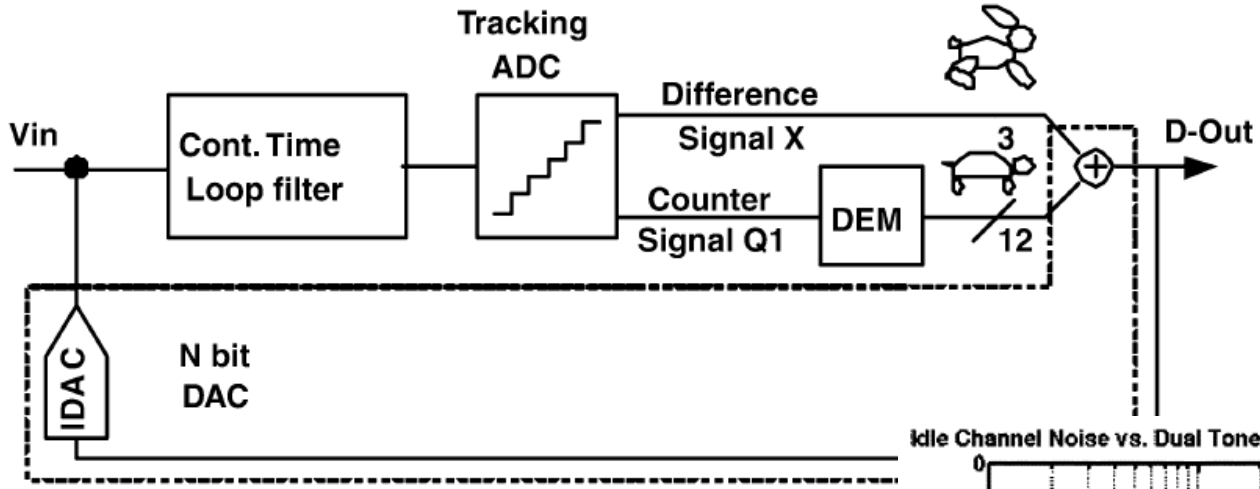
third-order 4-bit $\Delta\Sigma$ architecture.





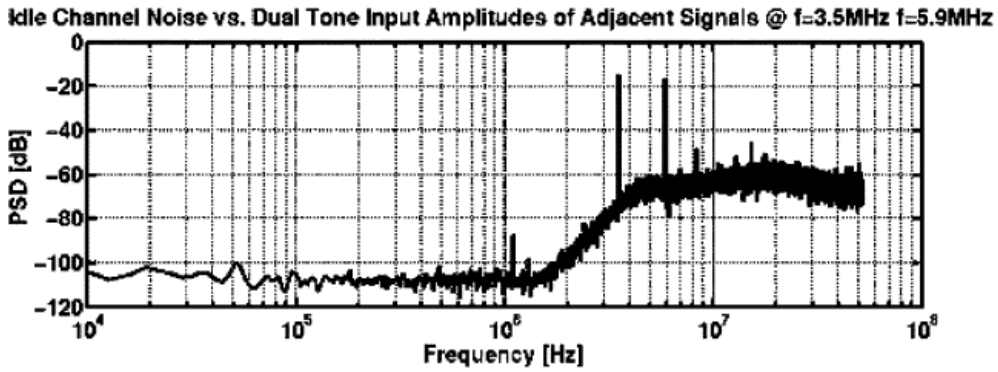




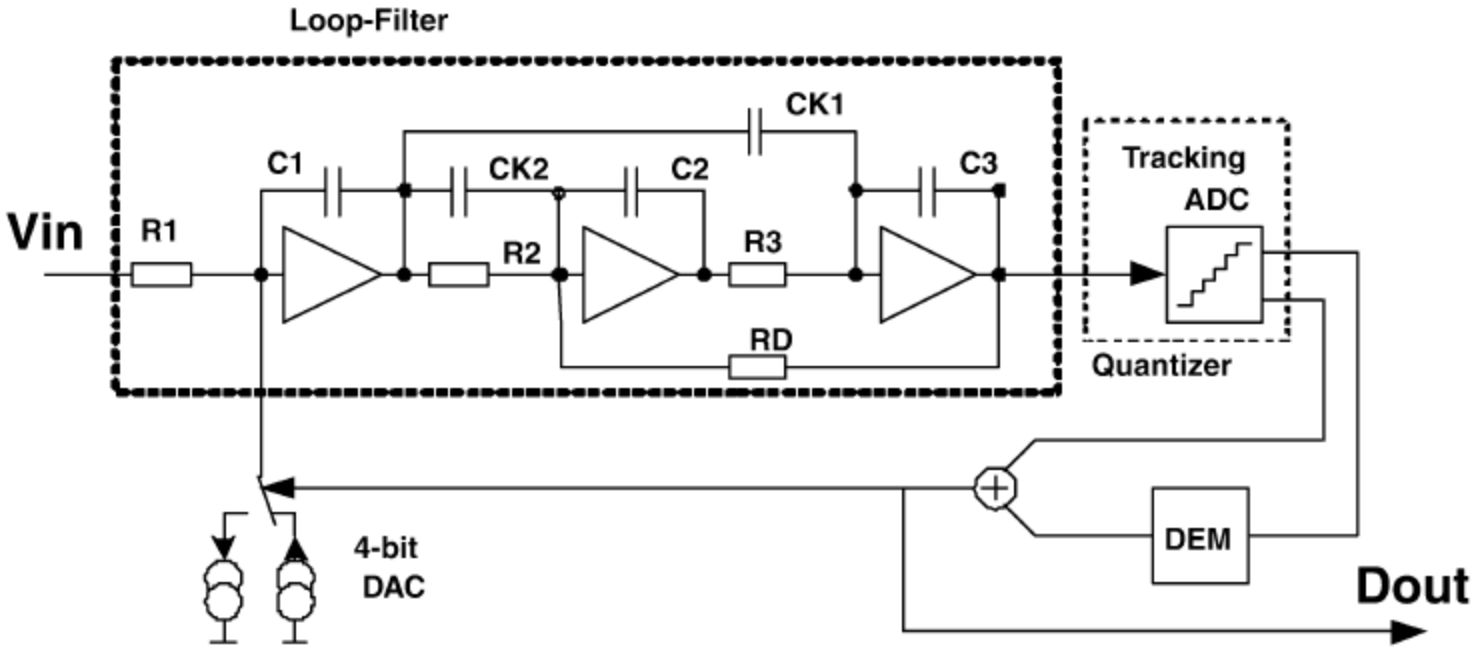


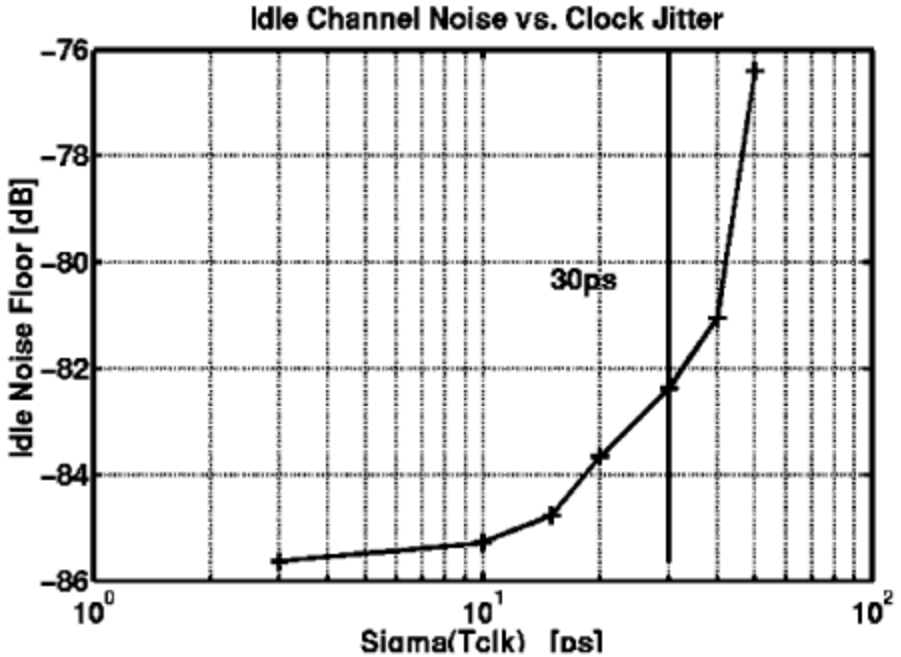
The DEM is usually slow and may lead to significant loop delay!

May require loop compensation



Nice feature: Robust against blockers!

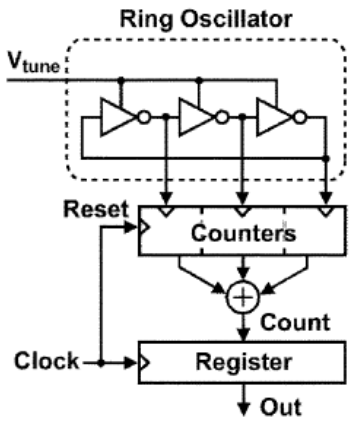


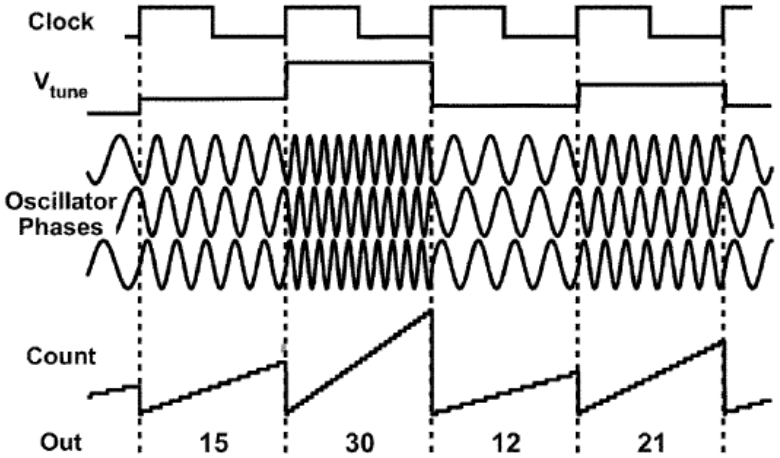


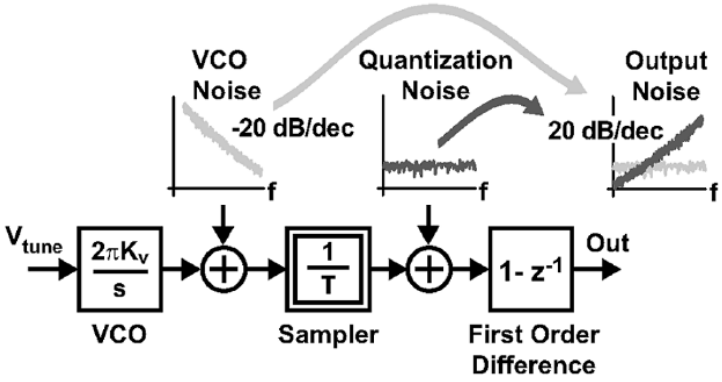
Sampling Frequency	104 MHz
Signal Bandwith	2 MHz
Peak SNR / SNDR	74 dB / 70dB @ fin=41KHz
Peak SNR / SNDR	72 dB/ 71dB @fin=625kHz
Power Consumption	3mW @ 1.5V
Clock Jitter requirements	< 30 ps
Core Area	0.3 mm^2
Technology	0.13 µm CMOS 1P/6M

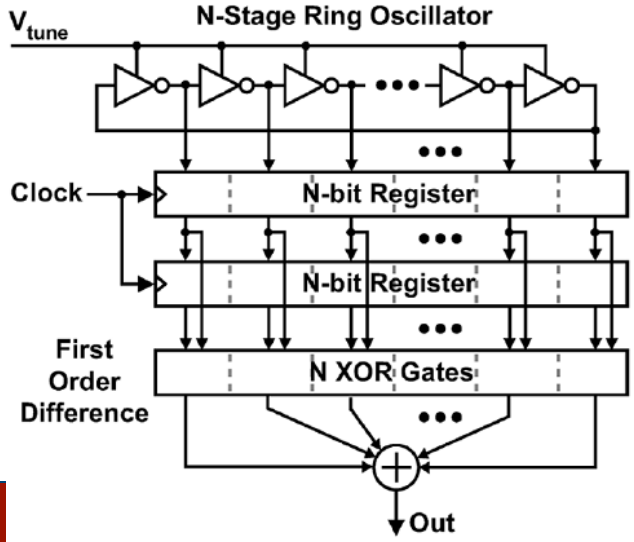
A 12-Bit, 10-MHz Bandwidth, Continuous-Time ΣΔ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer

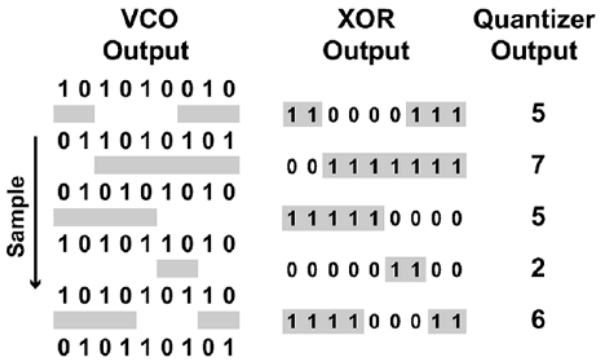
Matthew Z. Straayer, *Student Member, IEEE*, and Michael H. Perrott, *Member, IEEE*



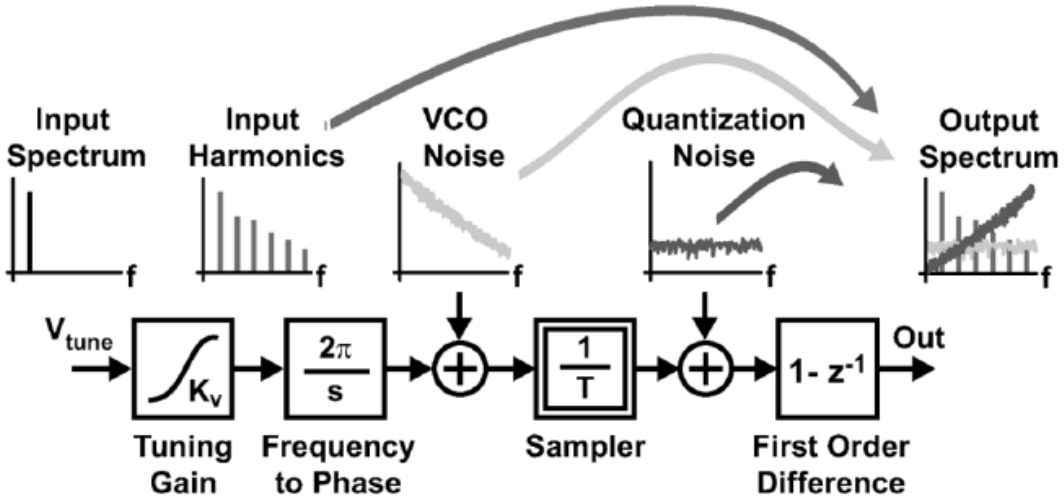


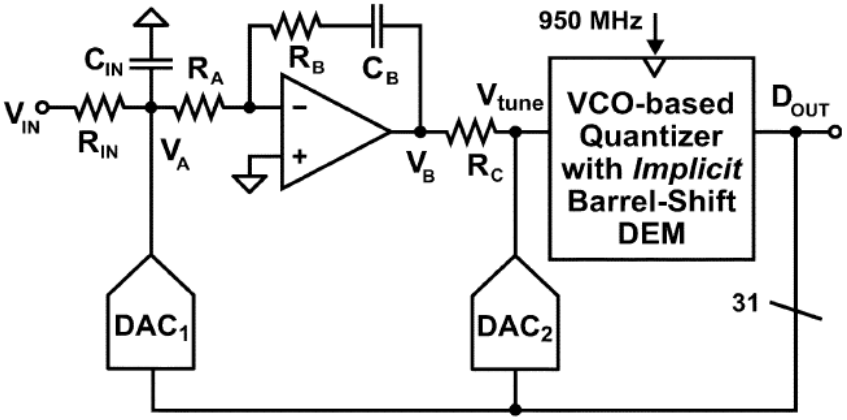


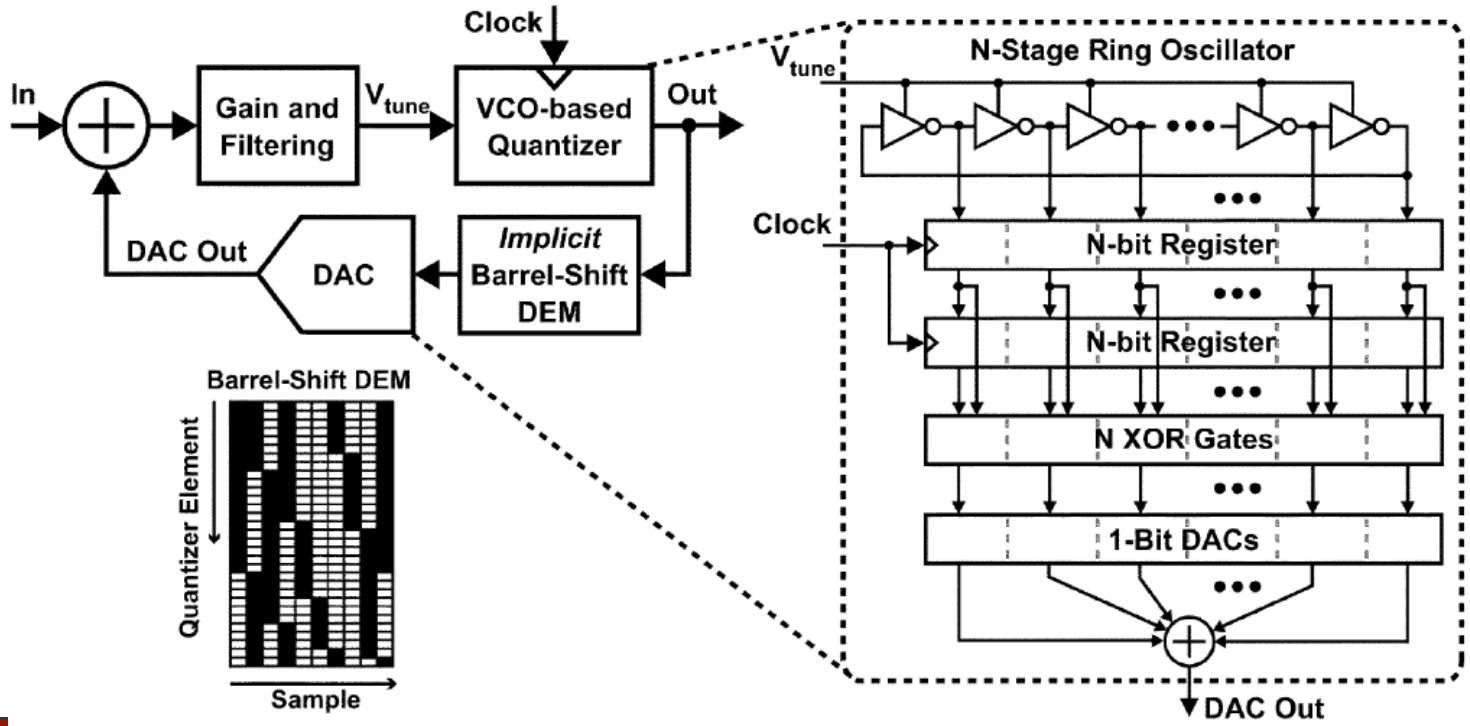


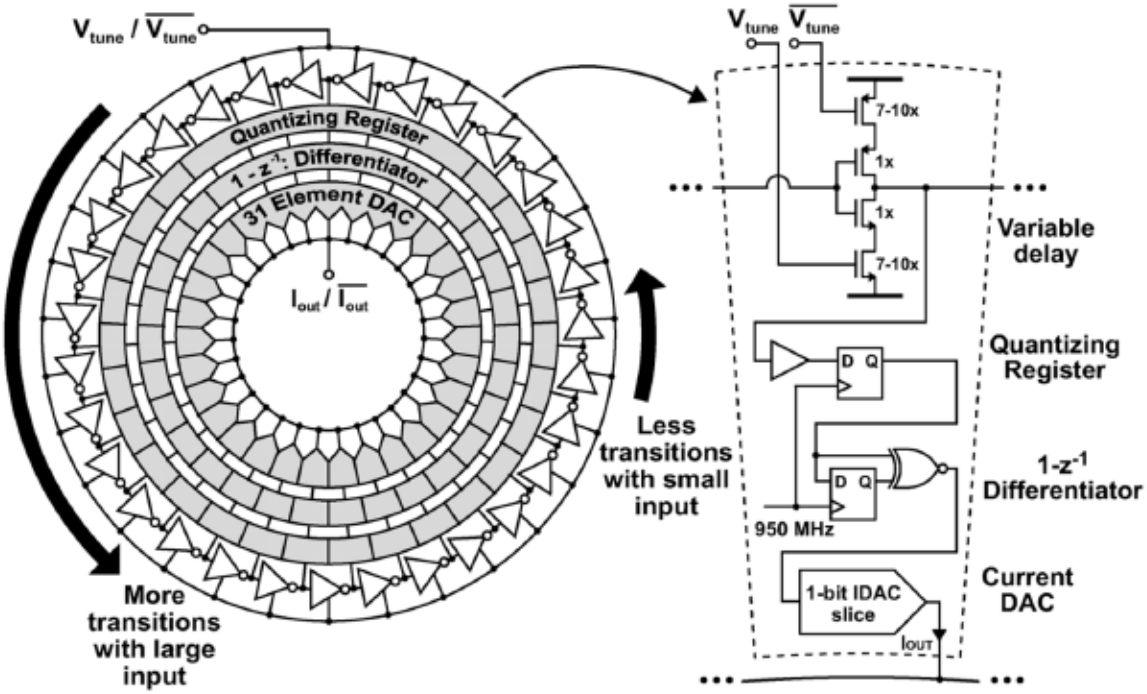


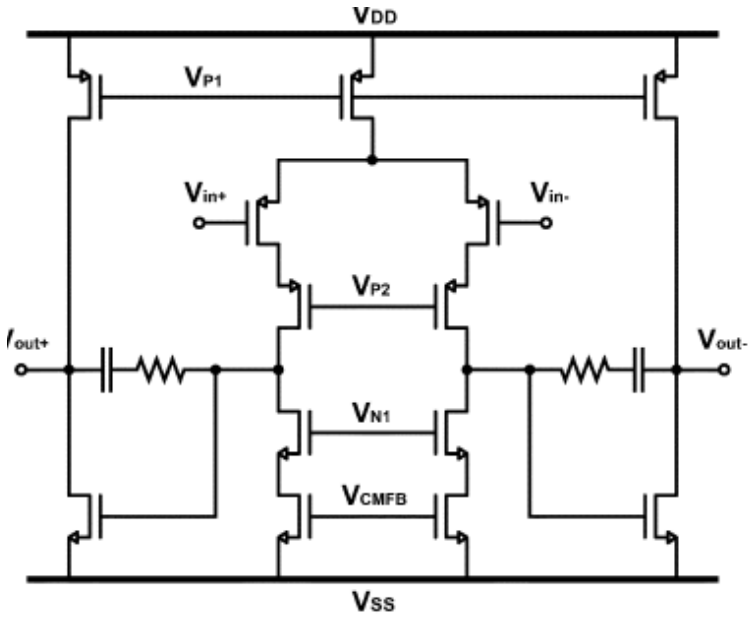
$F_{clock} > 2 \cdot F_{VCO}$


Input Spectrum
Input Harmonics
VCO Noise
Quantization Noise
Output Spectrum
f
V_{tune}
K_v
$\frac{2\pi}{s}$
$\frac{1}{T}$
$1- z^{-1}$
Out
Tuning Gain
Frequency to Phase
Sampler
First Order Difference


C_{IN}
R_A
R_B
C_B
V_{IN}
R_{IN}
V_A
V_B
V_{tune}
R_C
950 MHz
VCO-based Quantizer with *Implicit* Barrel-Shift DEM
D_{OUT}
DAC_1
DAC_2
31


Clock
In
Gain and Filtering
V_{tune}
VCO-based Quantizer
Out
DAC Out
DAC
Implicit Barrel-Shift DEM
Barrel-Shift DEM
Quantizer Element
Sample
N-Stage Ring Oscillator
V_{tune}
Clock
N-bit Register
N-bit Register
N XOR Gates
1-Bit DACs
DAC Out





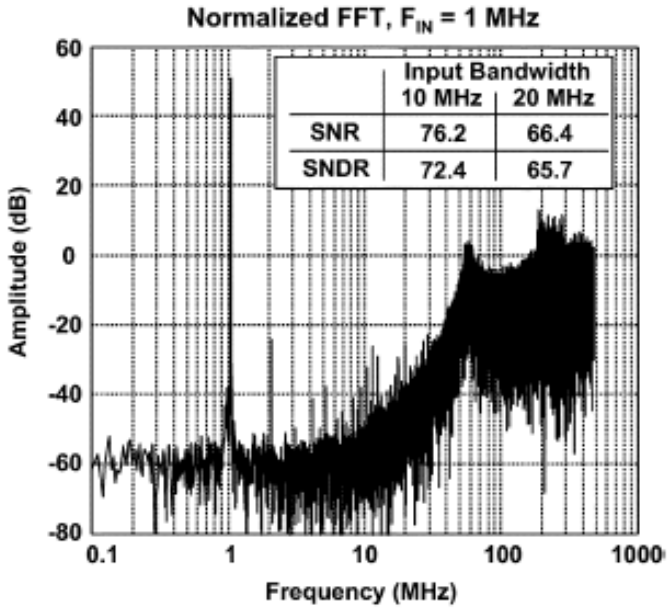


TABLE II
COMPARISON WITH PUBLISHED HIGH-SPEED CT ADCS

Ref.	F_S (MHz)	BW (MHz)	SNR (dB)	SNDR (dB)	Power (mW)
[12]	276	23	70	69	43
[13]	340	20	71	69	56
[14]	400	12	64	61	70
[15]	640	10	72	66	7.5
[16]	640	20	76	74	20
[17]	1000	8	63	63	10
This work	**950**	**10**	**86**	**72**	**40**