Fundamentals of Continuous-Time \(\Sigma\Delta\) Modulators

Jose Silva-Martinez
(amesp02.tamu.edu/~jsilva)

Department of ECE
Texas A&M University
Outline

- Fundamentals of Sigma-Delta Modulators
  - Noise and Signal Transfer Function
  - Error Function
  - Blockers tolerance

- System Limitations
  - Linear Range
  - Stability
  - Clock Jitter

- Building blocks
  - Filter issues
  - Quantizer
  - DAC issues
  - Clock Generation

- Conclusions
State of the art

![Graph showing P/\(f_{\text{sig}}\) vs. SN(D)R for different data rates and power levels.]

**LTE**

100mW @10MHz

10mW @10MHz

**Fig. 2.** Experimental ADC data and fundamental asymptotes for analog circuits containing a single amplifier and capacitor.
Nyquist-Rate and Oversampled A/D Conversion

- According to the ratio of sample frequency and Nyquist sample rate, A/D converters can be classified as,
  - Nyquist-rate A/D converter
  - Oversampled A/D converter

- For a Nyquist-rate A/D converter, the sample frequency is at, or slightly higher than, Nyquist sample rate of the input signal.

- For an oversampled A/D converter, the sample frequency ($F_s$) is much higher than the Nyquist sample rate ($F_{nyquist}$). The ratio of $M = F_s/F_{nyquist}$ is the oversample ratio (OSR).
Nyquist-Rate and Oversampled A/D Conversion

- One direct benefit of oversampled ADC is that the quantization noise is $M$ (M is the oversample ratio) times less than its Nyquist counterpart.
- Every time we double the sample frequency, the effective resolution increases with 3 dB (0.5 bit).

$$\frac{\Delta^2}{12} \times \frac{F_b}{F_s}$$

Frequency band of interest

$S_{nq}(f)$ Quantization noise PSD

The quantization noise outside of the frequency of interest should be filtered out by post digital filtering.
Reducing signal bandwidth decreases the integrated in-band noise level by 3 dB.

Increasing the oversampling ratio $F_s/2F_b$ by a factor of 4 increases the resolution by 6dB or equivalently 1 dB.

Changing the sampling frequency by a factor of 100 increases the SQNR by only 20 dB.

Very expensive: too much effort for additional 3.3 bits.

Can we do better than this?
Conventional (Nyquist) ADC

\[ \text{SQNR} = 6.02 \times n + 1.76 \]
Basic concept in $\Sigma\Delta$ Modulators

\[ STF = \frac{H(s)}{1 + H(s)} \]

\[ NTF = \frac{1}{1 + H(s)} \]
Identify the noise and signal and use Feedback to shape the noise!

Original ADC + noise

\[ Y(z) = E(z) + A(z)X(z) - A(z)Y(z) \]
\[ = E(z) \frac{1}{1 + A(z)} + X(z) \frac{A(z)}{1 + A(z)} \]
\[ = E(z) H_E(z) + X(z) H_X(z) \]

Objective
- Want to make STF unity in the signal frequency band
- Want to make NTF "small" in the signal frequency band

If the frequency band of interest is around DC \((0 \ldots f_B)\) we achieve this by making \(|A(z)| >> 1\) at low frequencies
- Means that NTF is \(<<1\)
- Means that STF \(\equiv 1\)

The assumption is that the DAC can do much better than the original ADC; is this realistic? Free lunch?
Oversampled A/D Conversion
(Double check Mason’s rule)

\[ H_e(z) = 1 - Z^{-1} = 1 - e^{-j \omega T} = e^{-j \frac{\omega T}{2}} \left( e^{+j \frac{\omega T}{2}} - e^{-j \frac{\omega T}{2}} \right) \]

\[ H_e(z) = e^{-j \frac{\omega T}{2}} \left( 2 j \sin \left( \frac{\omega T}{2} \right) \right) \]

\[ |H_e(z)| = 2 \sin \left( \frac{\omega T}{2} \right) \]

\[ Y(z) = E(z) \frac{1}{1 + \frac{1}{z-1}} + X(z) \frac{z^{-1}}{1 + \frac{1}{z-1}} \]

\[ = E(z) \left( 1 - z^{-1} \right) + X(z)z^{-1} \]

Check the input-output trajectories
Original E(z) is shaped by NTF

Original E(z) is amplified here!

Spot SQNR

\[ SQNR = \left| \frac{X(z)Z^{-1}}{E(z)H_e(z)} \right|^2 \]

\[ SQNR = \left| \frac{X(z)}{E(z)} \right|^2 \cdot \frac{1}{2 \sin \left( \frac{\omega T}{2} \right)} \]
Oversampled A/D Conversion

\[ SQNR = 1.5 \left( 2^N - 1 \right)^2 \left( 3 \frac{OSR^3}{\pi^2} \right) \]

Signal to Quantization Noise Ratio (SQNR)

- \( N \) = number of bits
- \( OSR = \frac{fs}{2fb} \)
- SQNR improves by 30dB when OSR increases by 10
- Or 9dB SQNR improvement when doubling OSR
Oversampled A/D Conversion

Typical spectrum for a 2\textsuperscript{nd} order system

Figure 3.6: Output spectrum of MOD2 with a −6-dBFS sine-wave input.

Understanding Delta-Sigma Data Converters, Schreier and Temes
Linearized Model: 2nd order
Multiple Feedback Modulator

\[ V(z) = \frac{a_1 a_2}{U(z) (z-1)^2 + (z-1)b a_2 + a_1 a_2} = \frac{a_1 a_2}{z^2 - (2-b a_2)z + (1+a_1 a_2 - b a_2)} \]

\[ U(z) = \frac{z^2 - (2r \cos(\omega_0 T))z + (1-r^2)}{(z-r e^{j\omega_0 T})(z-r e^{-j\omega_0 T})} \]

N.T.F. \[ \text{N.T.F.} = \frac{V(z)}{E(z)} = \frac{(z-1)^2}{(z-1)^2 + (z-1)b a_2 z + a_1 a_2} \]

Under the conditions \( a_1 a_2 = 1 \) and \( a_2 b = 2 \), then

\[ V(z) = z^{-2}U(z) + \left(1-z^{-1}\right)^2 E(z) \]

\[ U(z) - V(z) = \left(1-z^{-2}\right)U(z) - \left(1-z^{-1}\right)^2 E(z) \]

This is the real signal at the filter’s input: THINK ABOUT IT!
Linearized Model: 2\textsuperscript{nd} order
Multiple Feedback Modulator

\[ \frac{V(z) - U(z)}{1 - z^{-1}} z^{-1} a_1 = \{1 + z^{-1}\} z^{-1} a_1 U(z) - (1 - z^{-1}) z^{-1} a_1 E(z) \]

If \( a_1 > 0.5 \), hence the in-band output of the 1\textsuperscript{st} integrator is > than the input!

STF and NTF are definitely not enough to design a robust system!

\[ V(z) = z^{-2} U(z) + (1 - z^{-1})^2 E(z) \]

At the input of the first amplifier we have:

\[ U(z) - V(z) = \{1 - z^{-2}\} U(z) - (1 - z^{-1})^2 E(z) \]

At the output of the first integrator we have (saturation?)

Small for inband signals but what about the blockers?
2\textsuperscript{nd} order Multiple Feedback Modulator

\[
\text{STF} = \frac{V(z)}{U(z)} = \frac{b_3 (1 - Z^{-1})^2 + b_2 (1 - Z^{-1}) + b_1}{(1 - Z^{-1})^2 + a_3 Z^{-1} (1 - Z^{-1})^2 + a_2 Z^{-1} (1 - Z^{-1}) + a_1 Z^{-1}}
\]

\[
\text{STF} = \frac{V(z)}{U(z)} = b_3 (1 - Z^{-1})^2 + b_2 (1 - Z^{-1}) + b_1
\]

\[
\text{NTF} = \frac{V(z)}{E(z)} = (1 - Z^{-1})^2
\]

Amplifier input \( V_e(z) = \left\{ - b_2 (1 - Z^{-1}) - b_3 (1 - Z^{-1})^2 \right\} U(z) - (1 - Z^{-1})^2 E(z) \)
Generic model for the Feed-forward Modulator

\[ V = \{STF\}U + \{NTF\}E \]

\[ V = \left\{ \frac{L}{1+L} \right\}U + \left\{ \frac{1}{1+L} \right\}E \]

\[ V_e = U - V = \left\{ \frac{1}{1+L} \right\}U - \left\{ \frac{1}{1+L} \right\}E = \frac{U - E}{1+L} \]

\[ Y = V_e L = \left\{ \frac{L}{1+L} \right\}\{U - E\} \]

Be sure that \(|1+L| > 0\) for all frequencies; e.g. phase at the unity frequency

Very good for inband signals, but some issues for out of band signals specially if NTF > 1 at high frequencies

Little chance of overloading at the quantizer input
Generic model for the Feed-forward Modulator

\[ V = U + \left( \frac{1}{1+L} \right) E \]

**Very good STF but it is not very relevant in practice**

\[ V_e = U - V = -\left( \frac{1}{1+L} \right) E \]

**Excellent for both in-band and out-of-band blockers; minor issues if NTF>1 at high frequencies**

\[ Y = U + V_e L = U - \left( \frac{L}{1+L} \right) E \]

**Little chance of overloading at the quantizer input**

**But.. What about aliasing of HF signals? After Y we have the quantizer (S/H)!**
Generic model for a Hybrid Modulator

\[ V = \left( \frac{L_0 k}{1 + L_1 k} \right) U + \left( \frac{1}{1 + L_1 k} \right) E \]

Error Signal = \( V - E \)

\[ = \left( \frac{L_0 k}{1 + L_1 k} \right) U - \left( \frac{L_1 k}{1 + L_1 k} \right) E \]

(HIGH) Risk of excessive signal at the internal nodes

You have to analyze case by case; hard to make general conclusions

Once you define \( L_0 \) and \( L_1 \) and the topology you must analyze how \( L_1 \cdot V \) and \( L_0 \cdot U \) affect the signal swing at every internal node

Inband SNR is a strong function of \( L_0 k \)
High-order Feedforward Modulator based on Integrators

This architecture is very popular in CT modulators

No problem with non-touching loops nor with trajectories
non-touching loops

A major issue is the frequency response of the adder
Generic model for a Hybrid Modulator

\[ V = \left\{ \frac{L_0 k}{1 + L_1 k} \right\} U + \left\{ \frac{1}{1 + L_1 k} \right\} E \]

ErrorSignal = V - E = \left\{ \frac{L_0 k}{1 + L_1 k} \right\} U - \left\{ \frac{L_1 k}{1 + L_1 k} \right\} E

(HIGH) Risk of excessive signal at the internal nodes

You have to analyze case by case; hard to make general conclusions

Once you define Lo and L1 and the topology, you must analyze how L1*V and Lo*U affects the signal swing in every node

Inband SNR is a strong function of Lok
Fundamentals on MASH architectures

Quite relevant topology: Notice that the auxiliary ADC processes the quantization error $E_1$.

What about $E_2$?

Any other option?

\[
V(z) = H_1(z)V_1 - H_2(z)V_2
\]

\[
V_1(z) = STF_1(z)U + NTF_1(z)E_1
\]

\[
V_2(z) = STF_2(z)E_1 + NTF_2(z)E_2
\]

Then

\[
V(z) = H_1\{STF_1 * U + NTF_1 * E_1\} - H_2\{STF_2 * E_1 + NTF_2 * E_2\}
\]

\[
V(z) = \{H_1 * STF_1\}U + \{H_1 * NTF_1 - H_2 * STF_2\}E_1 - \{H_2 * NTF_2\}E_2
\]
Fundamentals on MASH architectures

Figure 4.22: The L-0 cascade (Leslie-Singh) structure.

If $H_1 \ast NTF_1 - H_2 \ast STF_2 = 0$

Then

$$V(z) = \{H_1 \ast STF_1\}U - \{H_2 \ast NTF_2\}E_2$$

$$SQNR = \left( E_1 \right)^2 \left( \frac{STF_2}{NTF_2} \right)^2 \left( \frac{STF_1 \ast U}{NTF_1 \ast E_1} \right)^2$$

Analog Intensive MASH topology
Sigma-Delta Modulators
Design Issues

Jose Silva-Martinez
Texas A&M University
Electrical and computer Engineering

(Amesp02.tamu.edu/~jsilva)

Part 1.2
Linearized Discrete-Time Model

\[ Y(z) = H(z) \cdot [X(z) - Y(z)] + E(z) \]

\[ \Rightarrow Y(z) = \frac{H(z)}{1+H(z)} \cdot X(z) + \frac{1}{1+H(z)} \cdot E(z) \]

\[ \Rightarrow Y(z) = z^{-1} \cdot X(z) + (1-z^{-1}) \cdot E(z) \]

\[ H(z) = \frac{z^{-1}}{1-z^{-1}} \]

Signal Transfer Function:
\[ \text{STF} = \frac{Y(z)}{X(z)} = z^{-1} \leftarrow \text{Delay} \]

Noise Transfer Function:
\[ \text{NTF} = \frac{Y(z)}{E(z)} = 1-z^{-1} \leftarrow \text{HP} \]

Caveat: \( E(z) \) may be correlated with \( X(z) \) – not “white”.
1\textsuperscript{st}-Order Noise Shaping

Doubling OSR increases SQNR by 9 dB (1.5 bit/oct).
Doubling OSR (M) increases SQNR by 15 dB (2.5 bit/oct).

Signal Transfer Function:
\[ \text{STF} = z^{-2} \]

Noise Transfer Function:
\[ \text{NTF} = (1 - z^{-1})^2 \]

In-band quantization noise:
\[ N_e^2 \approx \frac{\Delta^2}{12} \cdot \frac{\pi^4}{5M^5} \]
Generalization \((L^{\text{th}}\text{-Order Noise Shaping})\)

Modulator transfer function:
\[
Y(z) = z^{-L}X(z) + \left(1 - z^{-1}\right)^L E(z)
\]

In-band quantization noise:
\[
N_e^2 \approx \frac{\Delta^2 \cdot \pi^{2L}}{12 \cdot (2L + 1) \cdot \text{OSR}^{2L+1}}
\]

\[
SQNR = \left(\frac{3}{2}\right) \left(2^N - 1\right)^2 \left(\frac{(2L + 1) \cdot \text{OSR}^{2L+1}}{\pi^{2L}}\right)
\]

- Doubling OSR \((M)\) increases SQNR by \((6L+3)\) dB, or \((L+0.5)\) bit.
- Potential instability for 3\(^{\text{rd}}\)- and higher-order single-loop \(\Sigma\Delta\) modulators.

\[
SQNR(\text{dB}) = 6.02N + 1.76 + (2L + 1)10\log_{10} \text{OSR} - 10\log_{10} \frac{\pi^{2L}}{2L + 1}
\]
Equivalence of Continuous-Time & Discrete-Time $\Sigma\Delta$

- The key feature of the $\Sigma\Delta$ modulator is the noise shaping (NTF)
- To achieve equivalence between a continuous-time and discrete-time implementations, **Loop Gain should have the same properties**
- How can we realize the same NTF using continuous-time and discrete-time loop filters?

> The NTF is mainly determined by the transient response of the loop filter and the feedback DAC!
Types of Feedback DAC with Rectangular Pulses

- **NRZ**: Easy to design
- **RZD**: More tolerant to excess loop delay
Impulse Invariant Transformation

Transformations can be easily applied by decomposing the original DT (Z-domain) loop filter into partial fractions and use S-domain equivalences for the Z-domain poles to get the CT loop filter.
“Inherent Anti-aliasing” for narrow-band applications

$H_c(s)$ has a low-frequency gain over 40 dB, with a $-3$dB frequency equal to ADC bandwidth and unity gain frequency between 5-10 times higher.

Check $H_c(s)$ transfer function!
Oversampled A/D Conversion: Feedforward architecture

- Eq stands for the quantization noise
- Ed stands for DAC non-idealities (jitter + thermal noise)
- Filter’s thermal noise is accounted in Eh

- The modulator’s output becomes
  \[ Y = STF \times (X + E_d + E_h) + NTF \times E_q \]
- The error signal (Filter’s input) is
  \[ V_e = NTF \times \left\{ H(s) \times ZOH(X + E_d + E_h) + Z^{-1} \times E_q \right\} \]

\[
\begin{align*}
STF &= \frac{H(s) \times ZOH(s)}{1 + H(s) \times ZOH(s) \times Z^{-1}} \\
NTF &= \frac{1}{1 + H(s) \times ZOH(s) \times Z^{-1}}
\end{align*}
\]
The system parameters are defined as

- The lowpass transfer function $H(s)$ provides large loop gain (Noise shaping)
  - DC gain $>>0$ dB
  - Enough phase margin at 0 dB gain

- $Z$ is a complex number (phase)
- Loop stability is fundamental

$$STF = \frac{H(s) \cdot ZOH(s)}{1 + H(s) \cdot ZOH(s) \cdot Z^{-1}}$$

$$NTF = \frac{1}{1 + H(s) \cdot ZOH(s) \cdot Z^{-1}}$$

$$Z = e^{j\omega T_s}$$

$$ZOH(z) = T_s \cdot \sin c\left(\frac{\omega T_s}{2}\right)$$
Oversampled A/D Conversion

Feed-forward configuration

\[ Z = e^{j\omega T_s} \]

\[ ZOH(z) = T_s \sin c \left( \frac{\omega T_s}{2} \right) \]

Notice that

\[ ZOH(f) = \sin c \left( \pi \frac{f}{f_s} \right) \]
**Oversampled A/D Conversion**

Use Mason’s rule again!

\[ Z = e^{j\omega T_s} = \cos(\omega T_s) + j\sin(\omega T_s) \]

\[ ZOH(z) = T_s \cdot \sin c\left(\frac{\omega T_s}{2}\right) \]

\[ L(f) = H(z) \cdot ZOH(z) \cdot Z^{-1} \]

- **L(f)** is defined as the loop gain
- Phase of **L(f)** is quite important for stability
- **Z** is quite relevant for phase of **L(f)**
Continuous-Time $\Sigma\Delta$ Modulators

- For in-band frequencies STF is determined by $H(f)$
- At medium-high frequencies, the blocker rejection is limited (LTE)
- Peaking if phase of $L(f)$ phase margin is not enough
- At high-frequencies, the anti-alias is mainly provided by the sinc function rather than by the filter

$$\text{STF} = \frac{L(f) \ast Z}{1 + L(f)}$$

$$\text{NTF} = \frac{1}{1 + L(f)}$$
Remarks on DAC non-idealities. Same analysis apply to the input referred filter’s noise

 DAC non-idealities are reflected at the ADC output similarly to the signal

 Baseband noise can be directly mapped to ADC input (Ed and Eh)

 Non-linearities in DAC that translate HF noise into baseband affects directly SQNR

 DAC is an extremely critical component
Oversampled A/D Conversion

- Remarks on Filter’s operation: Filter’s input

For the single feedback loop architectures, the inband signal is usually very small: Nice property but...

Transition band is more critical for filter’s linearity (neighbor channels); is this bad? Could be worse and it is!

Medium and high frequency $1/(1+L)$ gain could be around 2-10 dB!

Filter must be designed for out-of-band blockers!
Remarks on Filter’s operation: Filter’s input

\[ V_e = \frac{X + E_d + E_h}{1 + L(s)} + NTF * Z^{-1} * E_q \]

- \( E_f \) is an out-of-phase replica of the \( X + E_f + E_h \) if \( L(f) >> 1 \)
- When loop gain reduces, the loop is less effective and all HF input signals appear at filter input
- Filter must be very linear at HF to minimize signal intermodulation distortions
- Filter must be designed for the blockers
- Blocker tolerance is a major issue in broadband applications (WiMAX)
Continuous-Time $\Sigma\Delta$ Modulators

- This is a realistic model
- Check the phase of the loop at the unity gain frequency!

\[ STF = \frac{L(f) \ast Z}{1 + L(f)} \]

\[ NTF = \frac{Z^{-1/2}}{1 + L(f)} \]
Stability Issues: $\Sigma \Delta$ Modulators

- Check the phase contribution of the **filter** and the **delay** element!
- Check the **phase of the loop** at the unity gain frequency!
- Can you stabilize the loop employing the conventional filter design approach?
- **Additional parasitic poles!**

$$\begin{align*}
\text{STF} &= \frac{L(f) \ast Z}{1 + L(f)} \\
\text{NTF} &= \frac{Z^{-1/2}}{1 + L(f)}
\end{align*}$$
Stability Issues: $\Sigma\Delta$ Modulators

- With a filter with 2 zeros (finite gain at high frequency)
- Hard to stabilize the loop if the unity gain frequency is close to $F_s/2$! (Very Low OSR)
- Notice that the delay element add -180 degrees at $f=F_s/2$
- If the loop unity gain frequency is not beyond $f=F_s/4$, then maximum phase contribution due to the delay element is $<-90$ degrees
Stability Issues: $\Sigma \Delta$ Modulators

- Not very difficult to stabilize the loop if the unity gain frequency is below $Fs/4$! (not very Low OSR); e.g. around 100Mhz if clock frequency is 400MHz

- Notice that larger oversampling ratio allow you to reduce the filter gain at high-frequency

- Out-of-Band noise is distributed in wider $n$=bandwidth, hence smaller noise density but same integrated noise
Oversampled A/D Conversion
Multiple Feedback architecture

This architecture presents several interesting properties, but be careful with its drawbacks!

- \( \text{Eq} \) stands for the quantization noise
- \( \text{Ed} \) stands for DAC non-idealities (jitter + thermal noise)
- Filter’s thermal noise is accounted in EH1,2
- D1,2 are the DAC coefficients

\[ Y = STF * \left( X + E_d + E_{H1} \right) + NTF * E_q + STF2 * E_{H1} \]

\[ STF = \frac{H_1(s) * H_2(s) * ZOH}{1 + \left\{ D1 * H_1(s) + D2 \right\} * \left\{ H_2(s) * ZOH * Z^{-1} \right\} } \]

\[ NTF = \frac{ZOH}{1 + \left\{ D1 * H_1(s) + D2 \right\} * \left\{ H_2(s) * ZOH * Z^{-1} \right\} } \]

\[ STF2 = \frac{H_2(s) * ZOH}{1 + \left\{ D1 * H_1(s) + D2 \right\} * \left\{ H_2(s) * ZOH * Z^{-1} \right\} } \]
Oversampled A/D Conversion
Feedback architecture

Notice that in-band STF is still approximately unity (1/D1 if D1H1 >> D2) up to the unity gain frequency

The error signal becomes:

\[
V_e = \frac{(X + E_d + E_{H1})(1 + D2 * H_2(s) * ZOH * Z^{-1})}{1 + \{D1 * H_1(s) + D2\} * \{H_2(s) * ZOH * Z^{-1}\}} + \text{NTF} * Z^{-1} * \left( H_2(s) * E_{H2} + E_q \right)
\]

In-band signal level at \( V_e \) is approximately obtained as

\[
V_e \approx \frac{(X + E_d + E_{H1}) * D2 + E_{H2}}{D1 * H_1(s) + D2} + \frac{E_q}{\{D1 * H_1(s) + D2\} * \{H_2(s)\}}
\]

\[
Y = \text{STF} * \left( X + E_d + E_{H1} \right) + \text{NTF} * E_q + \text{STF2} * E_{H2}
\]

\[
\text{STF} = \frac{H_1(s) * H_2(s) * \text{ZOH}}{1 + \{D1 * H_1(s) + D2\} * \{H_2(s) * \text{ZOH} * Z^{-1}\}}
\]

\[
\text{NTF} = \frac{\text{ZOH}}{1 + \{D1 * H_1(s) + D2\} * \{H_2(s) * \text{ZOH} * Z^{-1}\}}
\]

\[
\text{STF2} = \frac{H_2(s) * \text{ZOH}}{1 + \{D1 * H_1(s) + D2\} * \{H_2(s) * \text{ZOH} * Z^{-1}\}}
\]
Oversampled A/D Conversion Feedback architecture

\[ Y = STF \cdot (X + E_d + E_{H1}) + NTF \cdot E_q + STF2 \cdot E_{H2} \]

\[ STF = \frac{H_1(s) \cdot H_2(s) \cdot ZOH}{1 + L(f)} \]

\[ NTF = \frac{ZOH}{1 + L(f)} \]

\[ STF2 = \frac{H_2(s) \cdot ZOH}{1 + L(f)} \]

- Out of band STF is quite small; excellent for blockers rejection
- NTF follows the ZOH at very high frequencies, Minimizing the alias issue
- For STF2, again, the ZOH helps, but..
- The ZOH is excellent filter around f=fs

\[ L(f) = \{ D1 \cdot H_1(s) + D2 \} \cdot \{ H_2(s) \cdot ZOH \cdot Z^{-1} \} \]

The ZOH provides -4 dB attenuation at f=0.5fs and -20 dB at f=0.9fs
Oversampled A/D Conversion
Feedback architecture

For in-band signals apparently is fine:

\[
V_{e_1} = \frac{(X + E_d + E_{H_1}) \left(1 + D2 \ast H_2(s) \ast ZOH \ast Z^{-1}\right)}{1 + L(f)}
\]

- For in-band signals apparently is fine:

\[
V_{e_1} \approx \frac{(X + E_d + E_{H_1}) D2}{D1 \ast H_1(s) + D2}
\]

- At the output of H1(s) we get

\[
V_{H1-out} \approx \left(\frac{D2}{D1}\right)(X + E_d + E_{H_1})
\]

- This signal could be excessive for H2

For out-band signals:

\[
V_{e_1} = (X + E_d + E_{H_1}) \left(1 + D2 \ast H_2(s) \ast ZOH \ast Z^{-1}\right)
\]

- Most of the blockers and HF noise sources are present at H1 input
Oversampled A/D Conversion
Feedback architecture

For in-band signals:
\[ V_{e2} = \frac{ZOH \cdot Z^{-1} \cdot (H_2(s) \cdot E_{H2} + E_q)}{1 + L(f)} \]

At medium and HF only the ZOH helps

\[ V_{e2} = \frac{E_{H2}}{H_1(s)} + \frac{E_q}{H_1(s) \cdot H_2(s)} \]

Looks like \( E_{H2} \) and \( E_q \) are not the main issue in this topology.
Oversampled A/D Conversion
Multiple Feedback architecture

This linear model is probably more appropriated for the feedback architecture!

**ZOH does not affect the numerator of NTF**

\[
Y = STF \ast (X + E_d + E_{H1}) + NTF \ast E_q + STF \ast E_{H2}
\]

**Eq** stands for the quantization noise

**Ed** stands for DAC non-idealities (jitter + thermal noise)

Filter’s thermal noise is accounted in EH1,2

**D1,2** are the DAC coefficients

**STF**

\[
STF = \frac{H_1(s) \ast H_2(s) \ast ZOH}{1 + \left\{D1 \ast H_1(s) + D2\right\} \ast \left\{H_2(s) \ast ZOH \ast Z^{-1}\right\}}
\]

**NTF**

\[
NTF = \frac{1}{1 + \left\{D1 \ast H_1(s) + D2\right\} \ast \left\{H_2(s) \ast ZOH \ast Z^{-1}\right\}}
\]

**STF 2**

\[
STF 2 = \frac{H_2(s) \ast ZOH}{1 + \left\{D1 \ast H_1(s) + D2\right\} \ast \left\{H_2(s) \ast ZOH \ast Z^{-1}\right\}}
\]
Oversampled A/D Conversion
Feedback architecture

Notice that in-band STF is still approximately unity (1/D1 if D1H1>>D2) up to the unity gain frequency; D1 is usually set as 1

The error signal becomes:

\[ V_e = \frac{(X + E_d + E_{H1})(1 + D2 * H_2(s) * ZOH * Z^{-1})}{1 + \{D1 * H_1(s) + D2\} * \{H_2(s) * ZOH * Z^{-1}\}} + NTF * Z^{-1} * (H_2(s) * ZOH * E_{H2} + E_q) \]

In-band signal level at Ve is approximately obtained as

\[ V_e \approx \frac{(X + E_d + E_{H1}) * D2 + E_{H2}}{D1 * H_1(s) + D2} + \frac{E_q}{\{D1 * H_1(s) + D2\} * \{H_2(s) * ZOH\}} \]
Oversampled A/D Conversion
Feedback architecture

Out of band STF is quite small; excellent for blockers rejection

NTF does not follows the ZOH at very high frequencies

For STF2, again, the ZOH helps, but...

The ZOH is excellent around f=fs

The ZOH provides -4 dB attenuation at f=0.5fs and -20 dB at f=0.9fs
Oversampled A/D Conversion
Feedback architecture

\[ V_{e1} = \frac{(X + E_d + E_{H1})(1 + D2 \ast H_2(s) \ast ZOH \ast Z^{-1})}{1 + L(f)} \]

- For in-band signals apparently is fine if D2 is not very large
  \[ V_{e1} \approx \frac{(X + E_d + E_{H1})D2}{D1 \ast H_1(s) + D2} \]

- At the output of H1(s) we get
  \[ V_{H1-out} \approx \left( \frac{D2}{D1} \right)(X + E_d + E_{H1}) \]

- This signal could be excessive for H2

- For out-band signals:
  \[ V_{e1} \equiv (X + E_d + E_{H1})(1 + D2 \ast H_2(s) \ast ZOH \ast Z^{-1}) \]

- Most of the blockers and HF noise sources are present at H1 input
Oversampled A/D Conversion
Feedback architecture

For in-band signals:

\[ V_{e2} = \frac{Z^{-1} \left( H_2(s) \ast ZOH \ast E_{H2} + E_q \right)}{1 + L(f)} \]

At medium and HF only the ZOH helps

\[ V_{e2} = \frac{E_{H2}}{H_1(s)} + \frac{E_q}{H_1(s) \ast H_2(s)} \]

Looks like \( E_{H2} \) and \( E_q \) are not the main issue in this topology
DAC Non-idealities

- **Excess loop delay**: Constant delay between ideal and implemented DAC feedback pulse
  - Decision time required by quantizer affecting latches used for synchronizing DAC inputs
  - Finite response time of DAC to its clock and inputs
  - Excess Loop Delay can be incorporated: $Z^{-1} \rightarrow Z^{-1+\Delta}$

- **Inter-symbol interference**: Finite slew rate of DAC outputs with unequal rise and fall times
  - Additional noise and tones fold into baseband

- **Clock jitter in DAC**

- **DAC and Filter Non-linearity**

  Processed by STF
  Not noise-shaped
Typical Quantizer: Flash Architecture

- **S/H** operates at clock rate
- Huge input capacitance if \( N > 6 \)
  - Kick back noise
- Requires a precise low-impedance resistive ladder:
  - Power-accuracy-Speed tradeoff
- Limited by comparator
  - Speed and accuracy
  - Offset voltage
- Hard to improve its resolution

**State of the art:** \( \sim 2.4 \text{ GS/s} \) 6 bits resolution
Flash Based Quantizer Architecture

- Reference ladder consists of $2^N$ equal size resistors
- Input is compared to $2^N-1$ reference voltages.
- Massive parallelism
- Fastest ADC architecture
- Latency = $1T = 1/f_s$
- Throughput = $f_s$
- Complexity = $2^N$
ADC Input Capacitance

\[ \sigma^2(V_{T0}) = \frac{A_{VT0}^2}{WL} \Rightarrow C_g = 10 \, \text{fF/\mu m}^2 \]

- N = 6 bits → 63 comparators
- \( V_{FS} = 1\text{V} \) → 1 LSB = 16mV
- \( \sigma = \text{LSB}/4 \) → \( \sigma = 4\text{mV} \)
- \( A_{VT0} = 10\text{mV} \cdot \mu \text{m} \) → \( L = 0.24\mu \text{m}, \quad W = 26\mu \text{m} \)

<table>
<thead>
<tr>
<th>N (bits)</th>
<th># of comp.</th>
<th>( C_{in} ) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>15</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>63</td>
<td>3.9</td>
</tr>
<tr>
<td>8</td>
<td>255</td>
<td>16</td>
</tr>
</tbody>
</table>

- Small \( V_{os} \) leads to large device sizes, hence large area and power.
- Large comparator leads to large input capacitance, difficult to drive and difficult to maintain bandwidth.
Kick-back noise and coupling capacitors

- Preamp delay and $V_{th}$ of sampling switch ($M_9$) are both signal-dependent → signal-dependent sampling point (aperture error)
- A major challenge of distributing clock signals across $2^N-1$ comparators in flash ADC with minimum clock skew (routing, $V_{th}$ mismatch of $M_9$)
Fully-Differential Comparator

- Double-balanced, fully-differential preamp
- Switches (M_7, M_8) added to stop input propagation during regeneration
- Active pull-up PMOS added to the latch
**DAC Non-idealities**

### Sources of jitter error

- **Pulse-width jitter**: Random variation in charge fed back per clock cycle
  - Wide-band clock phase noise modulates out-of-band ADC inputs and quantization noise to in-band

- **Pulse-position jitter**: Random variation in integration interval of constant charge
  - Amplitude errors due to PP jitter are at least 1st-order noise-shaped

### Jitter errors in rectangular DAC pulse

- $t_{pn} = (b - a)T_S + D_{tn}$  \(\text{Pulse-position jitter}\)
- $t_{dn} = aT_S + D_{tn}$  \(\text{Pulse-position jitter}\)

---

\[H(s) \circledast T_S = \frac{1}{F_s}\]

\[V_{in} \rightarrow H(s) \rightarrow V_{dac}(t) \rightarrow \text{DAC} \rightarrow e_{samp}(t) \rightarrow D_{out}\]
Binary-Weighted CR DAC

\[ C_u = \text{unit capacitance} \]

- Binary-weighted capacitor array → most efficient architecture
- Bottom plate @ \( V_R \) with \( b_j = 1 \) and @ GND with \( b_j = 0 \)
**Binary-Weighted C-DAC**

- $C_p \rightarrow$ gain error (nonlinearity if $C_p$ is nonlinear)
- INL and DNL limited by capacitor array mismatch

$$V_o = \left( \frac{2^N C_u}{C_p + 2^N C_u} \right) \cdot V_R \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$

$$V_o = \left( \frac{\sum_{j=1}^{N} b_{N-j} \cdot 2^{N-j} C_u}{C_p + C_u + \sum_{j=1}^{N} 2^{N-j} C_u} \right) \cdot V_R$$
Stray-Insensitive C-DAC

\[ V_o = \left( \frac{2^N C_u}{2^N C_u + \frac{C_p + 2^{N+1} C_u - C_u}{A}} \right) \cdot V_R \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j} \]

Large gain A needed to attenuate summing-node charge sharing
**Binary-Weighted Current Steering DAC**

- Current switching is simple and fast.
- \( V_o \) depends on \( R_{\text{out}} \) of current sources without op-amp.
- INL and DNL depend on matching, not inherently monotonic.
- Large component spread \( (2^{N-1}:1) \)

\[
V_o = IR \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}
\]
- 2^N current cells typically broken up into a (2^{N/2} X 2^{N/2}) matrix
- Current source cascoded to improve accuracy
- Coupled inverters improve synchronization of current switches.
Randomization and Dummies

- Column and row randomization to improve INL

Dummy-cell

Active-cell
Example: “8+2” Segmented Current DAC

DAC Non-idealties in CT ΔΣ ADCs - 2

Effects of DAC non-linearity

- Non-linearity caused due to mismatch between different output levels of DAC
  - Variation in feedback levels yields signal-dependent feedback charge error directly fed to the modulator input.

- Low resolution feedback DAC requires linearity better than overall modulator
This is a major (hot) research area in multi-bit sigma-delta modulators. Several alternatives have been reported; main trends are:

- Randomize the errors such that the non-linear errors are converted in noise instead of tones that degrades SNDR
  - Dynamic element matching techniques
  - Pseudo Randomizers such as Rotators
  - Digital signal processors
  - Drawbacks?

- Calibration
  - By design using large overdrive voltages and large dimensions
  - Pre-calibration of current cells
  - Other options?

DAC Calibration (Signal-to-Distortion Ratio)
Current Cell Design Considerations

Matching considerations

- Sizing of current source transistors

\[
W^2 = \frac{1}{2K_p \left(\frac{\Delta I_d}{I_d}\right)^2} \left[ \frac{A_B^2}{(V_{gs} - V_t)^2} + \frac{4A_{V_t}^2}{(V_{gs} - V_t)^4} \right]
\]

\[
L^2 = \frac{K_p}{2I_d \left(\frac{\Delta I_d}{I_d}\right)^2} \left[ \frac{A_B^2}{(V_{gs} - V_t)^2} + 4A_{V_t}^2 \right]
\]

Output impedance

- Greater than 700kΩ over 100MHz signal bandwidth
  - Sufficient for 12-bits static (INL) and dynamic linearity (SFDR)

Trade-off

- Higher overdrive voltage provides better area efficiency at the expense of reduced output swing
- Larger area results in greater parasitic capacitances which limit the speed of operation

<table>
<thead>
<tr>
<th>DACi</th>
<th>Unit current</th>
<th>(W/L), m=4</th>
<th>Total area, µm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC1-coarse</td>
<td>610uA</td>
<td>203µ/3.84µ</td>
<td>7795</td>
</tr>
<tr>
<td>DAC1-fine</td>
<td>35uA</td>
<td>48µ/16µ</td>
<td>7680</td>
</tr>
<tr>
<td>DAC2</td>
<td>1.55mA</td>
<td>323µ/2.4µ</td>
<td>6976</td>
</tr>
<tr>
<td>DAC3</td>
<td>960uA</td>
<td>255µ/3µ</td>
<td>6885</td>
</tr>
<tr>
<td>DAC4</td>
<td>790uA</td>
<td>231µ/3.36µ</td>
<td>6985</td>
</tr>
</tbody>
</table>
**Multi-bit DAC Architecture: DEM**

- Dynamic Element Matching (DEM), Self-calibration combined to achieve high linearity
- When DAC$_i$ is under calibration, demultiplex Data$_i$ to dummy current cell

![Diagram of Multi-bit DAC Architecture: DEM](image_url)
Dynamic Element Matching

Representing DAC input $v$ using a thermometer DAC

- $v = 1$ can be represented by any one of $I_{1-8}$
- Averaging all possible combinations produces the ideal output
- Use different combinations to represent a given code
- Errors are randomized

Graph showing $v = 1$ and $v = 3$ with corresponding currents and timing.
Implementation of DEM Scheme

- Shifter performs a Rotate-right shift on its inputs
- PN-sequence generator indicates number of shifts
- DEM is operated at 2GHz to maximize randomization
PN-Sequence Generator

- Generates maximal length sequence based on 3\textsuperscript{rd}-order primitive polynomial

\[ P(x) = x^3 + x^2 + 1 \]

State: 1011
At the end of a calibration cycle, $C_{CAL}$ attains the correct $V_{GS}$ required to generate $I_{ref}$.
Multi-bit Calibrated DAC

- Calibration control signals generated using a N-bit CMOS Ring Counter
- Extra dummy current cell used to implement continuous background calibration
Current Calibration Circuit

Calibration reference:
Shared by all Current Cells

Unit Current Cell
Simulation Results

Output Spectrum

- Frequency (MHz)
- Power (dB)

<table>
<thead>
<tr>
<th>Mismatch</th>
<th>DEM</th>
<th>Self-calibration</th>
<th>SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>N</td>
<td>N</td>
<td>73.8</td>
</tr>
<tr>
<td>Y</td>
<td>N</td>
<td>N</td>
<td>55</td>
</tr>
<tr>
<td>Y</td>
<td>Y</td>
<td>N</td>
<td>63.6</td>
</tr>
<tr>
<td>Y</td>
<td>N</td>
<td>Y</td>
<td>70</td>
</tr>
<tr>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>72.7</td>
</tr>
</tbody>
</table>
Clock Jitter Sensitivity (SJNR)

- The effect of clock jitter is present at the input of the quantizer and DAC.
- Jitter induced noise at DAC output is processed according to the NTF, which is a serious problem for continuous-time sigma-delta modulators.
Modeling Clock Jitter in NRZ DACs

Error depends on the height & number of transitions in the DAC output waveform.

- NRZ DACs have a transition height $y(n) - y(n-1)$, one transition every $T_s$.
- RZ DACs have a transition height $2y(n)$, two transitions every $T_s$.

RZ DACs are MUCH more sensitive to clock jitter!
Review and advances in delta-sigma DAC error estimation based on additive noise modelling

Ivar Løkken · Anders Vinje · Bjørnar Hernes · Trond !

\[ e_{jit}(t) = \sum_{n=0}^{N-1} \left[ y_a(nT) - y_a((n-1)T) \cdot \frac{1}{T} \Pi_{j(nT)} \left( nT + \frac{j(nT)}{2} \right) \right] \cdot \text{sign}(j(nT)) \].

(23)

Considering a single error pulse on this form, for simplicity denoting its amplitude \( A \) and width \( J \), taking the Fourier transform gives the spectrum:

\[ E_J(f) = \int_{t=0}^{J} A \cdot e^{-i \cdot 2 \pi f \cdot t} |_{J\geq 0} = \int_{t=J}^{0} A \cdot e^{-i \cdot 2 \pi f \cdot t} |_{J<0} \]

\[ = \frac{A \cdot \sin(2\pi Jf)}{2\pi f} \cdot e^{-i \pi Jf} \]

\[ = A \cdot J \cdot \sin c(Jf) \cdot e^{-i \pi Jf}. \]

(24)
Jitter Insensitivity of Switched-Capacitor DACs

• So far, SC-DAC is the most jitter tolerant approach
• Quite precise and may not require further calibration procedures

**Drawbacks of the SC DAC**
• Peak current in the SC-DAC can be as high as 10 time IDAC used in the current mode DAC!
• Very demanding SR for the OPAMP: Power consumption
• Class AB OPAMP may help while dealing with this issue
Clock Jitter Sensitivity (SJNR)

Relationship between jitter and Phase noise: Let’s consider a jittered signal

\[ \cos \left( \omega_o t + \varphi_n \right) \]

The phase of the noisy signal is then computed as

\[ \omega_o \left( t + \frac{\varphi_n}{\omega_o} \right) = \omega_o \left( t + \frac{T \cdot \varphi_n}{2 \pi} \right) \]

Therefore, timing error can now be estimated as follows:

\[ \Delta T = \frac{\varphi_n}{2 \pi} \]

We can find the clock jitter variance employing the eye diagram, and making the following histogram
Clock Jitter Sensitivity (SJNR)

$$\cos(\omega_0 t + \varphi_n)$$

$$\left( \frac{\Delta T}{T} \right)^2 = \left( \frac{\varphi_n}{2\pi} \right)^2$$

Then

$$RMS\ J_{per} = \left( \frac{T}{2\pi} \right) \sqrt{\int_{-\infty}^{\infty} \phi_n^2(f)\,df}$$

RMS value of total jitter

$$RMS\ J_{per} = \left( \frac{T}{2\pi} \right) \sqrt{2 \int_{0}^{\infty} (L(f))\,df}$$

Timing spectrum is correlated with phase noise measured in the spectrum analyzer

$$L(f) = 10^{\frac{L(dBc)}{10}}$$

-160 -140 -120 -100 -80 -60 -40 -20 0

10.0k 100.0k 1.0M 10.0M 100.0M Hz
Jitter Issues: High Clock Frequency

The DAC error due to clock jitter:

\[ J_{\text{error}}(n) = \left( D_{\text{out}}(n) - D_{\text{out}}(n-1) \right) \left( \frac{\Delta T(t)}{T} \right) \]

In the frequency domain: Differential of Dout convolves with Jn(\(\omega\))

\[ J_{\text{error}}(\omega) = \left[ (1 - Z^{-1})D_{\text{out}}(\omega) \right] \otimes J_n(\omega) = \left[ \left( 2 \sin(\frac{\omega T_s}{2}) \right) D_{\text{out}}(\omega) \right] \otimes J_n(\omega) \]

In-band signal is shaped by \(1 - Z^{-1}\), then it is not very critical

Out-of-Band quantization noise and blockers convolve with the clock jitter
Effect of clock jitter and Quantization noise on SNR

\[ e_j(n) = (V_{out}(n) - V_{out}(n-1)) \frac{\Delta t(n)}{T} \]

then

\[ E_j(Z) = \left\{ (1 - Z^{-1}) \right\} \left( V_{out}(Z) \right) \otimes (J(Z)) \]

Or

\[ E_j(Z) = \left\{ (1 - Z^{-1}) \right\} \left( STF(Z) \ast V_{in}(Z) + NTF(Z) V_q(Z) \right) \otimes (J(Z)) \]

Therefore

\[ E_j(Z) = \left\{ (1 - Z^{-1}) \right\} STF \ast V_{in}(Z) \otimes J(Z) + \]

\[ + \left\{ (1 - Z^{-1}) \right\} NTF \ast V_q(Z) \otimes (J(Z)) \]

\[ \left| 1 - Z^{-1} \right| = 2 \left| \sin \left( \frac{\omega T_s}{2} \right) \right| \]

\[ P_{j,S} \approx 2 \int_0^{1/2OSR} \left| E_j(Z) \right|^2 d\theta \]

\[ P_{j,Q} \approx 2 \int_0^{1/2OSR} \left| (1 - Z^{-1}) \right| \left( NTF(Z) V_q(Z) \right) \otimes (J(Z)) \right|^2 d\theta \]

Quantization noise

Clock Phase Noise

SJNR is function of the convolution of NTF and J(Z)
Continuous-Time BP-ΣΔ ADC: Jitter effects

\[ SJNR_{NRZ} = 60 \text{ dB} \Rightarrow \]
\[
\left( \frac{OSR \cdot P_{in}}{4} \right) \left( \frac{T_s}{\sigma_j} \right)^2 > 1
\]
\[
\sigma_j \approx 10^{-3} \cdot T_s
\]

In absence of blockers, assuming white jitter, the jitter induced noise has been usually approximated as:

\[
SJNR_{NRZ} = 10 \log_{10} \left( \frac{P_{in}}{\int_{BW} J_n^2 \otimes (1 - Z^{-1})^2 \cdot P_{Quantization} \cdot df} \right)
= 10 \log_{10} \left( \frac{OSR \cdot P_{in} \cdot \text{sinc}^2 \left( \frac{\omega_0 T_s}{2} \right)}{4 \left( \frac{\sigma_j}{T_s} \right)^2} \right)
\]
**Continuous-Time ΣΔ ADC: Jitter & Blockers**

RF clock filtering is an effective method to partially overcome this issue!

J Silva et.al., SRC report Dec 2010

- High frequency blockers convolve with Jn and are folded back in band.
- Considering $P_{\text{blocker}}$ and $P_{\text{quantization}}$

\[
SJNR \approx 10 \log_{10} \left( \frac{P_{in}}{ \int_{BW} \left( J_n^2 \otimes (1 - Z^{-1})^2 \right) P_{\text{Quantization}} + J_n^2 \otimes (1 - Z^{-1})^2 P_{\text{Blocker}} df } \right)
\]

\[
SJNR_{noBlocker} - 10 \log_{10} \left( 1 + \frac{\int_{BW} \left( J_n^2 \otimes (1 - Z^{-1})^2 P_{\text{Blocker}} df } { \int_{BW} \left( J_n^2 \otimes (1 - Z^{-1})^2 P_{\text{Quantization}} df \right) } \right)
\]
Effect of clock jitter on SNR: Quantization noise + Blockers

\[ e_j (n) = (V_{out}(n) - V_{out}(n-1)) \frac{\Delta t(n)}{T} \]

\[ E_j(Z) = \left\{ (1 - Z^{-1}) (V_{out}(Z)) \right\} \otimes (J(Z)) \]

\[ E_j(Z) = \left\{ (1 - Z^{-1}) \text{STF} \ast V_{in}(Z) \right\} \otimes J(Z) + \]

\[ + \left\{ (1 - Z^{-1}) \text{NTF} \ast V_q(Z) \right\} \otimes (J(Z)) \]

\[ P_{j,S} \equiv 2 \int_{0}^{1/2 \text{OSR}} \left| E_j(Z) \right|^2 d\theta \]

\[ P_{j-inband} \equiv 2 \int_{0}^{1/2 \text{OSR}} \left| (1 - Z^{-1}) \left\{ (\text{STF} \ast V_{Blockers}(\omega) + \text{NTF} \ast V_q(\omega)) \otimes (J(\omega)) \right\} \right|^2 d(\omega T_s) \]
A Jitter-Tolerant 12-Bit ΣΔ Modulator

SNR>12 bits, Power < 20mW, BW= 20 MHz, OSR=10

Challenges:

- **Calibration procedure:** NTF will be optimized through the calibration tones
- **Low-sensitivity to clock jitter:** Emulated switched-capacitor DACs
- **Robust against blockers:** Feedback based topology
- **Extremely linear filters:** IM3 @ 20 MHz < 75 dB Full scale
**Main goal:** ENOB ≥ 14 bits, SQNR > 16 bits, Total power < 50mW, BW = 20 MHz, OSR = 10

- Fully calibrated modulator
- Low-sensitivity to clock jitter: clock jitter as high as 10 psecs (RMS)
- Robust against blockers: 5th-order feedback-based topology
## System-level Design Considerations

\[
SQNR(dB) = 6.02N + 1.76 + (2L + 1)10\log_{10} OSR - 10\log_{10} \frac{\pi^{2L}}{2L + 1}
\]

### Design Trade-offs:

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>Value Change</th>
<th>Trade-offs</th>
</tr>
</thead>
</table>
| Order of modulator, \( L \) | \( L \uparrow \) | - Reduced stability,  
- Less robust to PVT variations |
| Oversampling ratio, \( OSR \) | \( OSR \uparrow \) | Limited by \( f_T \) of technology                                      |
| Quantizer resolution, \( N \) | \( N \uparrow \) | - Improved stability  
- Improved clock jitter tolerance  
- More power, area in quantizer  
- Limited by non-linearity of feedback DAC |
| Max. NTF gain, \( NTF_{\text{max}} \) | \( NTF_{\text{max}} \uparrow \) | - Reduced stability  
- More sensitive to clock jitter |
| Max. stable amplitude, \( MSA \) | \( MSA \uparrow \) | \( L \downarrow, N \uparrow, NTF_{\text{max}} \downarrow \) |
System-level Optimization

- Order of modulator (L), and OSR set by target SQNR (~80dB) and settling time requirements on 1st integrator stage
  
  \[ L = 5, \text{OSR} = 10 \]

- Order of modulator (L), and OSR set by target SQNR (~80dB)
  
  \[ L = 5, \text{OSR} = 10 \]

- A number of tradeoffs involved

- Just picking values is not a good approach

- EDUCATED GUESSES!
Order of modulator ($L$), and OSR set by target SQNR (~80dB)

High-Q filters give you better SQNR (due to picking in the gain; better in-band noise)

Implications on filter’s signal swing and out-of-band noise?
System-level Optimization

- Maximum Signal Amplitude Increase with number of levels and with small NTF values

- Several tradeoffs involved
High-Q sections is synonymous of higher $\text{NTF}_{\text{max}}$ and better in-band NTF

However, MSA decreases, then it is unclear if your SQNR is better or not
### Loop Filter Design Considerations - 2

**5th Order CT Loop Filter**

<table>
<thead>
<tr>
<th>Block</th>
<th>Order</th>
<th>DC Gain (dB)</th>
<th>Cut-off freq. (MHz)</th>
<th>Q</th>
<th>IM3 (dB)</th>
<th>SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Biquad 1</td>
<td>2</td>
<td>20</td>
<td>18.4</td>
<td>3</td>
<td>-78</td>
<td>74</td>
</tr>
<tr>
<td>Biquad 2</td>
<td>2</td>
<td>20</td>
<td>10.8</td>
<td>4</td>
<td>-60</td>
<td>60</td>
</tr>
<tr>
<td>Integ</td>
<td>1</td>
<td>19</td>
<td>3.2</td>
<td></td>
<td>-60</td>
<td>60</td>
</tr>
<tr>
<td>Filter</td>
<td>5</td>
<td>59</td>
<td>20</td>
<td></td>
<td>&lt; -76</td>
<td>72</td>
</tr>
</tbody>
</table>
A 14 Bit Continuous-Time Delta-Sigma A/D Modulator With 2.5 MHz Signal Bandwidth

Zhimin Li and Terri S. Fiez, Fellow, IEEE

The resolution of an oversampling ΔΣ A/D modulator is a function of the oversampling ratio (OSR), loop order (L) and the number of quantizer bits (N), as expressed by

\[
DR = \frac{P_s}{P_N} = \frac{3}{2} \left( \frac{2L + 1}{\pi^{2L}} \right) (2^N - 1)^2 \text{OSR}^{2L+1}. \quad (1)
\]

\[
\text{SNR}_{\text{jitter}} = \frac{P_s}{P_{\text{jitter}}} = \frac{A^2/2}{\sigma^2 e_{\text{NRZ}}/\text{OSR}} = \frac{\text{OSR} \cdot A^2}{2\sigma^2 \Delta y_{\text{NRZ}} \left( \frac{\sigma_{\Delta y}}{T} \right)^2}
\]
Fig. 5. Output spectrum of the CT modulator for –3 dBFS input.
A Continuous-Time $\Sigma\Delta$ ADC With Increased Immunity to Interferers

Kathleen Philips, Member, IEEE, Peter A. C. M. Nuijten, Raf L. J. Roovers, Member, IEEE,
Arthur H. M. van Roermund, Senior Member, IEEE, Fernando Muñoz Chavero,
Macarena Tejero Pallarés, and Antonio Torralba, Senior Member, IEEE
A 20-mW 640-MHz CMOS Continuous-Time \(\Sigma\Delta\) ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB

Gerhard Mitteregger, Member, IEEE, Christian Ebner, Member, IEEE, Stephan Mechnig, Member, IEEE, Thomas Blon, Member, IEEE, Christophe Holuigue, and Ernesto Romani, Member, IEEE
Fig. 10. Four-bit quantizer with 4-bit flash ADC and reference voltage generation plus feedback DAC.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>PERFORMANCE SUMMARY</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sampling Frequency</strong></td>
<td>640MHz</td>
</tr>
<tr>
<td><strong>Conversion Rate</strong></td>
<td>40MS/s</td>
</tr>
<tr>
<td><strong>Input Range</strong></td>
<td>0-20MHz</td>
</tr>
<tr>
<td><strong>Peak SNR</strong></td>
<td>76dB</td>
</tr>
<tr>
<td><strong>THD</strong></td>
<td>-78dB</td>
</tr>
<tr>
<td><strong>Peak SNDR</strong></td>
<td>74dB</td>
</tr>
<tr>
<td><strong>ENOB</strong></td>
<td>12</td>
</tr>
<tr>
<td><strong>Process</strong></td>
<td>1.2V 130nm 1P8M CMOS</td>
</tr>
<tr>
<td><strong>Chip Area</strong></td>
<td>8.6mm²</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td></td>
</tr>
<tr>
<td>Modulator</td>
<td>20mW</td>
</tr>
<tr>
<td>Decimator 40MS/s</td>
<td>18mW</td>
</tr>
<tr>
<td>PLL 2.56GHz</td>
<td>12mW</td>
</tr>
<tr>
<td>I/O 1.8V</td>
<td>4mW</td>
</tr>
</tbody>
</table>
A 3-mW 74-dB SNR 2-MHz Continuous-Time Delta-Sigma ADC With a Tracking ADC Quantizer in 0.13-μm CMOS

Lukas Dörrer, Franz Kuttner, Patrizia Greco, Patrick Torta, and Thomas Hartig

third-order 4-bit ΔΣ architecture.
The DEM is usually slow and may lead to significant loop delay!

May require loop compensation

Nice feature: Robust against blockers!
A 12-Bit, 10-MHz Bandwidth, Continuous-Time $\Sigma\Delta$ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer

Matthew Z. Straayer, Student Member, IEEE, and Michael H. Perrott, Member, IEEE
TABLE II
COMPARISON WITH PUBLISHED HIGH-SPEED CT ADCS

<table>
<thead>
<tr>
<th>Ref.</th>
<th>$F_S$ (MHz)</th>
<th>BW (MHz)</th>
<th>SNR (dB)</th>
<th>SNDR (dB)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[12]</td>
<td>276</td>
<td>23</td>
<td>70</td>
<td>69</td>
<td>43</td>
</tr>
<tr>
<td>[13]</td>
<td>340</td>
<td>20</td>
<td>71</td>
<td>69</td>
<td>56</td>
</tr>
<tr>
<td>[14]</td>
<td>400</td>
<td>12</td>
<td>64</td>
<td>61</td>
<td>70</td>
</tr>
<tr>
<td>[16]</td>
<td>640</td>
<td>20</td>
<td>76</td>
<td>74</td>
<td>20</td>
</tr>
<tr>
<td>[17]</td>
<td>1000</td>
<td>8</td>
<td>63</td>
<td>63</td>
<td>10</td>
</tr>
<tr>
<td>This work</td>
<td>950</td>
<td>10</td>
<td>86</td>
<td>72</td>
<td>40</td>
</tr>
</tbody>
</table>