High linearity, Low cost SAW-less Radios

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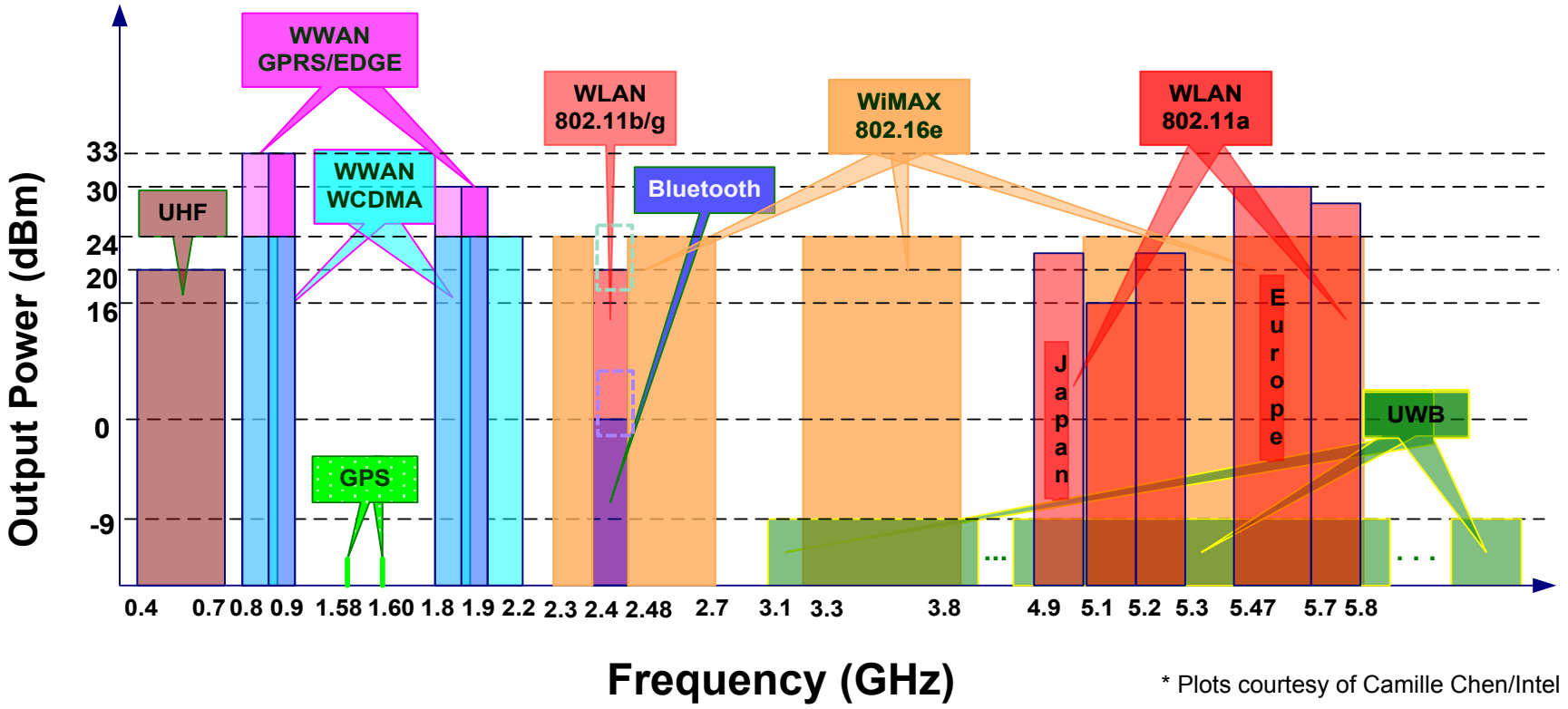
Outline

- Introduction
- Broadband LNAs with non-linearity cancellation
- Fully balanced LNTAs with P_{1dB} > 0dBm
- A 12 bit, 20MHz, C.T $\Delta\Sigma$ ADC
- Active Antenna
- Conclusions

Introduction

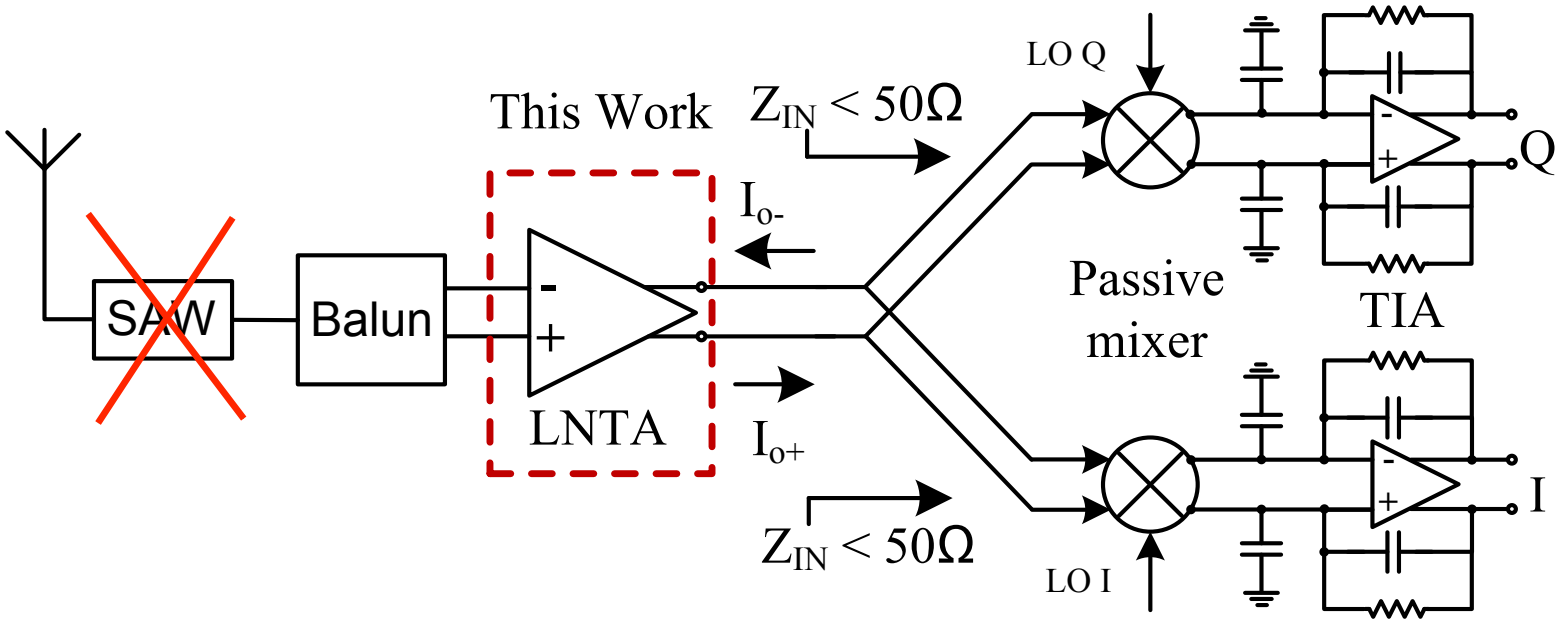


* Plots courtesy of Camille Chen/Intel

Low cost radio receivers for multi standard co-existence

- Low cost: SAW-less and Inductor-less solution.
- High linearity receivers to deal with strong out-of-band interferers

Targeted system



Direct Conversion Receiver Architecture:

Better performance in terms of noise, linearity and power consumption.

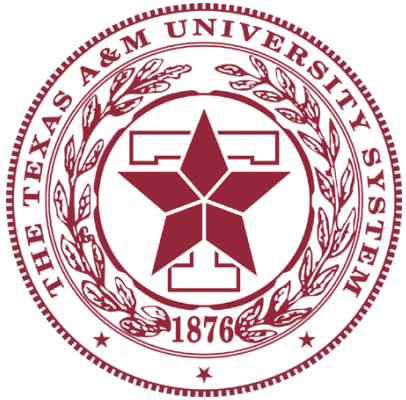
Linearity bottleneck → LNTA

Broadband CMOS LNAs with Nonlinearity Cancellation

Hemasundar M Geddada[1], José Silva-Martínez[1], and Stewart S. Taylor[2]

[1]Texas A&M University

[2]Intel Corporation



A 12-bit, 20Mhz, Analog-to-Digital Converter for Broadband Applications

H. M. Geddada, C. J. Park, H. J. Jeon,
J. Silva-Martinez, A. I. Karsilayan

SRC sponsored project
Task 1836.038

Outline

- Background and motivation
- Task overview and introduction
- Proposed ADC topology
- Digital current-DAC calibration
- Effect of blockers
- Static blocker filtering
- Saturation detection and attenuation for instantaneous blockers
- Effect of clock jitter
- Clock filtering for improving jitter tolerance
- Complete ADC design, chip floor-plan and performance summary
- Current status and conclusions

Background and Motivation

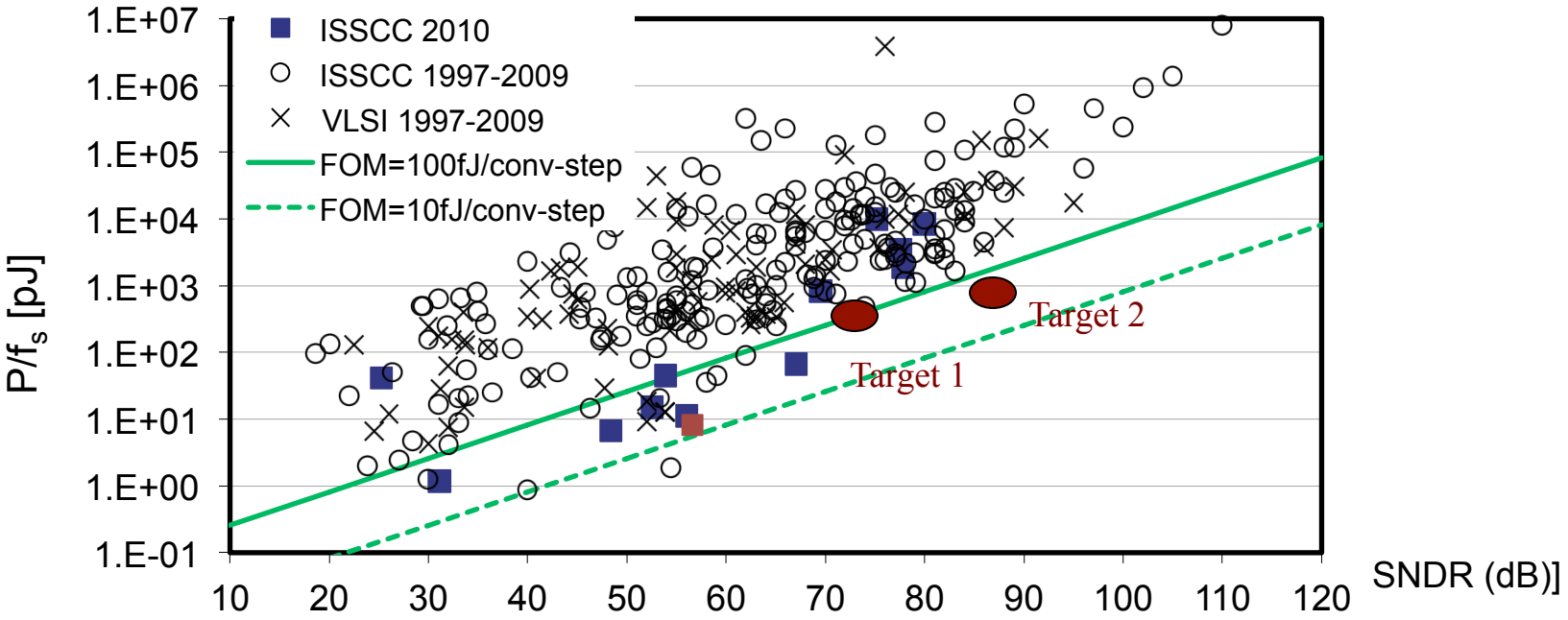
Key Needs

- Broadband analog-to-digital converters have been identified as a relevant need in the International Technology Roadmap for Semiconductors (ITRS)
- TxACE call for proposals indicates Broadband Analog-to-Digital conversion as a major industry need

Potential Applications

- Broadband wireless networks requiring high resolution analog-to-digital conversion solutions
- Multi-standard receiver applications where the desired signal has to be detected in the presence of strong out of band (OOB) blockers
- Mobile computing devices require low-power solutions

State-of-the-art and Targets



First Task:

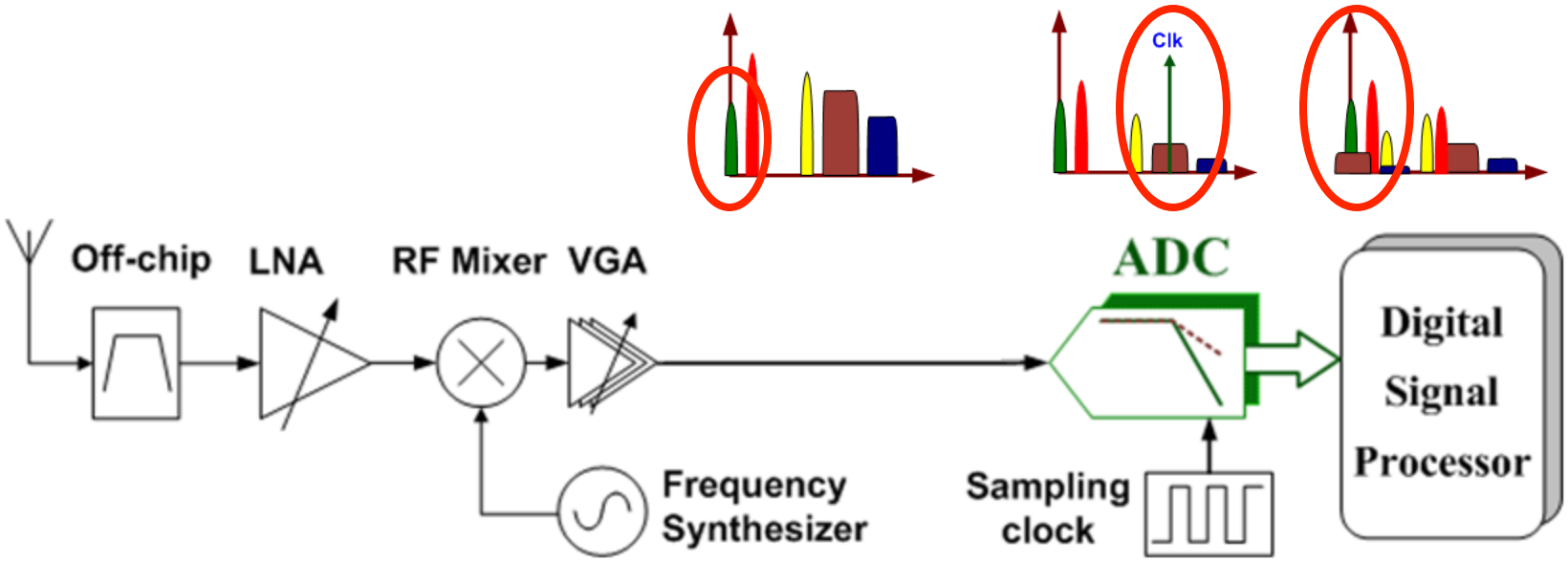
B. Murmann, http://www.stanford.edu/~murmann/adcsurvey.html.

- 5th order 12 bit, 20MHz ADC in 90nm technology
- Total power consumption of the core ADC < 20 mW
- Figure of merit in the range of 200 fJ/conversion step
- Highly blocker tolerant (blockers up to 0dBFS)
- Second Task:
- 15-bit ΔΣ modulator with quantization noise cancellation

Task Overview

- Efficient techniques for the design of low-voltage low-power $\Delta\Sigma$ modulators in deep-submicron technologies.
  - New digital calibration techniques to improve the linearity of the DAC.
  - A fully calibrated 5th-Order 20MHz 14-bit $\Delta\Sigma$ modulator with low blocker and jitter sensitivity.

DC Broadband Receiver



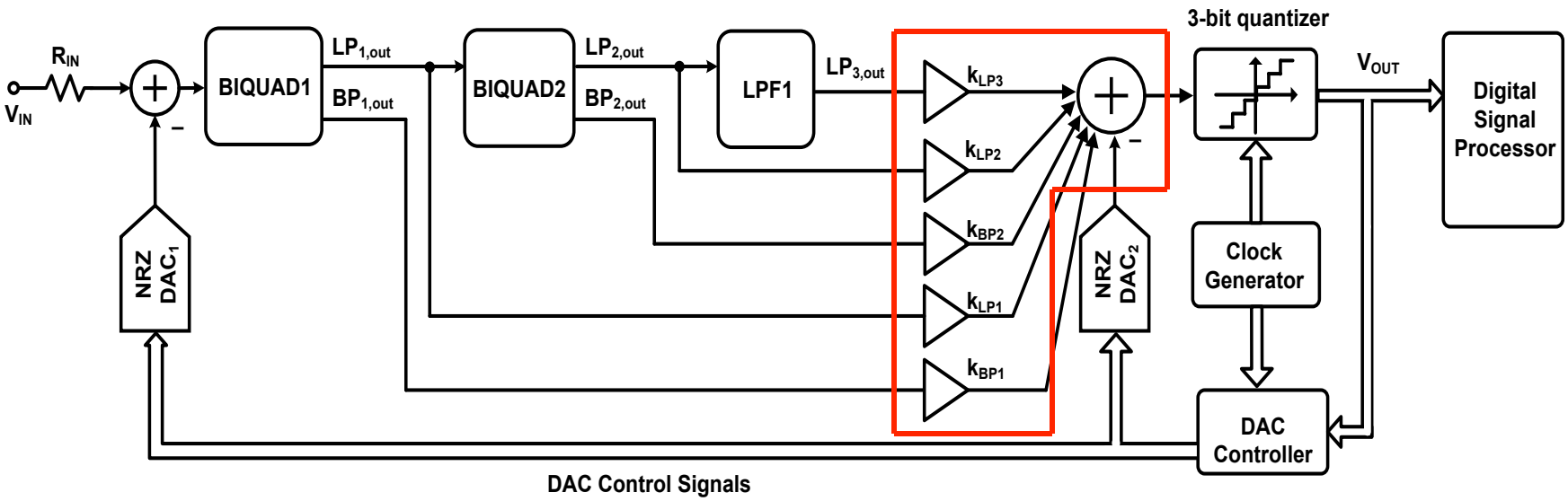
System issues in broadband systems:

- High frequency filtering is especially critical in broadband applications
- Blocker rejection: ADC filtering must be complemented by LP filtering

Trade-offs:

- Light filtering in front demands an ADC with higher Dynamic Range (DR)
- Higher DR ADC implies more power and more circuit complexity

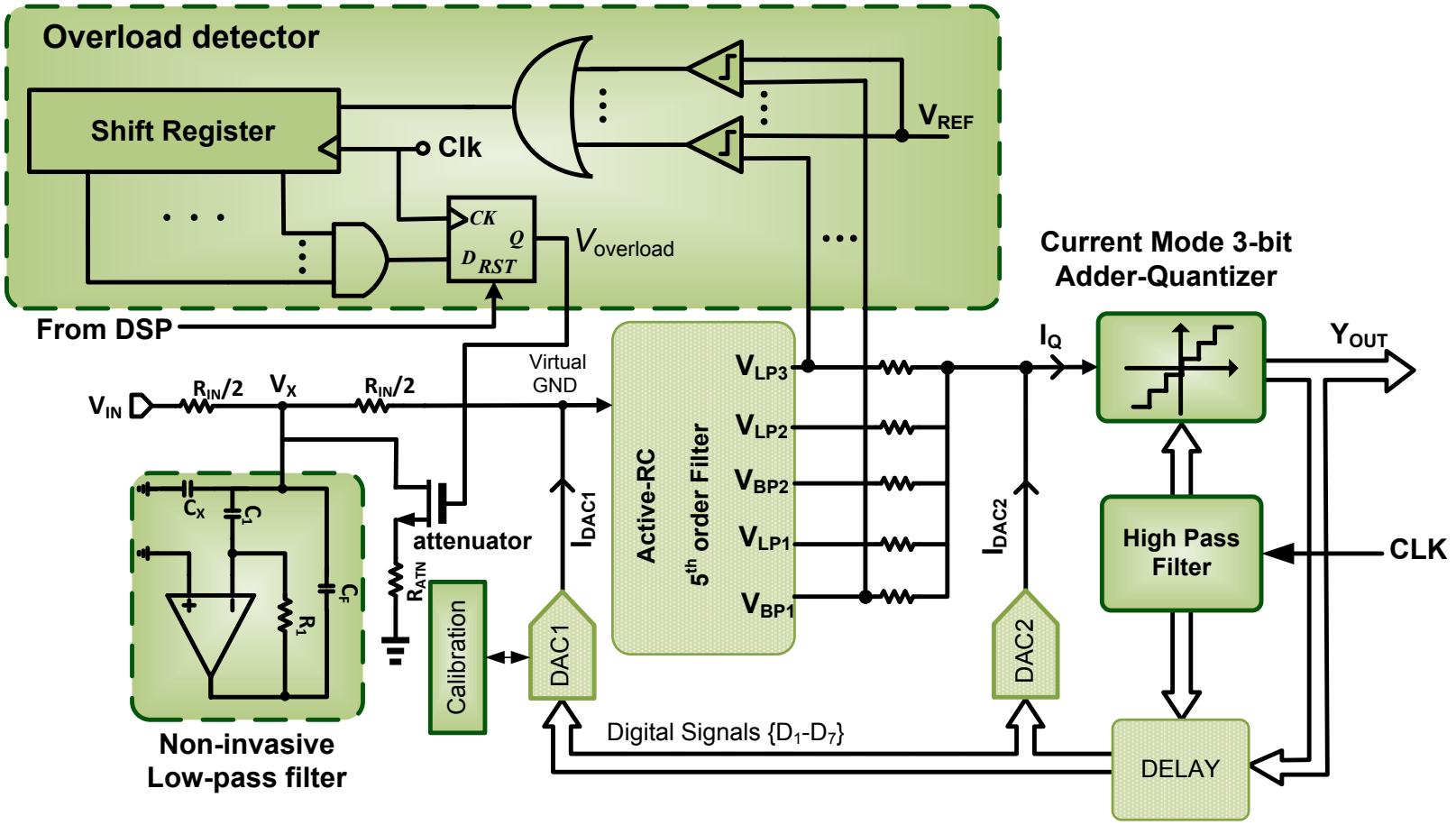
ADC Feed-Forward Architecture



5th Order CT Low-Pass ΔΣ ADC Feed-Forward Architecture

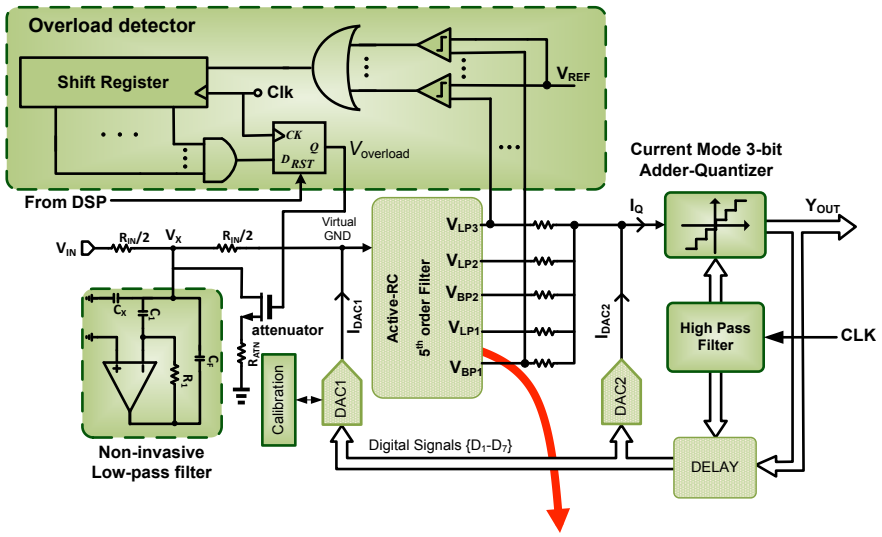
- Low power consumption
- Reduced complexity: one critical DAC
- Highly sensitive to DAC errors
- 1st order attenuation to OOB blockers and OOB peaking

Complete ΣΔ Modulator

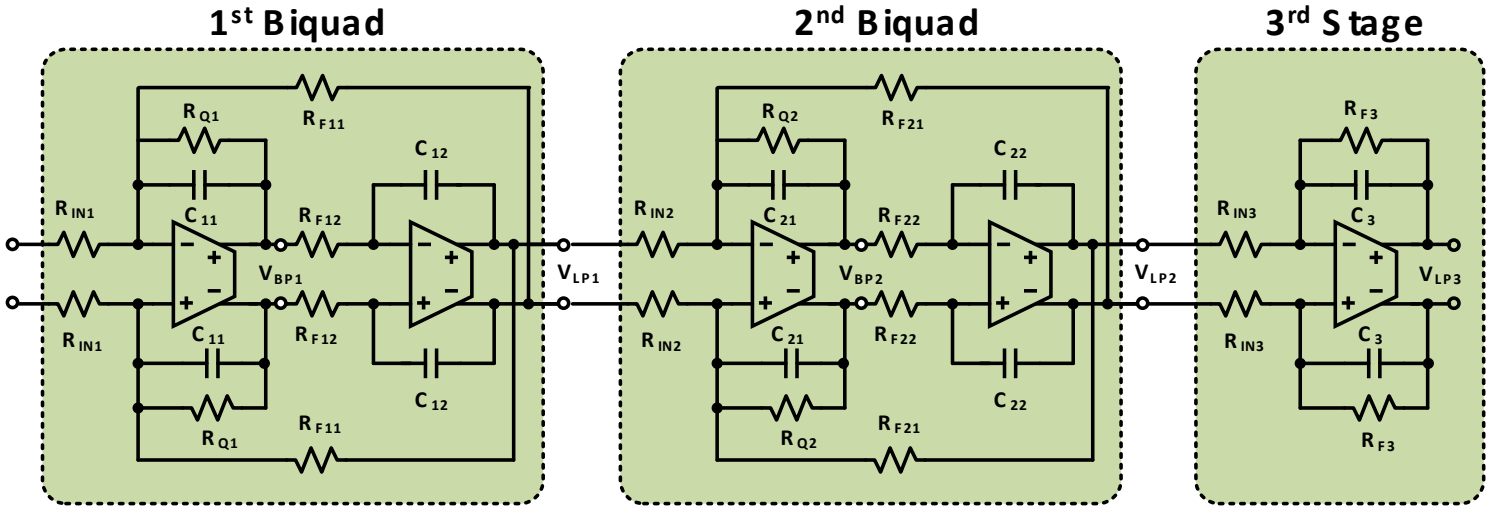


- Schematic of the full system

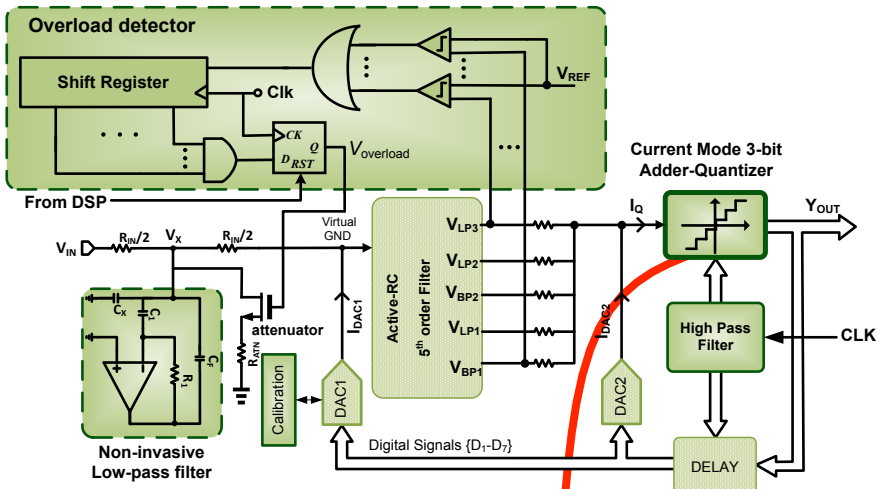
5th Order Loop filter



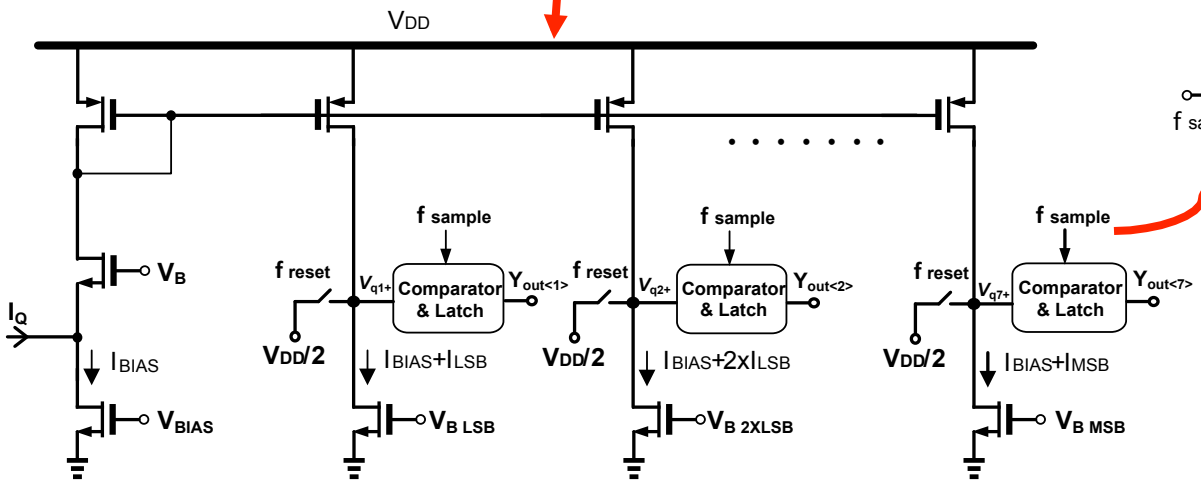
- 5th Order Active-RC loop filter
- Active RC realization to achieve high linearity
- Operational transconductance amplifiers use feed-forward compensation

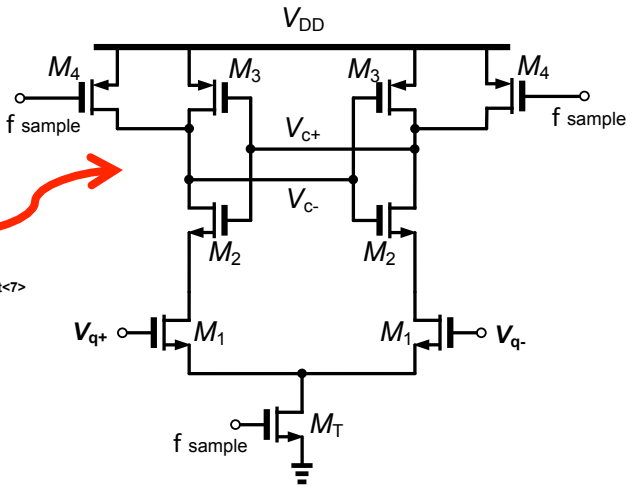


Current-Mode Adder-Quantizer



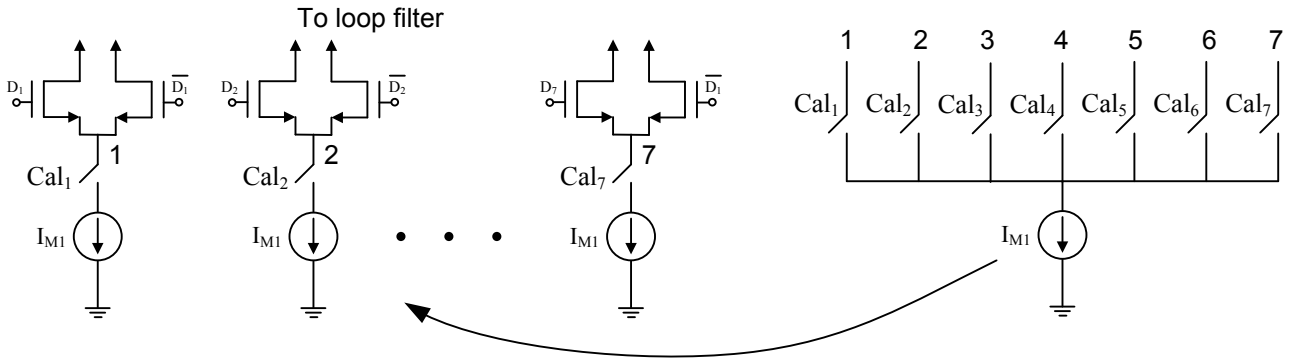
- Current-mode adder-quantizer realization
- Low power solution
- Reduced complexity





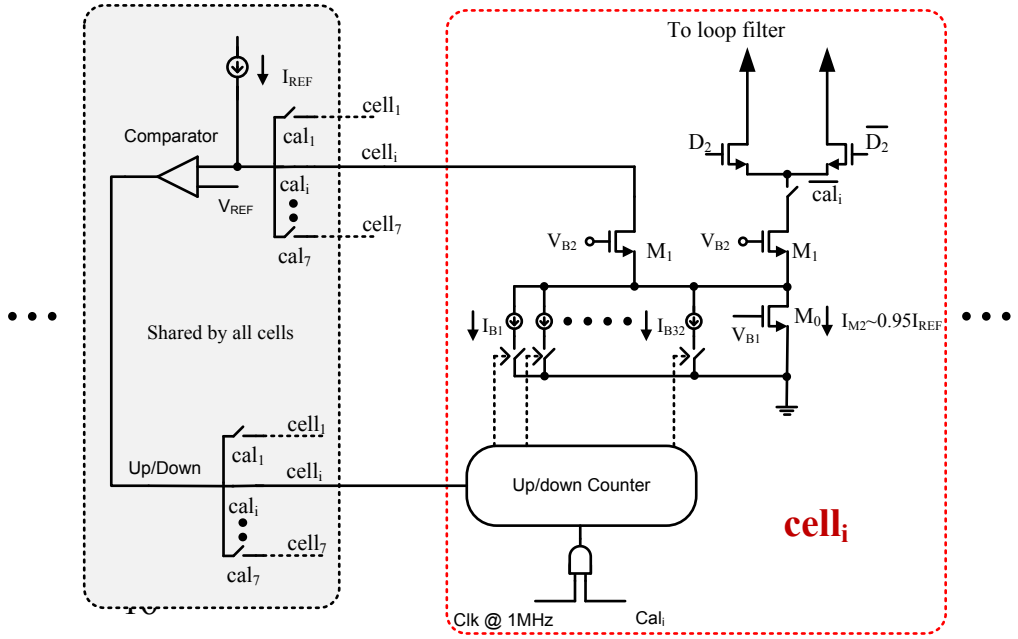
Efficient Current-Mode Adder-Quantizer Strong-Arm Comparator

Digital Calibration of DAC_1



- Online calibration
- Robust to process variations

Spare current source takes the position of current source being calibrated



Calibration Properties

- Robust to process variations
- 32 current sources
- Granularity ~ 0.15%
- Calibration is stored digitally
- Glitch free

Effect of Blockers

- **Blocker:**

  Any unwanted signal that degrade the sensitivity of receiver

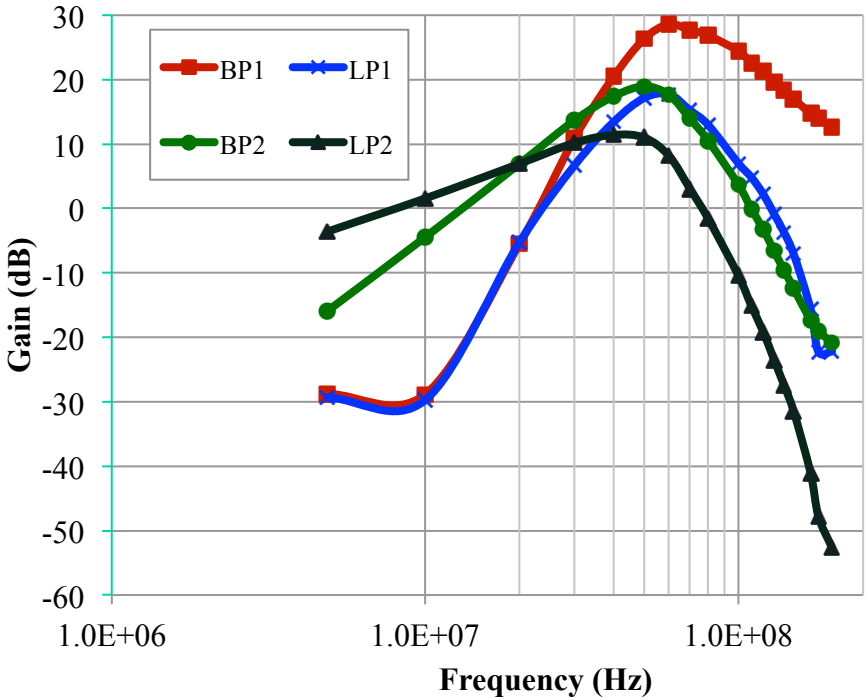
1. **Steady state:**
   Steady state blocker rejection depends on the OOB attenuation of the system
2. **Transient:**

   Large internal gain stages and finite delay in the feedback of $\Delta\Sigma$ loop makes the system vulnerable to blockers during transient

- **Main issues:**

1. Filter and/or quantizer saturation make the loop unstable and usually requires reset to be operative again
2. Higher order ADCs take long time (µseconds-seconds) to get back to linear operation after reset

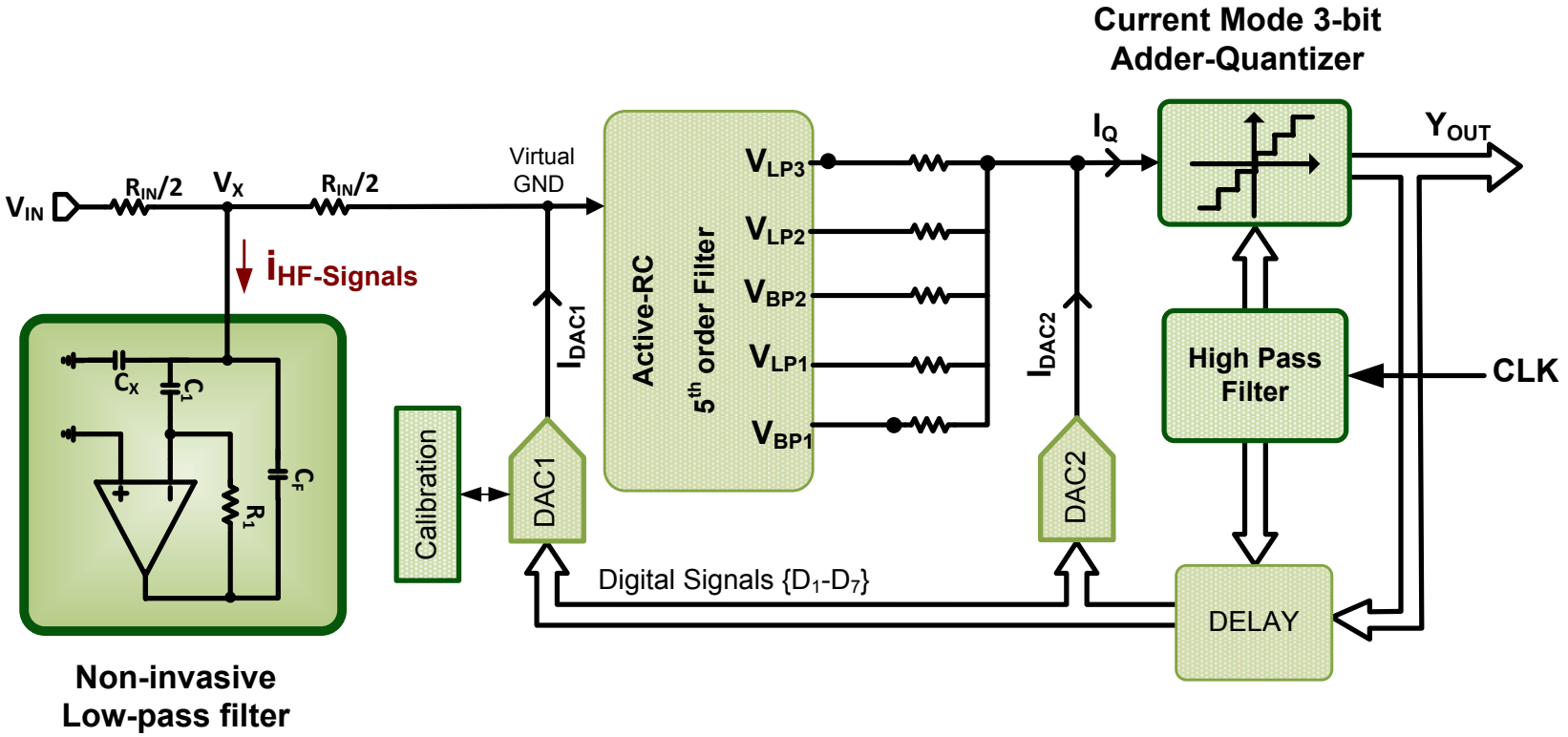
Closed-Loop Gain at Internal Nodes



- Feed-forward paths cause peaking at the internal nodes
- Adjacent/alternate channel frequency blockers at ~30-150MHz may overload internal nodes and quantizer.
- Large time constants are associated with the internal nodes for 10Mhz poles. So resetting the system is a slow process and not acceptable in real time communications.

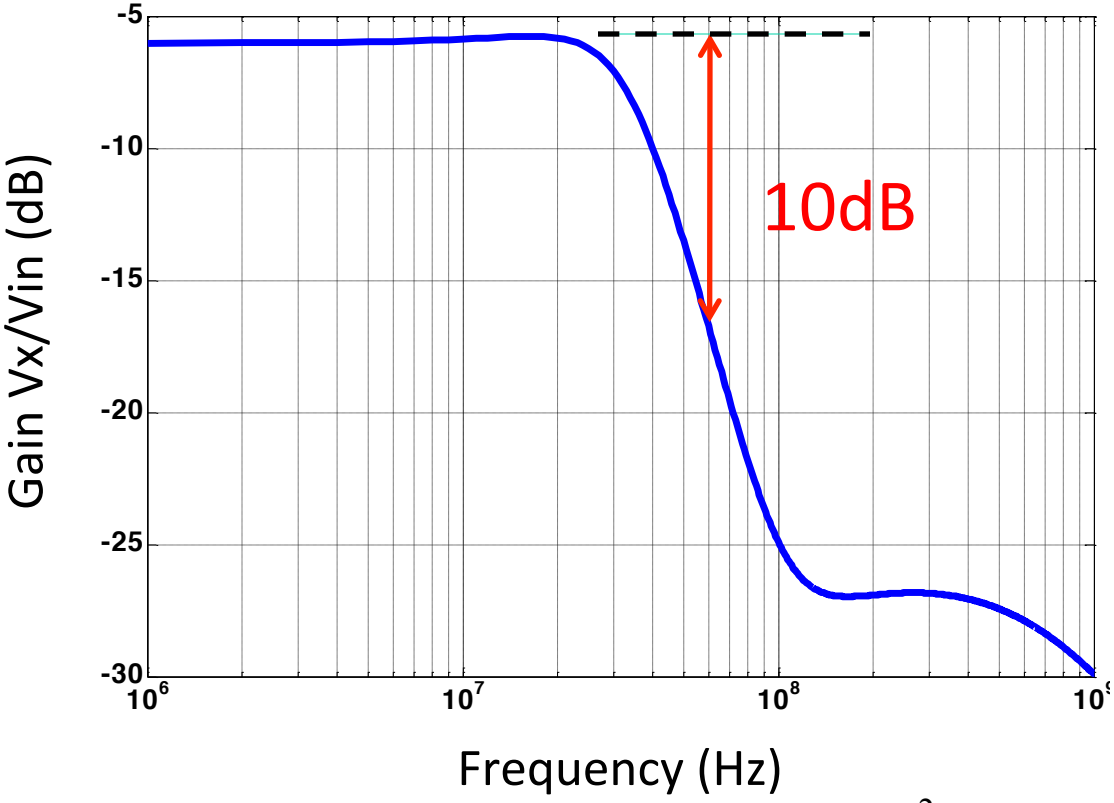
- There is not enough loop gain at critical frequencies to reduce the blockers at internal nodes.
- Improvement in the steady state blocker tolerance can be achieved by filtering critical frequency bands.

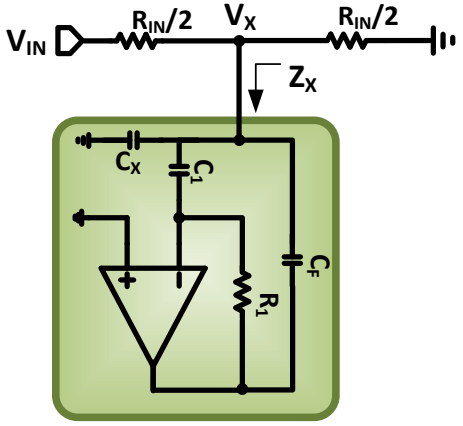
High-Frequency Blocker Filtering



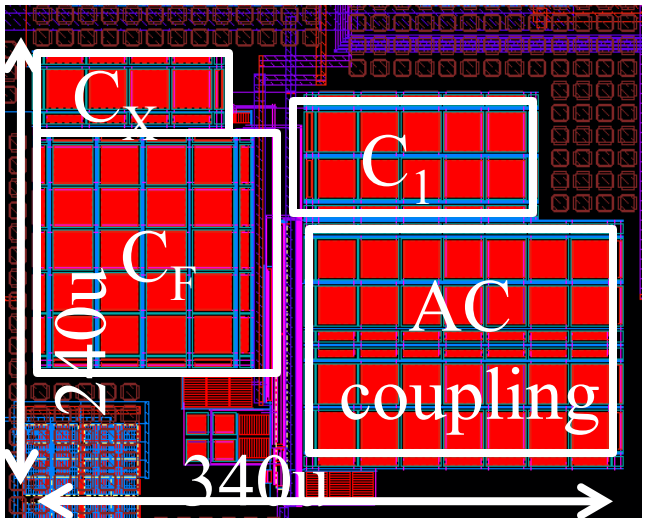
- Non-invasive LPF is implemented outside the loop
- Can also be integrated into the TIA (RF-IC 2011, Perez-Taylor-Silva-Karsilayan)
- In-band noise is not affected
- Low-power solution

Blocker Filtering: Non-Invasive LPF





Non-invasive
Low-pass filter



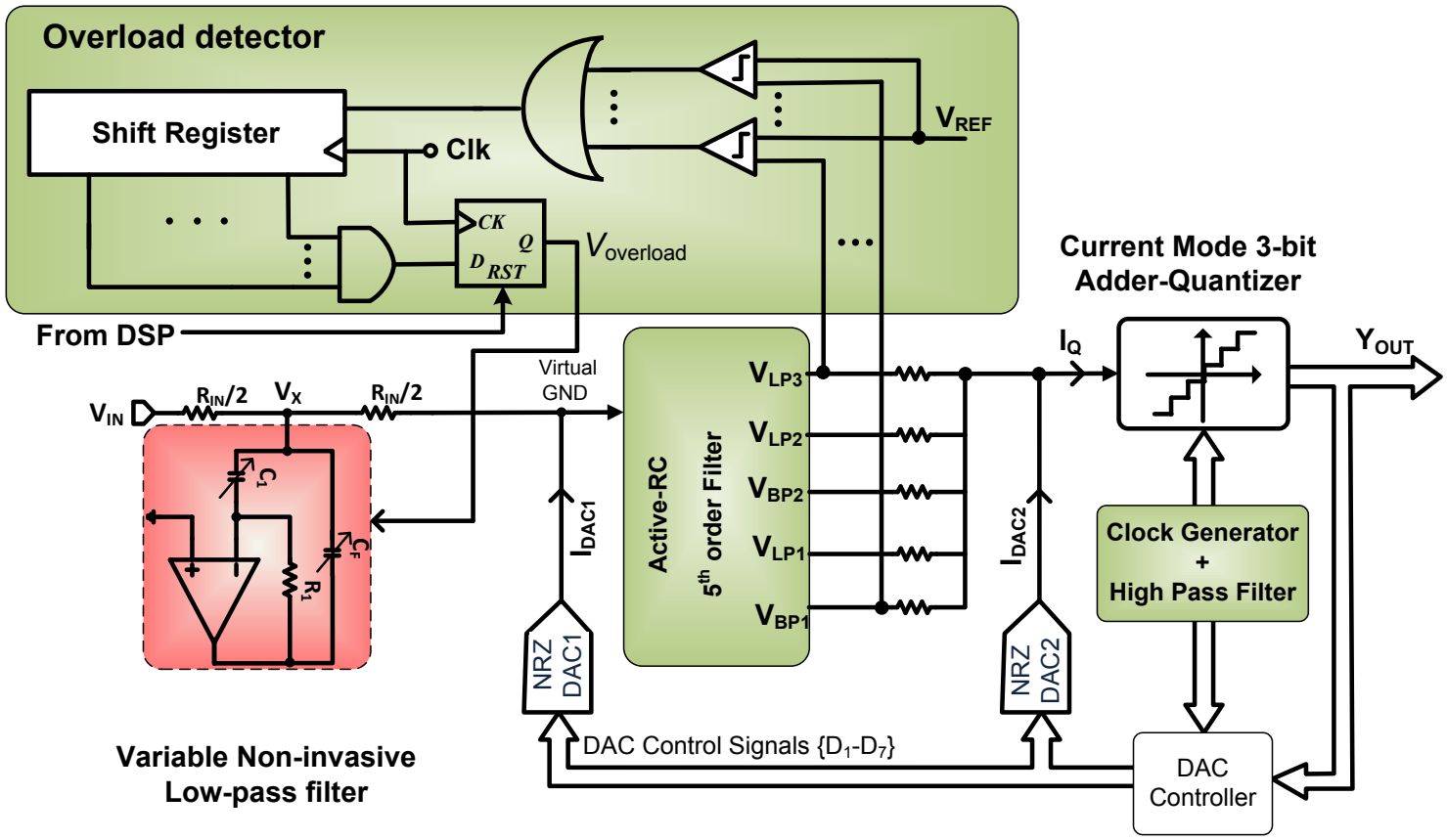
- 10dB attenuation at 60MHz
- Power: 2.25mW
- Area: 0.0816mm^2

$$Z_X = \frac{0.5\omega_0^{\,2} R_{IN}/2}{S^2 + \omega_0 S/Q}$$

$$f_0 = 20Mhz$$

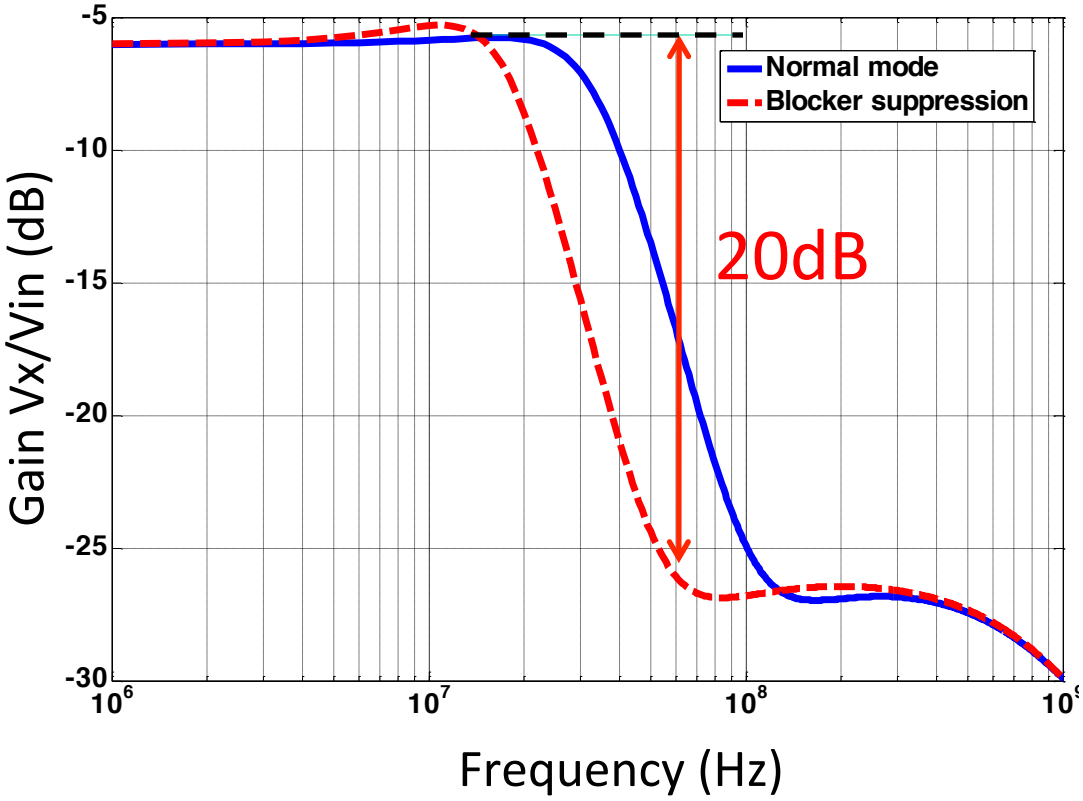
$$Q = 0.7$$

Programmable Non-Invasive LPF



- Programmable BW for the low pass filter
- Overload detector controls the BW of the LPF

Programmable Non-Invasive LPF



- In blocker suppression mode, LPF gives 20dB of attenuation at (60-80MHz).
- Band-edge droop is maintained to be less than 3dB at 20MHz.

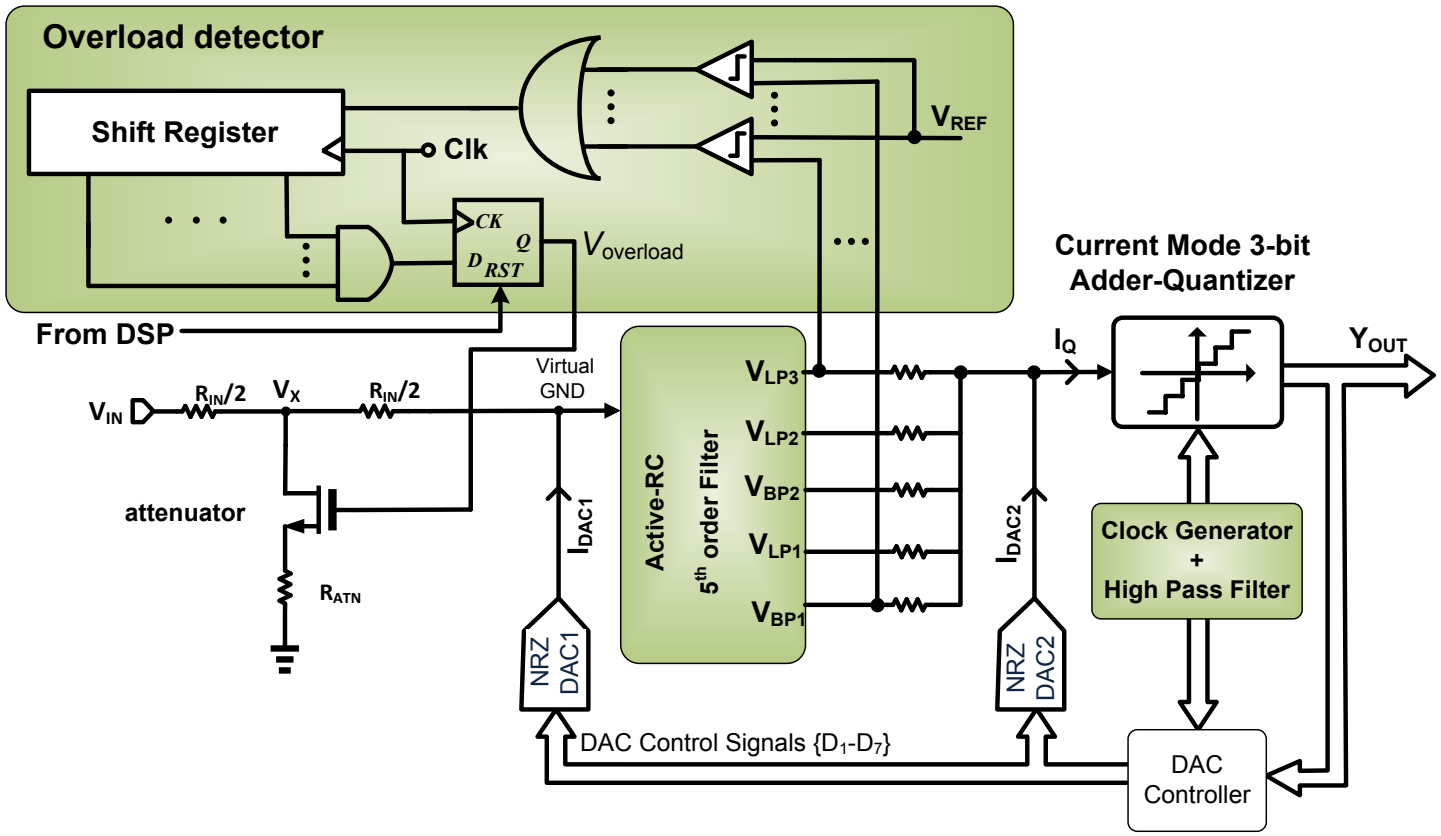
  → can be recovered in post digital processing.

Instantaneous Blockers

What are effects of the agile (fast time variant) blockers?

- Instantaneous blockers during transient may also saturate the ADC and then breaking the communication
- The protection technique must react very fast to avoid loop saturation
- In the case of strong blockers, moderate SNR is better than no communication
- High-frequency loop linearity is critical to minimize the power of inter-modulation products
- Regular feedback is not fast enough to react to the instantaneous blockers. Need a faster feedback to avoid the system from getting overload because of the instantaneous blockers.

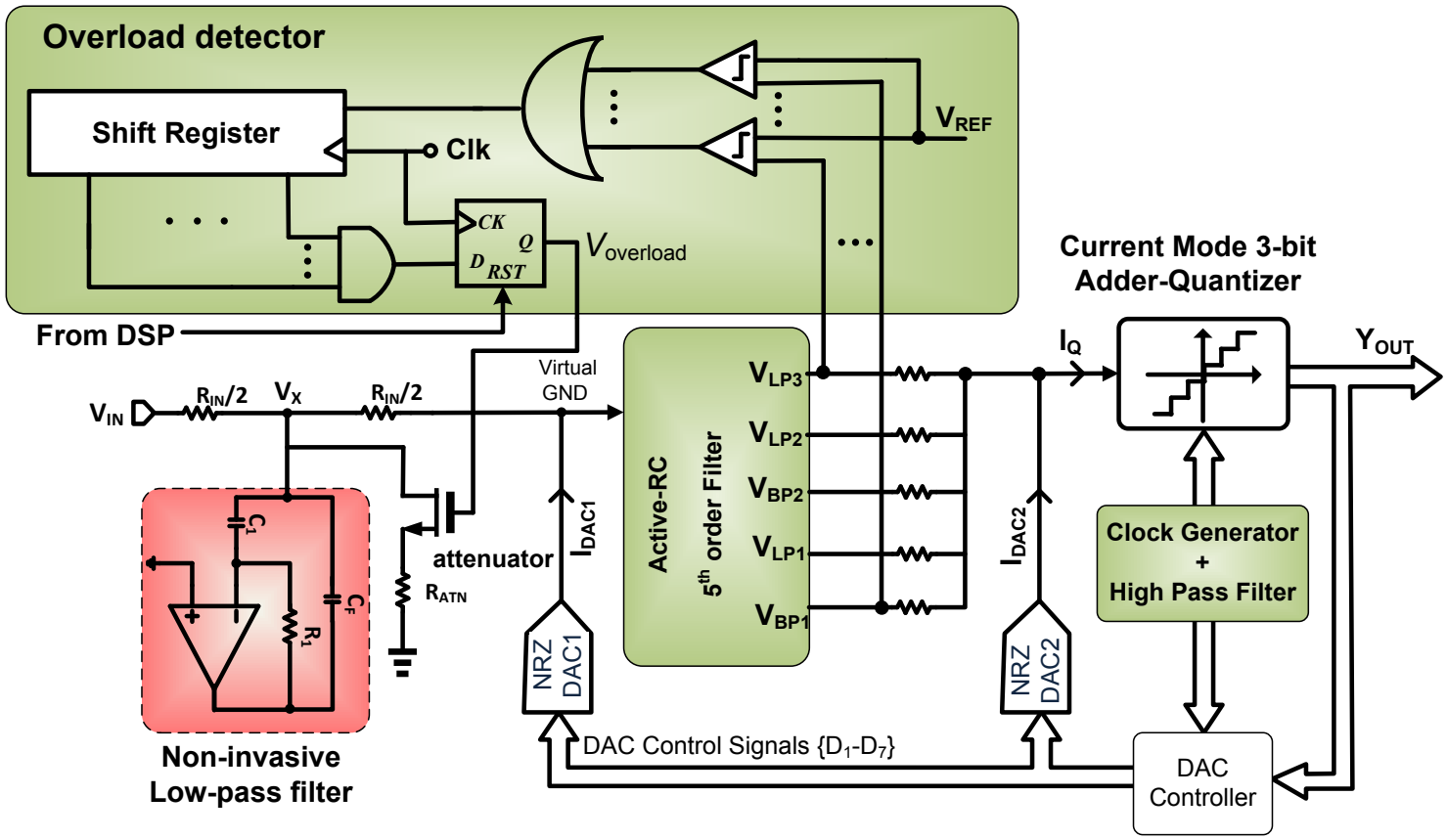
Saturation Detector & Attenuator



- Filter overload is detected through overload detectors
- The programmable (out of the loop) attenuator is activated when systematic overload is detected

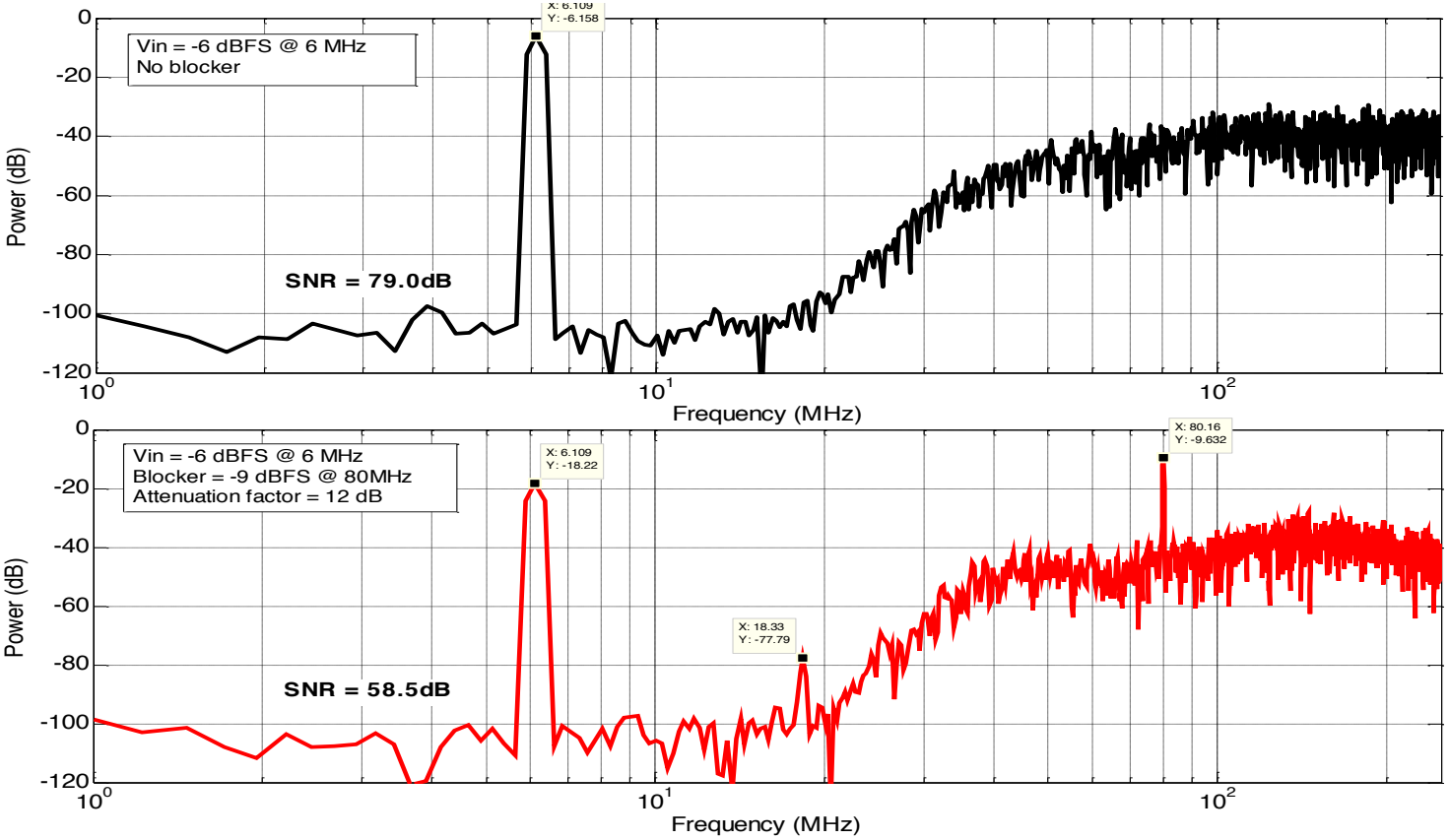
- SNR reduces but loop stability can be guaranteed

Blocker protection



- Static blocker filtering through the Non-invasive LPF
- Agile/fast blockers are attenuated through the Overload detector and attenuator

SNR in the Presence of a Blocker



No blocker
Quasi-Linear system

Saturation detector attenuates the input signal by 12dB

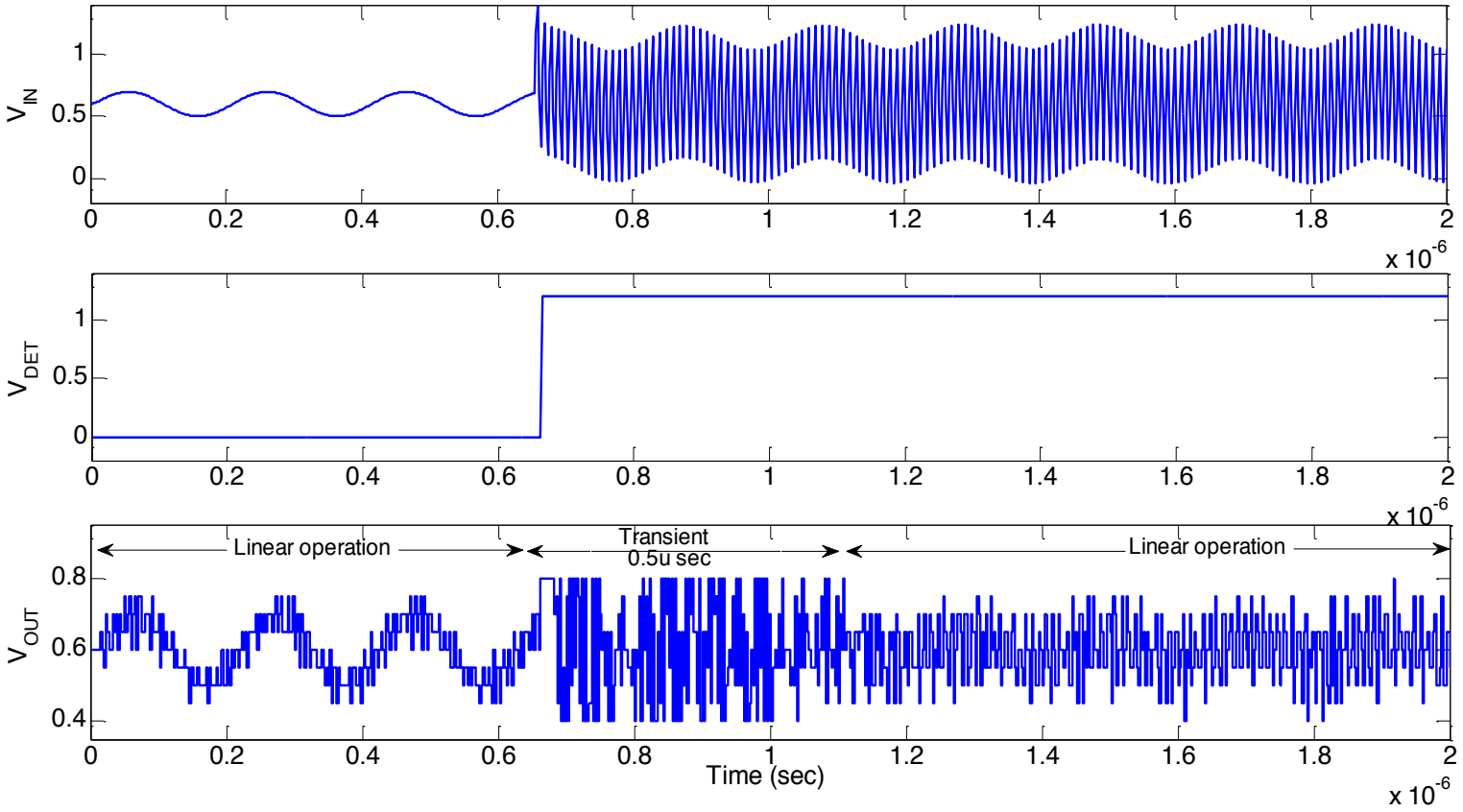
- SNR degradation in the presence of blocker is 29dB
- Additional decrement in SNR is due to rise in noise floor
- High internal voltage swings tends to push the system into the non-linear regime.

Loop Settling Time = 0.5µsec

Input signal

Saturation detector output

ADC output



Transient response of the ADC to an 8dBFS blocker at 100MHz in the presence of a -6dBFS in-band signal at 5MHz

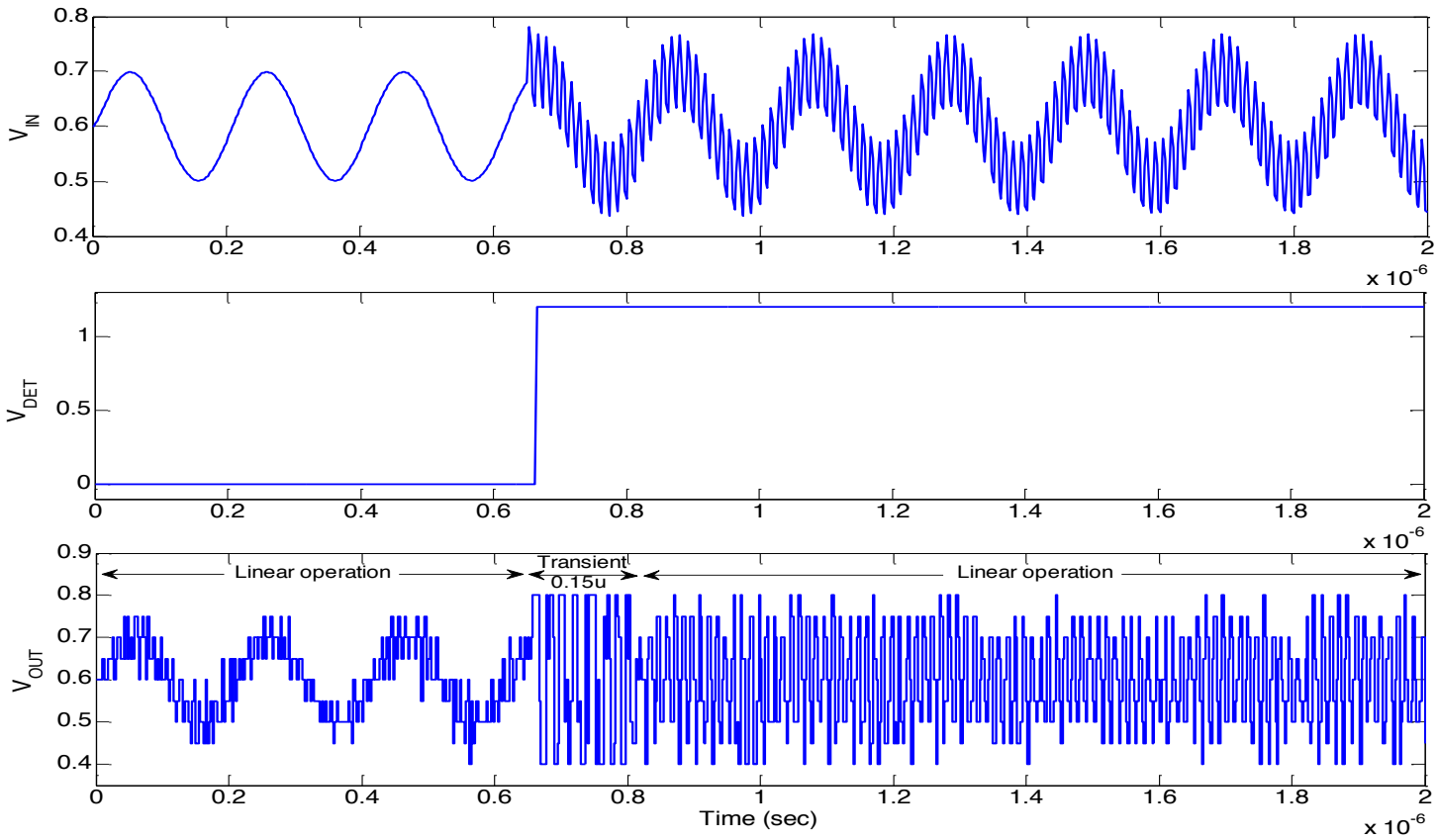
ADC stabilizes again after 0.5 µsecs

Loop Settling Time < 0.2µsec

Input signal

Saturation detector output

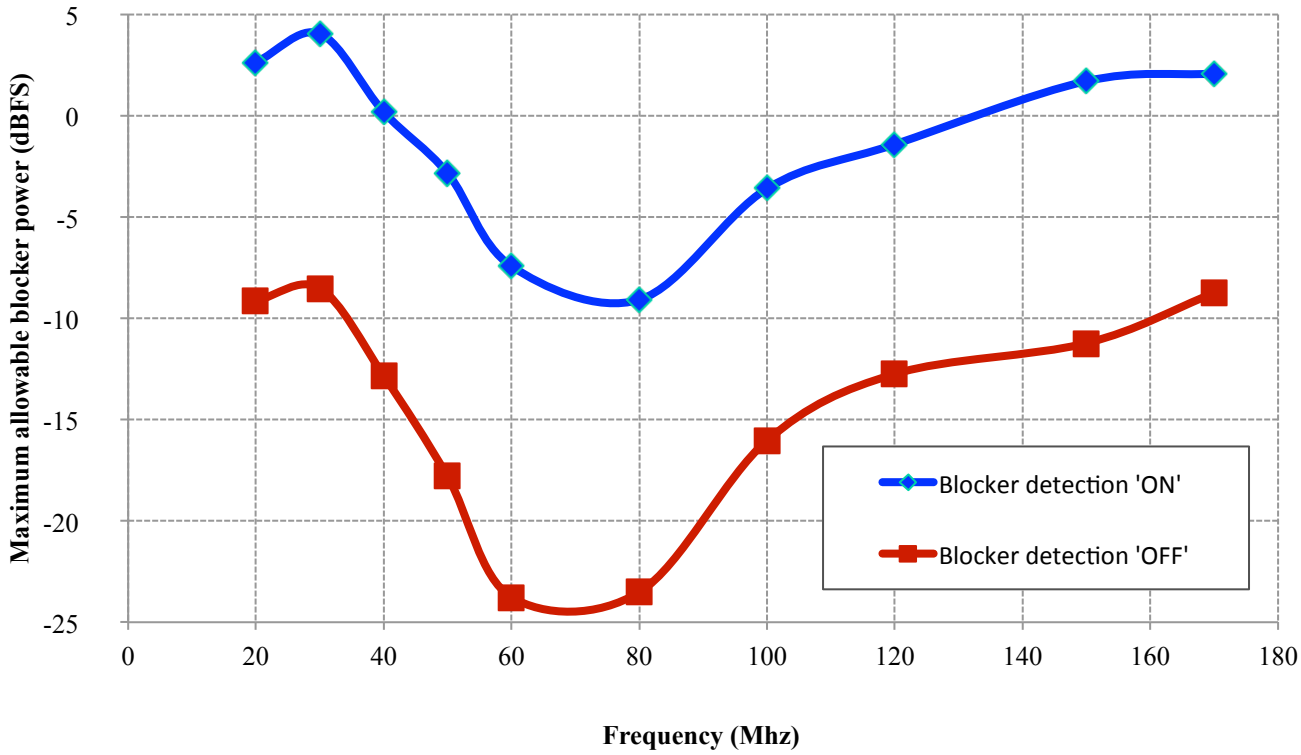
ADC output



Transient response of the ADC to the -9dBFS blocker at 40MHz in the presence of a -6dBFS in-band signal at 5MHz

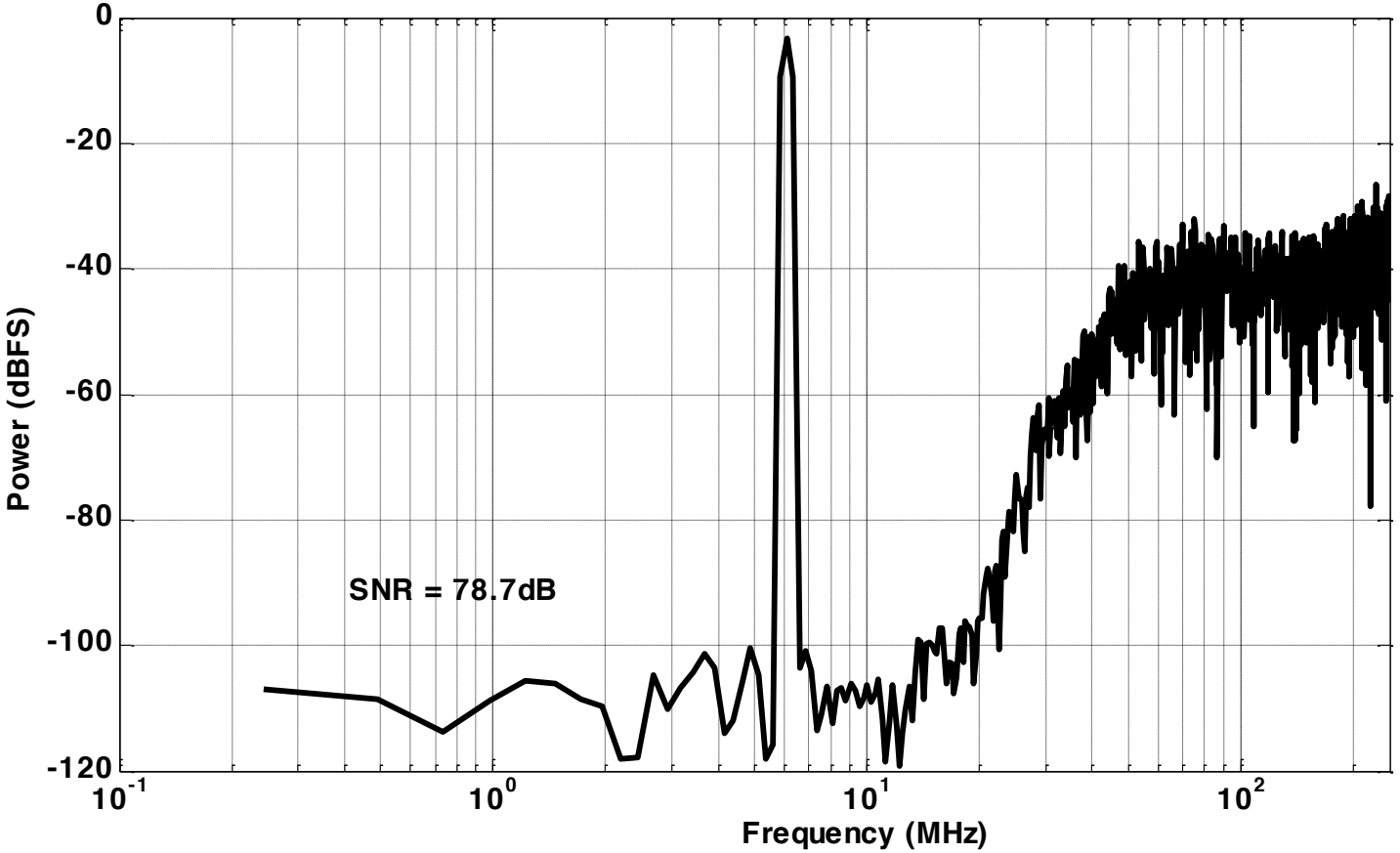
ADC stabilizes again after 0.15 µsecs

Blocker Tolerance with a 0/12 dB Attenuator



- Blocker tolerance performance in the presence of a -6dBFS in-band input signal and various conditions of the blocker signal
- The proposed techniques improve the blocker tolerance of the system by >12dB

Post-Layout Simulation



- SNR of the ADC from post-layout extraction
- Expected ENOB > 12 bits
- Tolerant to full-scale blockers

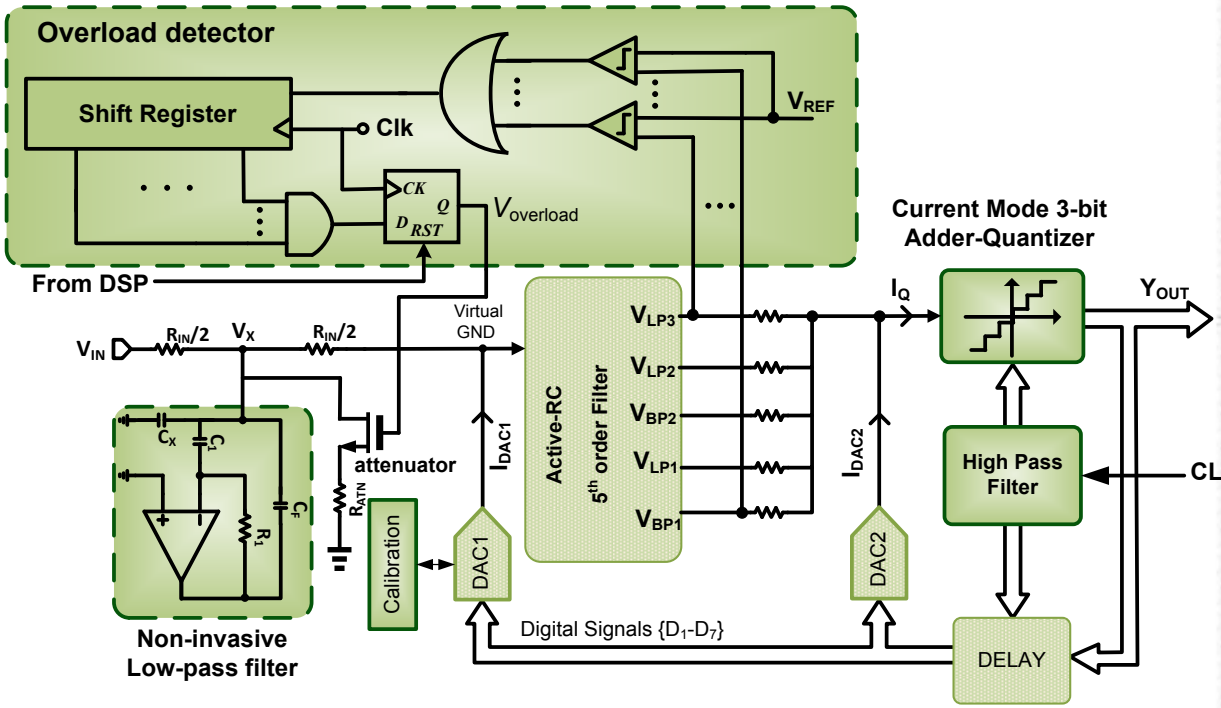
Summary: Blocker Tolerance

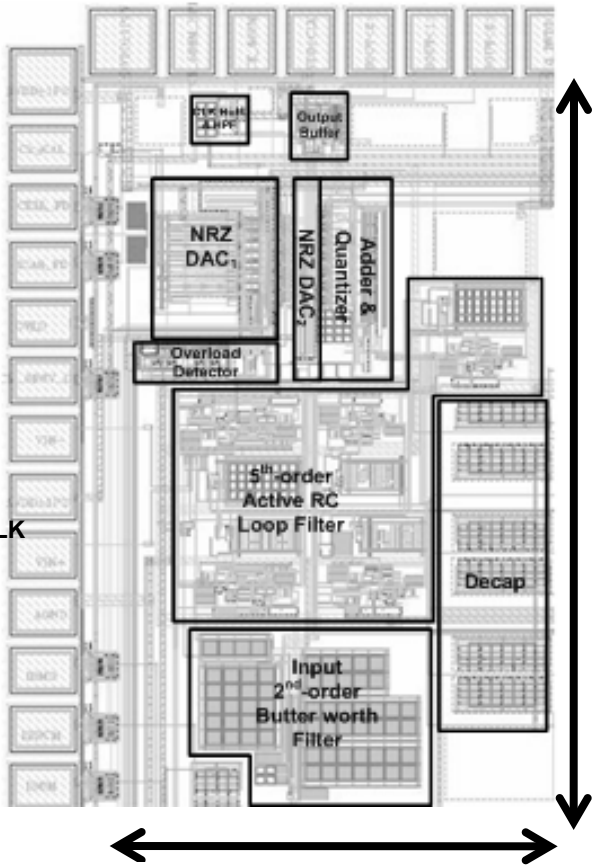
- Shunt complex impedance provides static blocker rejection especially at the critical frequencies.
- Overload detector and PGA prevents the ADC saturation during transients.
- Programmable complex impedance receives the signal from overload detector and toggles between to Normal and Blocker suppression mode.

Advantages

- Less power
- Loop parameters are not disturbed so fast settling times
- Protects the ADC from instantaneous/temporary blockers
- Moderate SNR is better than no communication or no SNR

Proposed Architecture and Layout





- Layout of the entire ADC using IBM 90nm CMOS process with 1.2x0.6mm^2 area
- Expected characterization: Late October 2011

Performance Summary of the ADC

Signal Bandwidth	20MHz
Oversampling Ratio	12.5
Order	5
Number of Quantizer Levels	8
Peak SNDR/SQNR	74dB/79dB
Maximum Stable Input Amplitude	-3dBFS
Blocker Tolerance in the Presence of a -6dBFS In-Band Signal	-9dBFS @ 80MHz
Settling Time After Blockers	<0.5µS
Static Power Consumption (ADC Core)	< 25mW
FOM (ADC Core)	154fJ/conv-step

Status of the Project

- Two targets are proposed for the task 1806.038:

1. 12 bit $\Delta\Sigma$ data converter : Taped out and currently testing
2. 15 bit $\Delta\Sigma$ data converter : Working on the schematic .
   - Currently developing low-power techniques to improve resolution of 15 bit $\Delta\Sigma$ data converter

Conclusions

- Digital DAC calibration is employed.
- Blocker rejection is achieved by overload detector, attenuator and shunt complex impedance.
- Jitter tolerance is improved by high-pass filtering the clock.
- 12 Bit ADC is implemented in a 1.2V, 90nm CMOS technology.
- 15Bit ADC is currently under design
- Mesh topology improves the SQNR, Embedded quantizer is a low power solution

Acknowledgements

SRC for supporting my PhD program

Analog and Mixed signal centre (AMSC), Texas A&M University, students

Jazz-Semiconductor support for chip fabrication.

NSF for their partial support

C.T. Fu, H. Xu, J. Duster and R. Bishop of Intel Corporation.

Intel Corporation

Publications

1. **H. M. Geddada**, J. Silva-Martinez and S. S. Taylor, "Fully Balanced Low-Noise Transconductance Amplifiers with P1dB > 0dBm in 45nm CMOS," IEEE European Solid-State Cir. Conf., Sept 2011.
2. **H. M. Geddada**, J. Silva-Martinez and S. S. Taylor, "Inductorless wideband CMOS LNAs with non-linearity cancellation," IEEE MWSCAS. Conf., Aug 2011. **(Best student paper award)**
3. J. Silva-Martinez, A. I. Karsilayan, **H. M. Geddada,** Aravind Padyana, C. J. Park, "A Blocker Tolerant Broadband Analog-to-Digital converter architecture" Techcon conference, SRC, Sep 2010.

Publications

4. **Geddada H. M**. ;Park, J.W.; Silva-Martinez, J. “Robust Derivative superposition Method for Linearizing Broadband LNA’s” IEE Electronics Letters Vol. 45 Issue: 9 April 2009 **(Top 2nd paper accessed for the month of May 2009).**

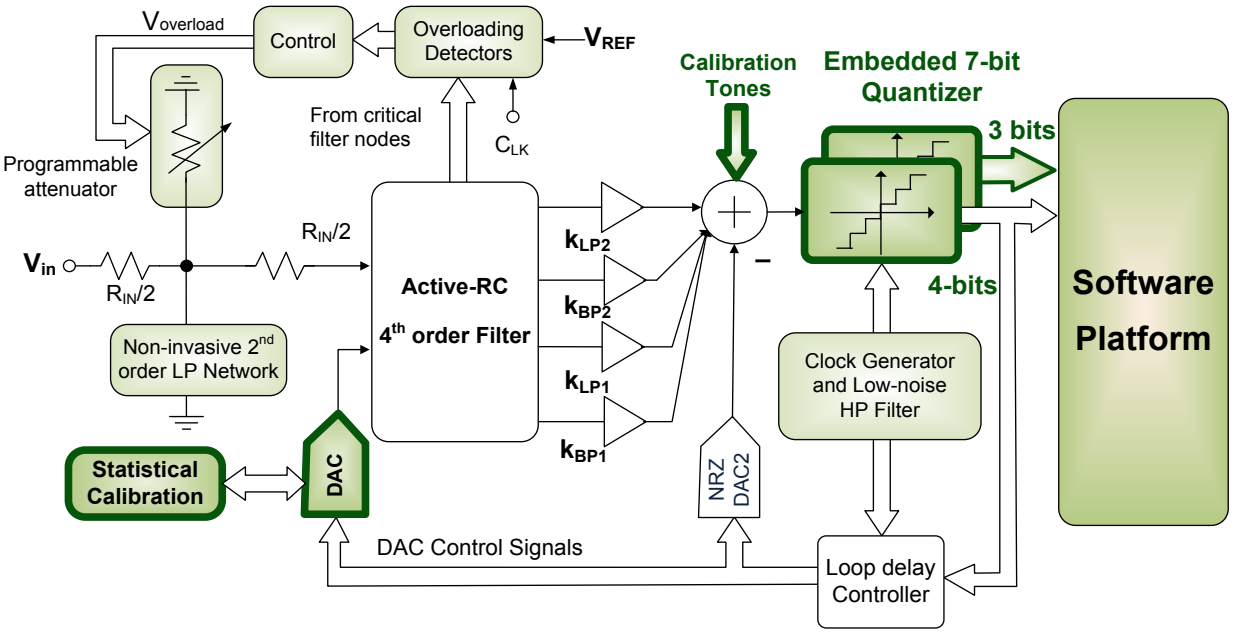
Q&A

Back up slides

Comparison with Prior Art

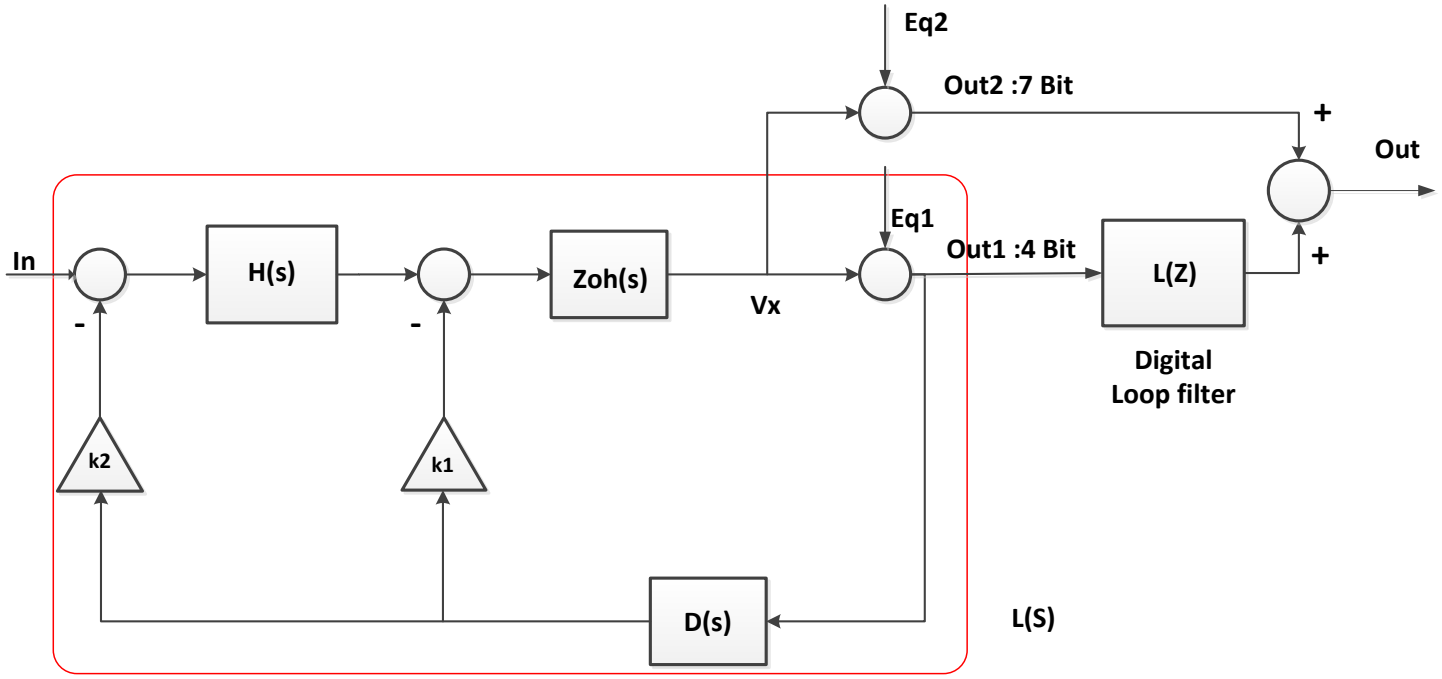
	Blaakmeer JSSC-2008	Ramzan ISSCC-07	Chen JSSC-08	Van de Beek ISSCC-08	This work Balun-LNA
Technology	65nm	0.13μm	0.13μm	45nm	0.18μm
BW [Ghz]	0.2~5.2	1~7	0.8~2.1	0.6~10	0.3~2.8
Av [dB]	13~15.6	17	**14.5	10	**9.6~12.5
NF [dB]	2.9~3.5	2.4	2.6	3	5.95~6.5
IIP3 [dBm]	**0~4**	**-4.1**	**16.0**	**6.0**	**16.8**
P_{1dB} [dBm]			**-11**	**-**	**0.5**
Vdd[v]	**1.2**	**1.4**	**1.5**	**-**	**2**
Power [mW]	14	25	17.4	30*	14.2
No. of coils	0	0	0	2	0
Area (mm^2)	0.009	0.019	0.0992	-	0.06
FOM	**16.22**	**6.343**	**102.3**		**34.3**

Target 2: 15bit ΣΔ Modulator



- Embedded 7-bit quantizer to improve the SQNR
- MSB 4 bits are used for the feedback
- Entire 7-bits are used to process modulator's output.

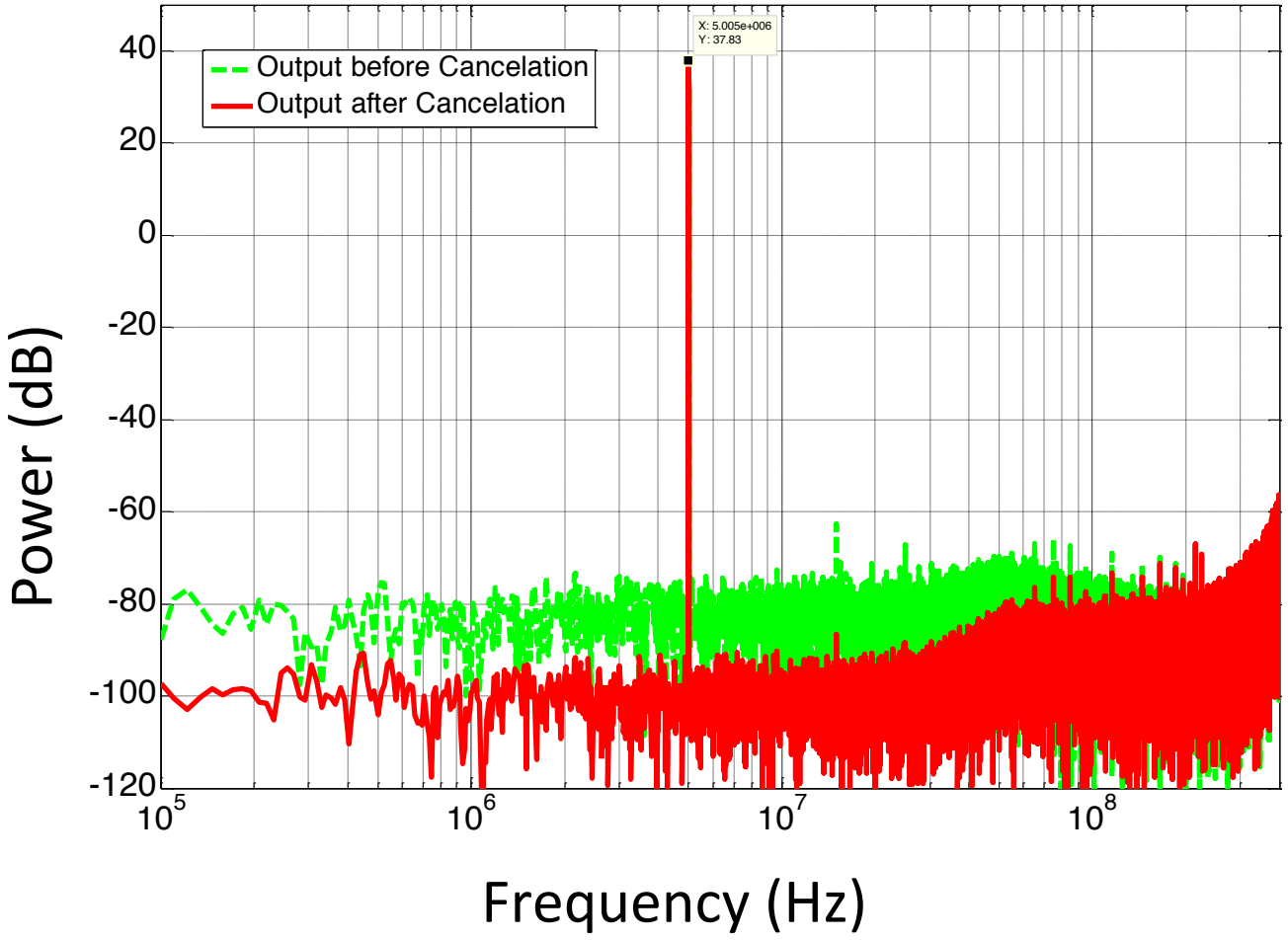
Target 2: 15bit ΣΔ Modulator



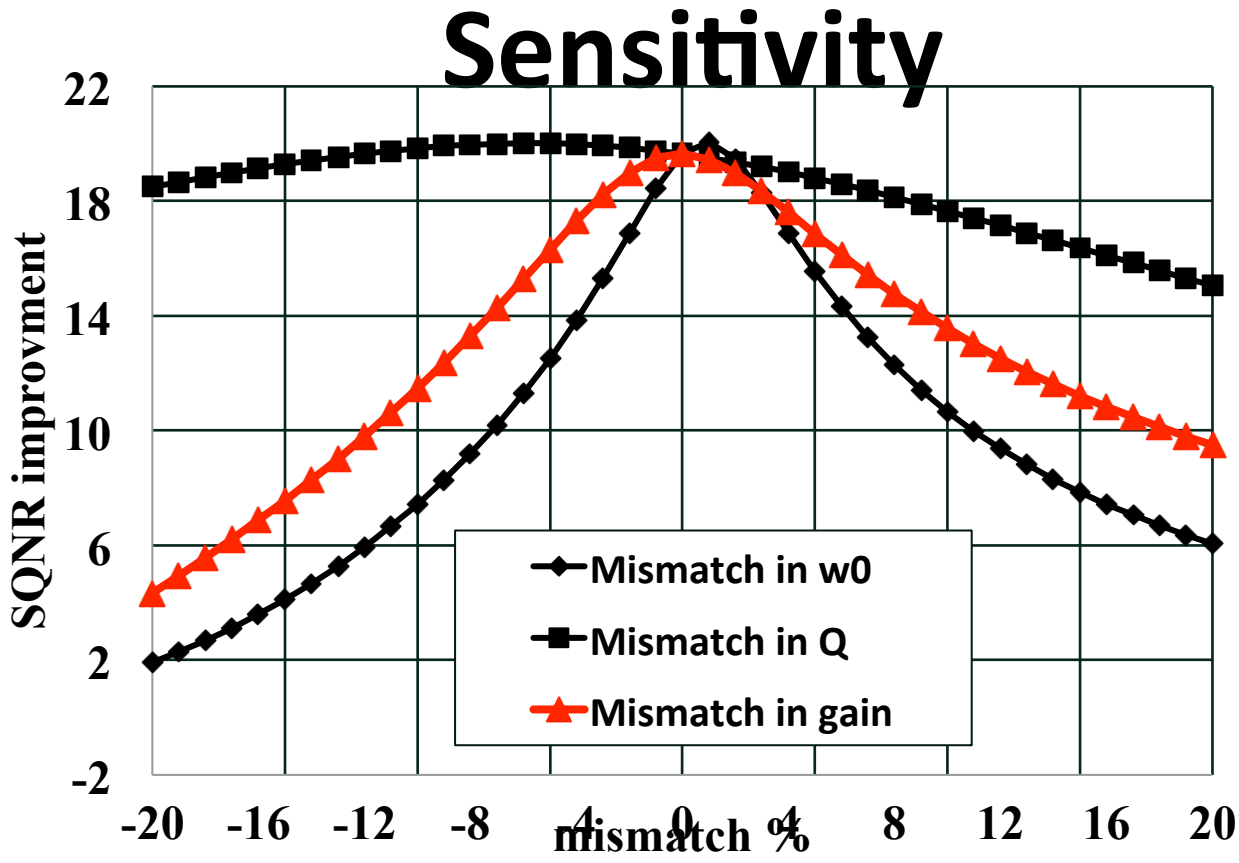
- Model showing quantization noise (Eq1) cancellation through Mesh topology.
- Embedded 7-bit quantizer to improve the SQNR

$L(Z)\big|_{z=e^s} = L(S)$ for proper cancellation of Eq1

Target 2: SQNR improvement

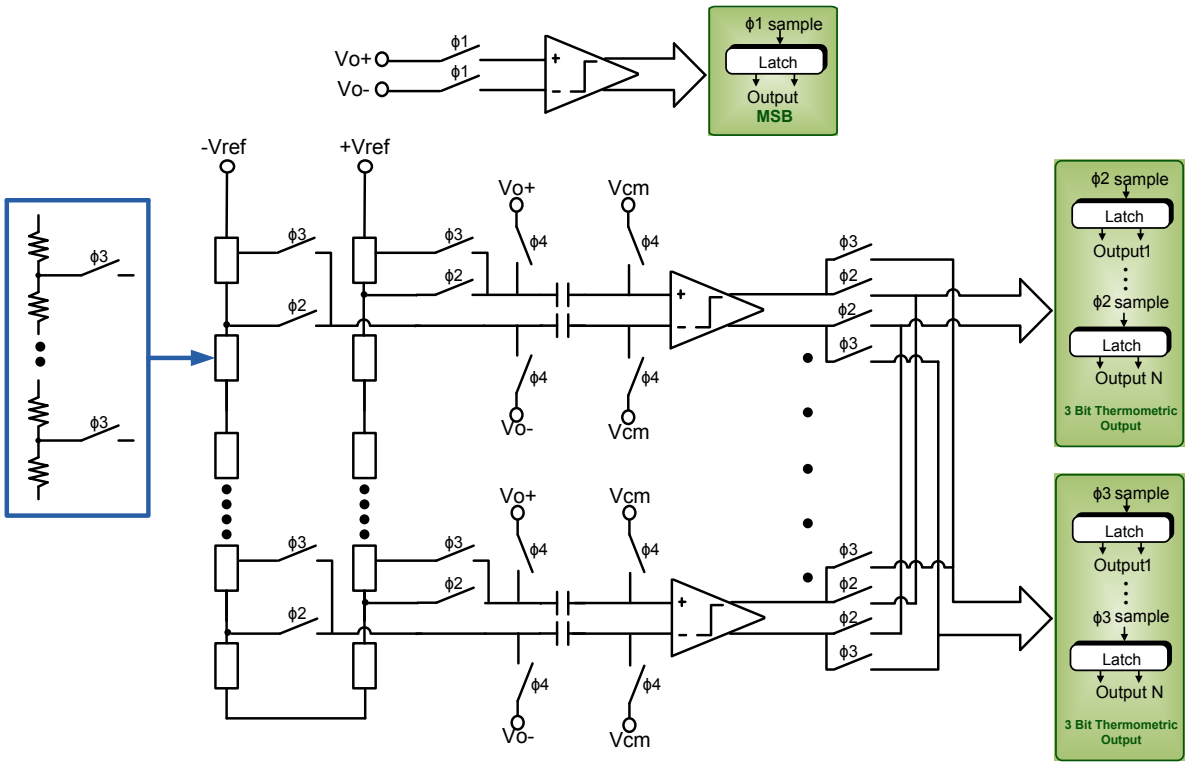


- SQNR improvement > 20dB



- SQNR sensitivity to mismatch in L(Z) and L(S).

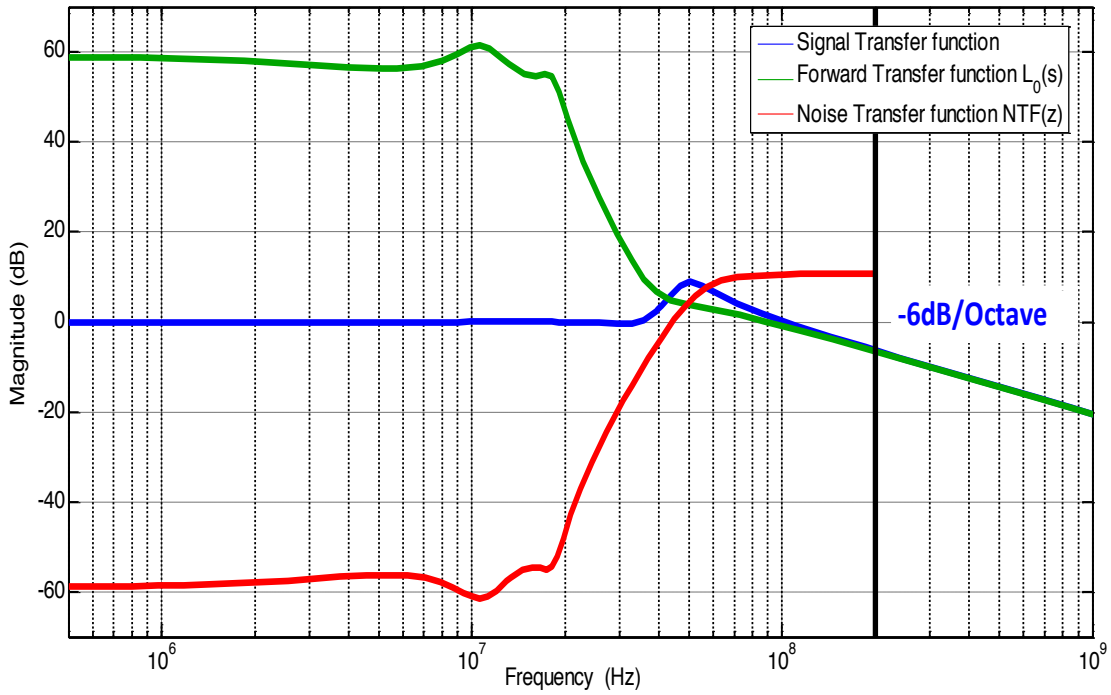
Embedded 7 Bit Quantizer



- 3 Step quantizer
- Low power solution

- ϕ1 Solve MSB
- ϕ2 Depending on MSB, place the sampling capacitors in the proper location and solve 3 coarse bits
- ϕ3 Move the capacitors to the proper segment and solve 3 fine bits
- ϕ4 Sample the signal for the next iteration.

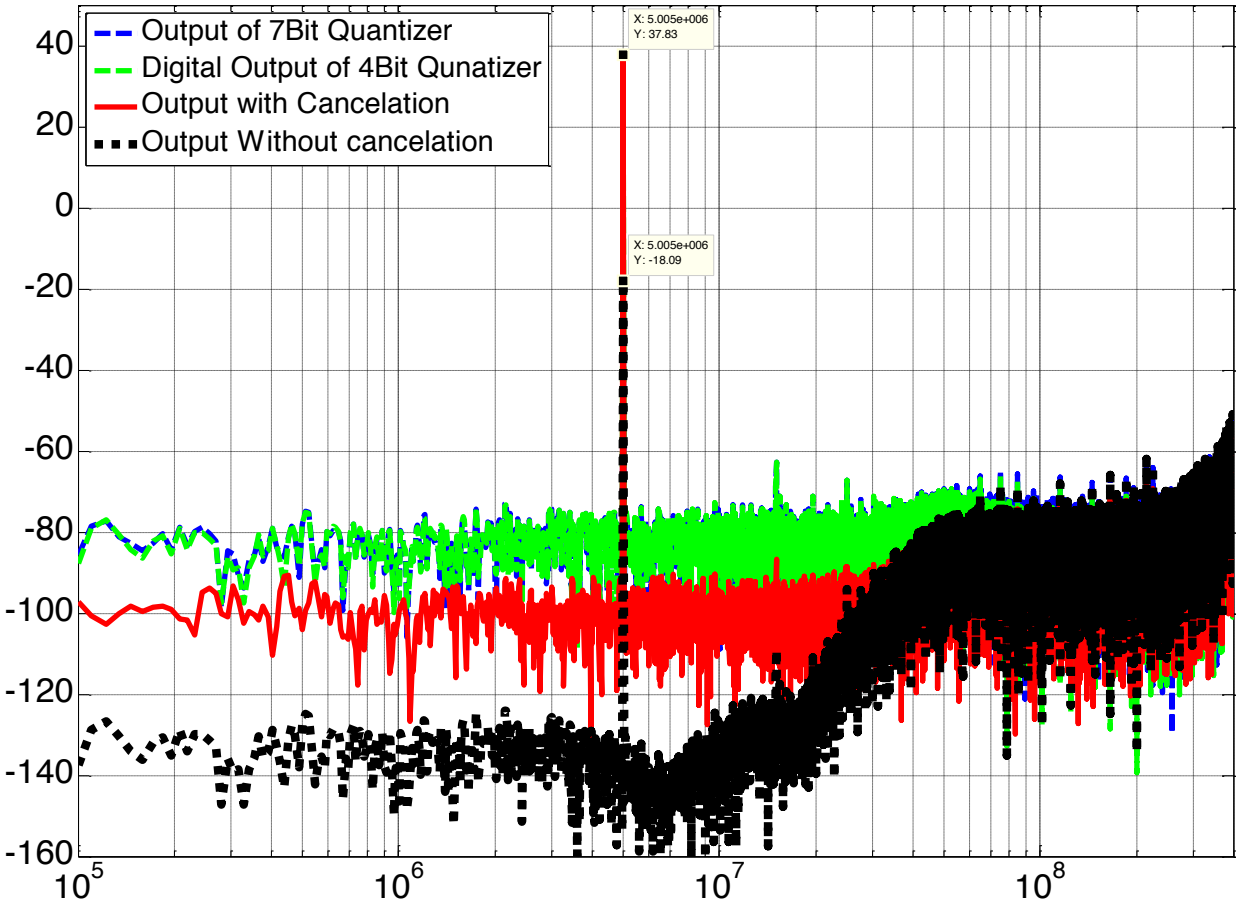
Closed-Loop Transfer Functions



- First-order high frequency roll-off for both STF and Filter transfer function
- Out of band peaking in the STF
- Around 10 dB NTF gain

- Potential saturation issues around 30-100 MHz

Target 2: SQNR improvement



- SQNR improvement