High linearity, Low cost SAW-less Radios

Jose Silva-Martinez

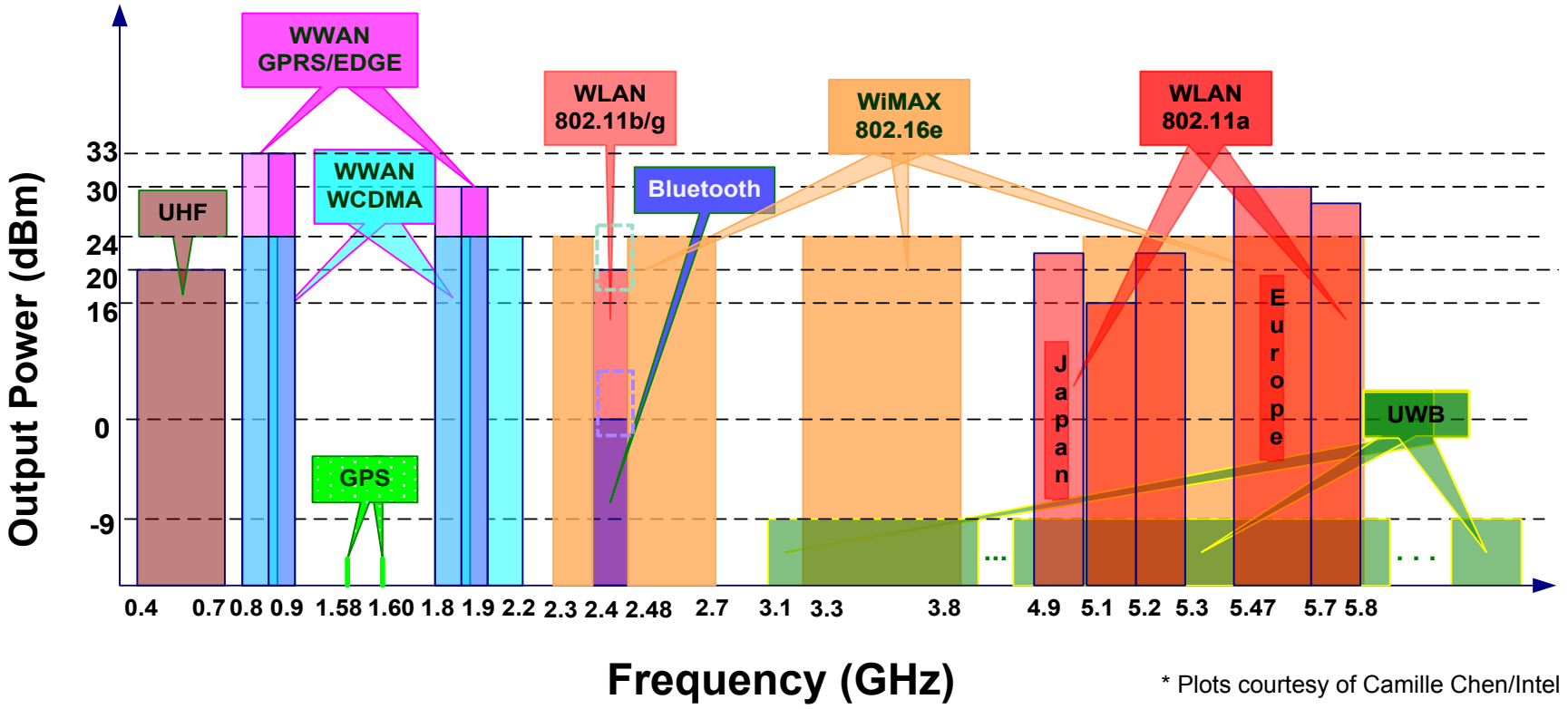
Slides provided by H. Mohan Geddada

Texas A&M University

Outline

- Introduction
- Broadband LNAs with non-linearity cancellation
- Fully balanced LNTAs with P_{1dB} > 0dBm
- A 12 bit, 20MHz, C.T $\Delta\Sigma$ ADC
- Active Antenna
- Conclusions

Introduction

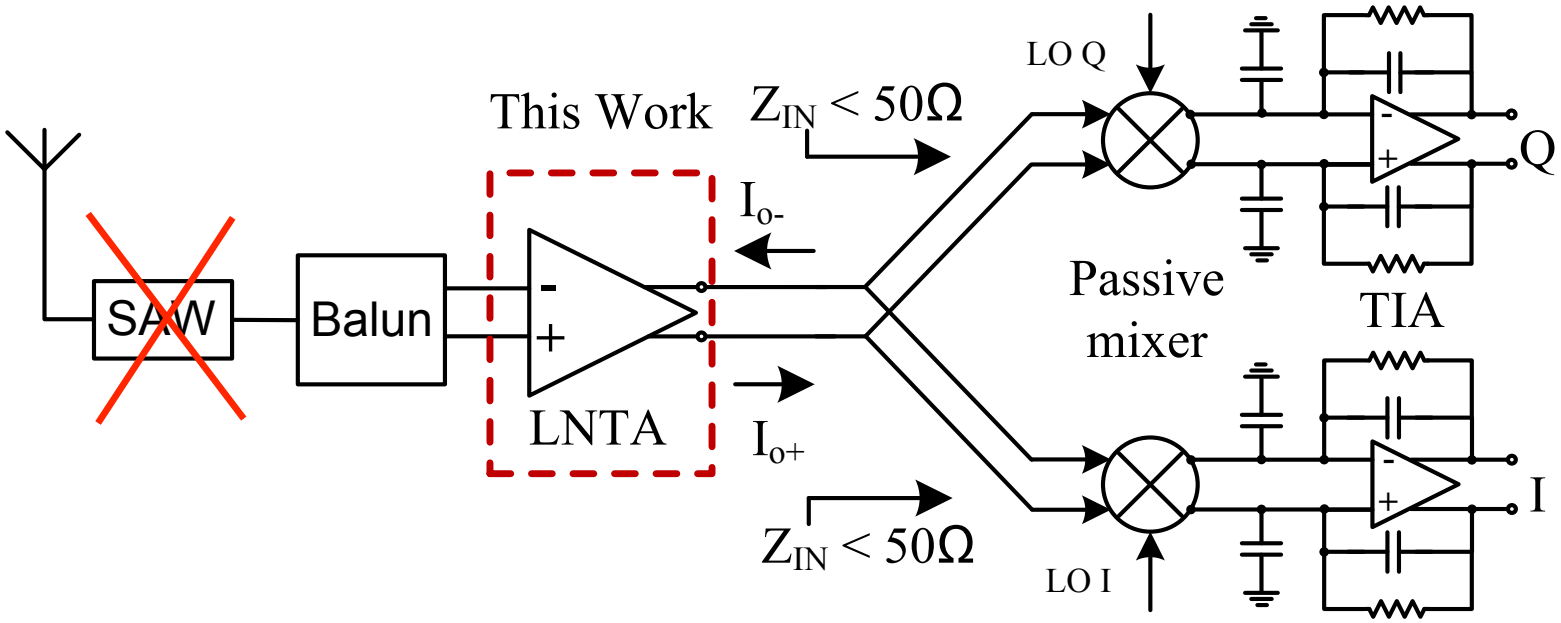


* Plots courtesy of Camille Chen/Intel

Low cost radio receivers for multi standard co-existence

- Low cost: SAW-less and Inductor-less solution.
- High linearity receivers to deal with strong out-of-band interferers

Targeted system



Direct Conversion Receiver Architecture:

Better performance in terms of noise, linearity and power consumption.

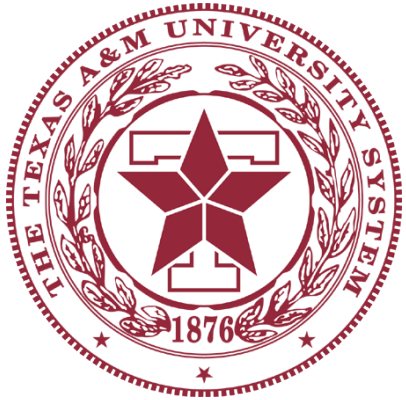
Linearity bottleneck → LNTA

Broadband CMOS LNAs with Nonlinearity Cancellation

Hemasundar M Geddada[1], José Silva-Martínez[1], and Stewart S. Taylor[2]

[1]Texas A&M University

[2]Intel Corporation

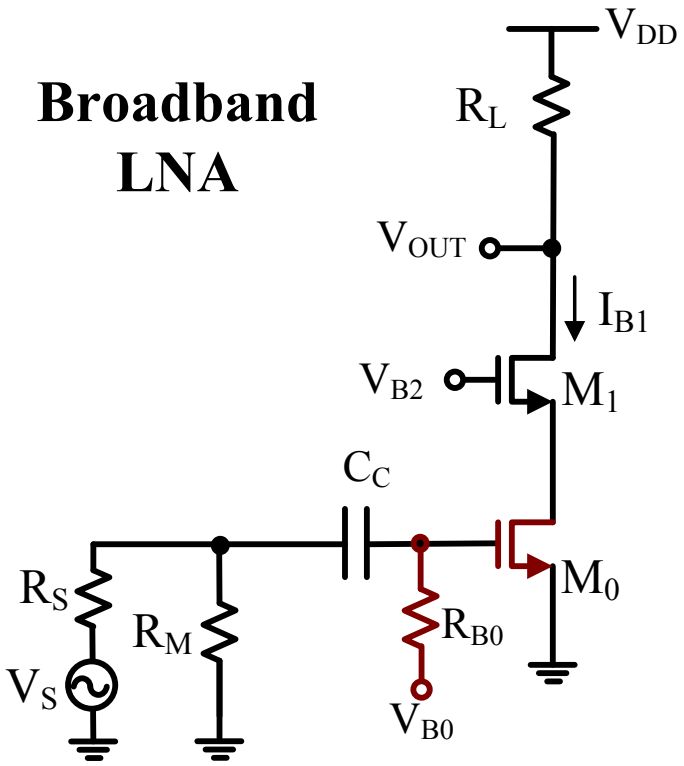


Outline

- Introduction
- State of the Art
- Proposed Derivative superposition
- Noise and distortion cancellation LNA
- Experimental results
- Conclusions

LNA Linearity Analysis

Broadband LNA



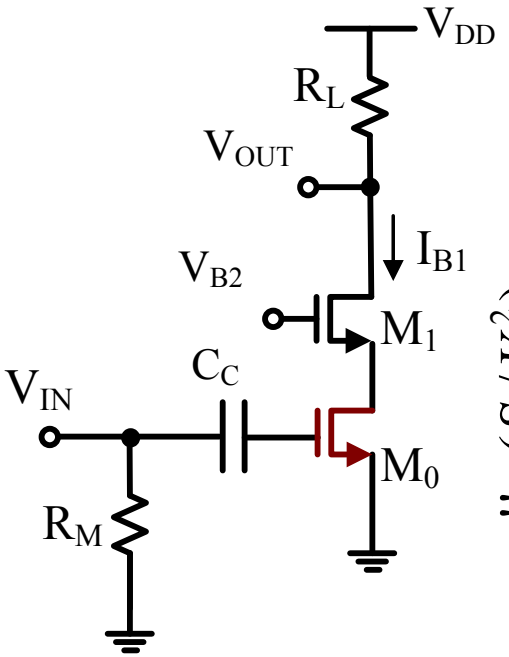
Resistive terminated LNA

$$I_d = I_{B1} + g_m v_{gs} + \frac{g'_m}{2!} v^2_{gs} + \frac{g''_m}{3!} v^3_{gs} + \ldots$$

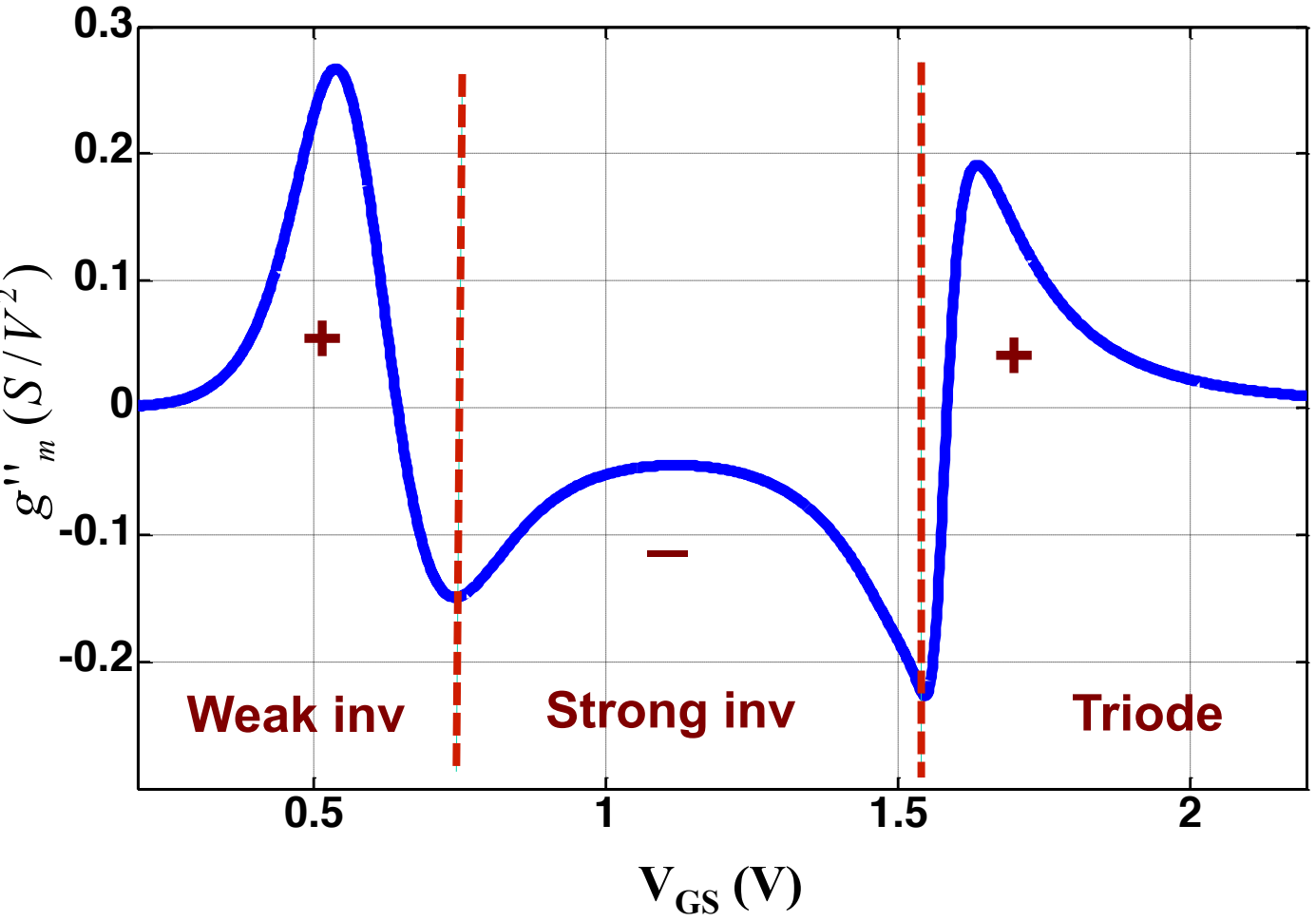
$$g''_m = \partial^3 I_D \big/ \partial V^3_{GS}$$

- A simple design for linearization technique path finding.
- Simplify the input matching network.
- g''_m is the dominant 3rd order distortion.

Characterization & observations

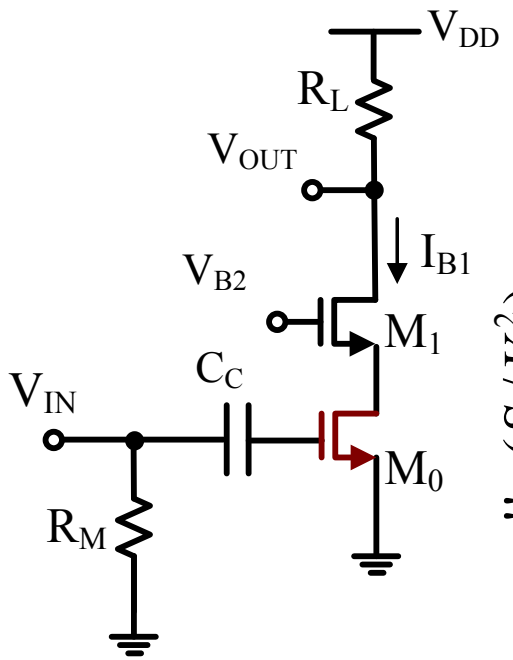


Broadband LNA



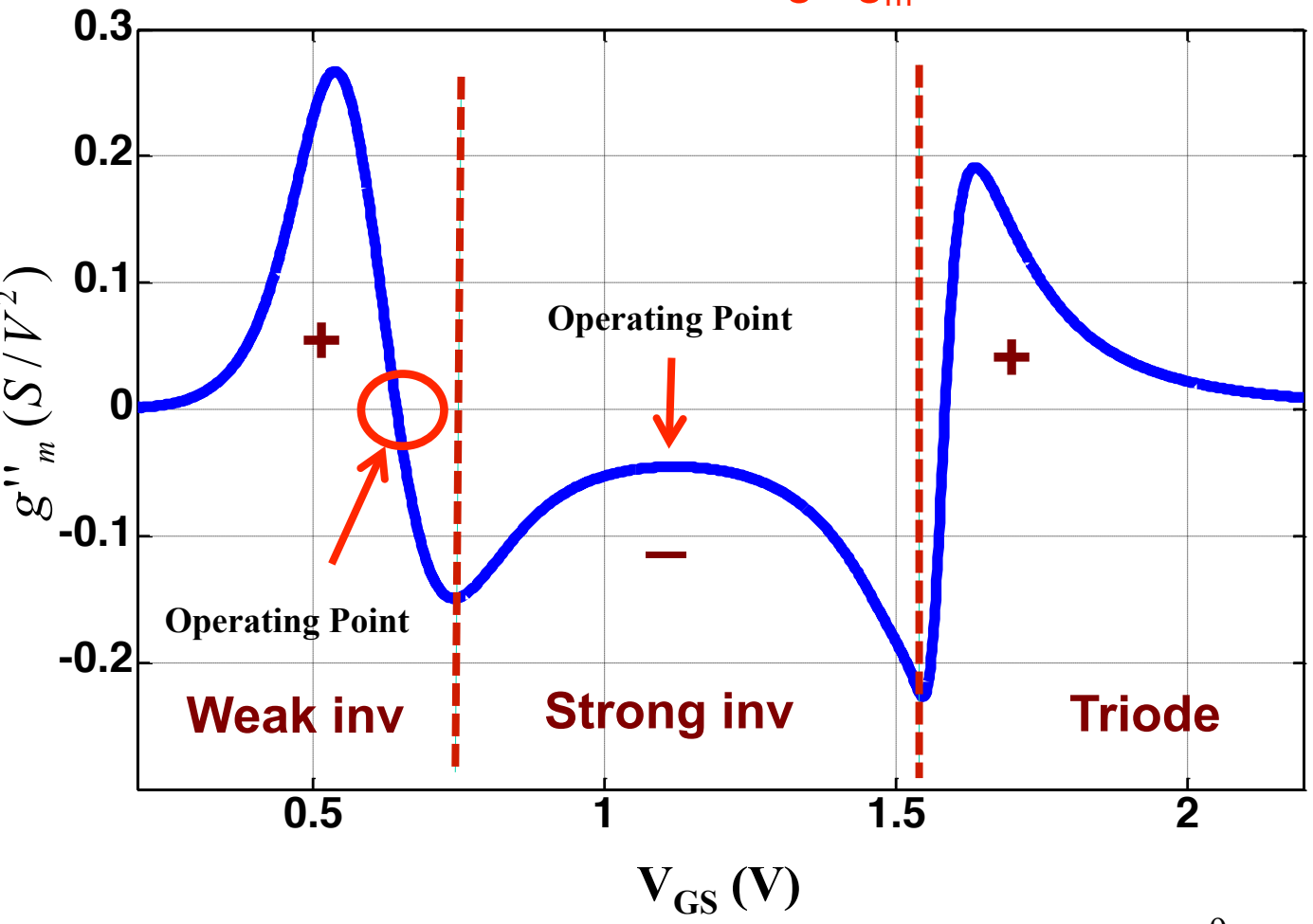
$$g''_m = \partial^3 I_D / \partial V^3_{GS}$$

Previous work



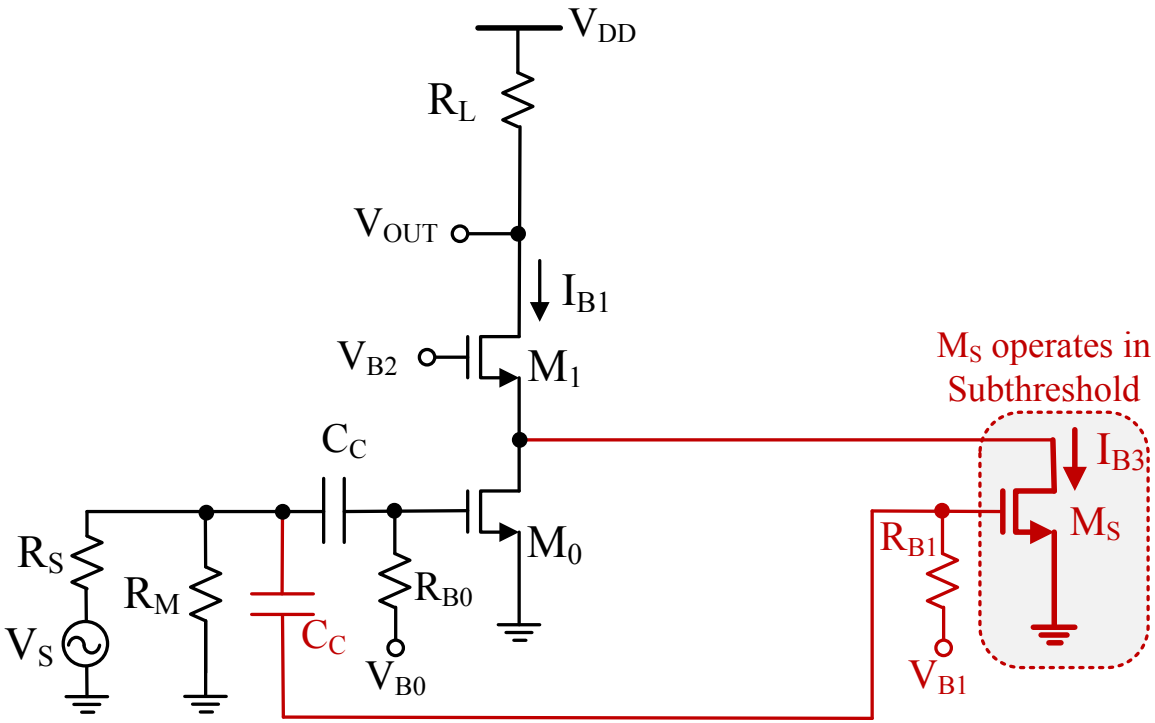
Optimum Gate biasing

- We want High g_m



- P.V.T. Sensitive
- Low g_m
- Good small signal linearity (IIP3), but Poor Large signal linearity (P_{1dB})

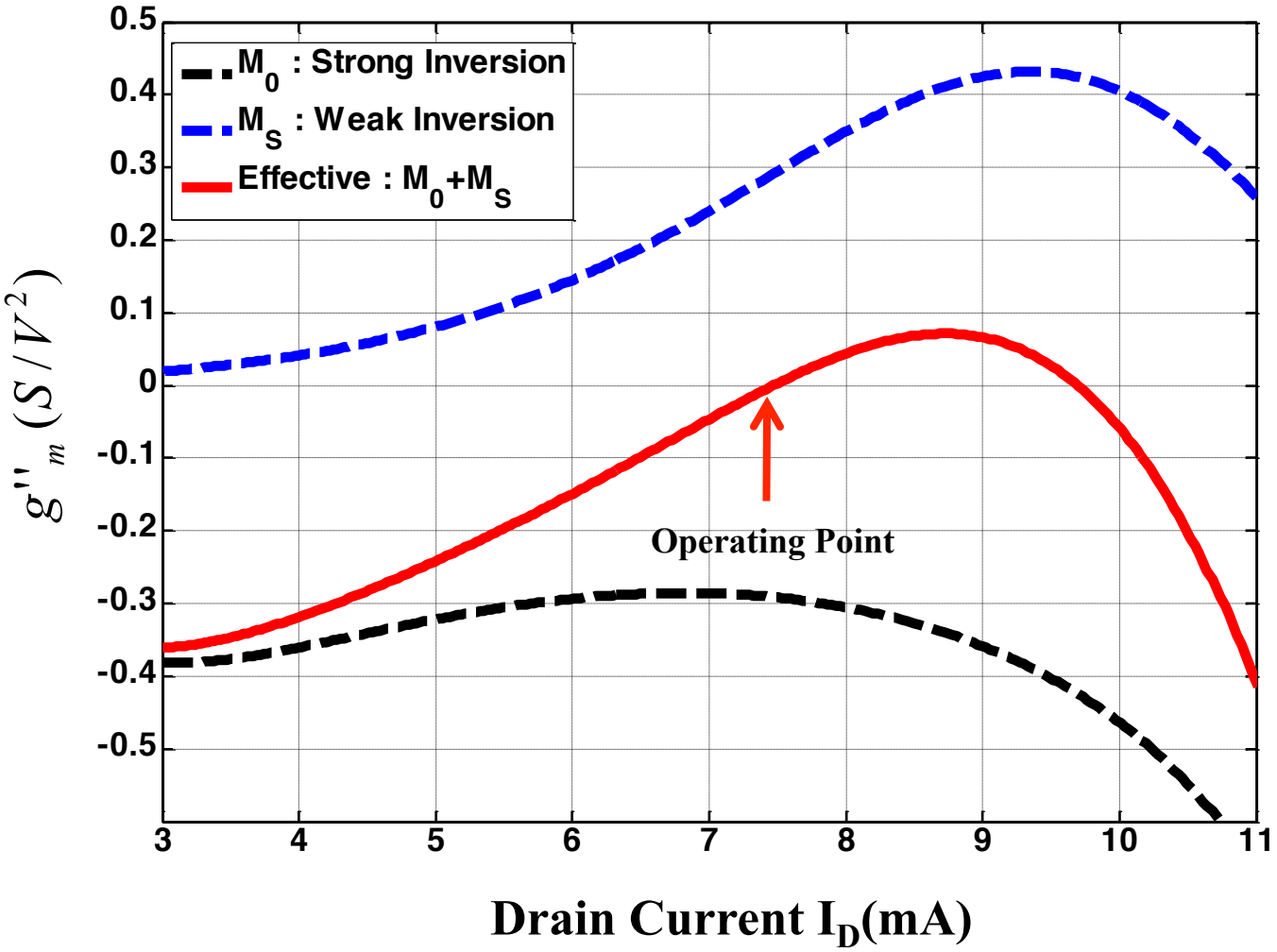
Previous work



Derivative Superposition (DS):

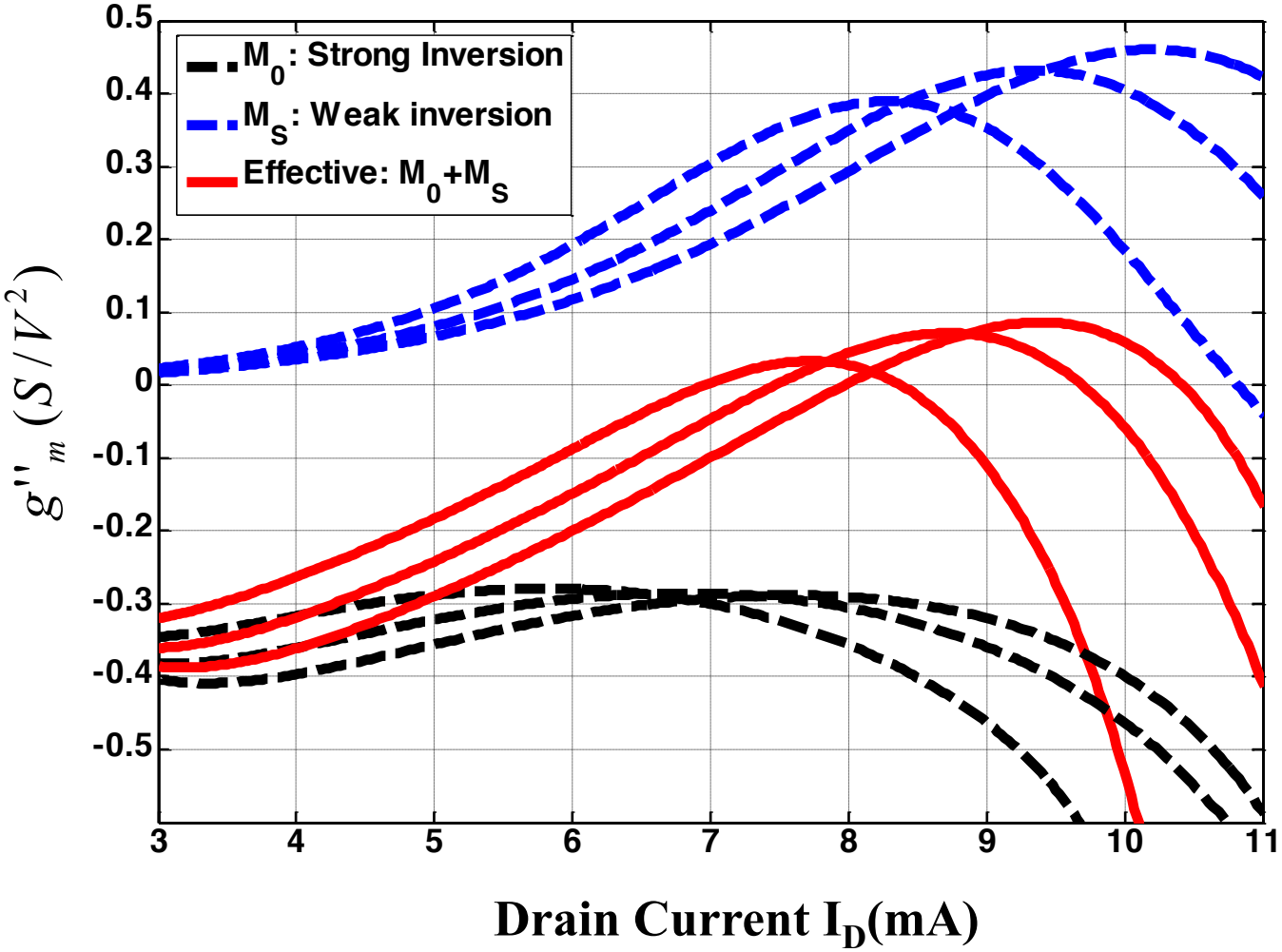
- M_0: Strong inversion
- M_S: Weak inversion

Previous work



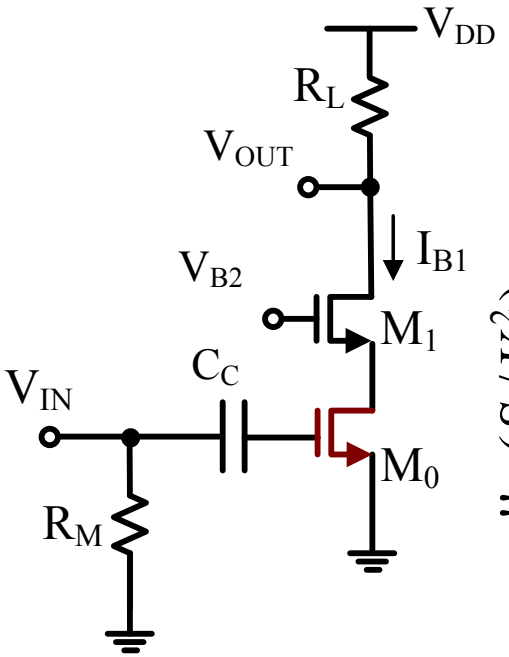
- Poor Large signal linearity (P_{1dB})

Previous work

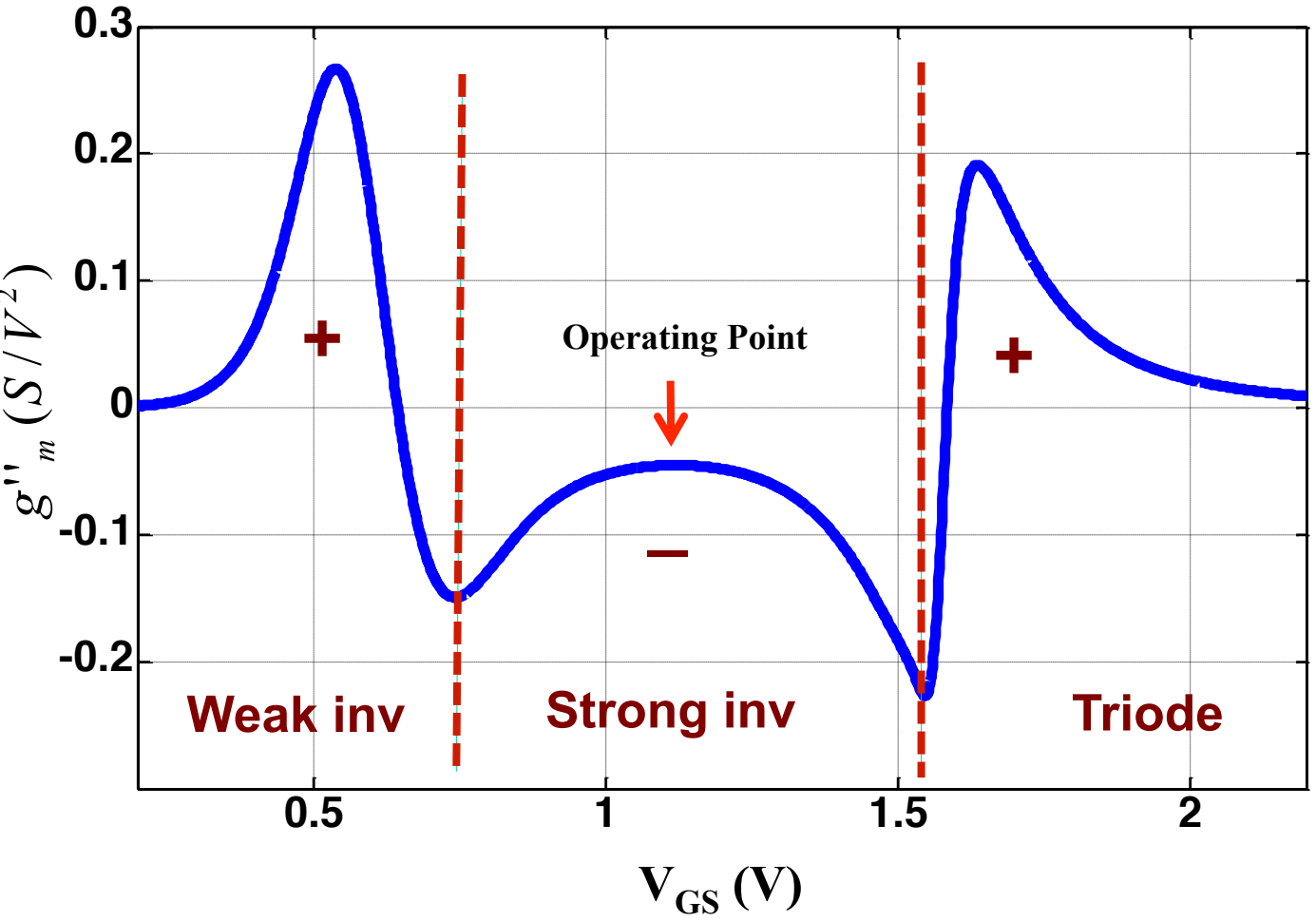


- Poor Large signal linearity
- P.V.T. sensitive

Re-visit Characterization: Fix VDS

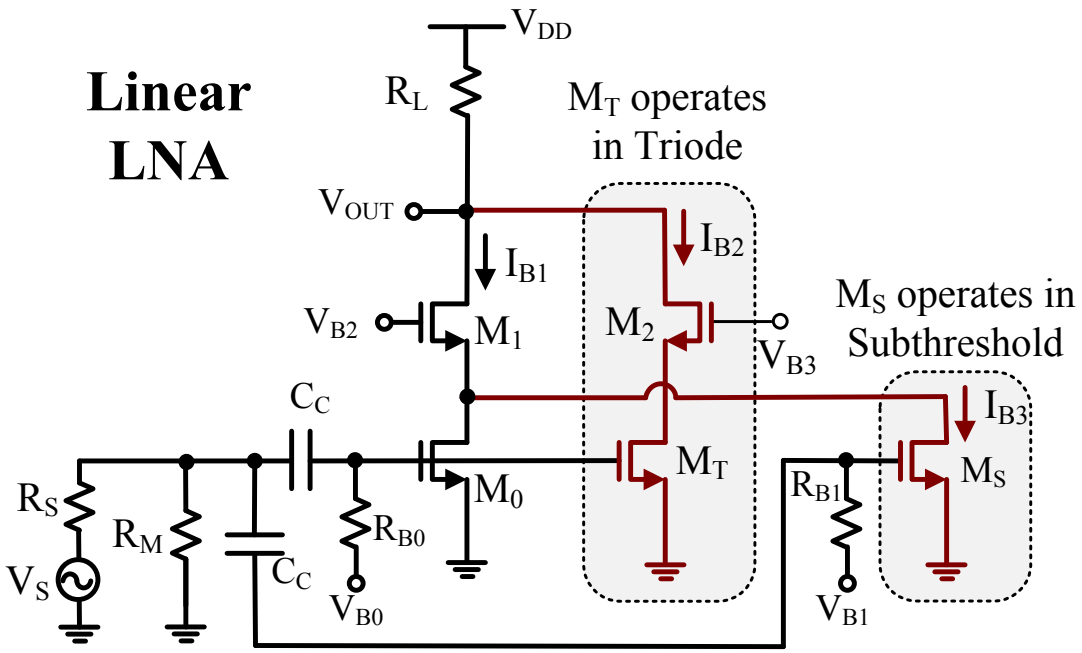


Broadband LNA



$$g''_m = \partial^3 I_D / \partial V^3_{GS}$$

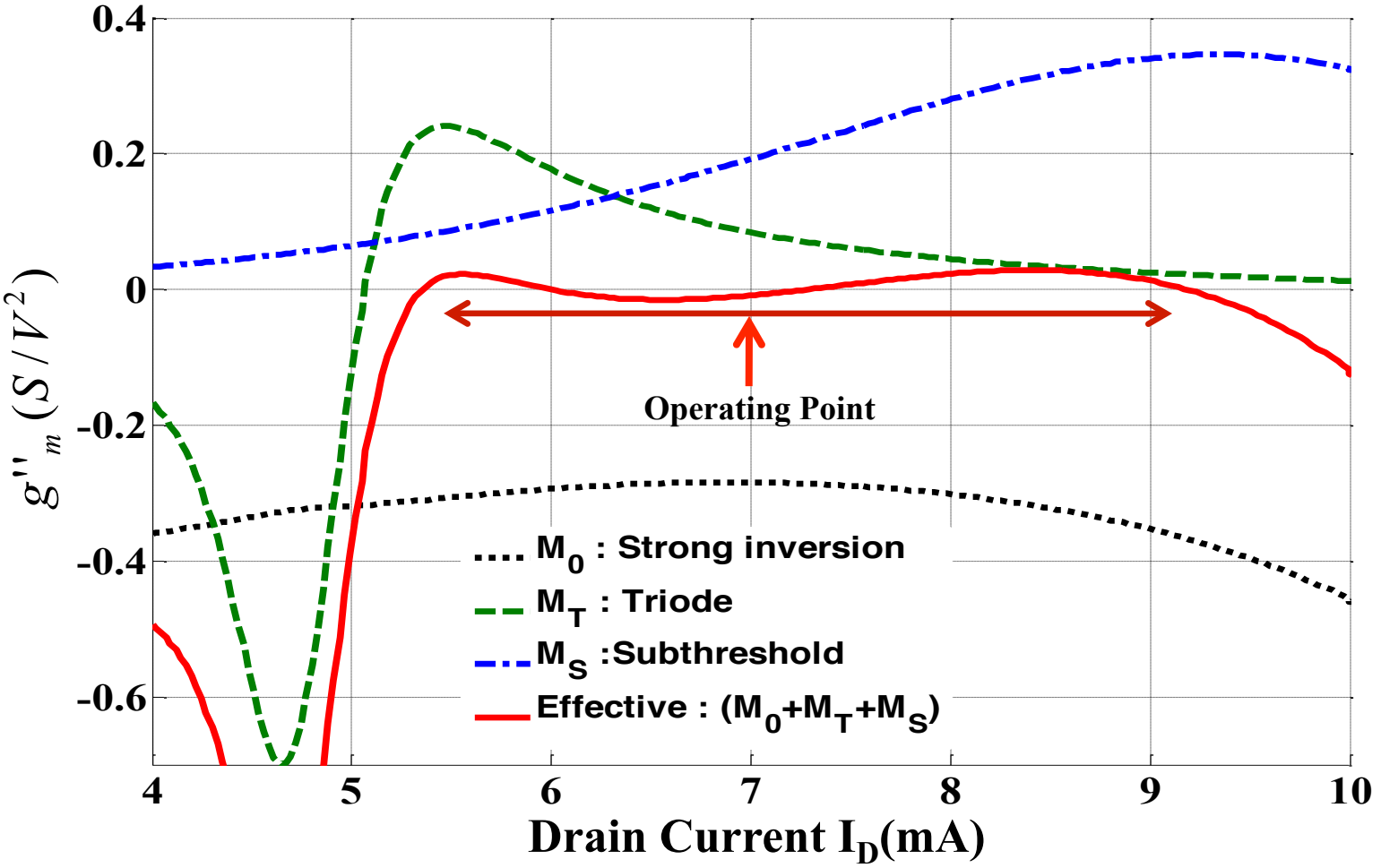
Proposed Linearization Technique



Robust Derivative Superposition (RDS):

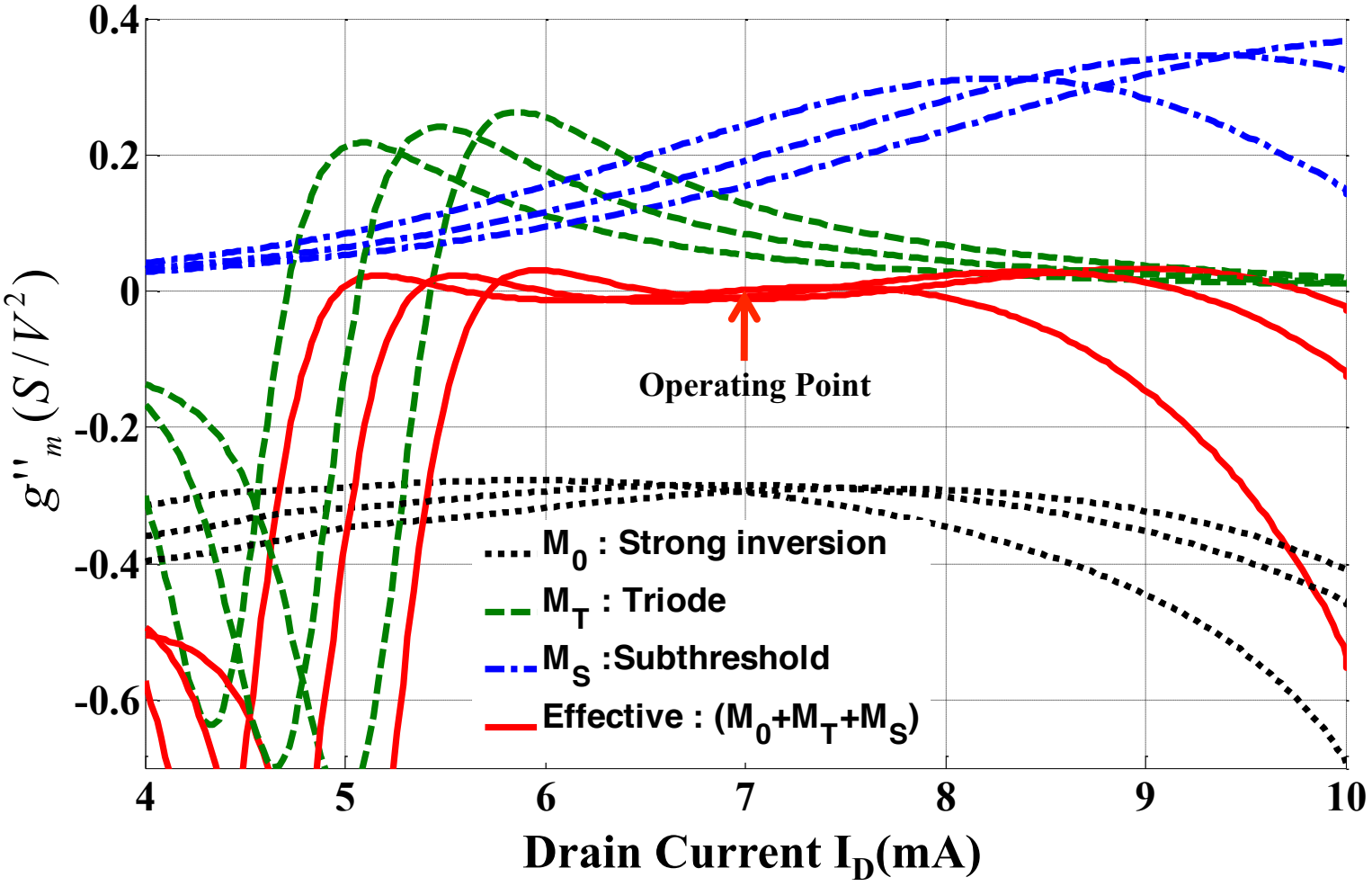
	Region	g_m	g''_m
M_0	Strong Inversion	POS	NEG
M_S	Weak Inversion	POS	POS
M_T	Triode	POS	POS

Robust Derivative Superposition



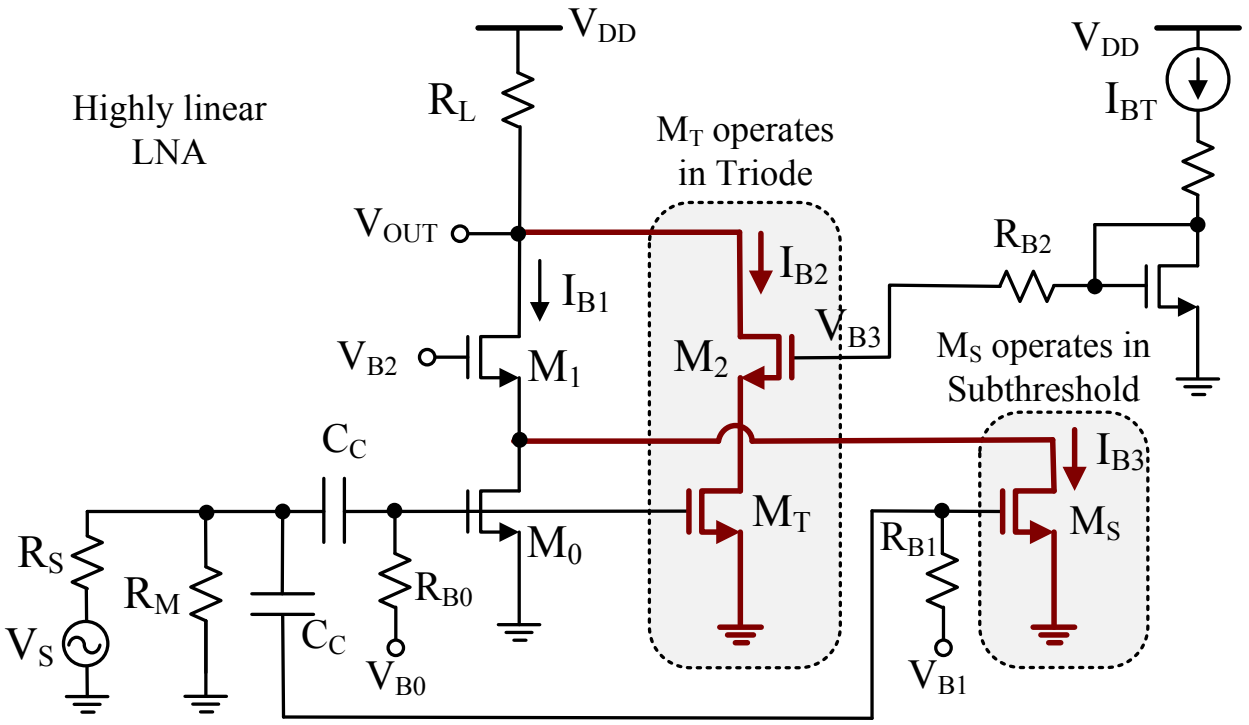
- **Wide range cancellation** of g”$_m$ →Good Large signal linearity
- Less P.V.T. sensitive

Robust Derivative Superposition



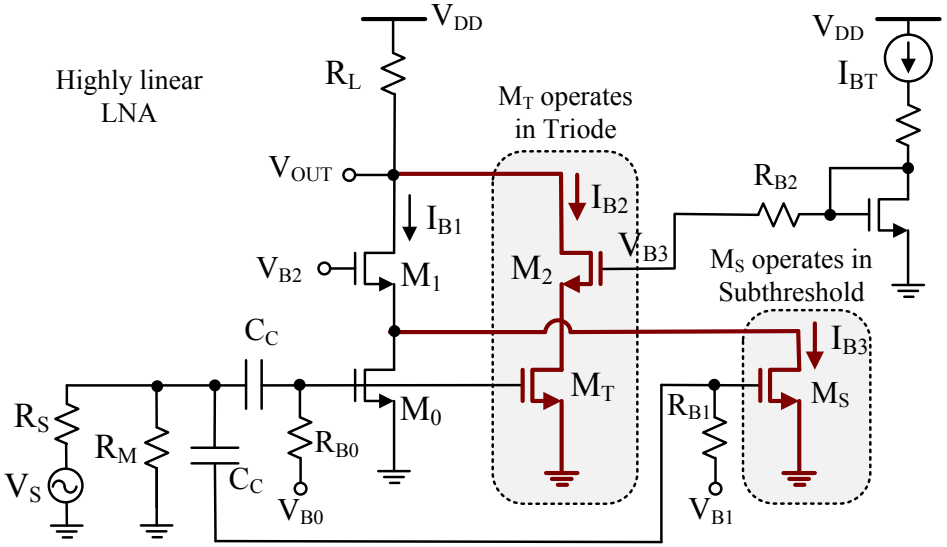
Good **wide range cancellation** of g”$_m$ at **various technology corners→ P.V.T. insensitive**

Design Considerations of RDS



- Fixed V_{DS} of M_T for robust cancellation among corners.
- M_2 avoids output impedance degradation due to $M_T(r_{ds})$.
- Similar delays in main path and the auxiliary paths ensure accurate nonlinearity cancellation.

Advantages of RDS technique



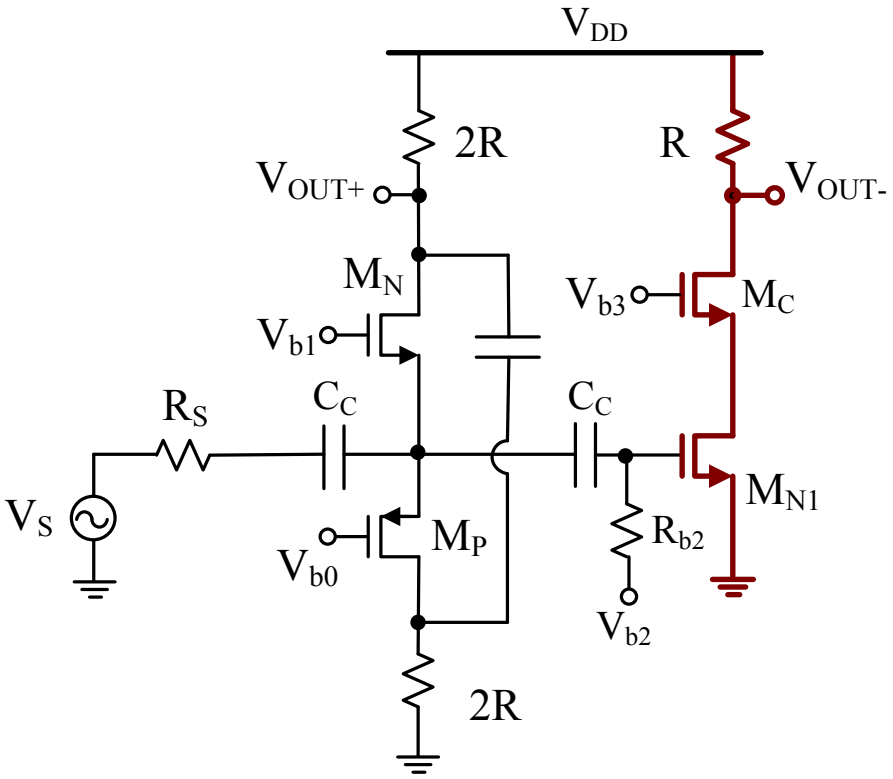
Best Paper Award:

IEEE MWCAS-2011

- Feed-forward compensation: No stability problems
- M_T and M_S are small transistors: No BW limitation
- $I_{B2}+I_{B3} < 8\%$ of I_{B1} : Little power penality
- M_T shares C_C with the M_0 :No additional coupling cap

"Robust Derivative superposition Method for Linearizing Broadband LNAs," H. M. Geddada, J. Won-Park and J. Silva-Martinez. IEE Electronics Letters, Vol. 45, pp. 435-436, April 2009.

Noise/distortion cancelling Balun-LNA

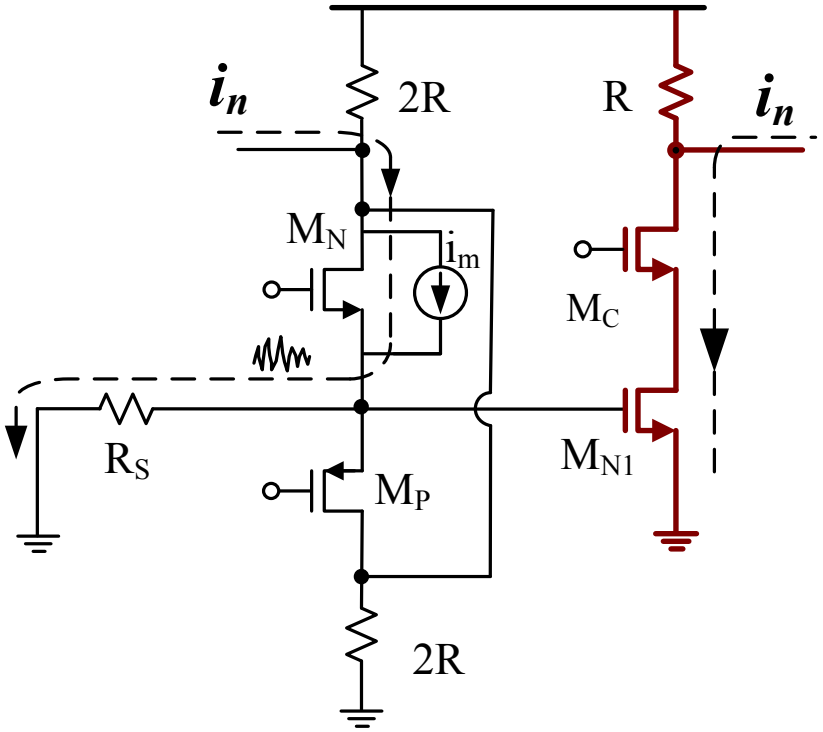


Blaakmeer et al
JSSC 2008

Common-gate common-source topology:

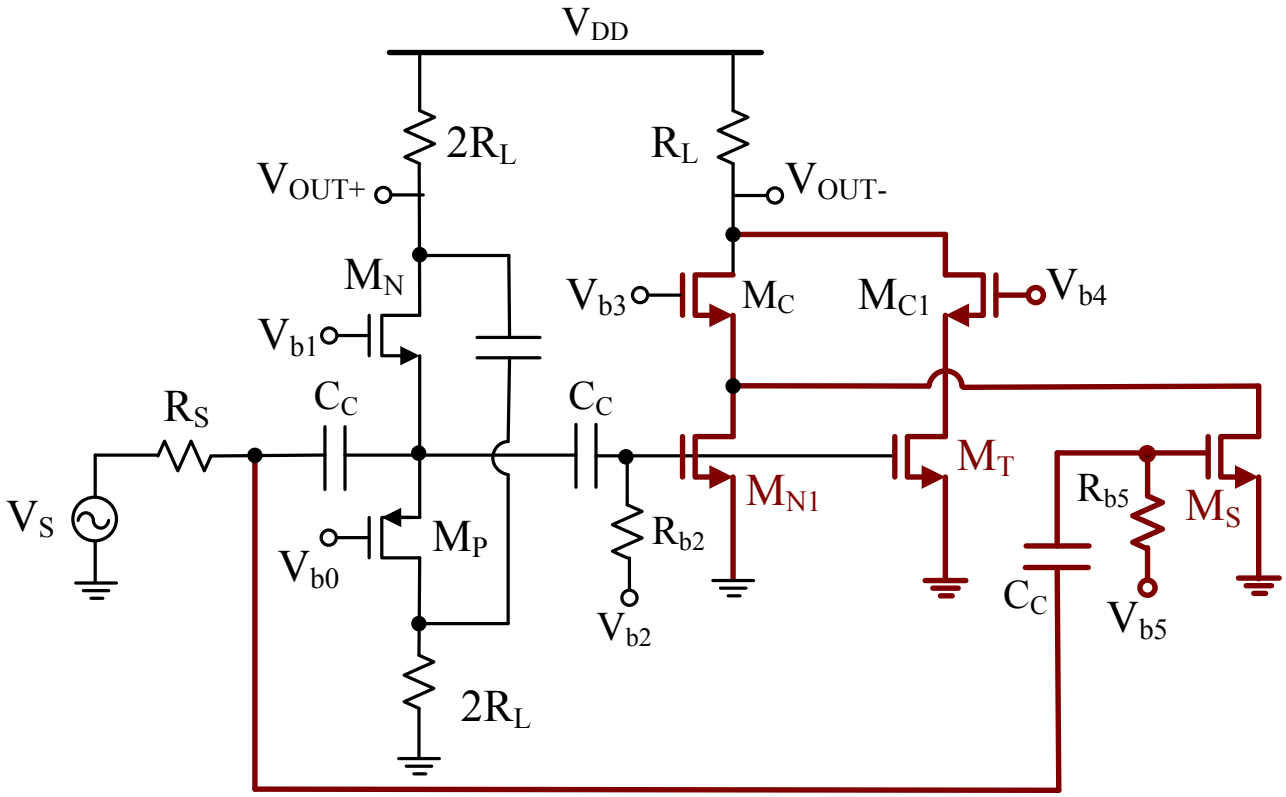
- Significant benefits such as balanced outputs as well as noise and distortion cancellation in the CG stage

Noise/distortion cancelling Balun-LNA



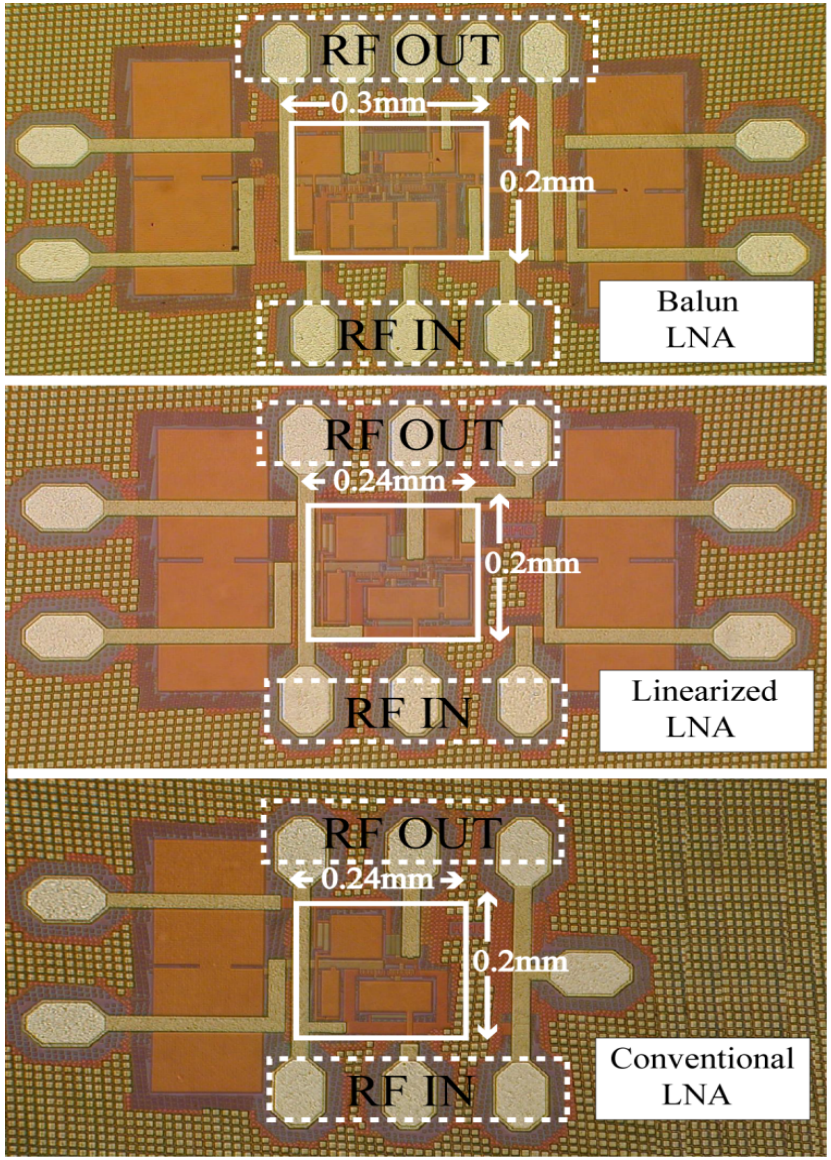
- Noise/distortion of M_N(MP) appears as common mode.
- **Noise/distortion performance limited by the CS stage.**
- **Use RDS to improve the linearity of CS stage.**

Noise/distortion Cancelling Balun-LNA



- Distortion in CS stage is reduced by RDS.
- Power overhead <8%.
- Noise overhead < 0.1 dB.

Chip Microphotograph

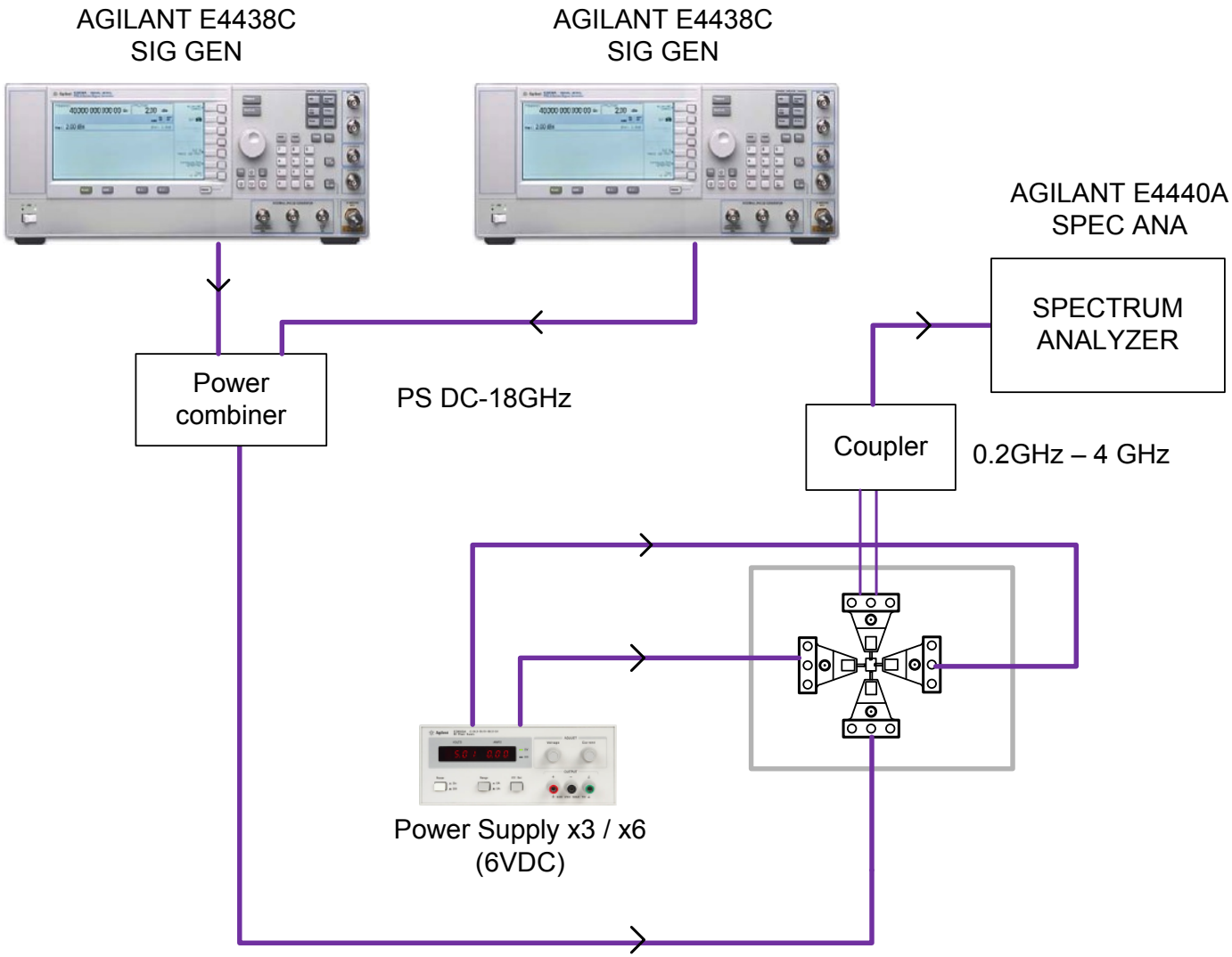


- Jazz 0.18um CMOS Tech..
- Wafer probing test.
- No output buffers.

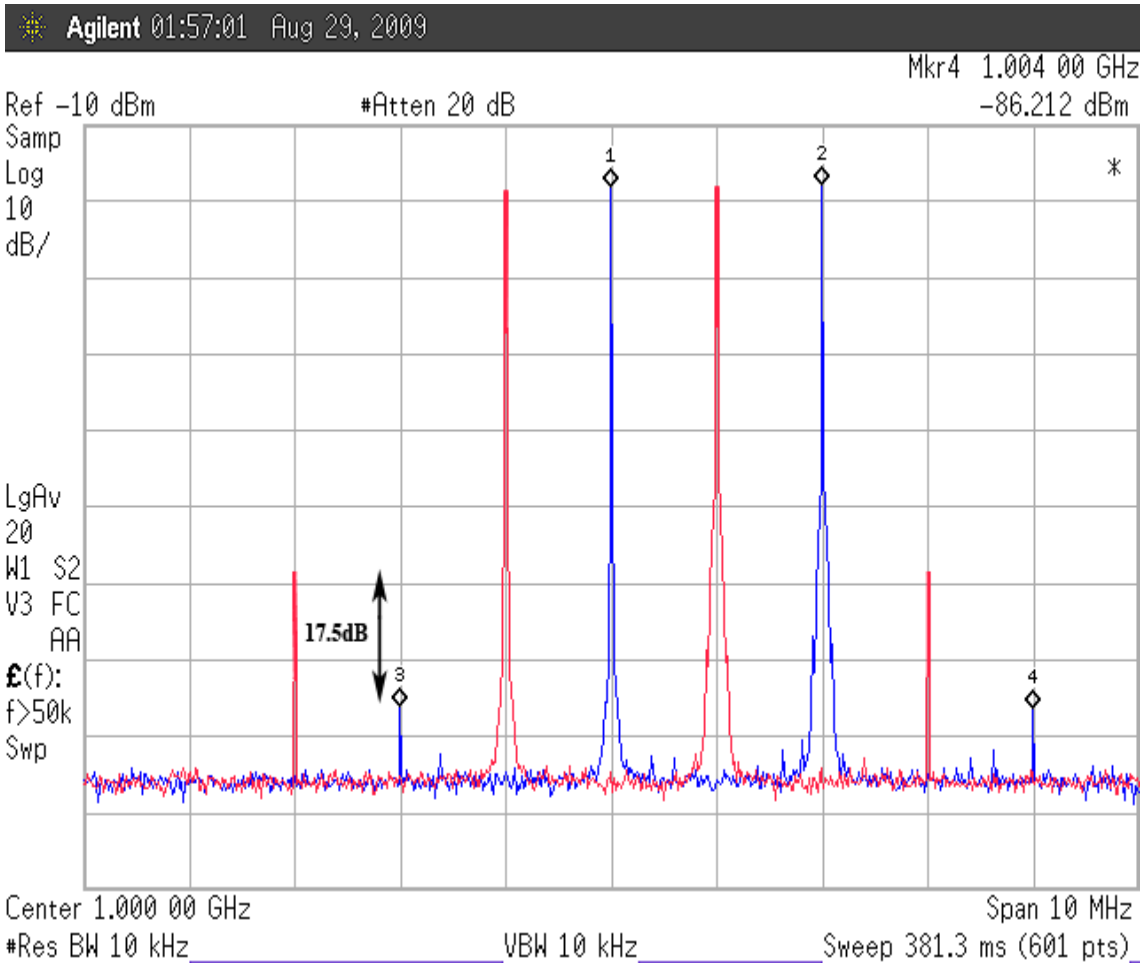
Silicon area: 0.06 mm^2

Measurement results

Test Setup for linearity



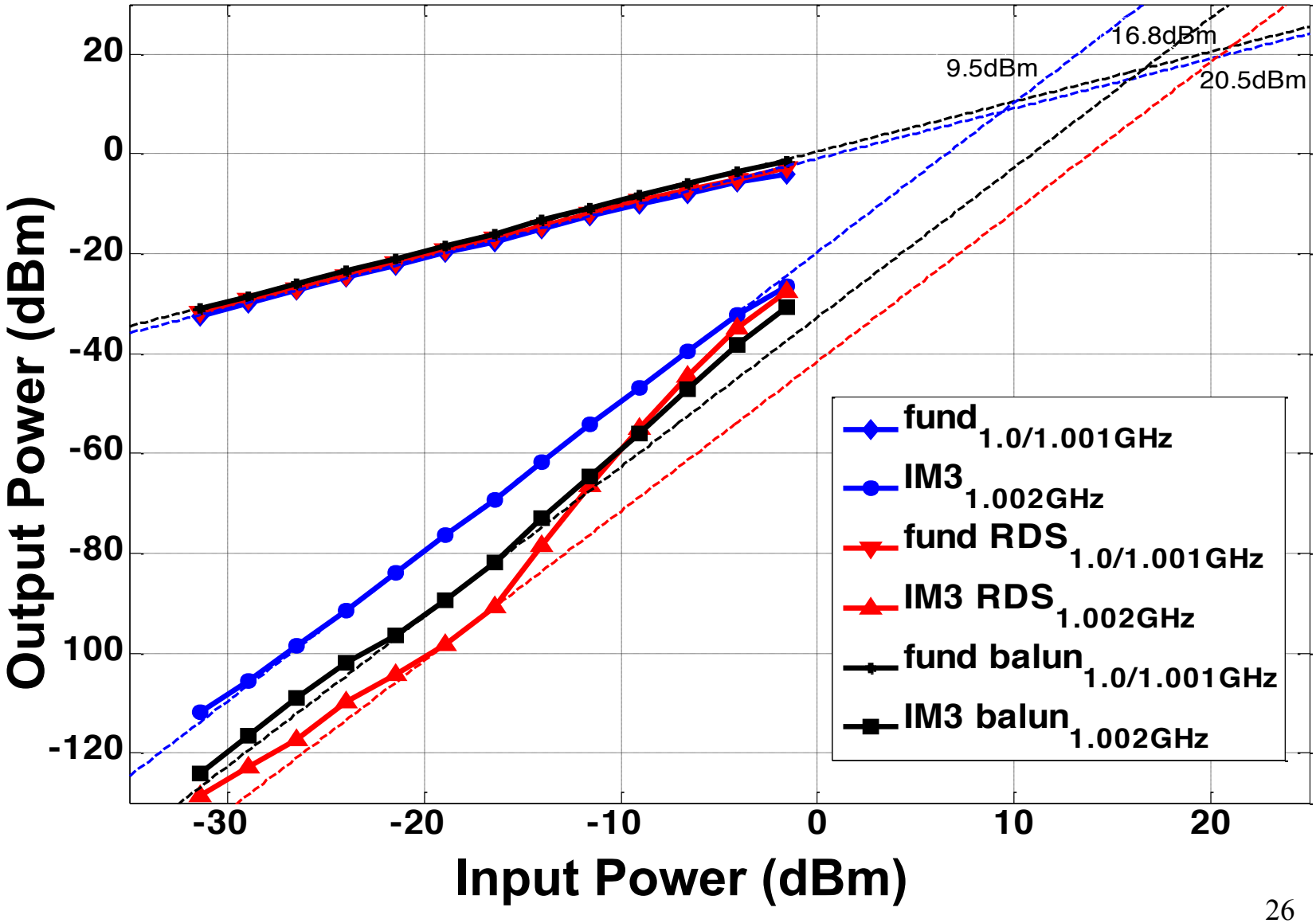
Measured LNA linearity



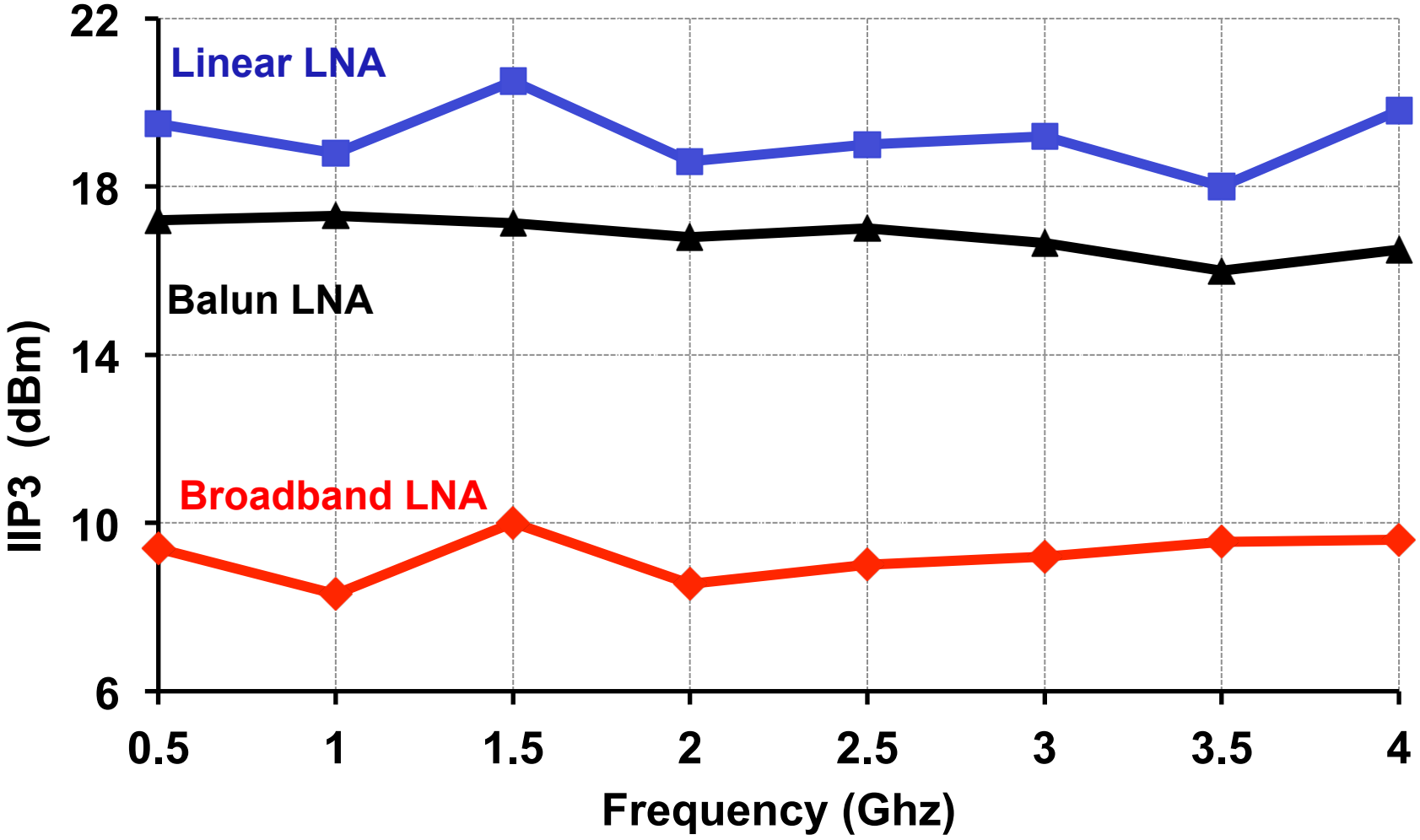
Two-tone test measurements with -16.5 dBm input power per tone at 1GHz with Δf = 2 MHz

Proposed (blue) LNA outperform the linearity of the conventional LNA (red) by 17.5dB

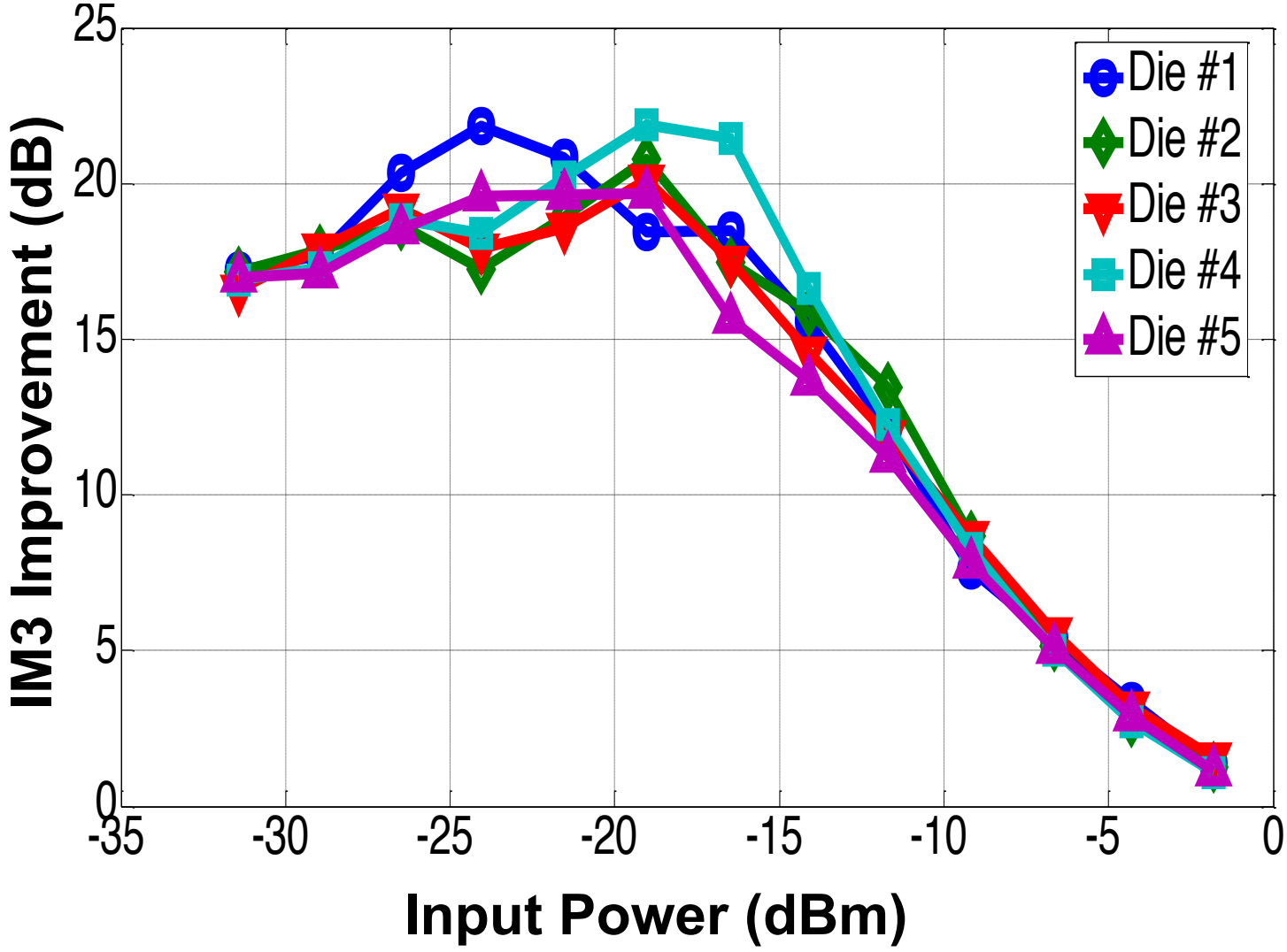
Measured LNA linearity



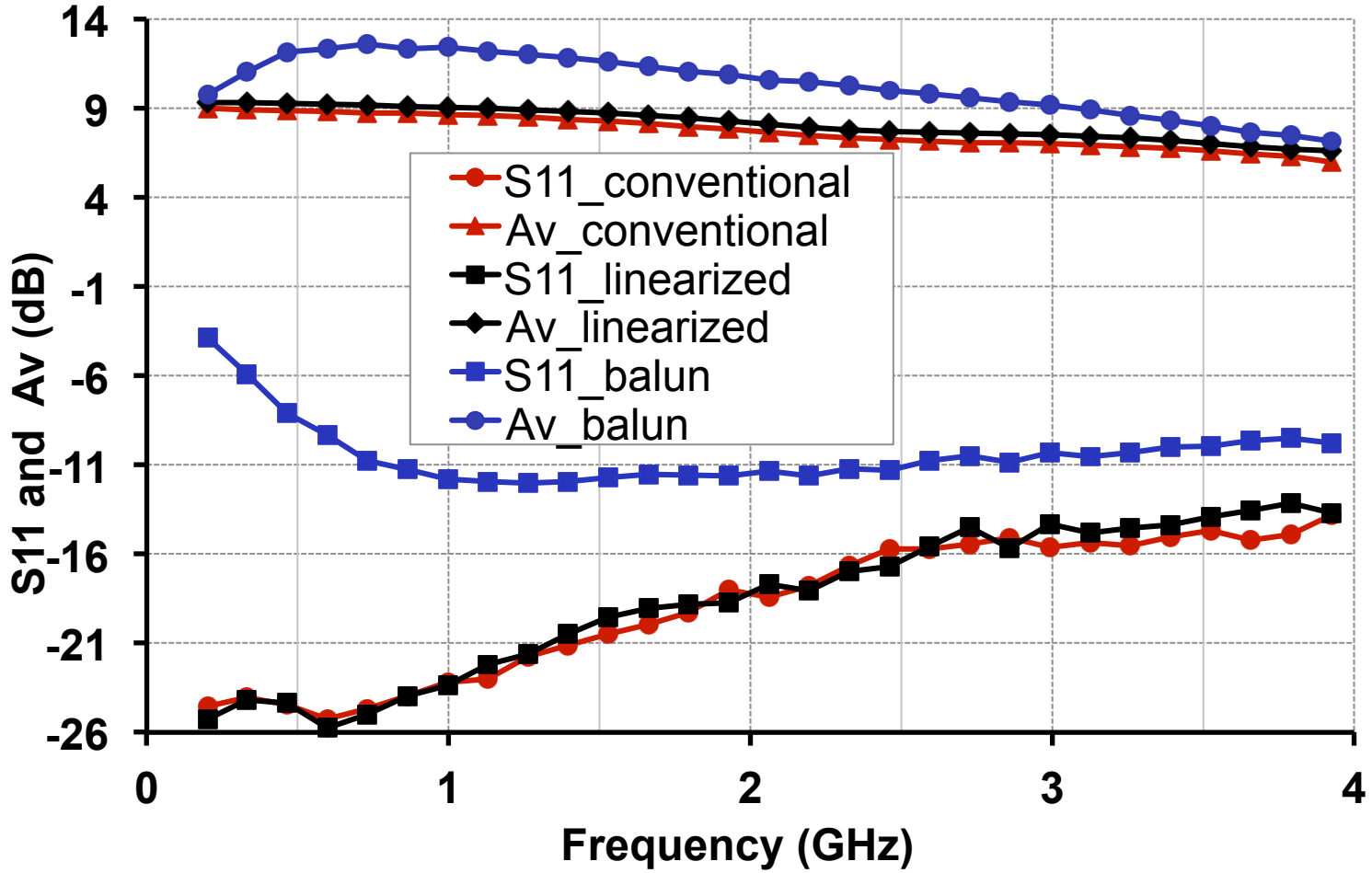
IIP3 vs Frequency



Linearity Performance of 5 Chips

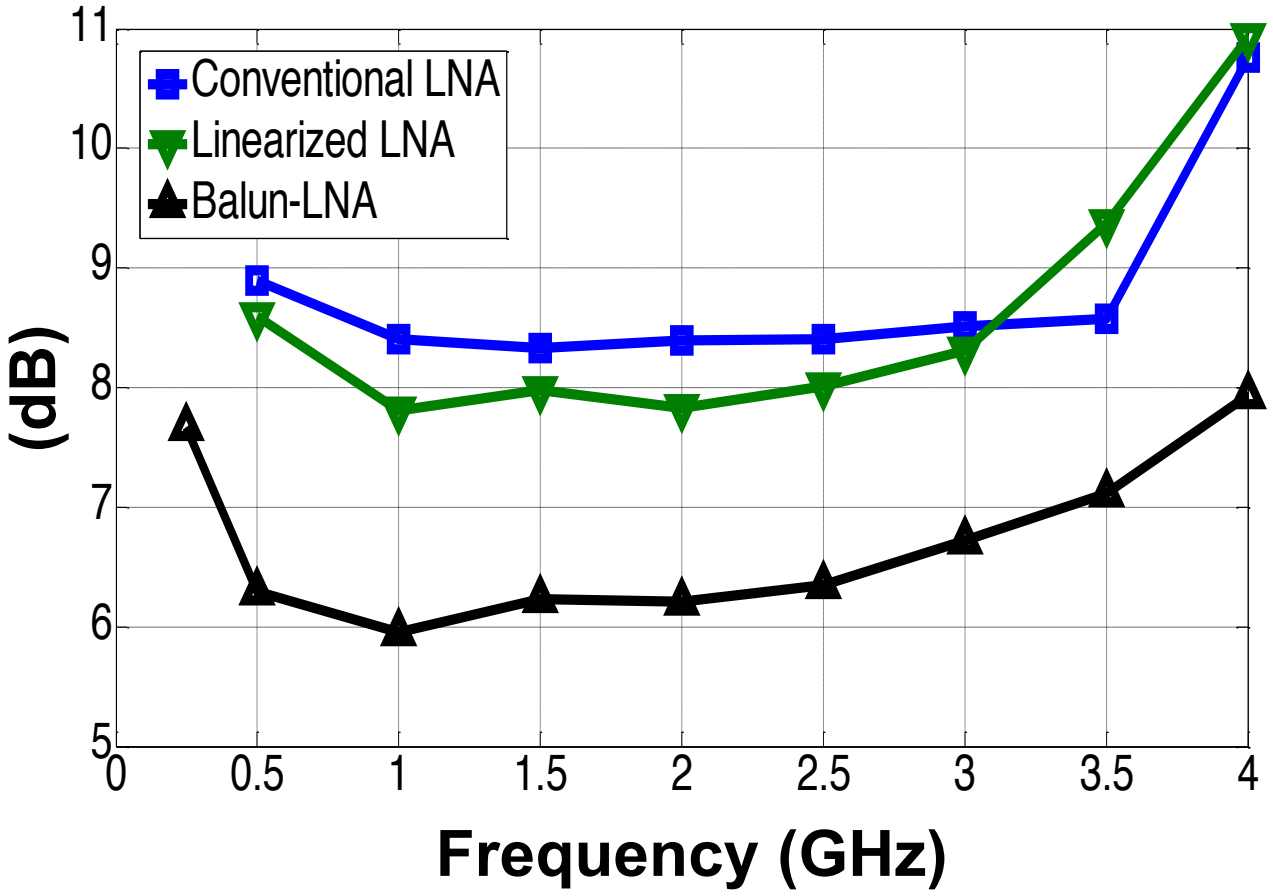


Input matching & gain Performance



Av = Internal gain: $$Av = S_{21} * \frac{Z_{22} + Z_{PORT}}{Z_{PORT}} + 3dB(balun)$$

Noise Figure



Comparison with Prior Art

	Blaakmeer JSSC-2008	Ramzan ISSCC-07	Chen JSSC-08	Van de Beek ISSCC-08	This work Balun-LNA
Technology	65nm	0.13µm	0.13µm	45nm	0.18µm
BW [Ghz]	0.2~5.2	1~7	0.8~2.1	0.6~10	0.3~2.8
Av [dB]	13~15.6	17	**14.5	10	**9.6~12.5
NF [dB]	2.9~3.5	2.4	2.6	3	5.95~6.5
IIP3 [dBm]	**0~4**	**-4.1**	**16.0**	**6.0**	**16.8**
P_{1dB} [dBm]	**-**	**-**	**-11**	**-**	**0.5**
Power [mW]	14	25	17.4	30*	14.2
No. of coils	0	0	0	2	0
Area (mm^2)	0.009	0.019	0.0992	-	0.06
FOM	**16.22**	**6.343**	**102.3**		**34.3**

** Includes V-to-I converter.*
***Internal gain (Gain after de-embedding)*

$$FOM = \frac{IIP3_{AVG}[mW].PowerGain_{AVG}[abs].BW[Ghz]}{Pdc[mW](F_{AVG}-1)}$$

Conclusions

- A highly linear LNTA for SAW-less radios is proposed
- A robust derivative superposition technique low-sensitive to the process variations with little penalty in power consumption (< 8%) and wideband frequency effectiveness was proposed.
- The proposed balun-LNA simultaneously achieves impedance matching, noise and distortion canceling, and a well-balanced output.
- The proposed technique was validated in a resistive terminated LNA and a balun-LNA.
- The proposed linearization approach can be extended to most of the existing topologies.

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Fully Balanced Low-Noise Transconductance Amplifiers with P_{1dB} > 0dBm in 45nm

Hemasundar M Geddada[1], José Silva-Martínez[1], and Stewart S. Taylor[2]

[1]Texas A&M University

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- Low power LNTA
- Experimental results
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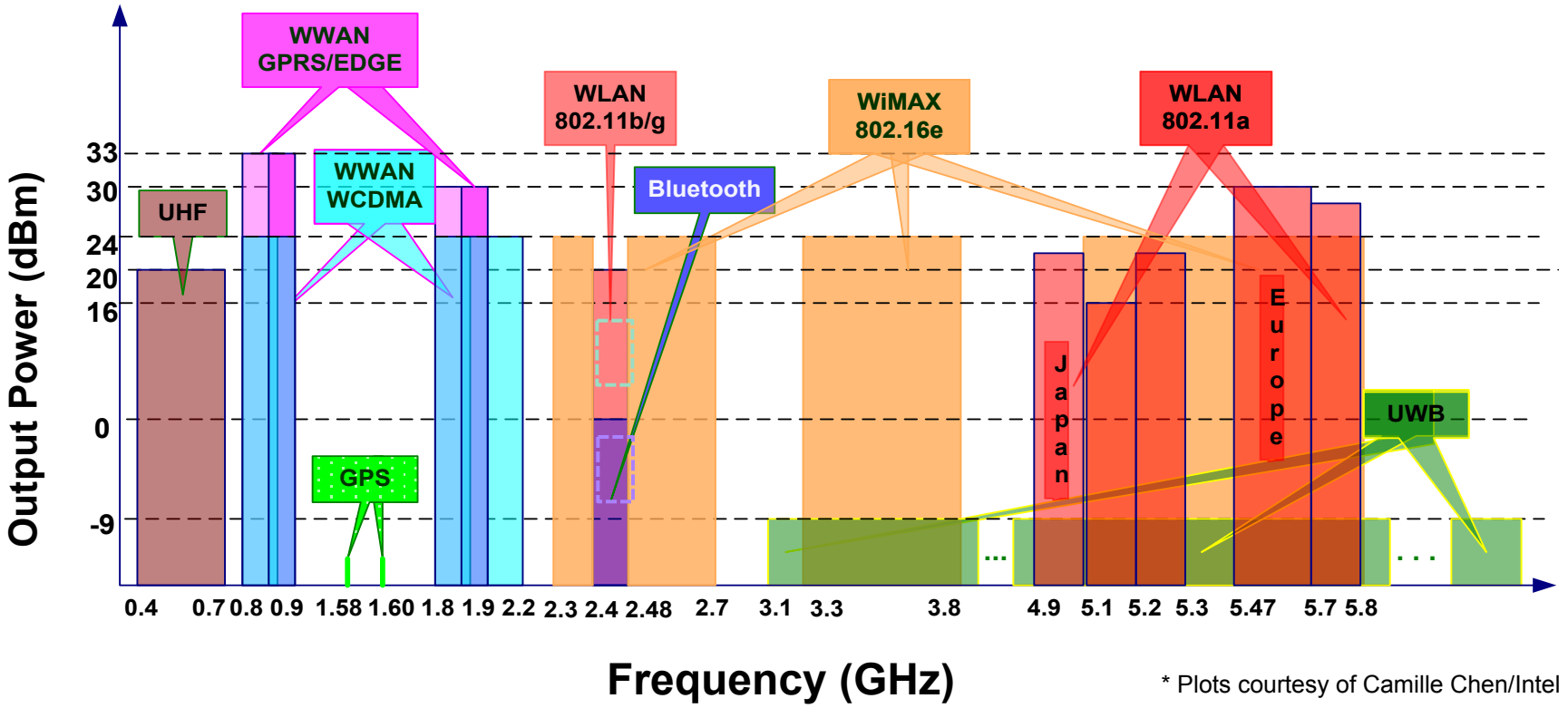
Introduction



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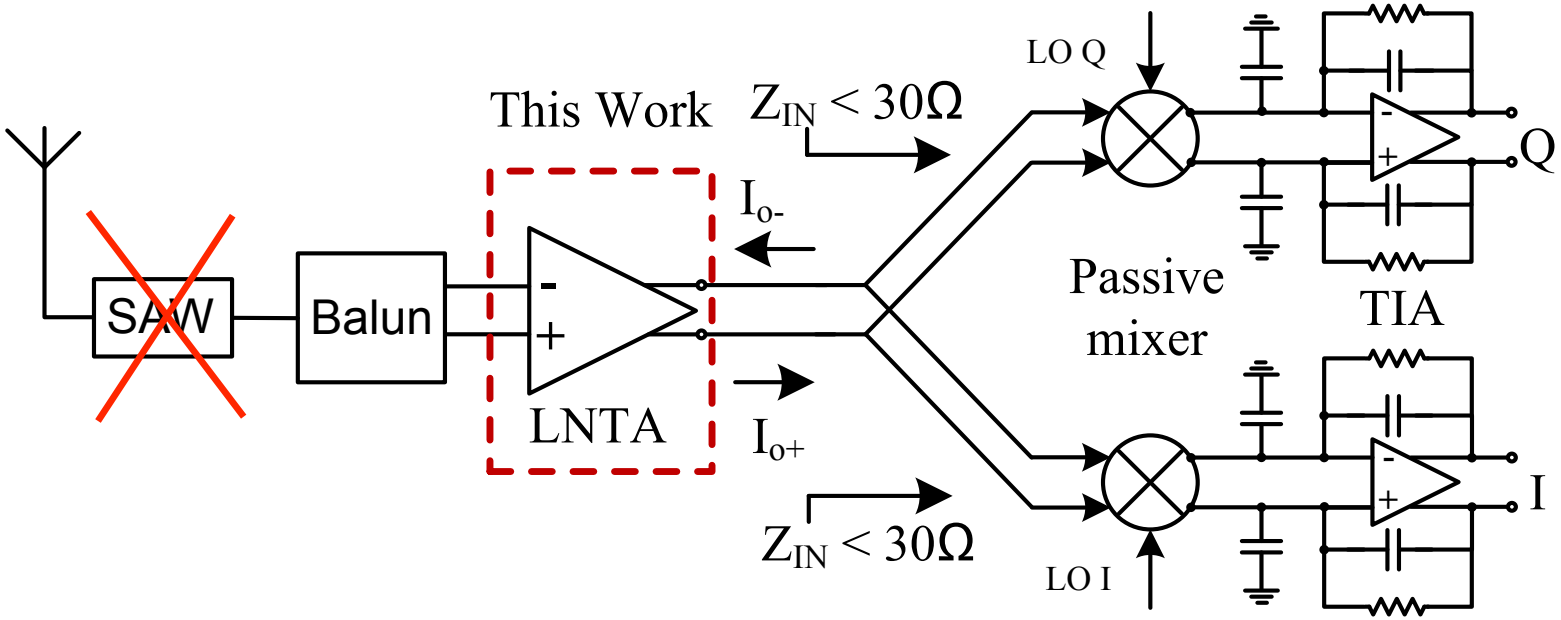
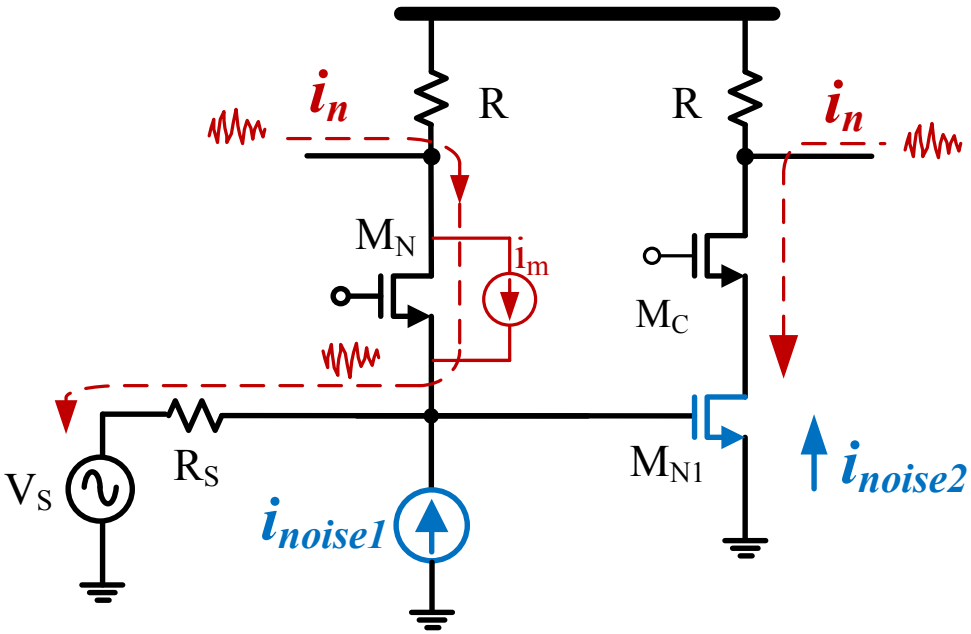


Direct Conversion Receiver Architecture:

Better performance in terms of noise, linearity and power consumption.

Linearity bottleneck → LNTA

Low-Noise Balun-LNA



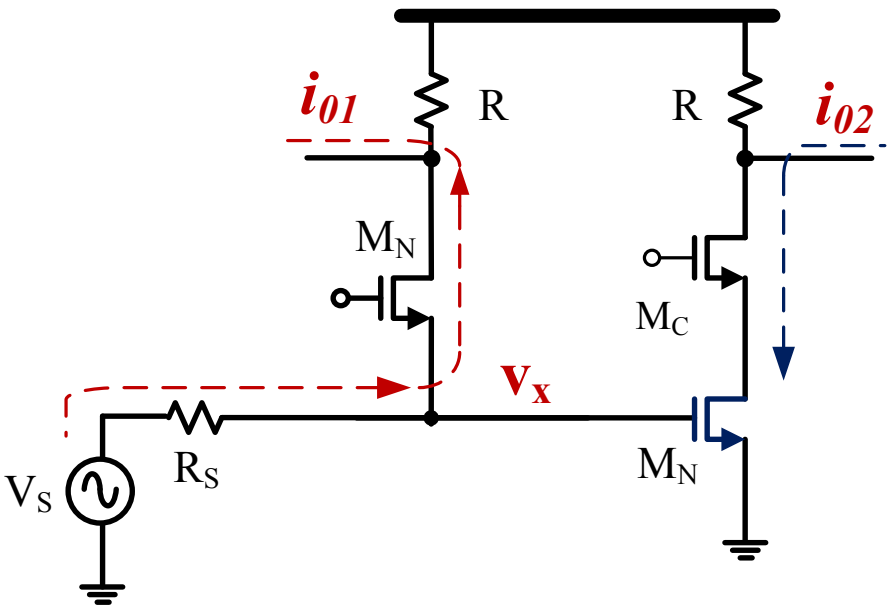
B. Gilbert (Micro-Mixer)
Blaakmeer et. al. JSSC 2008

i_n Cancellation condition for balanced operation

$$g_{mCS} = g_{mCG}$$

- Noise of M_N appears as common mode.
- Noise performance limited by the CS stage and bias.
- Trade off between NF and balanced outputs
- Limited linearity

Low-Noise Balun-LNA



$$i_{01} = \frac{V_S - V_X}{R_S}$$

For same Gmi=1/Rs

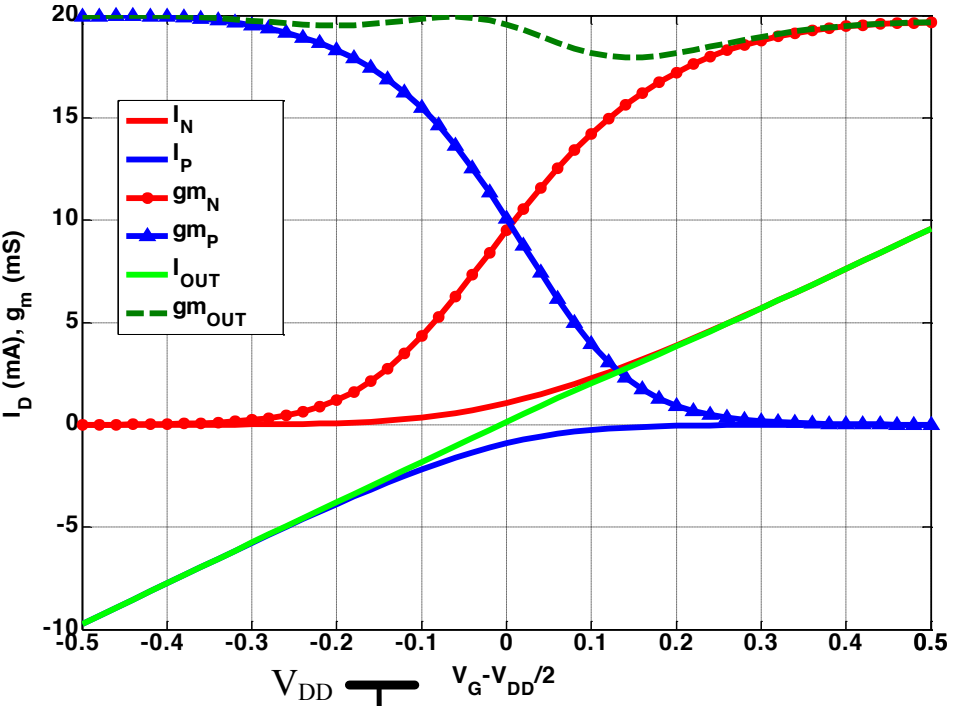
$$i_{01} = \sum_j Gmj\left(-V_X\right)^j$$

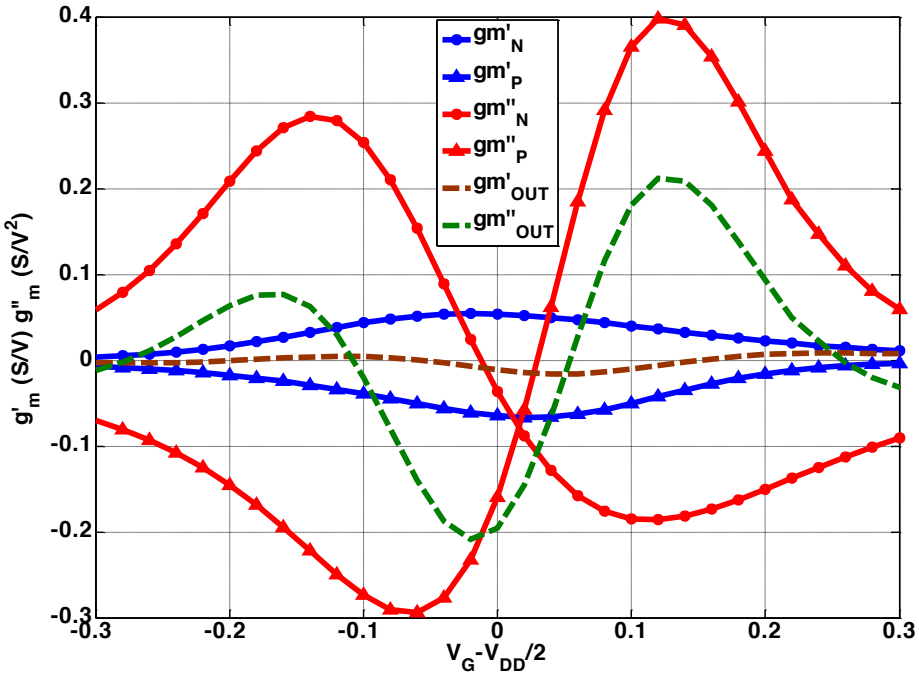
$$i_{02} = Gm1\left(V_X\right) + \sum_{j=2} Gmj\left(V_X\right)^j$$

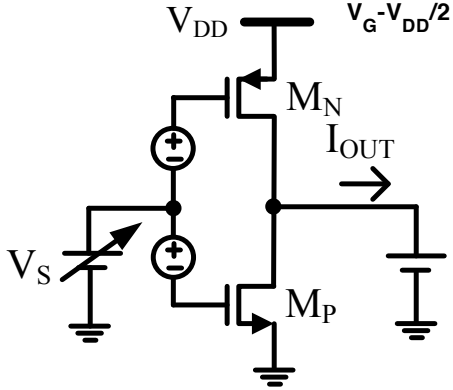
$$V_X = \left(\frac{V_S}{2} + C_2 V_S{}^2\right) + \sum_{j=3} C_j V_S{}^j$$

- Non-linearities in i_{01} can be converted in common-mode
- Cross products in i_{02} remain
- Vx is a strong function of the common-gate linearity

Complementary PMOS-NMOS: DC characteristics

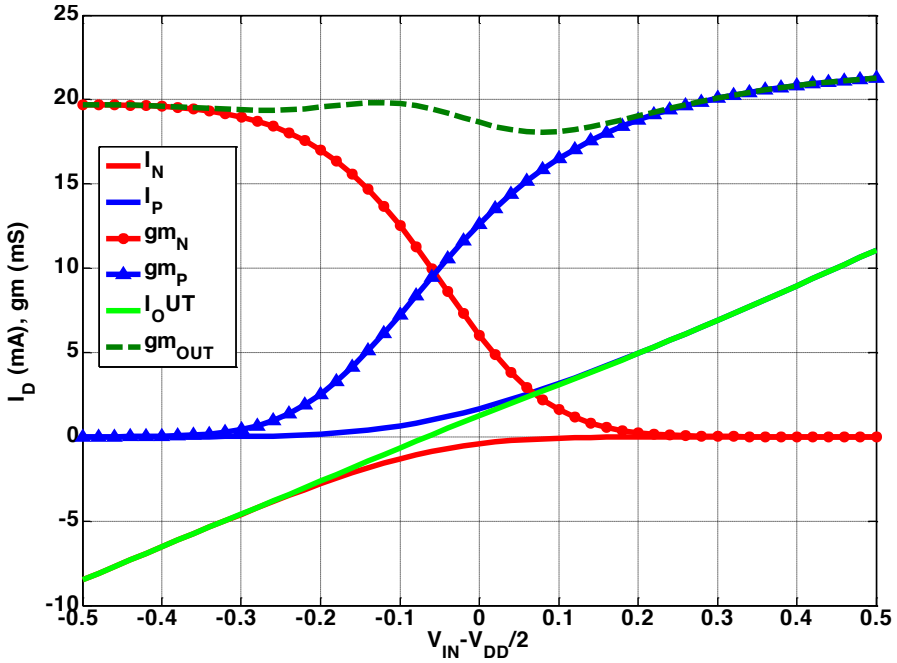


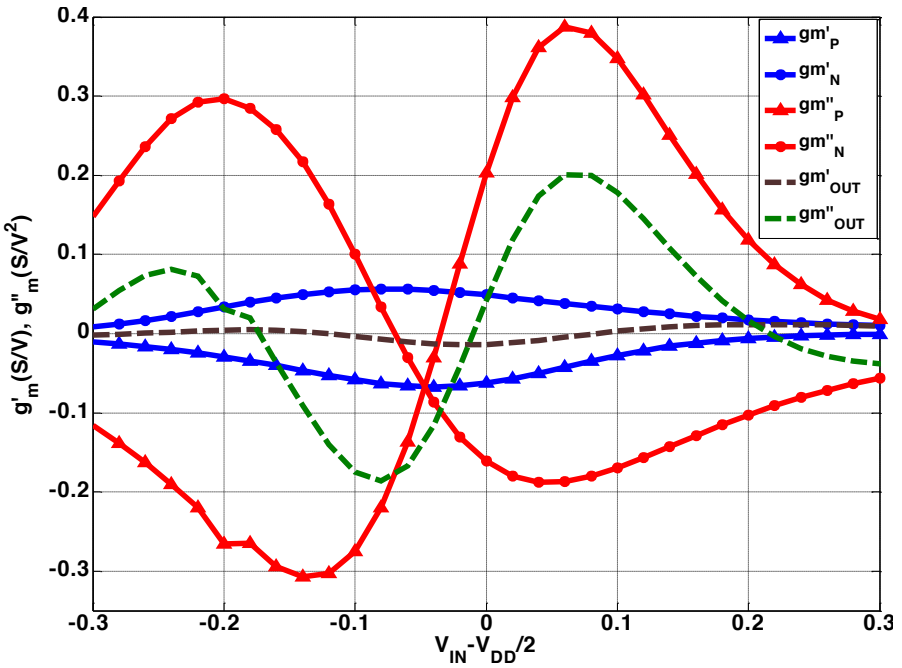


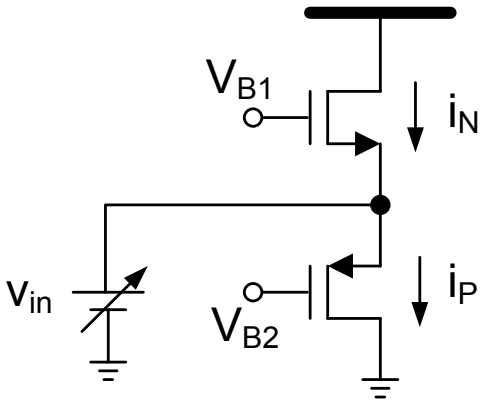


PMOS-NMOS combination makes gm'$_{OUT}$⇒0 and Minimizes gm"$_{OUT}$

Complementary PMOS-NMOS: DC characteristics



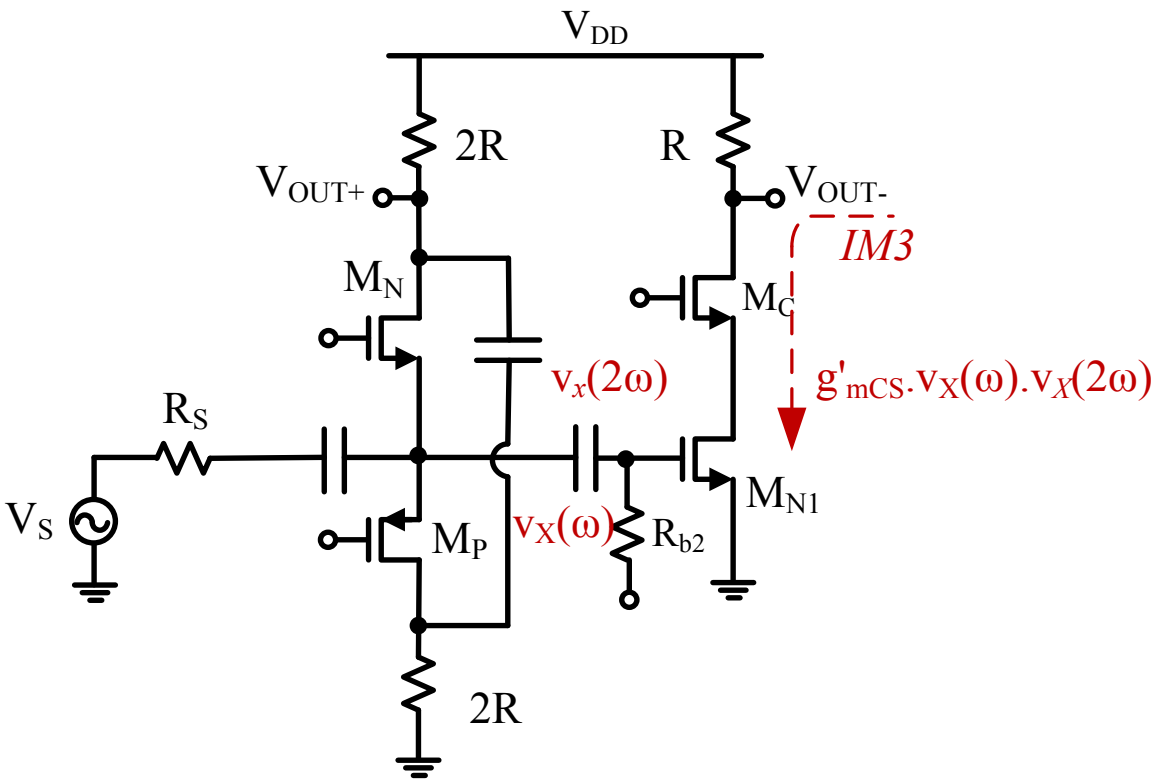




Proper PMOS-NMOS combination makes $gm'_{DIFF} \Rightarrow 0$;

Common Source voltage more linear!

Noise/distortion cancelling Balun-LNTA

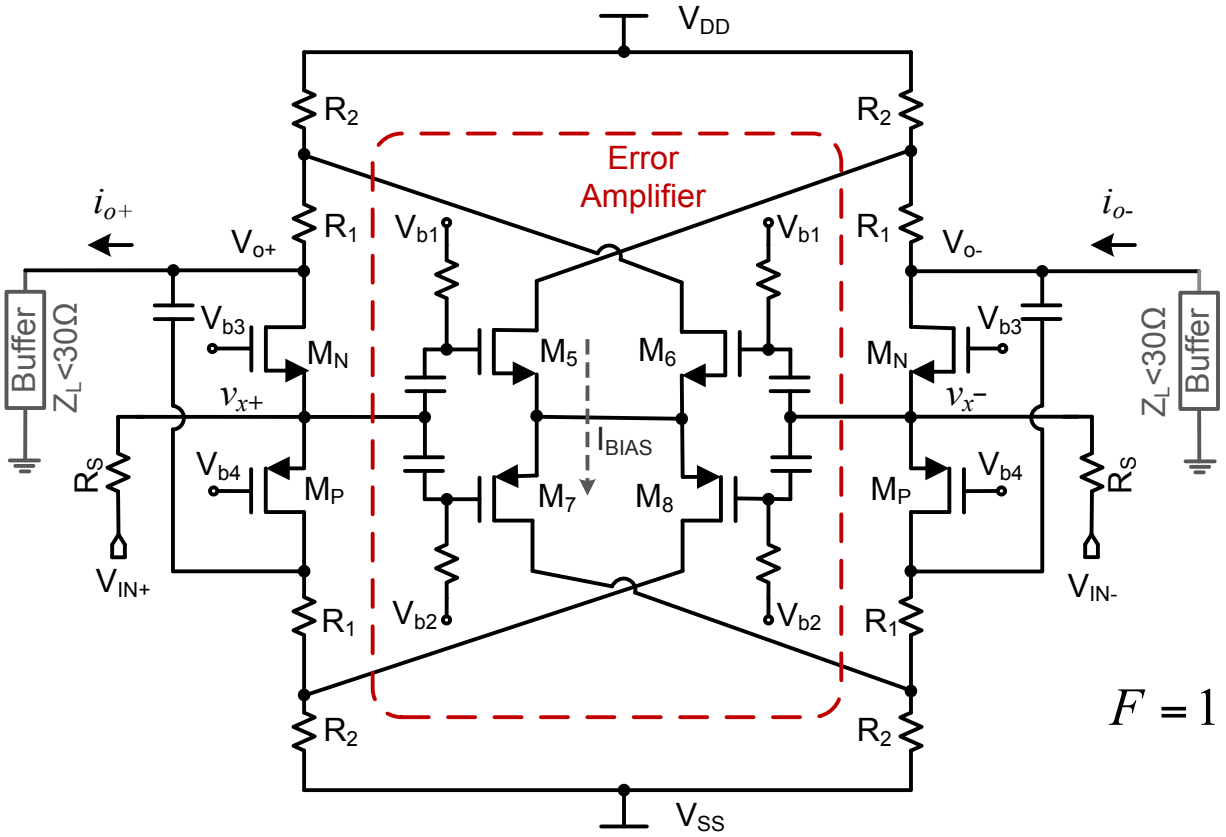


$$g'_{mCG} = g'_{mN} - g'_{mP} \sim 0$$

$$v_x(2\omega) \sim 0$$

- Input CG stage is implemented current reuse M_N-M_P
- PMOS-NMOS → Even order distortion cancellation.
- IM3 because 2nd order interaction is reduced.

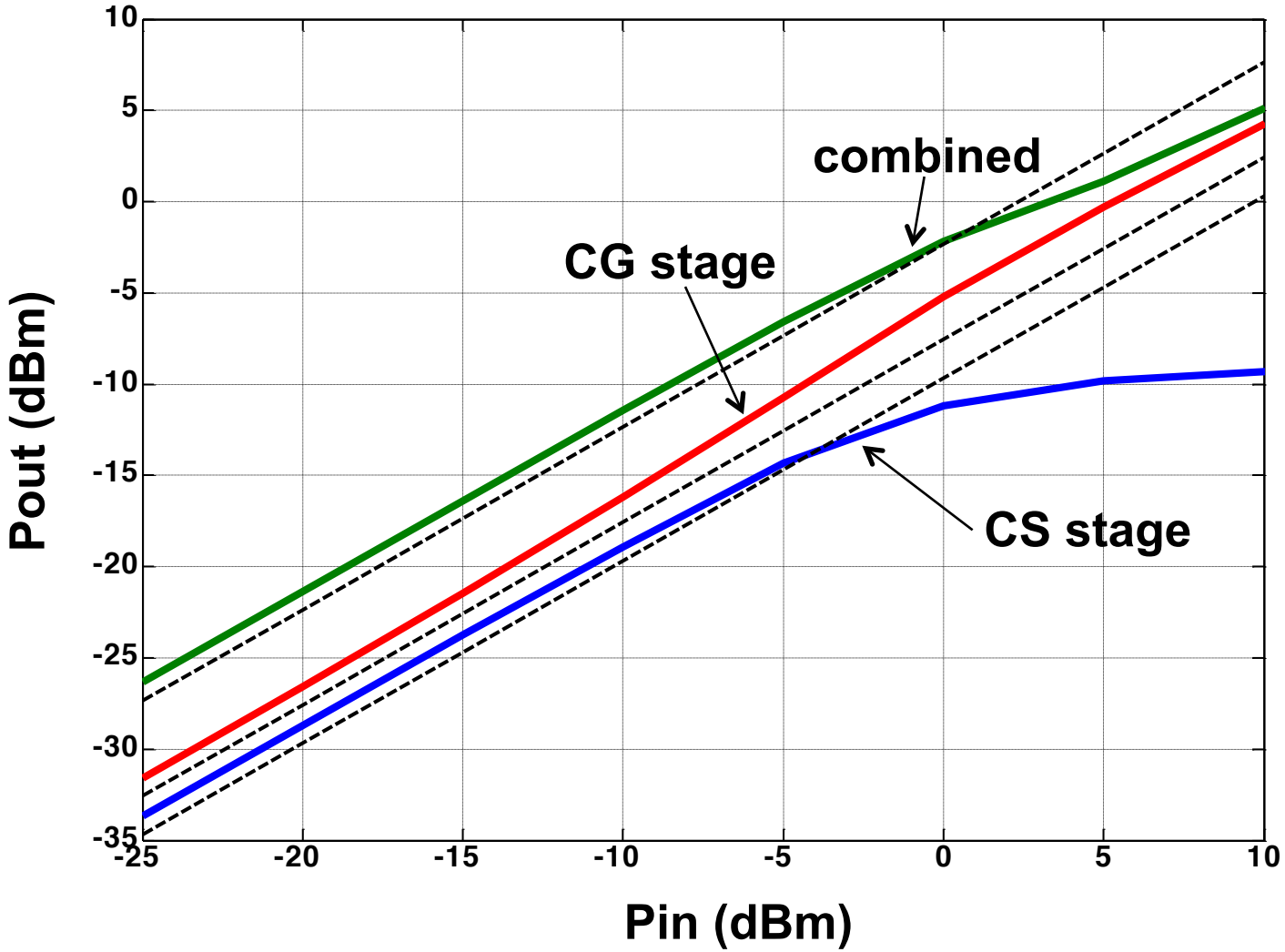
Noise/distortion Cancelling LNTA



$$F = 1 + F_{CG} + F_{CS} + F_{R1,R2}$$

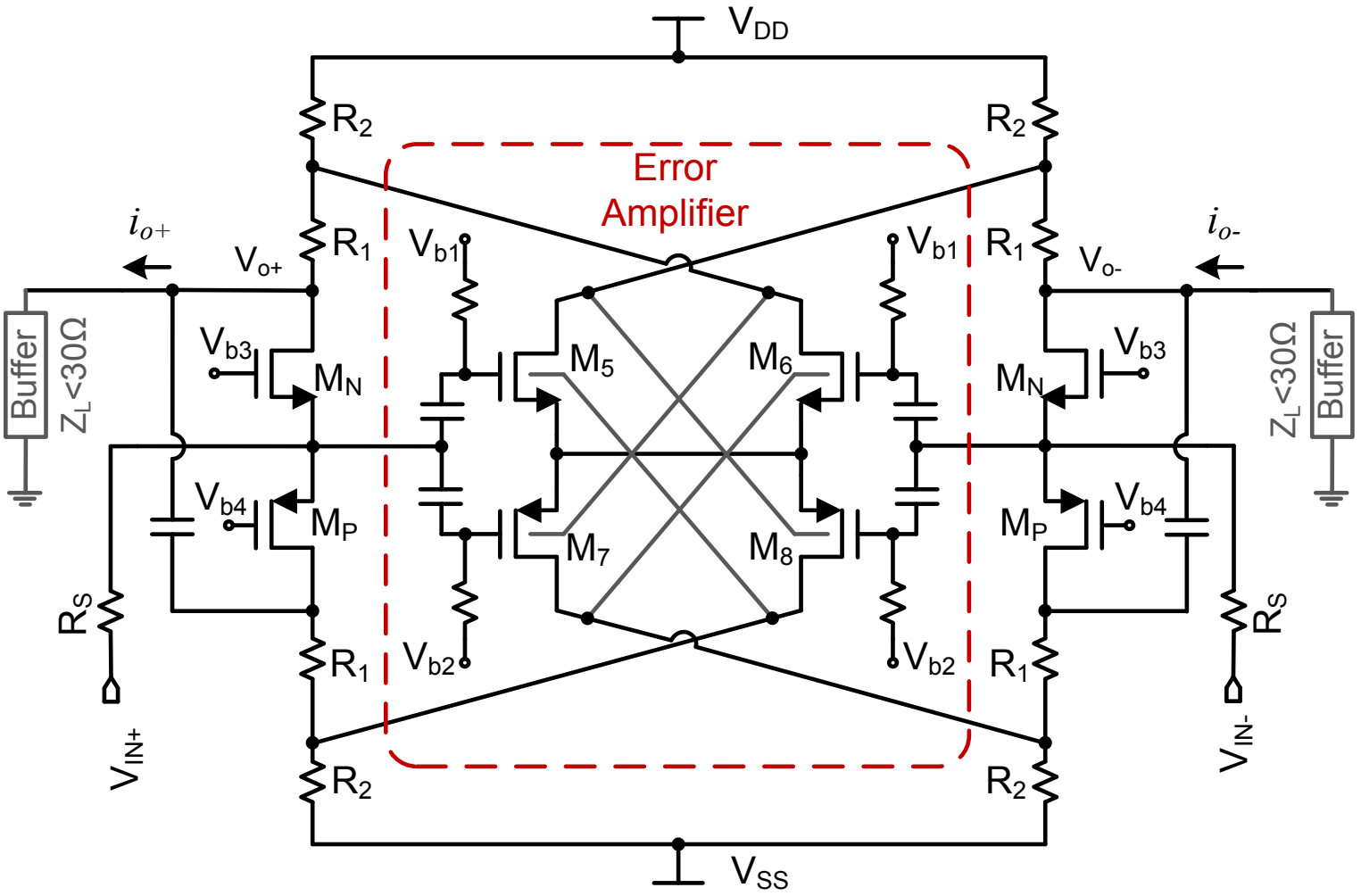
- Current re-use PMOS-NMOS error amplifier
- Error amplifier is implemented through PMOS-NMOS combination→g'_{mCS}~0

Large signal linearity, P_{1dB}



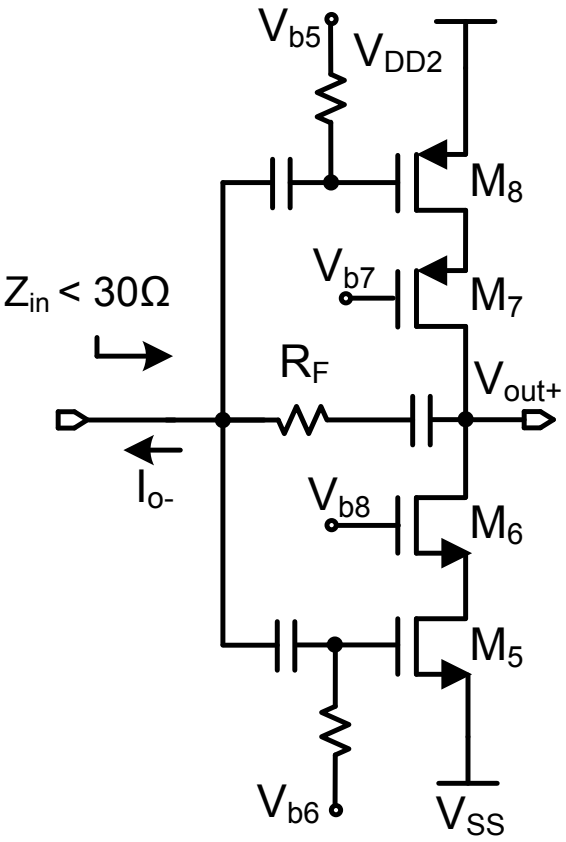
- Gain compression in the Error (CS) stage is counteracted by the Gain expansion in the CG stage

Low power LNTA



Bulk driven EA: transistor sizes and currents are scaled down to maintain the value of the original transconductance

On chip output buffer



$$Z_{IN} = C_P \parallel \frac{R_F + R_{OUT}}{1 + g_m R_{OUT}}$$

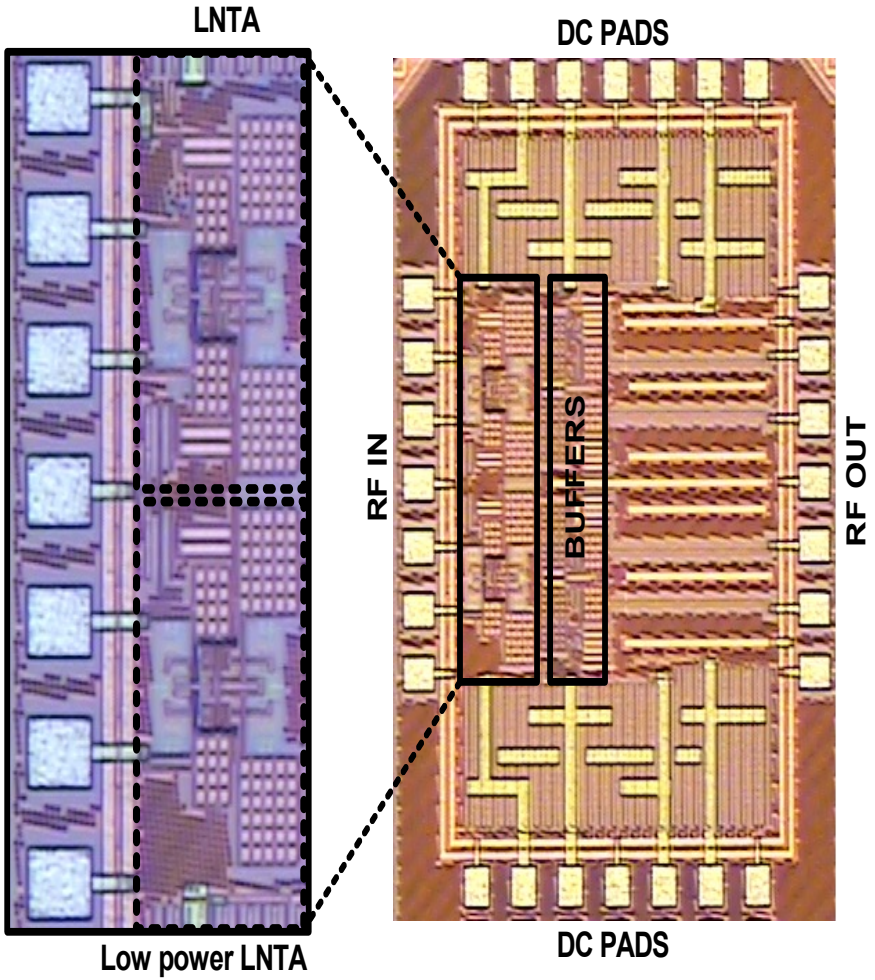
$$A_V = \frac{R_{OUT}(1 - g_m R_{OUT})}{R_F + R_{OUT}}$$

$$g_m = g_{m5} + g_{m8}$$

C_P= Input parasitic shunt cap

- Resistive feedback amplifier with Z_{IN} ~ 30Ω
- Programmable A_V in the 6-14dB range and S_{22}< -10
- Two gain modes to facilitate NF and Linearity measurement

Chip Microphotograph

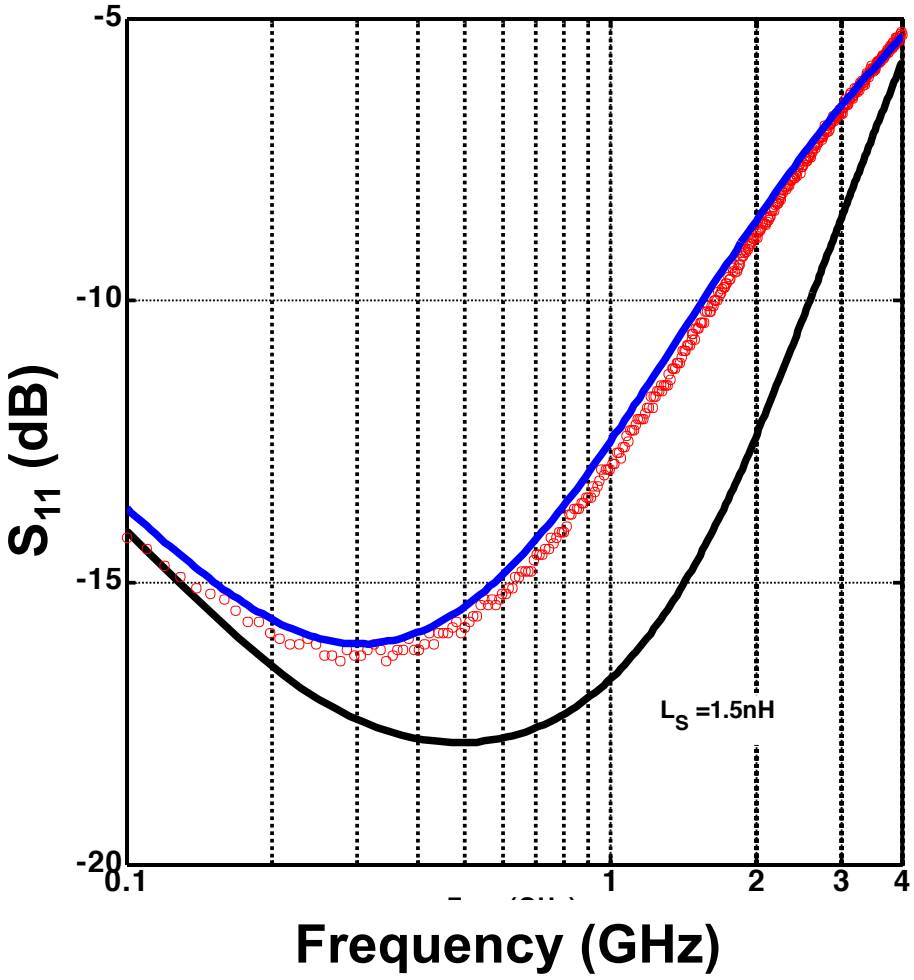


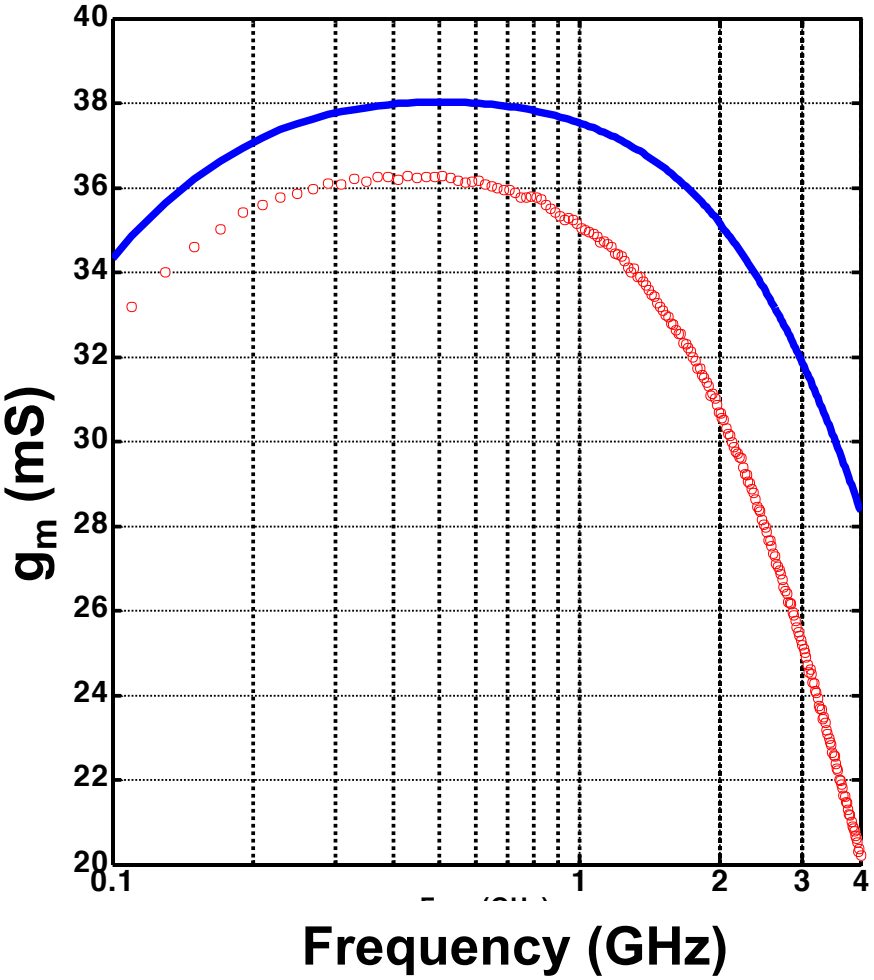
- 45nm CMOS Technology
- Wafer probing test.

Silicon area: 0.06 mm^2

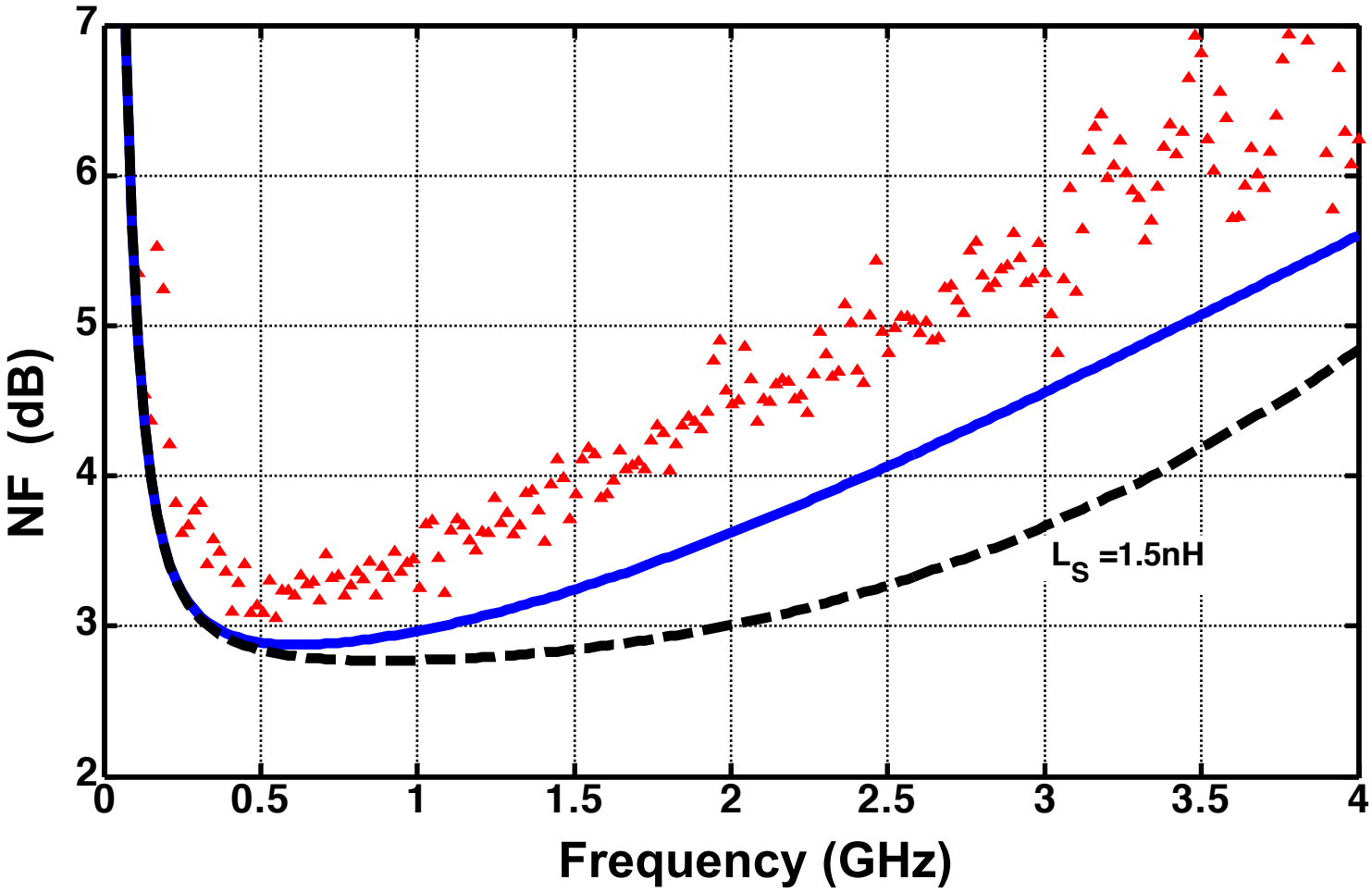
Measurement results

Input matching & Transconductance



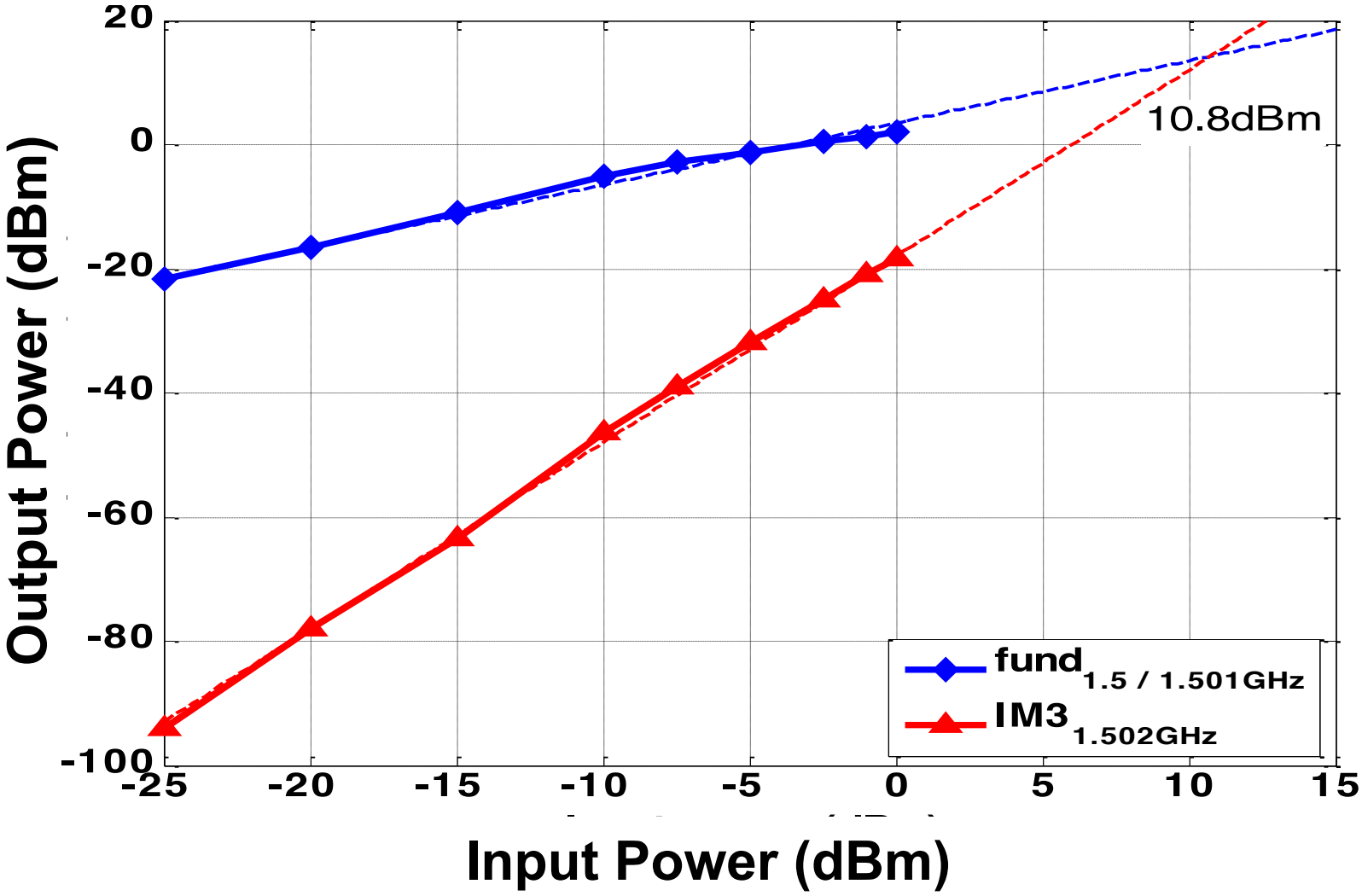


Noise Figure

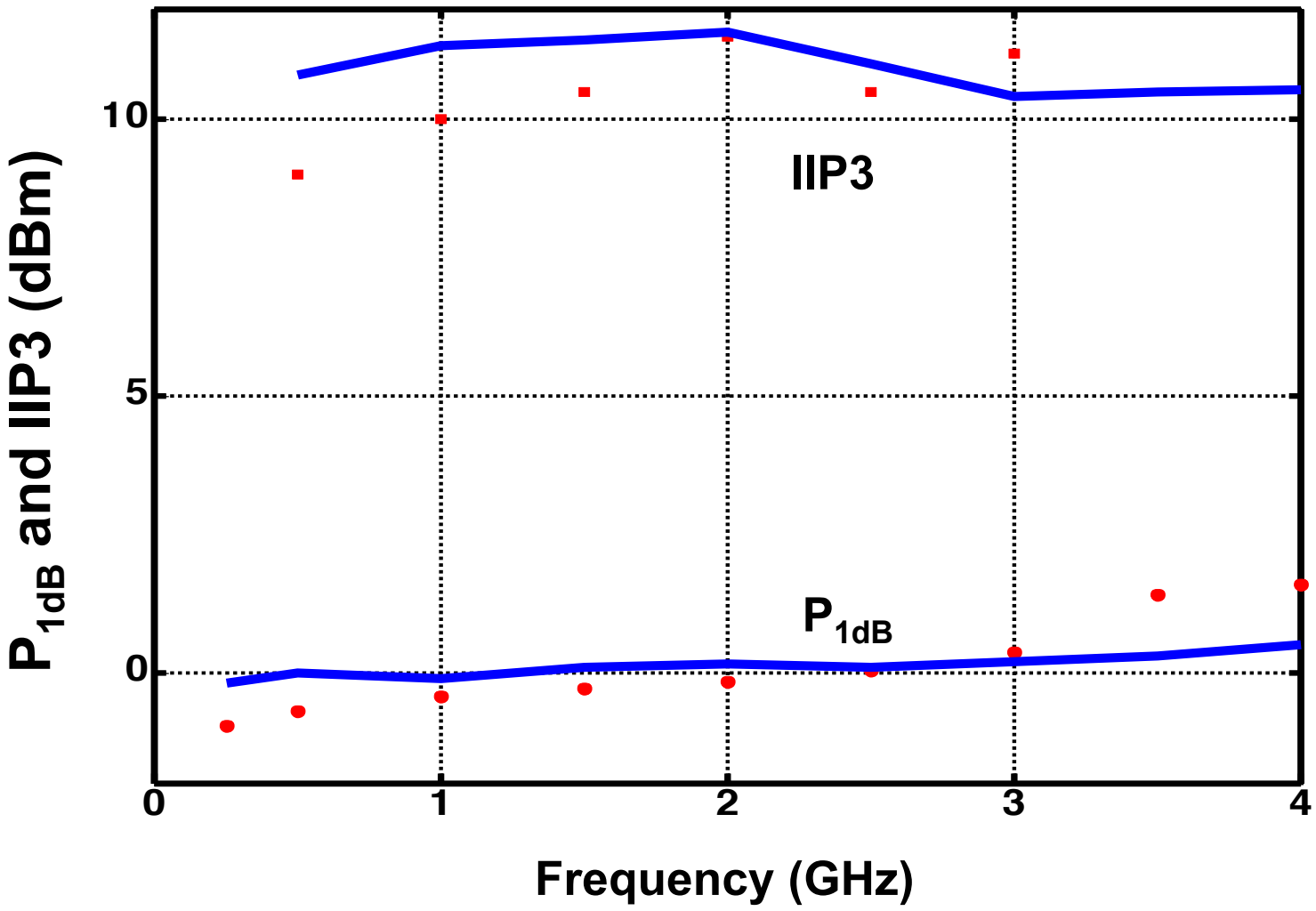


NF of LNTA (lines: simulations; markers: measurements, Ls = series inductance of 1.5nH at the input).

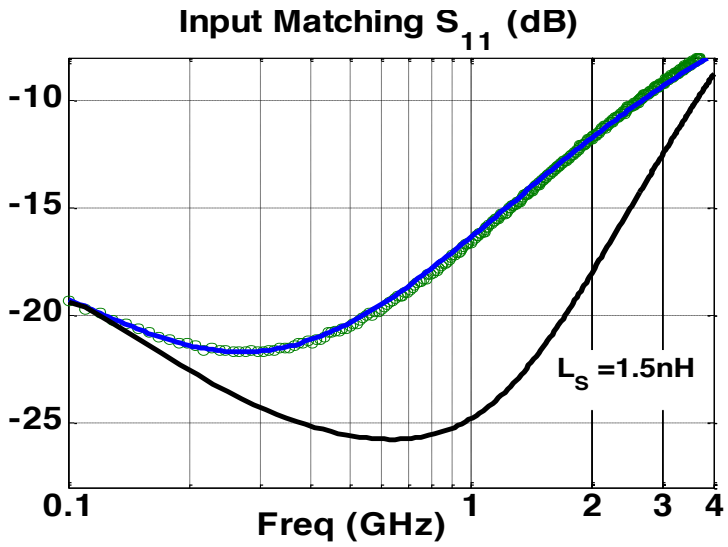
Measured LNTA linearity: 2-tone test

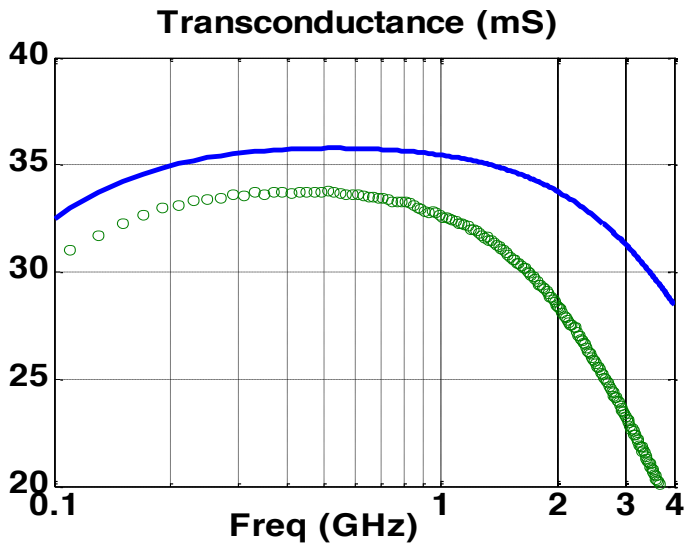


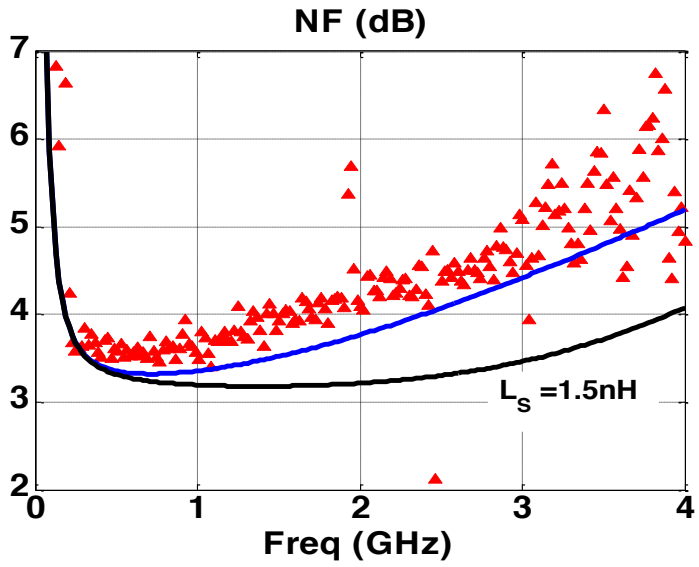
Measured LNTA linearity

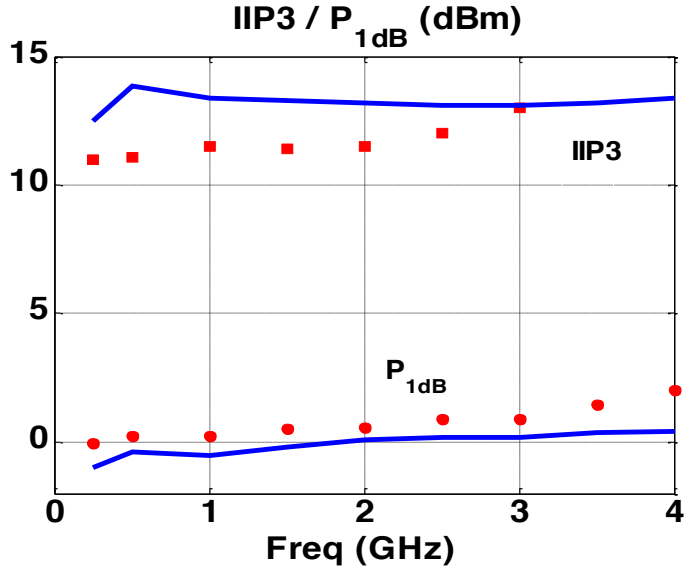


Results for Low-Power LNTA









Comparison with Prior Art

Parameter	JSSC 08	TMTT 10	ISSCC 08	ESSCIRC 10[+]	LNTA	LP LNTA
Technology	0.13µm	0.18µm	45nm	90nm	45nm	45nm
Freq (GHz)	0.8 - 2.1	1-3	0.6 - 10	0.4-3	0.1 - 2	0.1 - 3
S11 (dB)	<-8.5	<-9	-	<-10	< -9	< -9
Gain(dB)/ gm(mS)	14.5[φ]/ NA	16.9/ NA	10/ NA	15/ NA	11*/ 36.5	10.3*/ 34.5
NF_{min} (dB)	2.5	2.6	3	2.3	3	3.4
IIP3 (dBm)	16	-0.7	6	>5	10.8	12
P_{1dB} (dBm)	**-11 ****	**-11****	**-**	**-10**	**0**	**0.4**
Supply (V)	1.5	1.8	-	2	2.2	2.2
Power (mW)	17.4	12.6	30[Δ]	-	35.2	20
Area (mm^2)	0.099	0.073 [θ]	-	-	0.06	0.06

** Internal gain (removing the R_L of 30Ω); φ Internal gain ** graphically estimated; Δ includes the power of the V-to-I converter; θ active area; + LNA performance de-embedded from receiver front-end*

Conclusions

- Highly linear LNTAs for SAW-less radios is proposed
- The proposed architectures achieve P_{1dB} over 0dBm within the entire 0.2-2(3) GHz frequency band.
- The proposed LNTAs simultaneously achieves impedance matching, partial noise and distortion canceling, and a well-balanced output.
- Room for noise, linearity and power efficiency improvements