# New RF-to-Digital Architectures for Broadband Communication Systems

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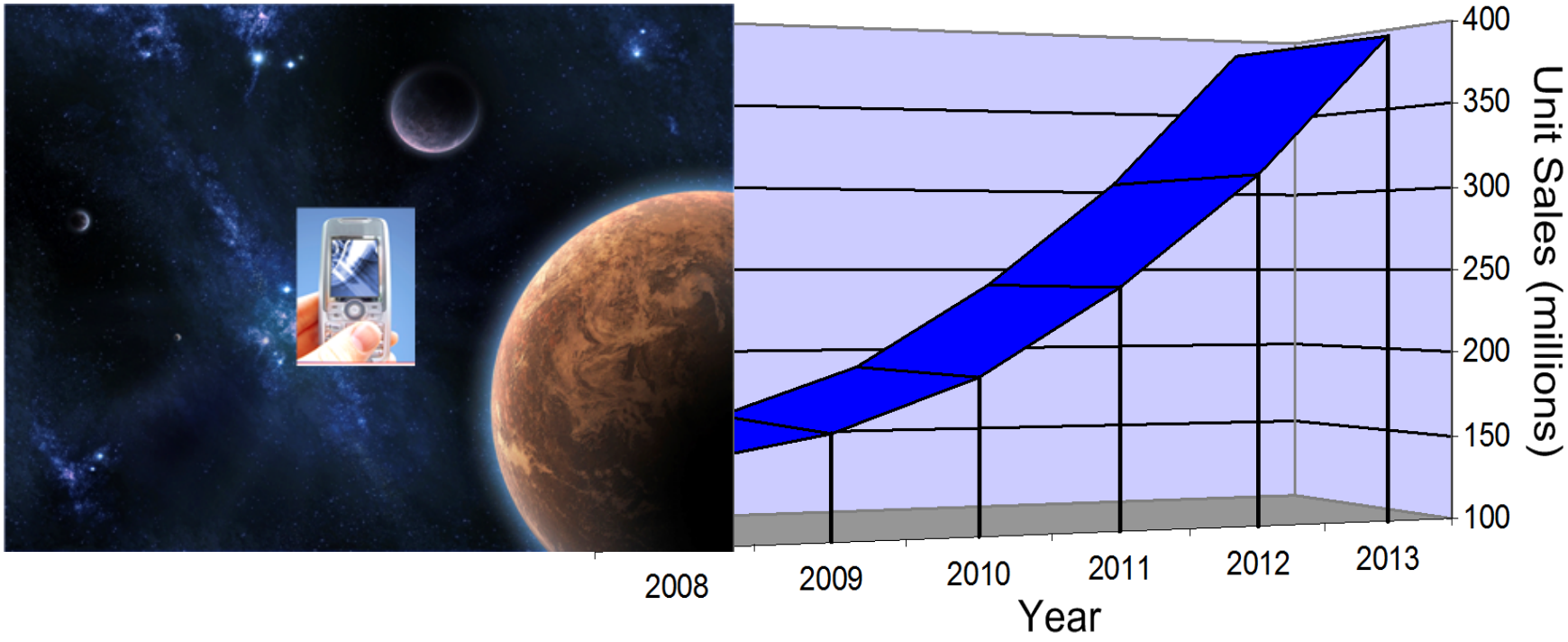
# Outline

- Introduction
- Multi-standard receivers: Front-End Design issues
  - Superheterodyne, Direct Conversion and Digital radio
- RF to Digital Architectures
  - Bandpass Sigma-Delta modulators
- Practical Limitations
  - RF BP-ADC
  - Design Challenges
  - SNDR Limitations
- Digital Assisted Architecture
  - Measuring the NTF function
  - Digitally Assisted Calibration Scheme
  - 200 MHz Prototype
- Concluding remarks

# The Smartphone market




- **Global smartphone market projected to grow**
  - **Anticipated global unit sales to approach 400 millions in 2013**
    - **(market research report from Forward Concepts Co)**
  - **Projected revenue in 2012: $32.2 billion**
    - **(source: In-Stat Group)**

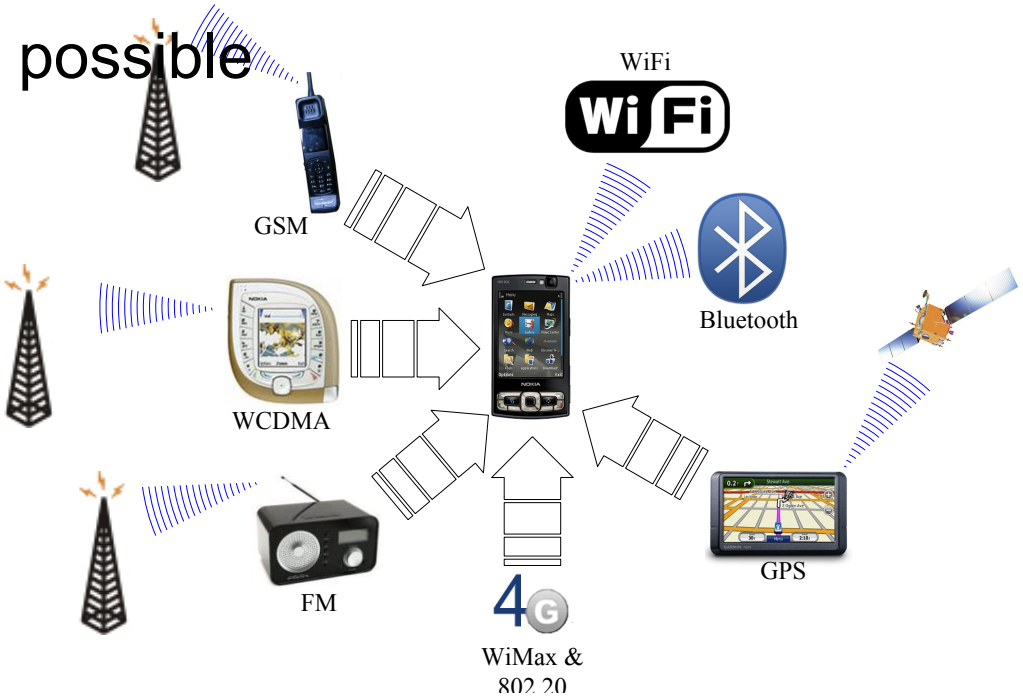
# Multi-standard Wireless Systems

– Multiple services

– Reuse circuits as much as possible
- Power
- Area
- Competitiveness

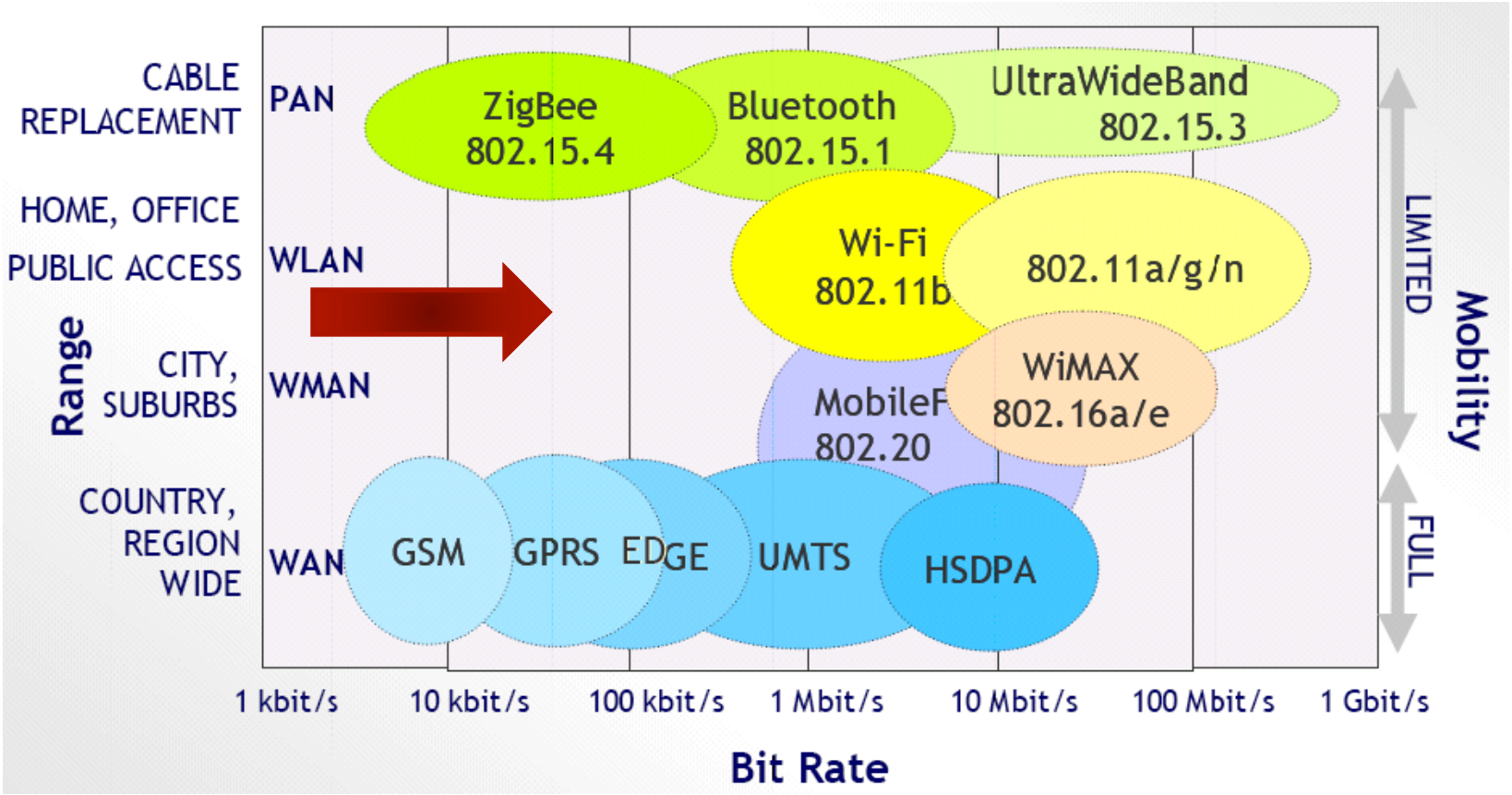
– Smaller Cell phone, stronger function, longer battery duration

– Use of digital (analog unfriendly) nanometric tecnologies



# Multi-standard Wireless Systems

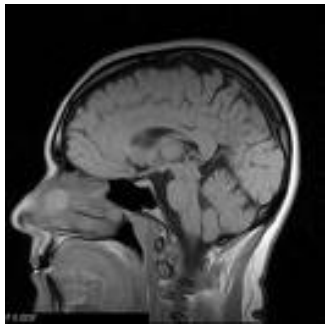
- Exponential growth in mobile computing and broadband wireless
- Major need for high dynamic range, wide-bandwidth, low power ADCs.



# Potential Applications

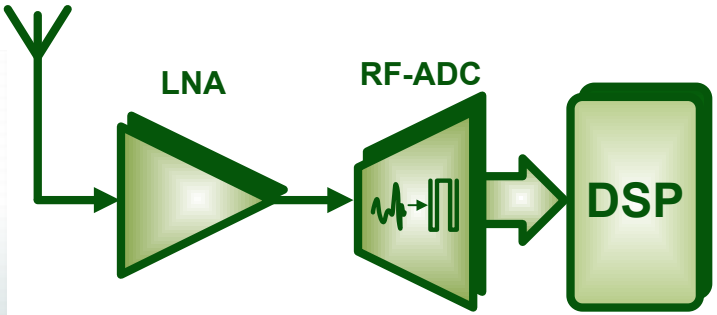
Magnetic Resonance Imaging

Future Multi-standard Radios



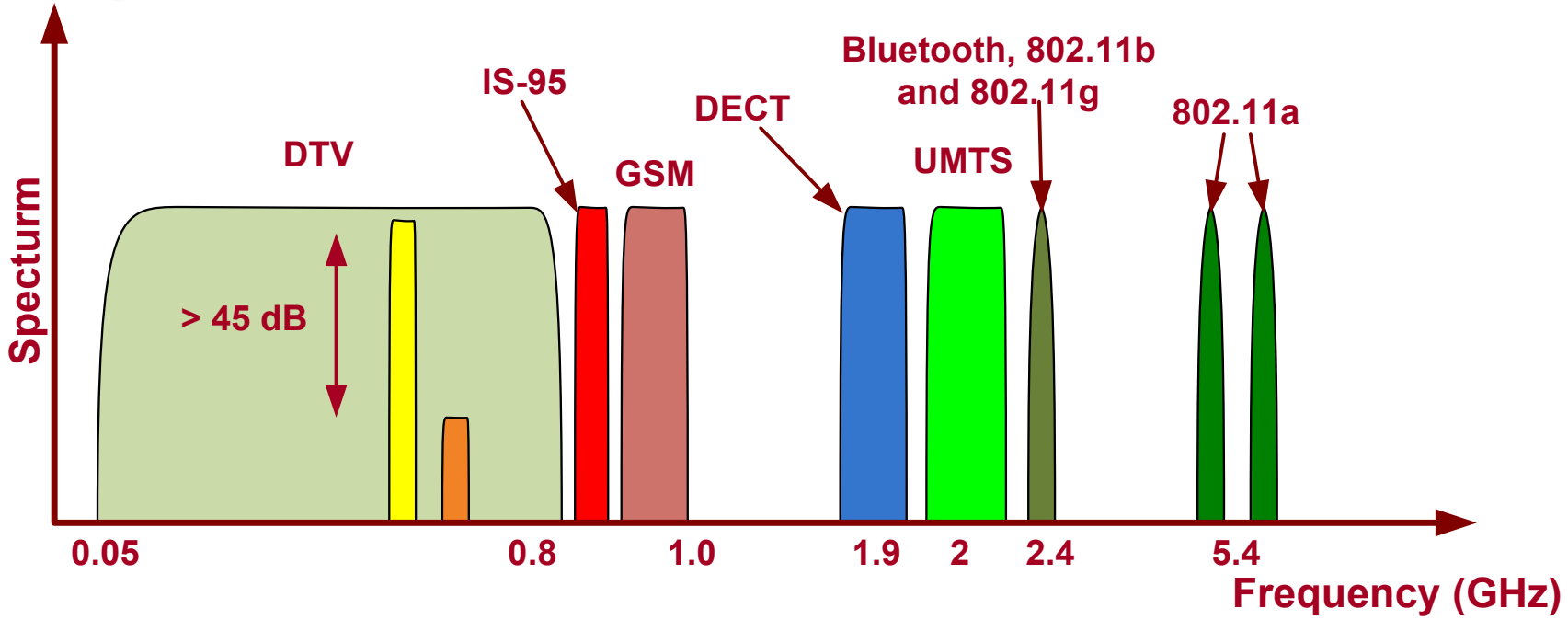
Cognitive radios

Software Defined Radios



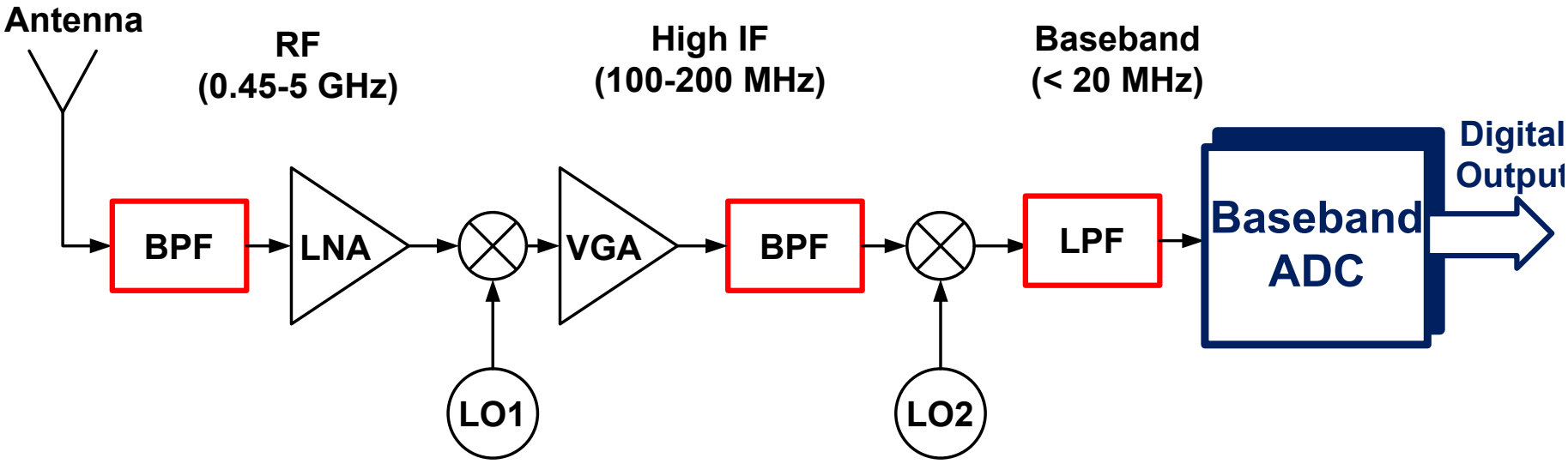

Future mmWR standards

# Design Issues: BW requirements for higher connectivity



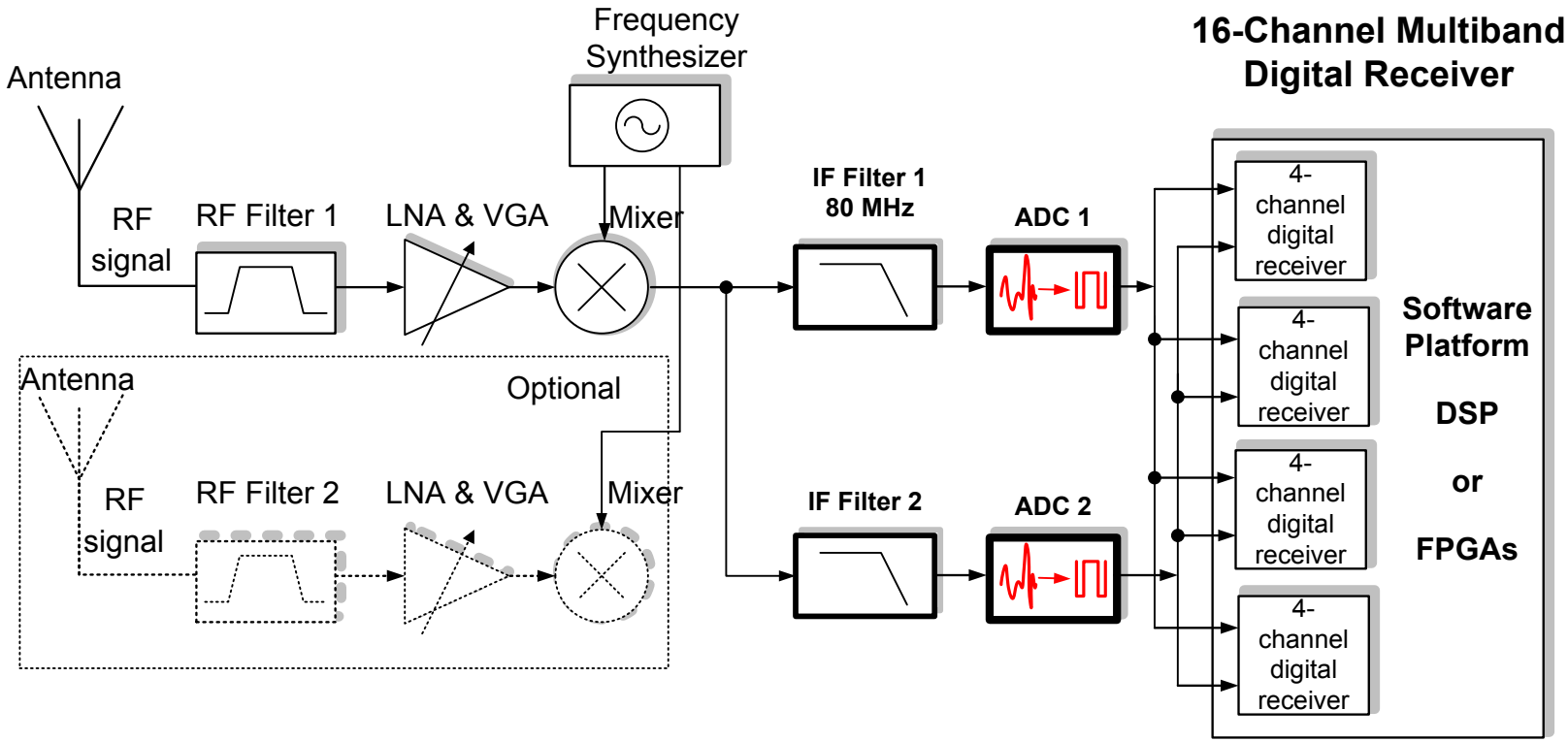

- Higher flexibility on operational frequency and bandwidth, higher blocker rejection, higher dynamic range
- Receiver Architectures:
- Super-heterodyne, Low-IF, Direct Conversion, High-IF, Digital Radio

# Super-heterodyne Receiver



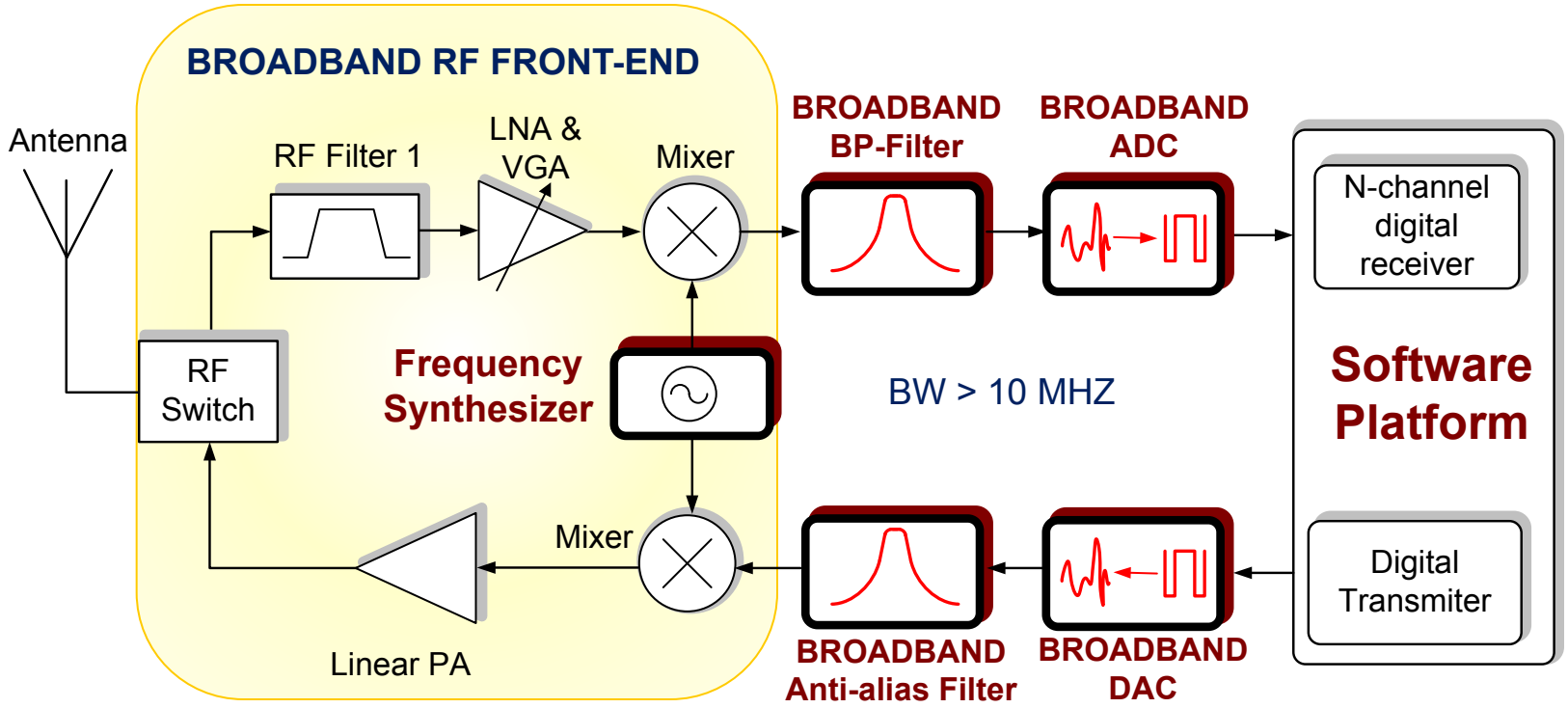

- Invented by Armstrong in 1918
- Hardware specific radio architecture
- Extensive filtering to relax ADC specs
- Suitable for narrow-band applications

# Efficient radio transceiver: Direct Conversion




- Mixer prevents its use in ultra-Wideband Receivers (Alias issue)
- RF filters are required; (1 receiver per service)
- Bank of receiver front-ends; ADCs can be shared

# IF Radio Receiver: A step towards the Digital Radio




- Minimize the hardware: BW in the range of 10-20 MHz to accommodate Video Standards
- Best IF frequency? Above 1 GHz (LC circuits) or ~ 200 MHz (Active solution)

# Non-Conventional Approaches to Receivers

- **Sample rate, downsampling and filtering**

R. Crochiere and L. Rabiner, *Multirate Digital Signal Processing*. Englewood Cliffs, NJ: Prentice Hall, 1983.

- **Sampling with built-in anti-aliasing**

Y. S. Poberezhskiy et.al. "Sampling and signal reconstruction circuits performing internal antialiasing filtering and their influence on the design of digital receivers and transmitters," *TCASI*, Jan. 2004.

- **A discrete-time RF sampling receiver**

R. B. Staszewski, et. al. "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, Dec. 2004.

- **SDR receiver**

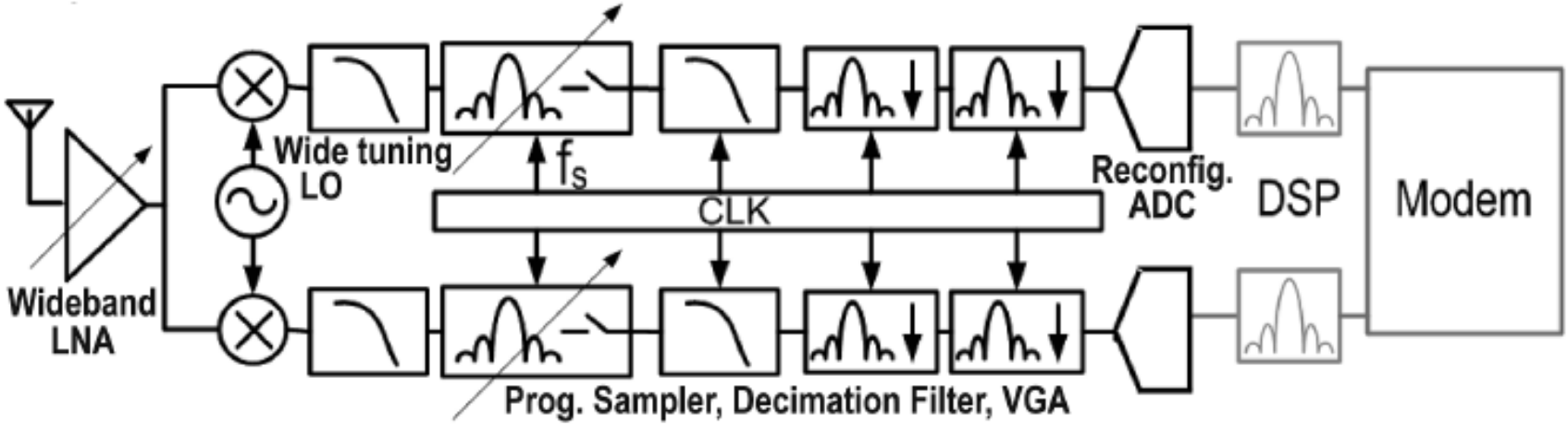
Abidi, "The path to software-defined radio receiver", IEEE JSSC, May 2007

- **Frequency-domain-sampling receivers**

S. Hoyos and B. M. Sadler, "Ultra-wideband analog to digital conversion via signal expansion," *IEEE Transactions on Vehicular Technology*, Sept. 2006.

**Other Architectures are presented in this workshop**

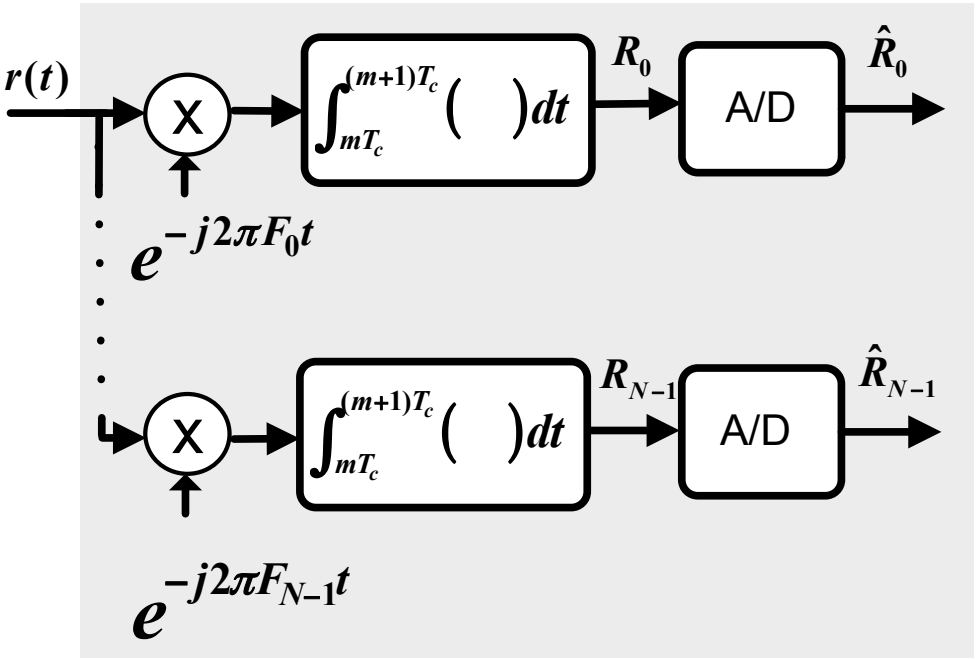
# Sinc(f) Filtering for SDR receivers

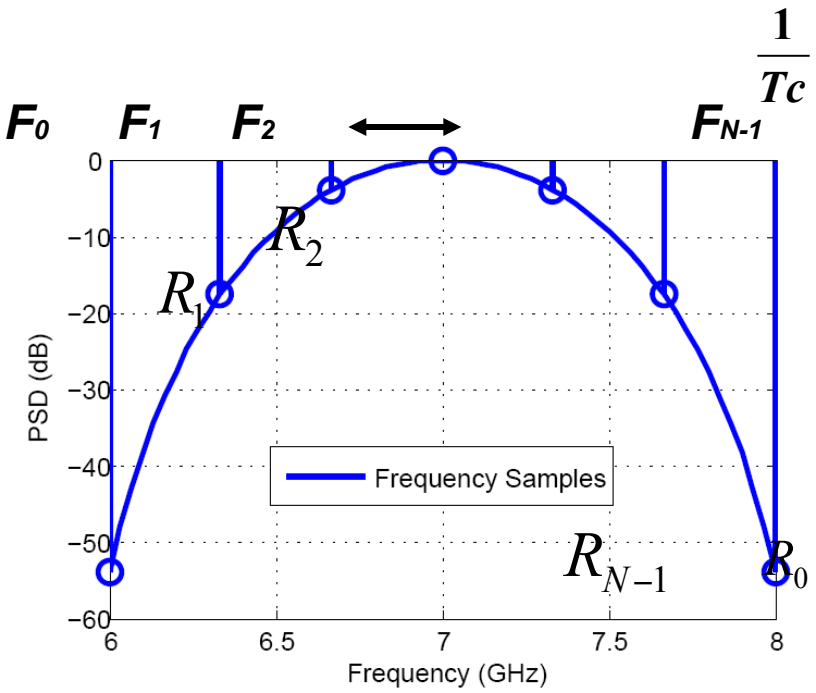



- Direct conversion with tunable LO in the freq. range 800 MHz to 6 GHz.
- Cascade of $sinc^N$ filters followed by decimation to achieve the initializing needed.
- Good for narrowband signals as a single ADC can handle the bandwidth. But SDR should also be good for wideband and ultra-wideband signals. Need parallel ADC to sample at a fraction of Nyquist rate. Parallelization of the front-end will be needed if want to keep the ADC sampling rate down.

A. Abidi, “The path to software-defined radio receiver”, IEEE JSSC, May 2007

# Frequency-Domain ADC Based on Fourier Coefficients



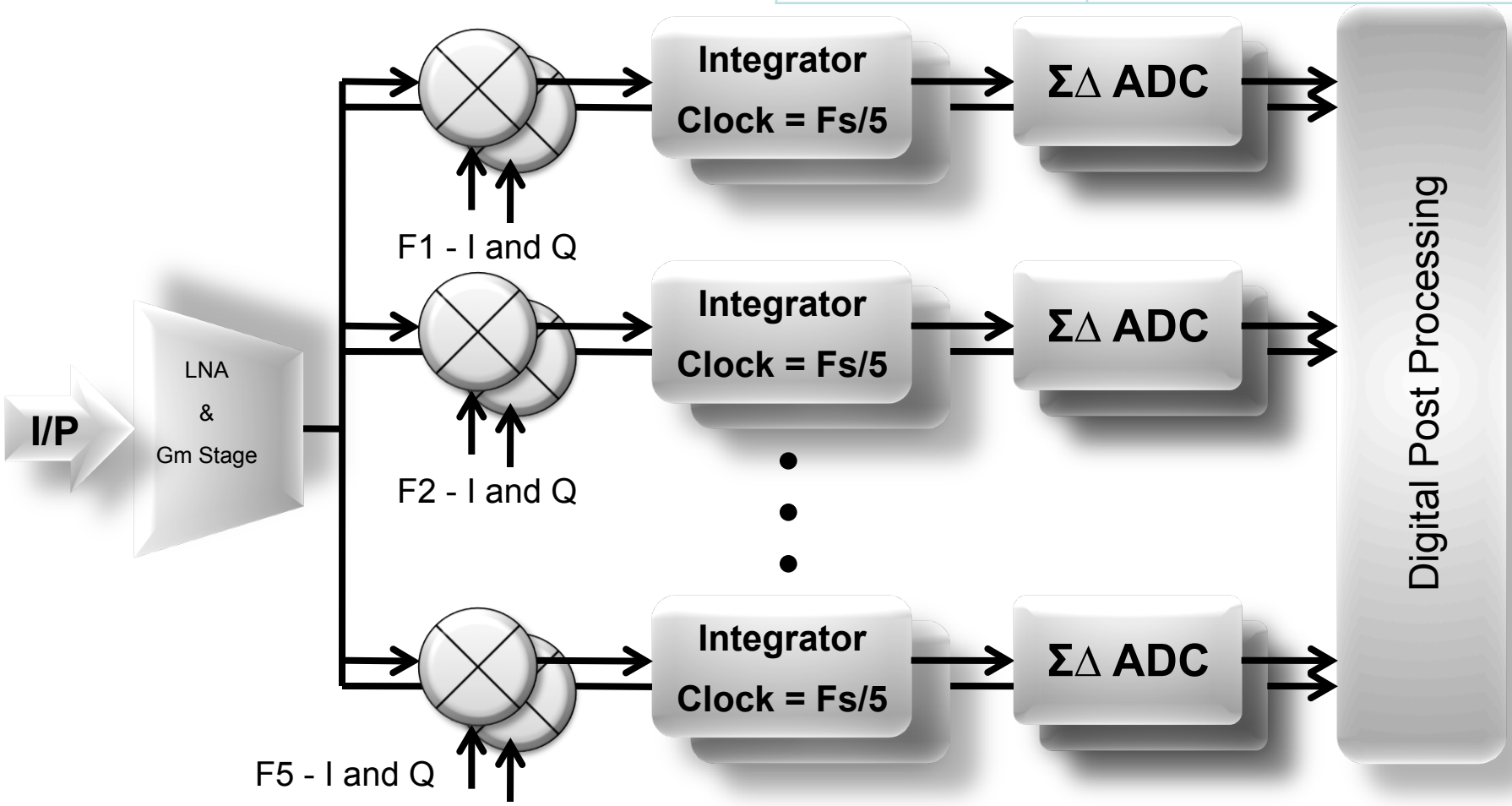

- Mixers and integrators.
- Lower frequency sample and hold requirements.
- ADC speed is dictated by the time frames

- No signal reconstruction. Parallel digital processing.
- Optimal bit allocation minimizes quantization error. Some samples may not be quantized at all.

S. Hoyos and B. M. Sadler, "Ultra-wideband analog to digital conversion via signal expansion," *IEEE Transactions on Vehicular Technology*, Sept. 2006.

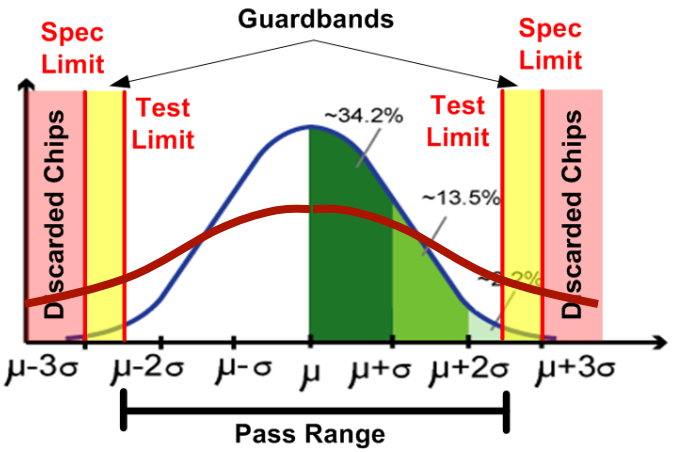
# Multi-Standard Receiver Front-end

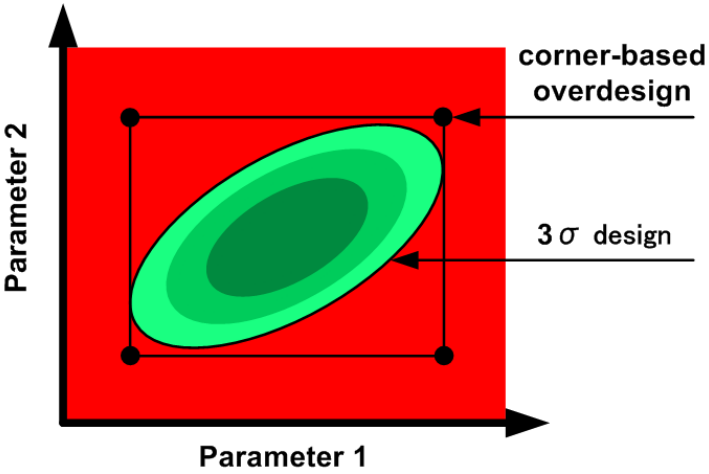
| STANDARD | SPECIFICATIONS |
|---|---|
| UWB | 500 M S/s and 5 bits |
| 802.11 G | 50 M S/s and 8 bits |
| Bluetooth | 1 MHz and 12 bits |
| GSM | 200 KHz and 14 bits |



# The single-chip Transceiver Paradigm

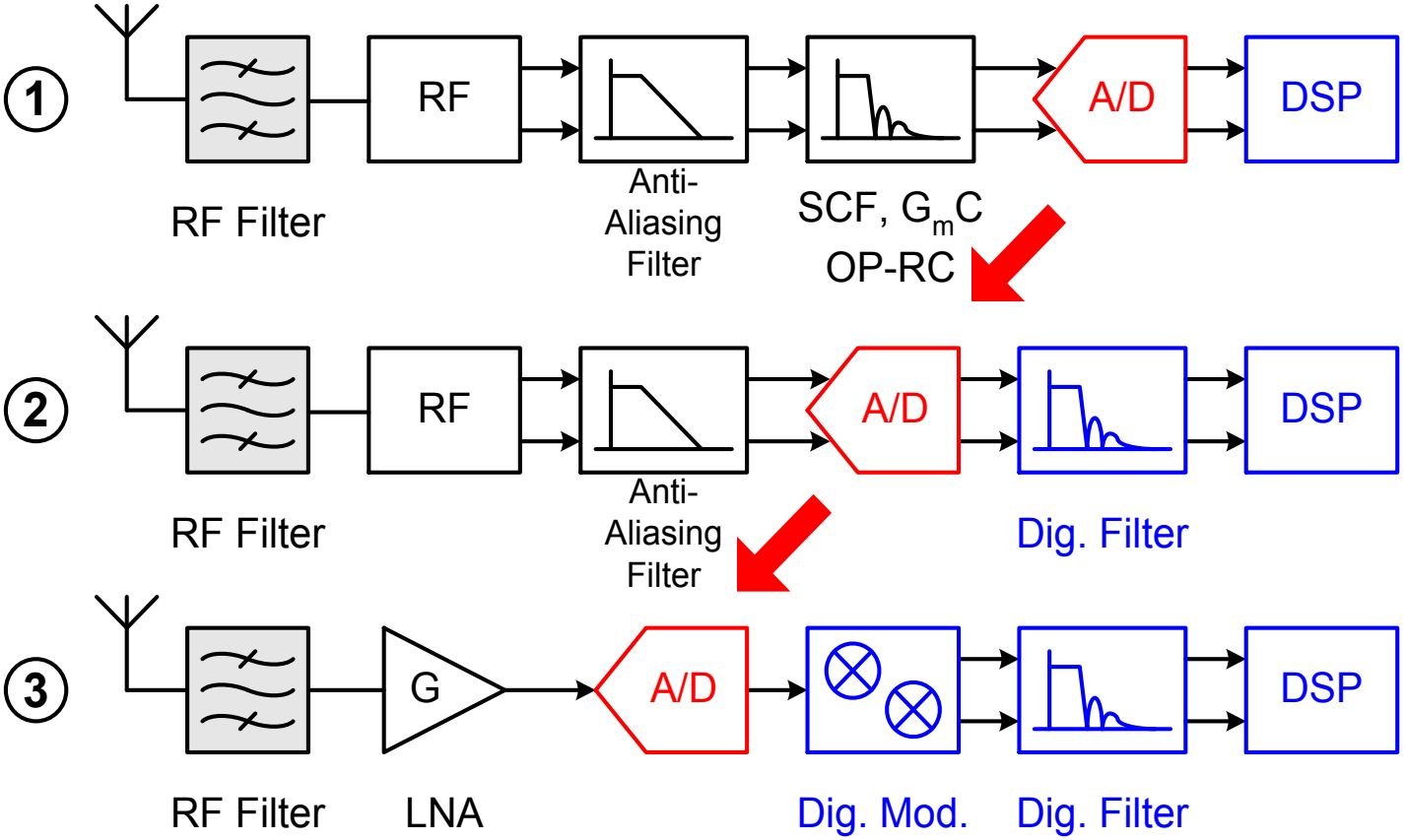
- **Modern technologies:**
  **"Digital intensive" System-on-Chip (SOC) environment**
  - **Scaling of transistor dimensions in digital CMOS technologies**
  - **Increased intra-die variability from device scaling**
  - **Defect densities increase in newer technologies**
  - **Yields decrease as SOC chip sizes increase**
  - **Yield impact on analog specifications leads to process corner-based overdesign to allow for analog parameter variations**
  - **Increased test cost**

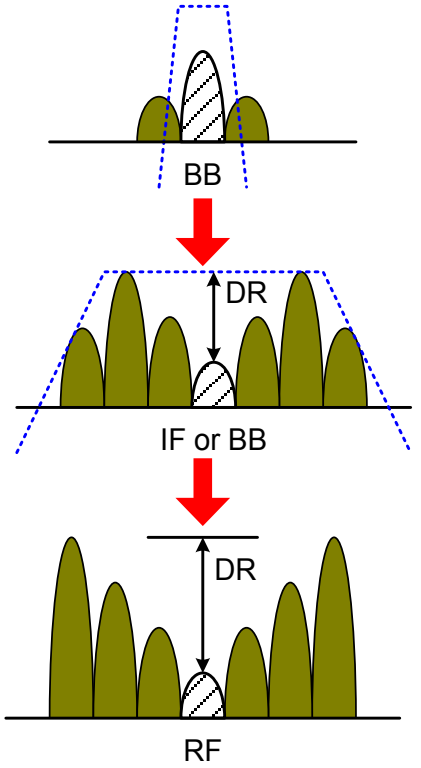



**Critical Analog components must be minimized**

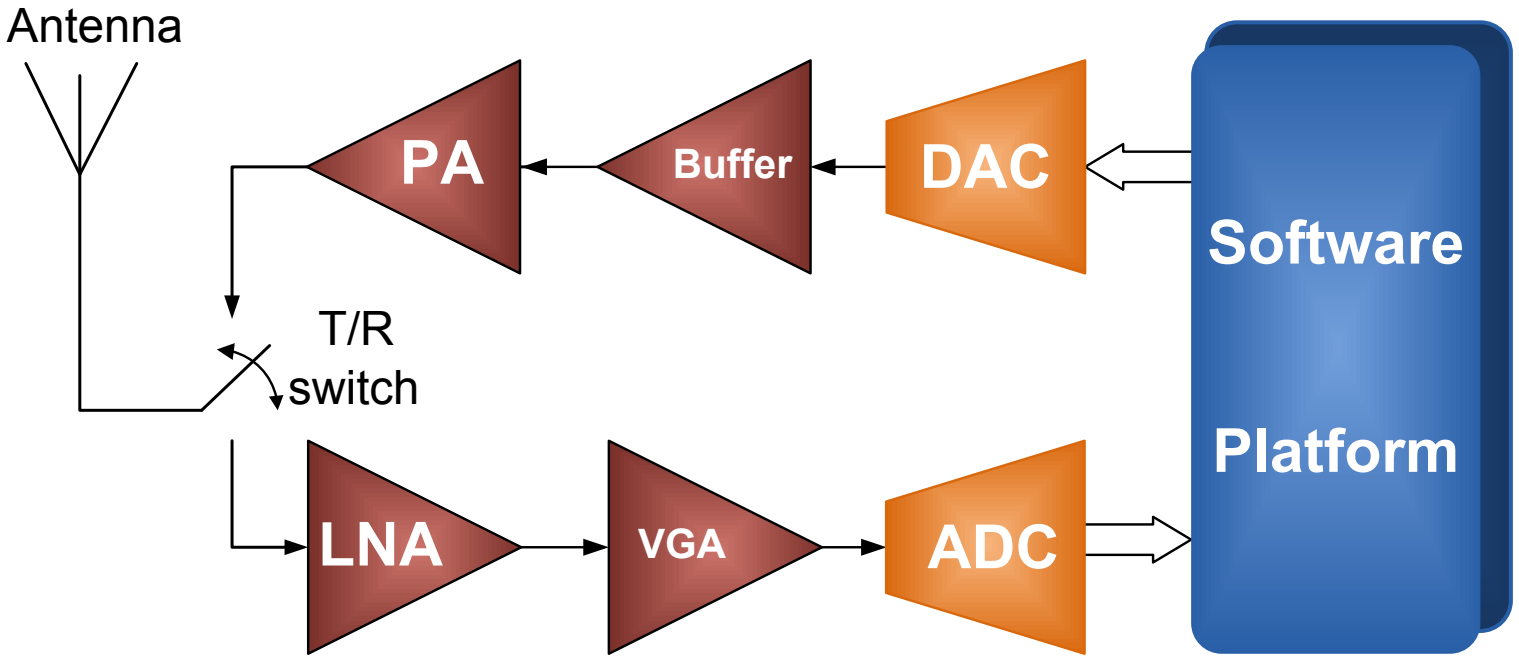
# Roadmap for high-resolution Receivers: Paradigm



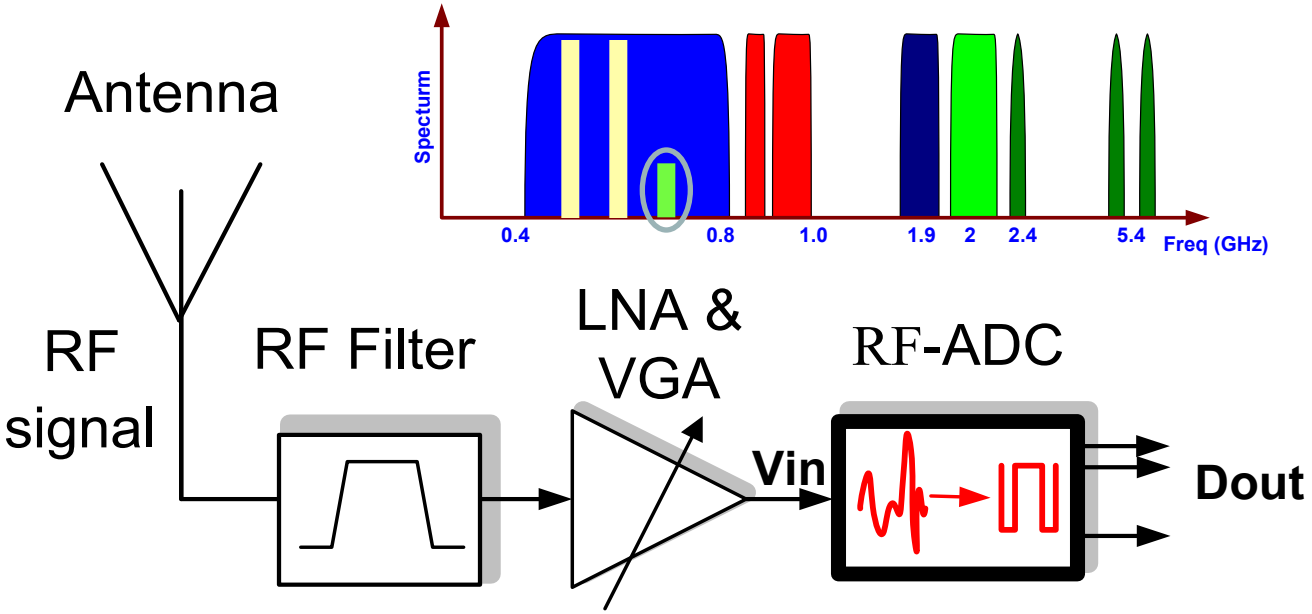

- How much RF processing should be done before the ADC?
- The front-end must be scalable and configurable to fit multiple standards.
- Better performance at higher frequency.

# Software radio transceiver: Ultimate goal



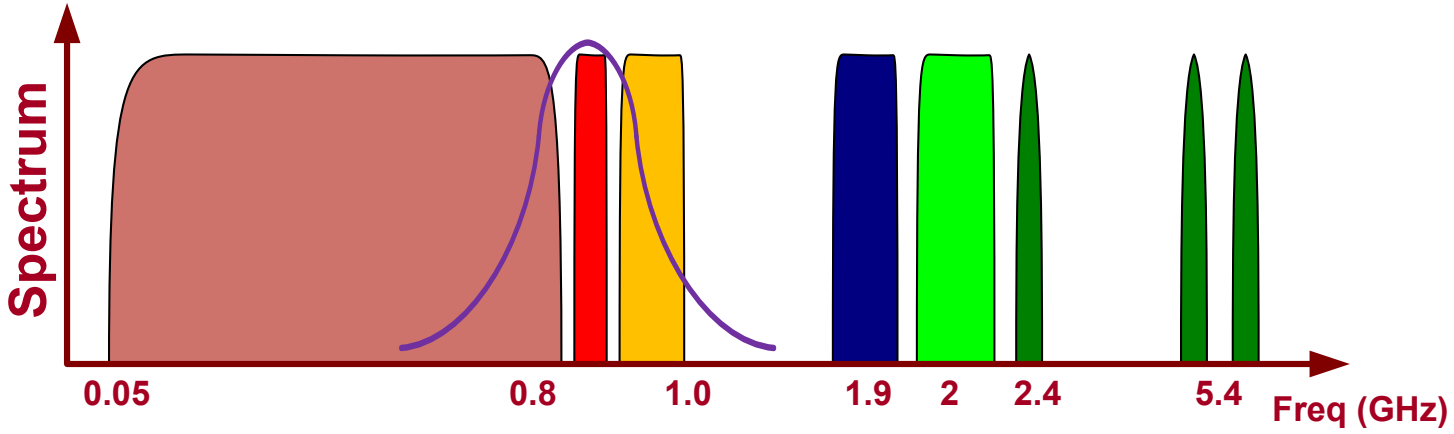

- Concept introduced by Mitola in 1991
- Modulation/demodulation functions in software
- Flexible multi-standard software architecture

# RF-to-Digital Conversion: Co-existence



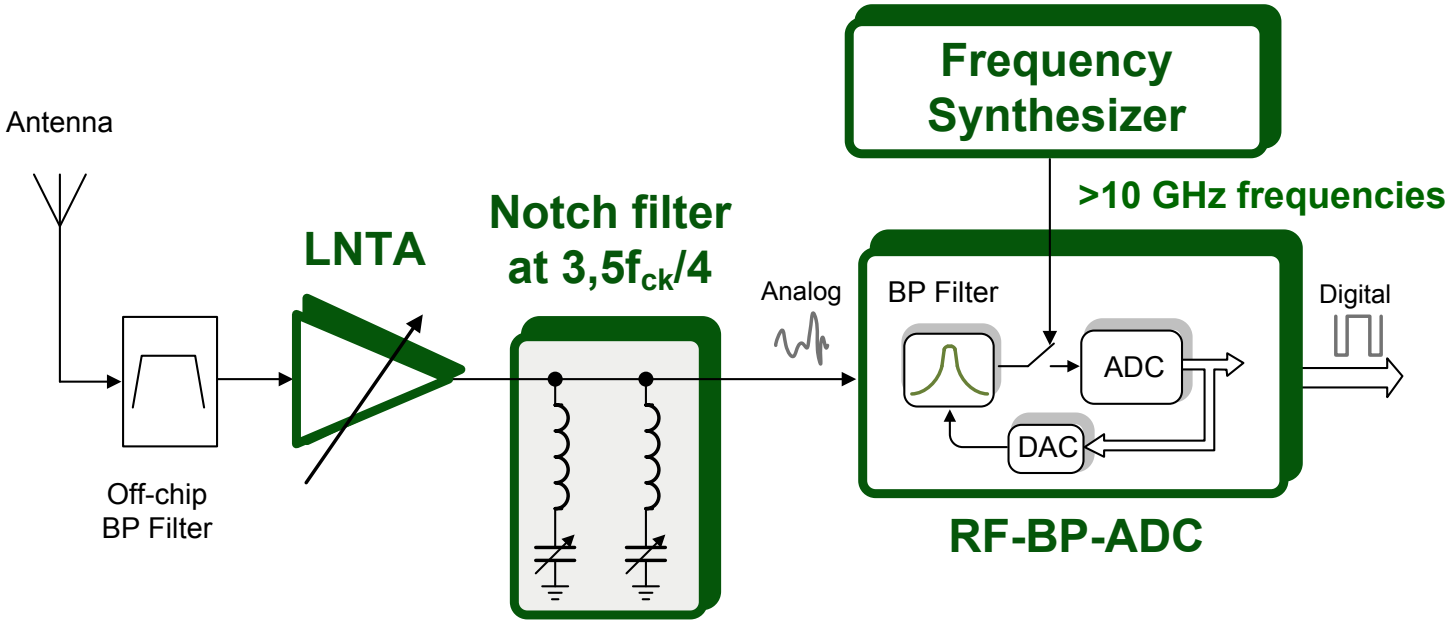

- Is it practical to design a multi-standard solution based on this architecture?
- Dynamic range required?
  - DTV ➔ SNRsignal=40 dB; Blockers > 40 dB; Peak-to-RMS > 12 dB: **ADC resolution over 90 dB !!!**
- Even if possible, Power consumption required?
- Can we use programmable bandpass filters? (back to the past)

# RF-to-Digital: Fundamental Issues




- Lowpass ADC are further affected by flicker noise, more prominent in deep submicron technologies
- Power is excessive for all blocks, and linearity is a killing factor.
- Too much effort processing several standards at the same time!
- Most of the services are "narrow-band"; BW< 20 MHz
- Does it make sense to use Bandpass ADCs?
- Programmability could be added to make this approach more attractive
- **Design issues?**

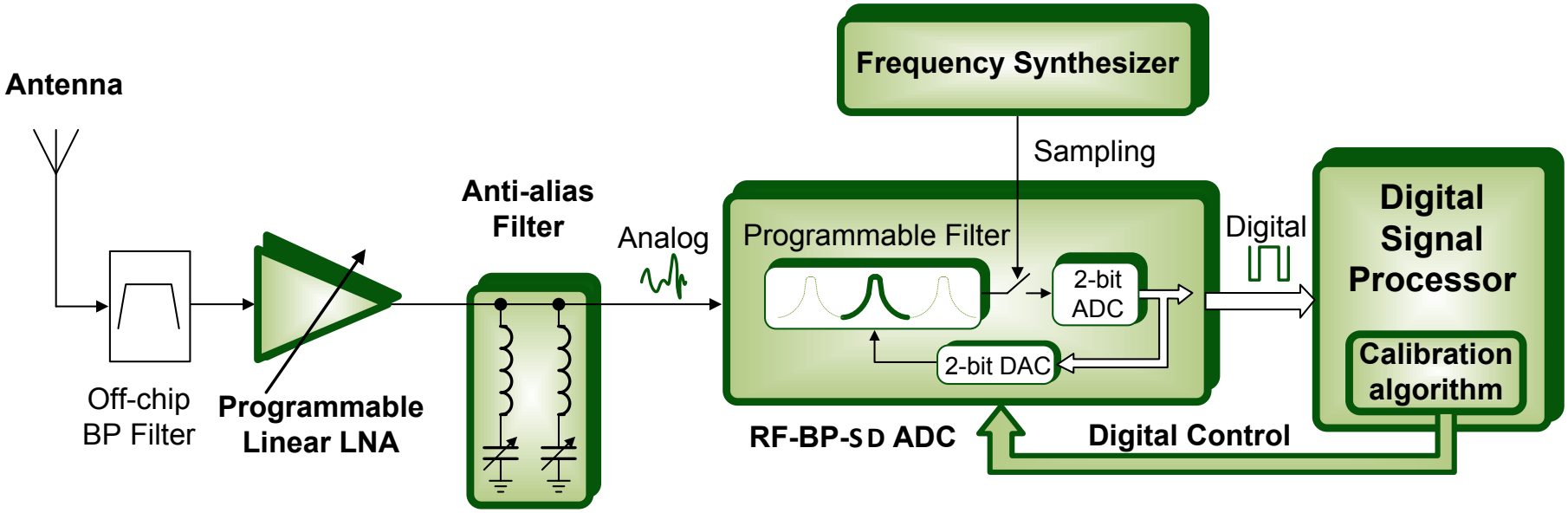
# Mixer-less RF-to-Digital Bandpass Converter




## For fck/4 Architectures:

- Linear Low-Noise Transconductance Amplifier
- Critical blockers at 3fck/4 and 5fck/4 have to be attenuated
- First ADC stage is an LC-BP Resonator, tolerant to large signals
- Active devices can be allocated after the first resonator
- PVT variations, Clock Jitter, and Excess Loop Delays are critical

# Design Issues: Mixer-less RF-to-Digital Converter




## Architecture:

- Oversampled Bandpass ADC
- Linear Low-Noise Amplifier
- LC programmable filtering to attenuate critical blockers
- Programmable continuous-time filtering in front of the quantizer
- Fast digital processor used for calibration and signal processing
- Flexible frequency synthesizer

# Continuous-Time BP-ΣΔ ADC: Tradeoffs

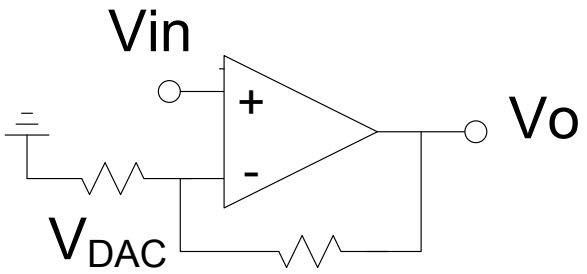
$$SNR\,(dB) = 10 * \log_{10}\left[\frac{3}{2}\frac{(N+1) * OSR^{N+1}}{\pi^{N}}\right] + 6.02 * (B-1)$$

$N \rightarrow order\ of\ \ filter, OSR \rightarrow oversampling\ ratio$

$B \rightarrow number\ of\ \ bits\ in\ comparator$

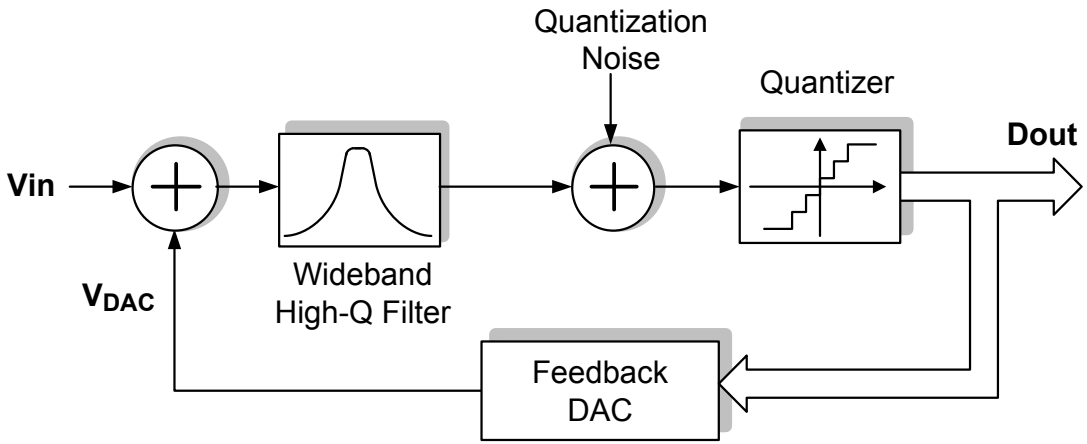
- **SNR increases with higher N**
  - **Loop stability becomes a problem (for practical implementations N≤6)**
- **SNR increases with higher OSR**
  - **Highest sampling frequency is determined by the $f_t$ of the technology, clock jitter, speed of the comparator and DACs**
- **SNR increases with multi-bit quantizer and DACs.**
  - **Design complexity of Multi-bit Quantizer and multi-bit DAC.**
  - **B in the range 1-4; hard to handle at RF**

# Design Issues: Closed-Loop Feedback




$$\text{Error} = v_{in} - v_{DAC} \cong \frac{v_{in}}{\text{Loop gain}}$$

$$v_{DAC} \cong \left( \frac{R_{in}}{R_{in} + R_f} \right) v_0$$



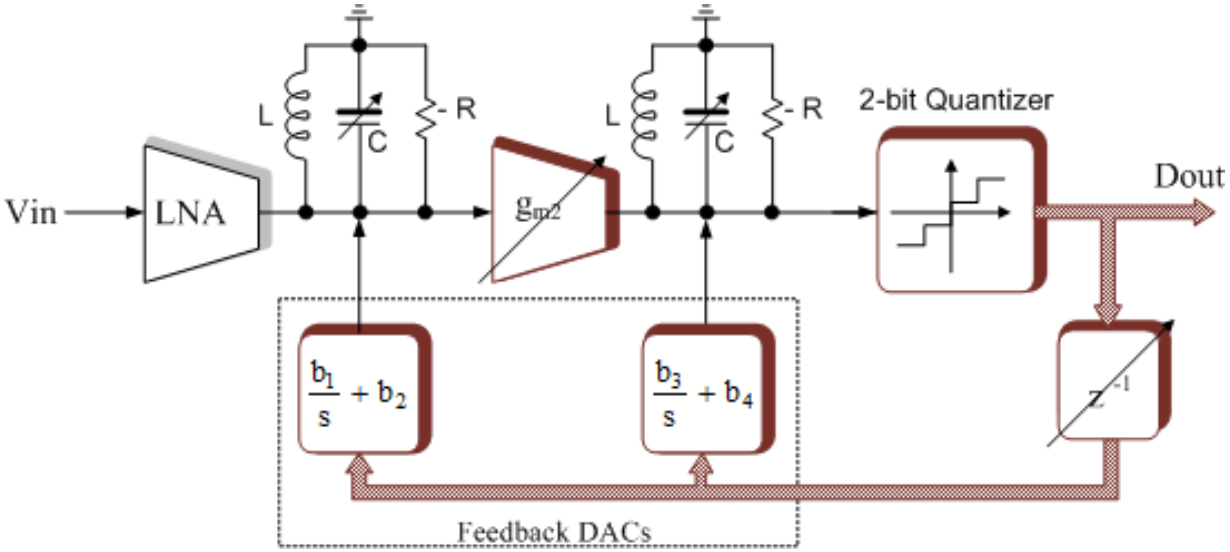

**Quantization noise is generated at the quantizer :**

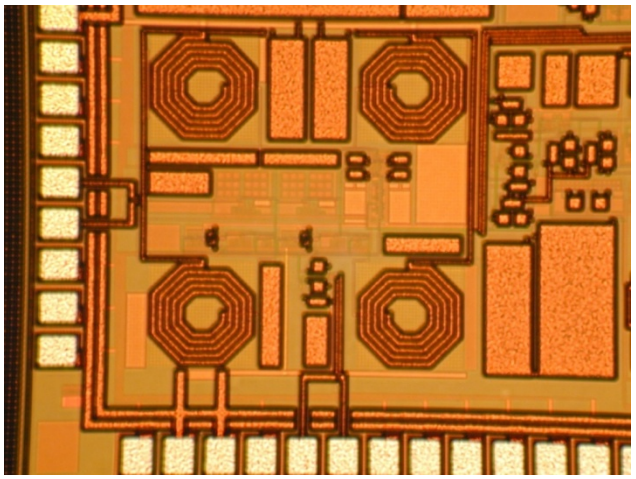
- **Multi-bit quantizer reduces the quantization error and jitter effects**

**For large in-band loop gain, DAC linearity determines system linearity:**

- **Feedback forces Vin=$V_{DAC}$**
- **Dout ≅ $V_{DAC}$/DAC Conversion Gain**
- **DAC non-linearity is directly reflected in Dout non-linearity**

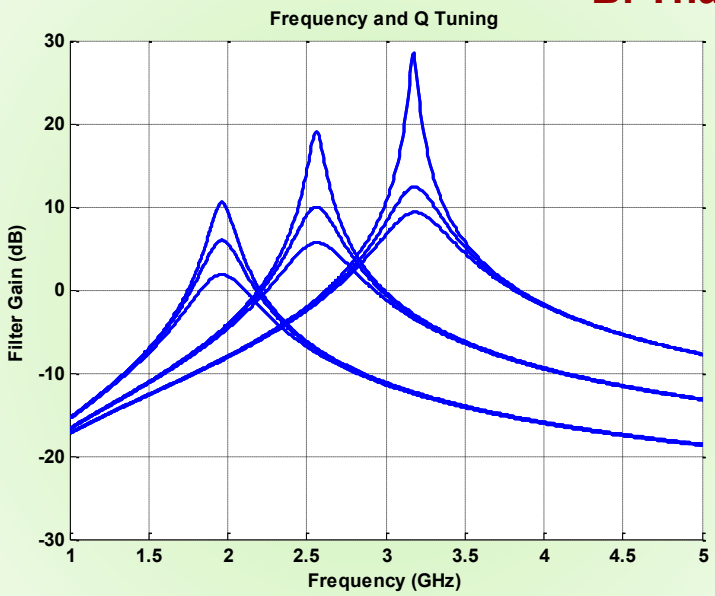
# 4th Order BP ΣΔ covering 2-4 GHz

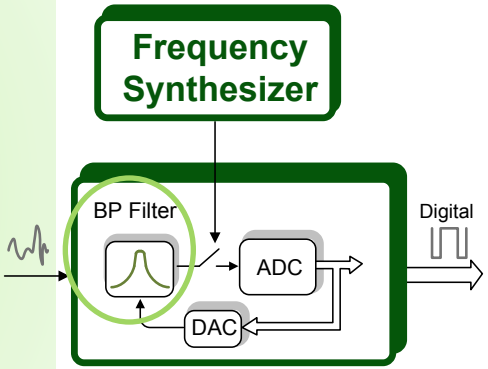


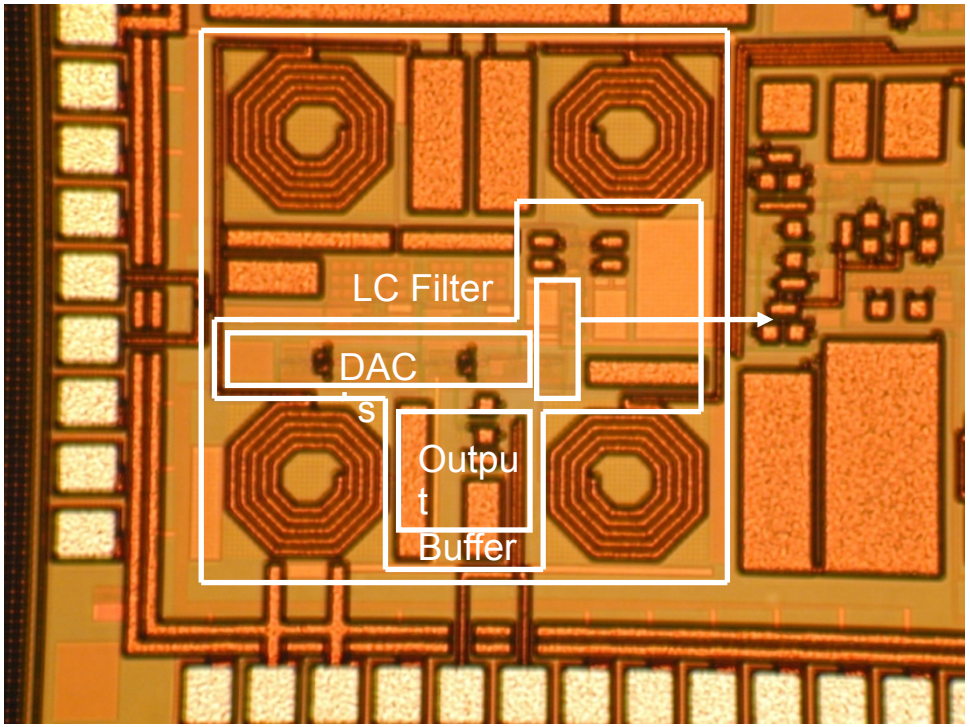
B. Thandri, *Feb 2007, JSSC.*

- Directly coupled to the LNA
- Adjustable loop delay
- Programmable Center Frequency
- Adjustable Negative resistor
- 2-bit RF quantizer



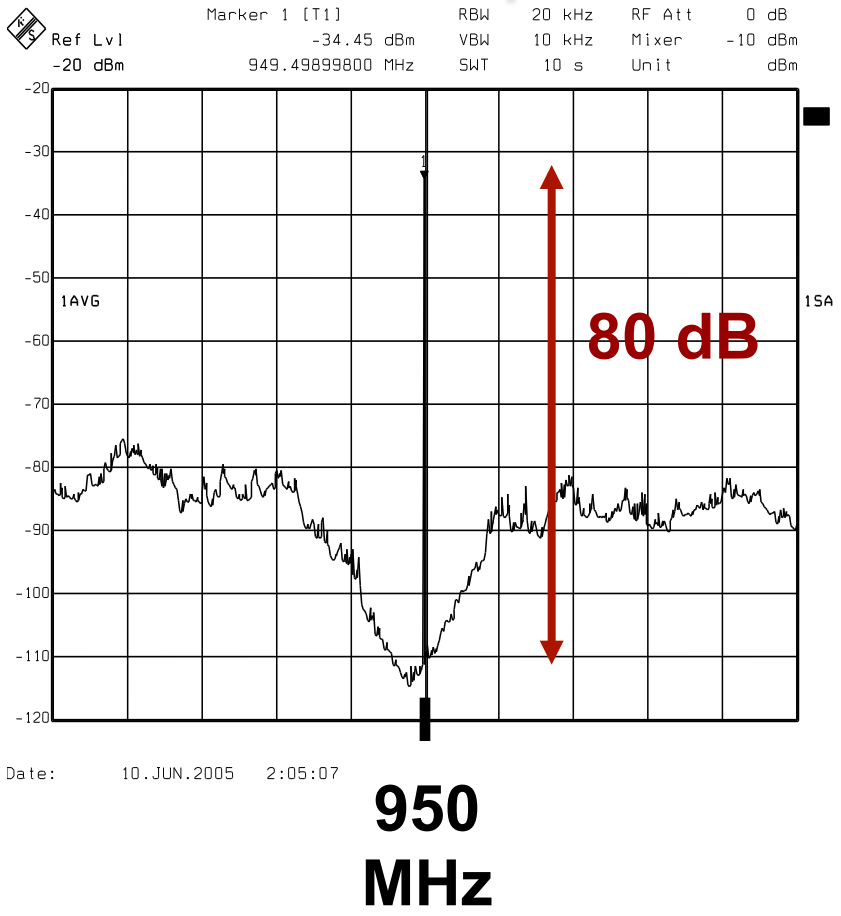



# Over 10-bit 950 MHz Bandpass ADC




Area = 1.08 mm$^2$ IBM 0.25 µm SiGe BiCMOS

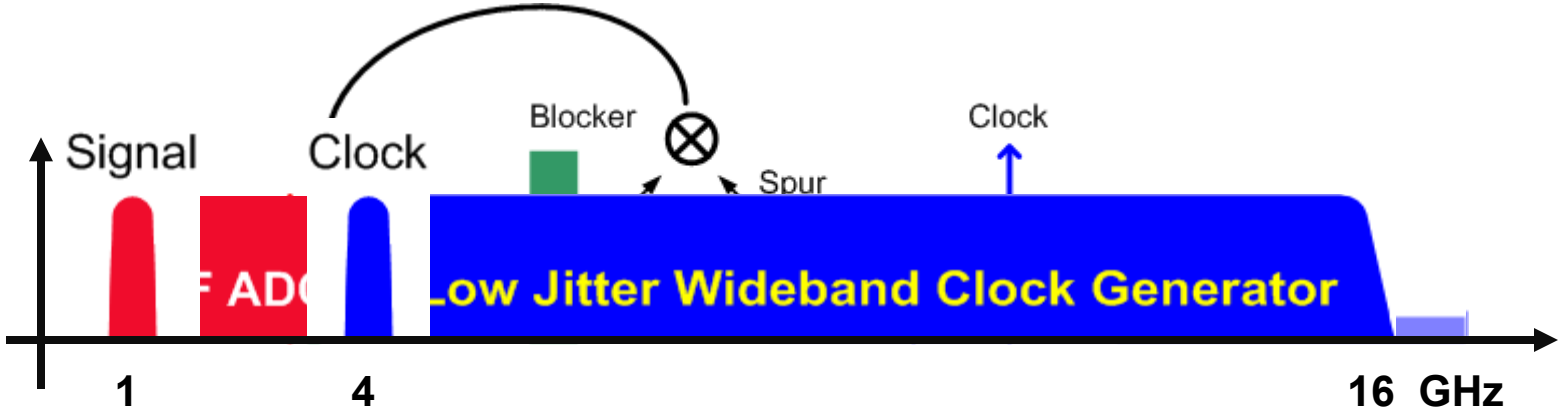
## Measured spectrum




**950 MHz**

**Bharath Kumar Thandri and Jose Silva-Martinez, "A 63 dB SNR, 75 mW bandpass RF ΣΔ ADC at 950 MHz using 3.8 GHz clock in 0.25 µm SiGe BiCMOS technology," *February 2007, IEEE Journal of Solid-State Circuits*.**

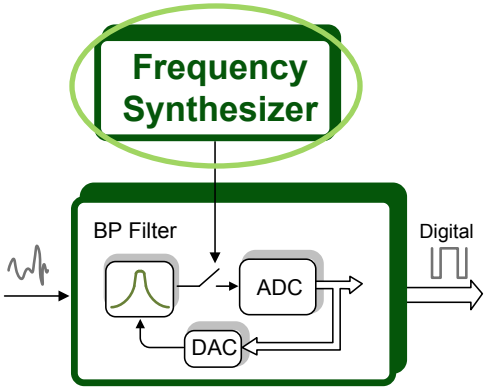
# BP ΣΔ covering 2-6 GHz: Clock Issues



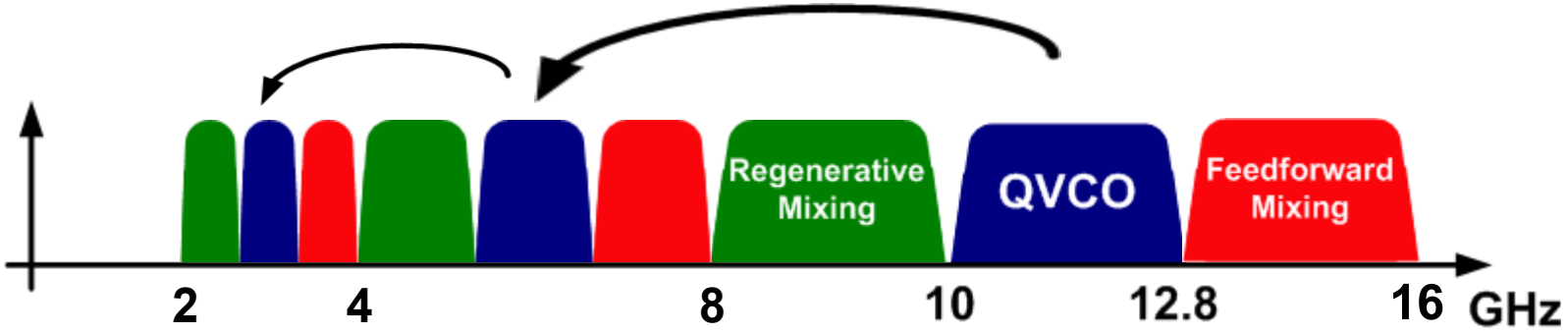

**Design Issues:**

- 4-time ratio of the sampling clock to carrier frequency
- 4 ~ 16 GHz ultra-wide continuous frequency tuning
- Low phase noise and spurious tones:

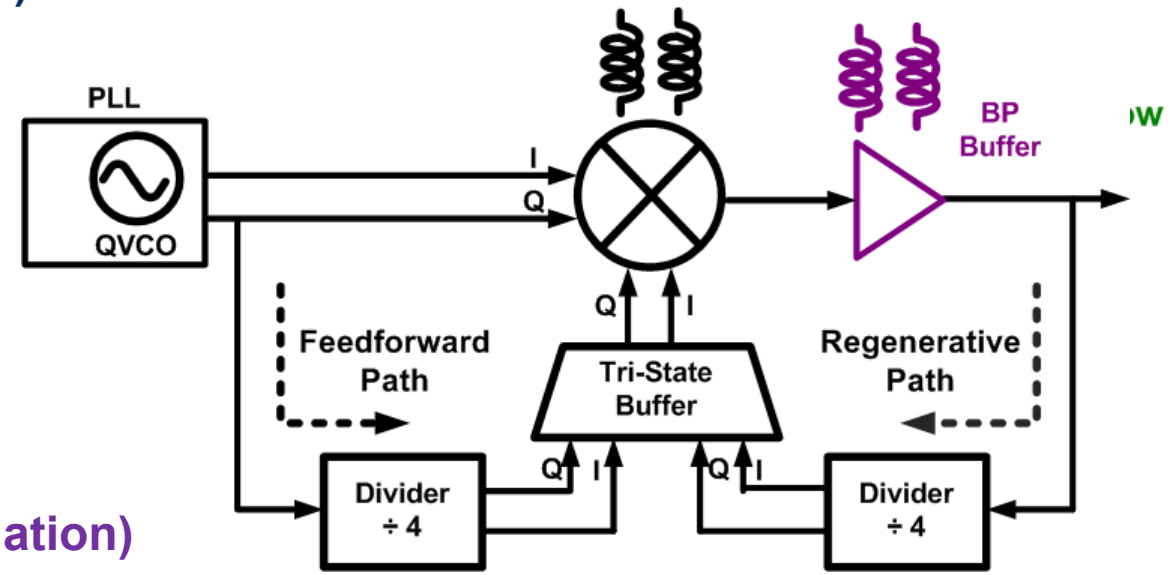
  The **phase noise** and **spurious tones** convolve with **quantization noise** and **blockers**. The convolved signal inside the signal bandwidth degrades SNR.



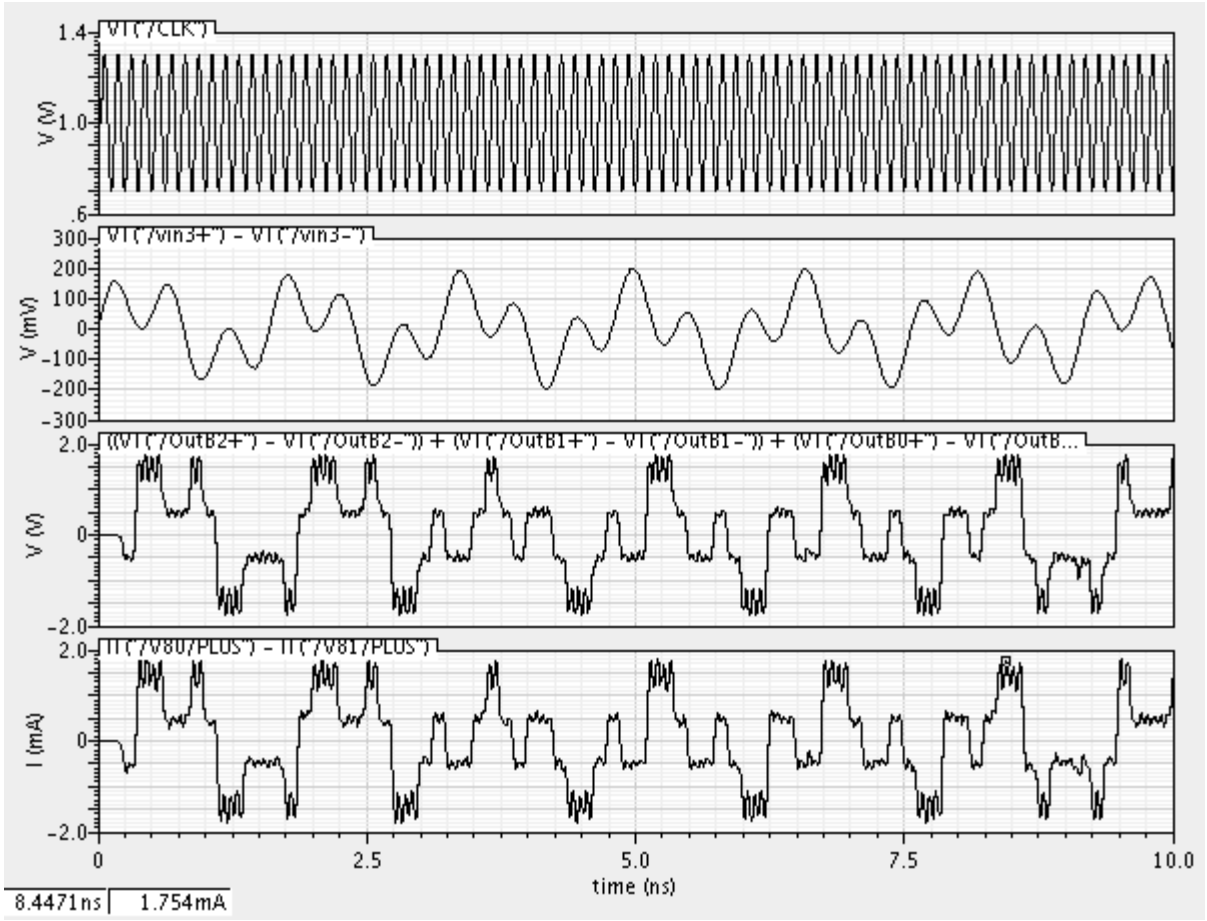
# Low-Jitter Wideband Clock Generation




- QVCO-Based PLL (25%)
- Feedforward mixing (1.25X)
- Regenerative mixing (0.8X)
- Tri-state Buffer (Band Selecting)
- BP Buffer (Noise and Spur attenuation)
- Divide and conquer



# Quantizer-DAC Test: 8GHz Clock




**Clock Signal**

**Multi-tone Input Signal**

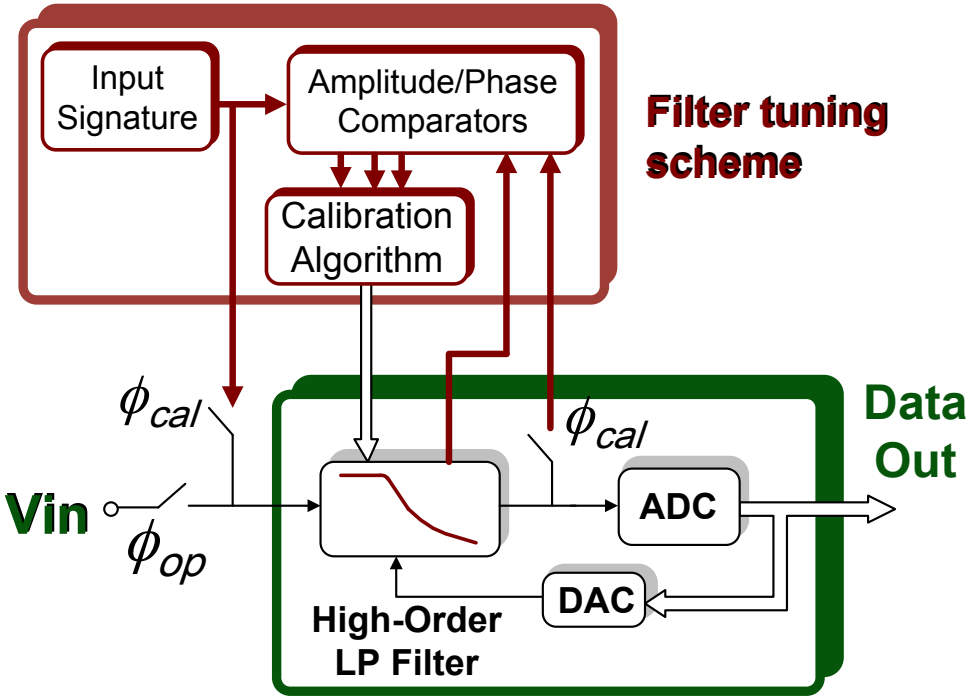
**Quantizer Output**

**DAC Output**

**Dynamic test for a two-bit quantizer-DAC**

**DAC gain present significant variations**

# Calibration: Conventional Master-Slave Technique

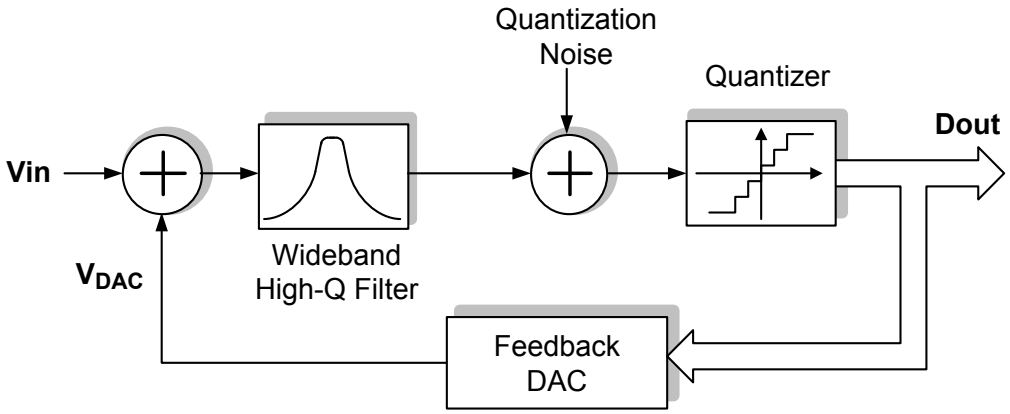



- Input and output signal power are compared to measure power gain
- Phase can also be compared
- Errors in the tuning scheme limit accuracy
- Analog based calibration scheme

- Re-configurable off-line technique
- Input signatures must be generated
- Multi-tone input signals increase fault coverage
- Analog Switches may limit system linearity
- Does not ensure stability (loop gain is not fully tuned)
- Excess loop delay due to quantizer and DAC?
- Hard to use in RF applications

# Calibration: Critical non-idealities

- Excess loop delay
- Quantizer metastability
- Variations in loop Gain
- Adjust for optimal Loop Filter Parameters
  - (PVT variations ~ 20%)

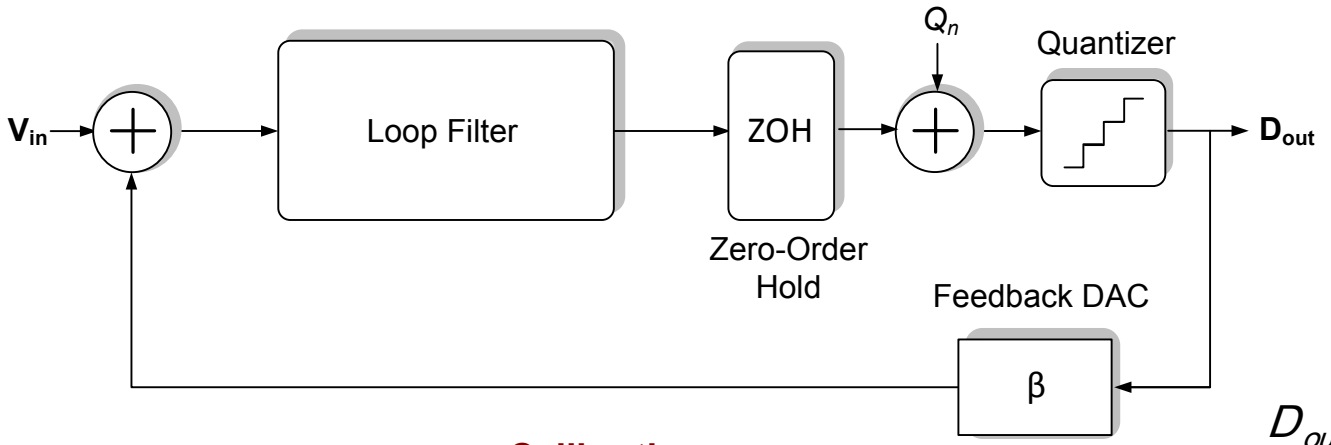



- **The goal is the tuning of the entire loop gain for the best possible Noise Transfer Function:**

**Global NTF Tuning Strategy**

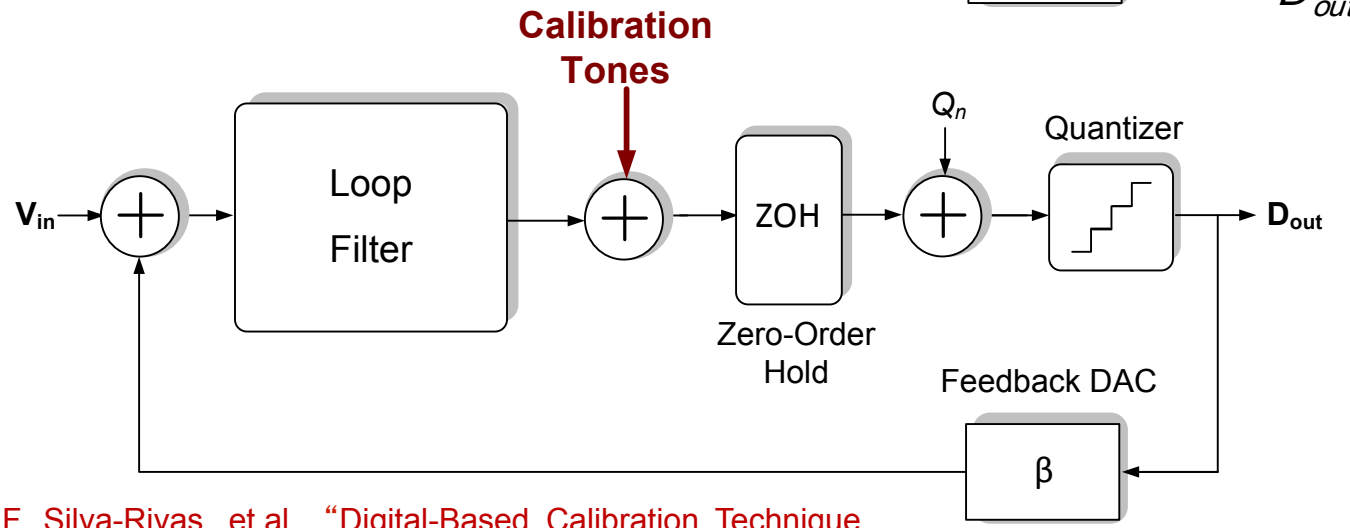
**How the NTF can be measured?**

# Calibrating the Noise Transfer Function (NTF)




- NTF is the most critical function.
- Hard to predict its variations

$$D_{out} = (STF)Vin + (NTF)Qn$$



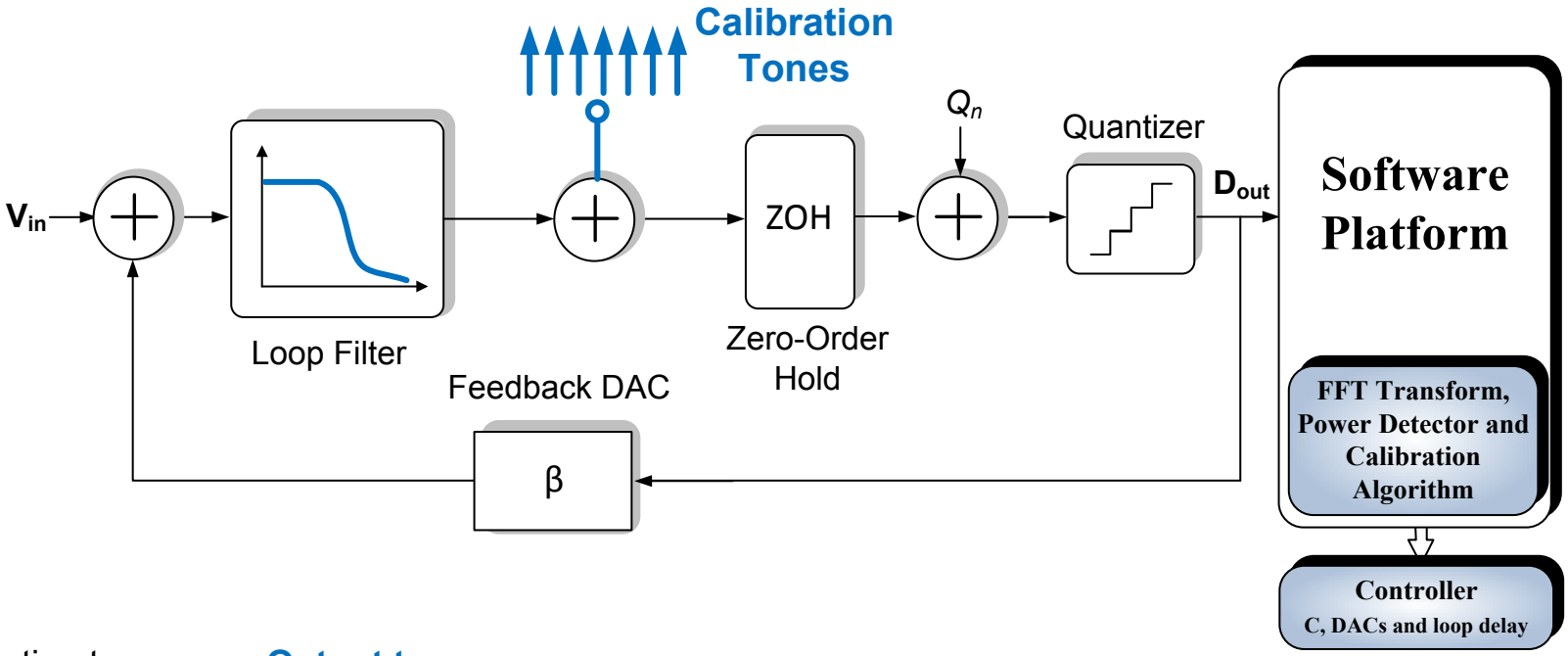

- Lets accurately measure NTF, and then correct it

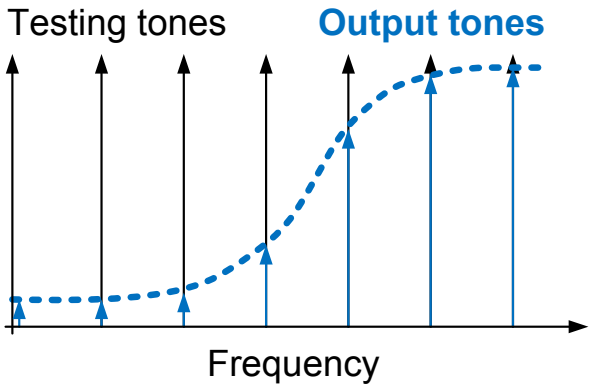
$$D_{out} = (STF)Vin + (NTF)Qn + \left(\frac{NTF}{ZOH}\right)CAL_{tones}$$

F. Silva-Rivas, et.al., "Digital-Based Calibration Technique for Continuous-Time Bandpass Sigma-Delta Analog-to-Digital Converters," Analog Integrated Circuits and Signal Processing, Oct. 2008.

J. Silva-Martinez, Plenary lecture, XXII Conference on Design of Circuits and Integrated Systems, Nov 2007

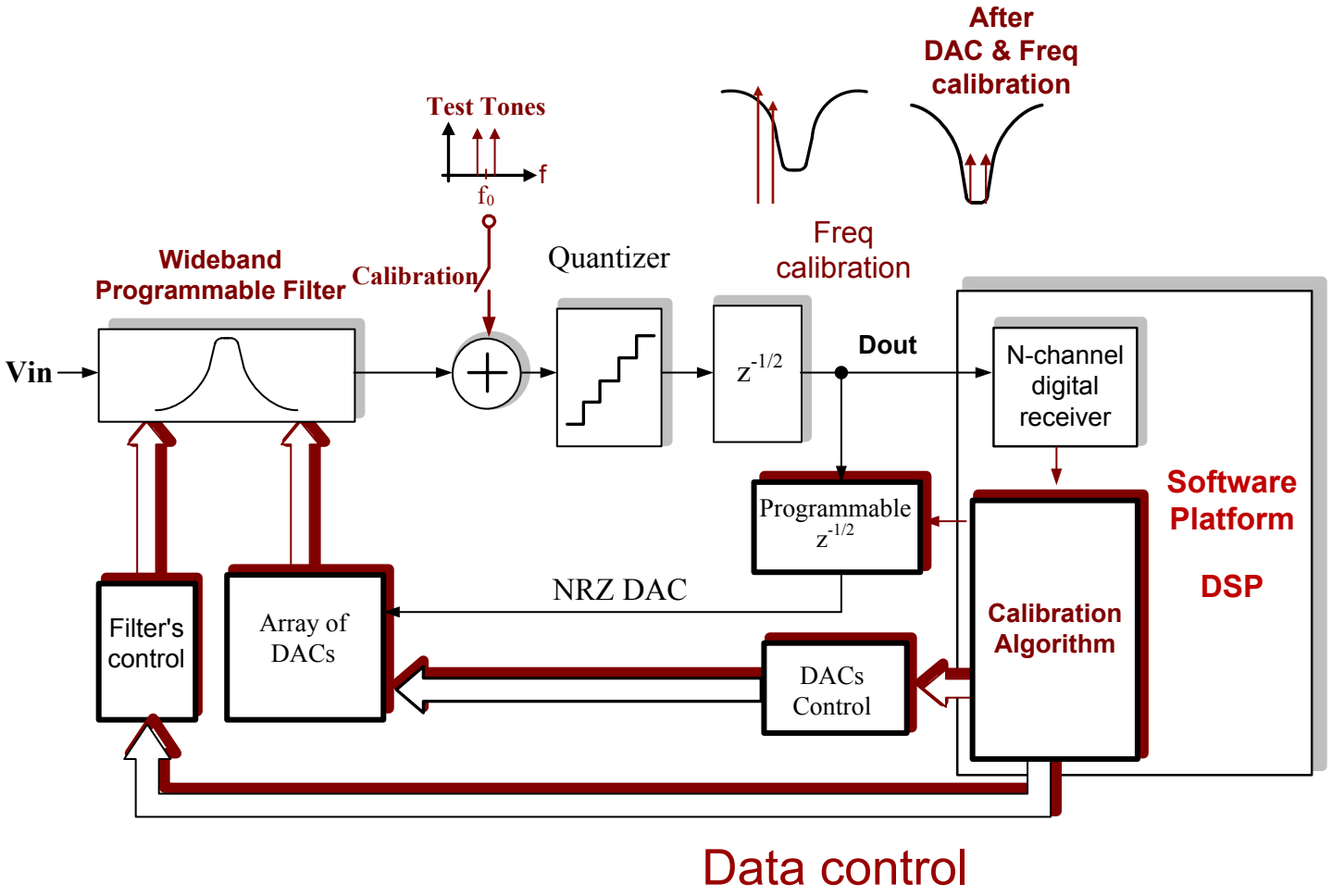
# Calibrating the Noise Transfer Function (NTF)



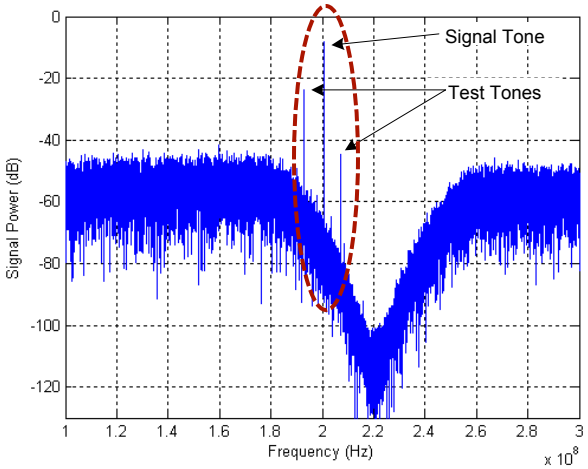

- **Measure the NTF (in digital domain) using non-critical calibration signatures**
- **The tones are arranged such that increase NTF visibility**

# Digitally assisted calibration scheme

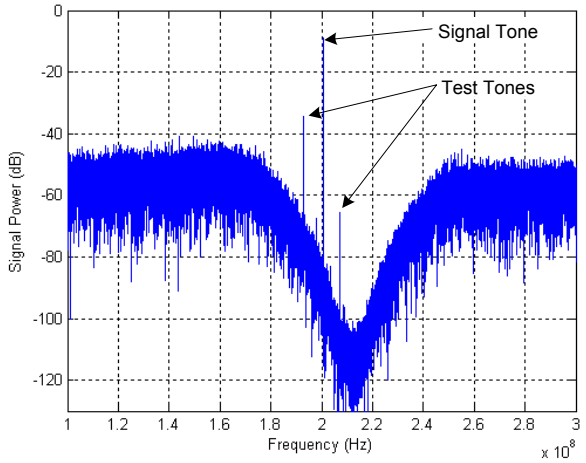



A 6th-Order 200MHz IF Bandpass Sigma-Delta Modulator With over 68dB SNDR in 10MHz Bandwidth, C.Y. Lu, et.al., *IEEE J. Solid-State Circuits,* June 2010.

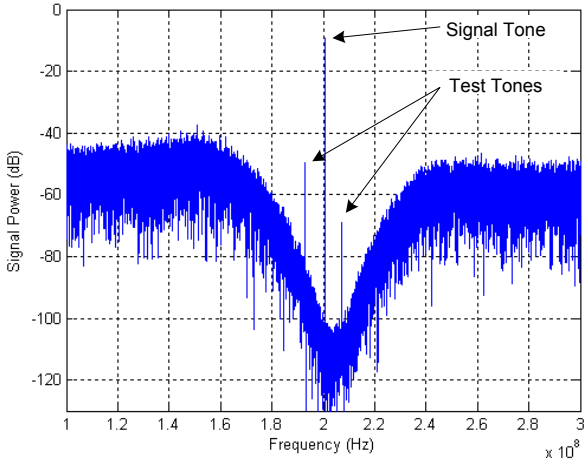
# Calibrating the Noise Transfer Function (NTF)



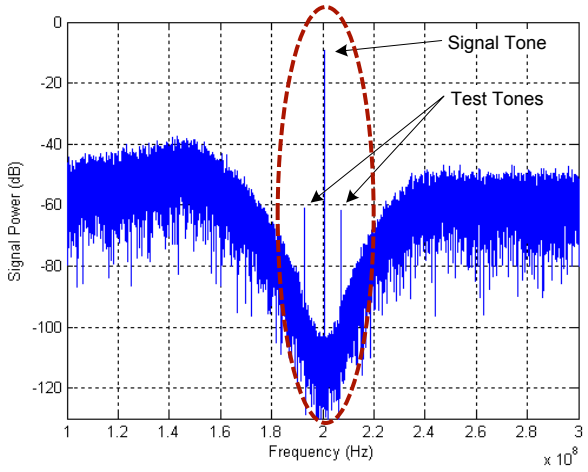

a) Uncalibrated ADC. SNR = 34dB




b) Calibration after 3 Iterations. SNR = 48dB



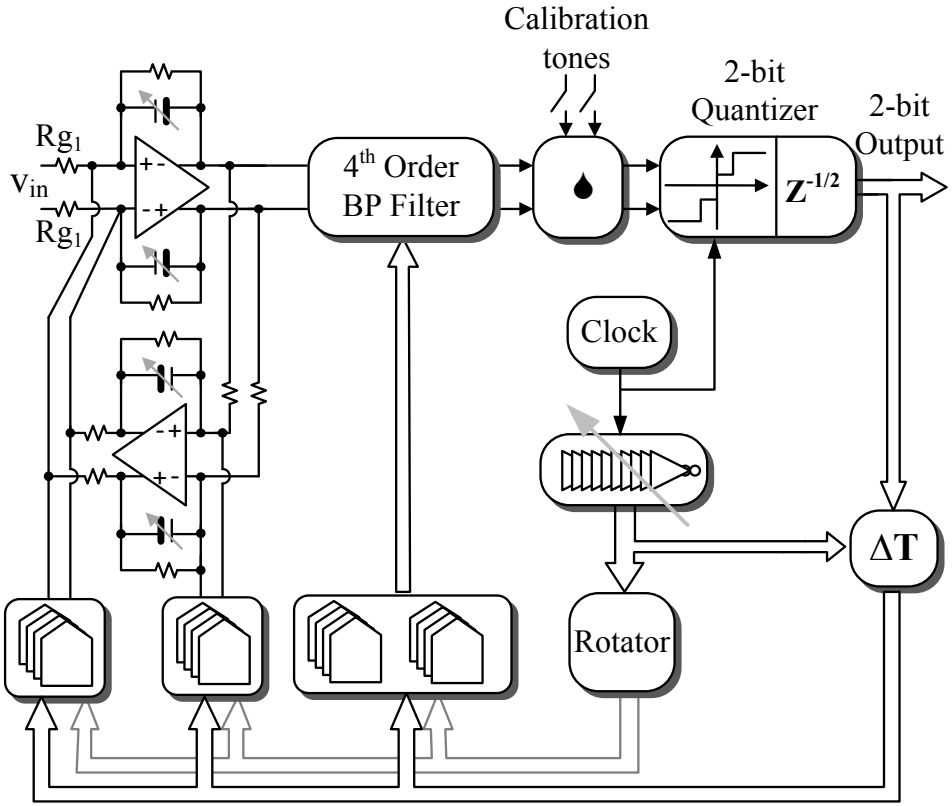

c) Calibration after 6 Iterations. SNR = 60dB

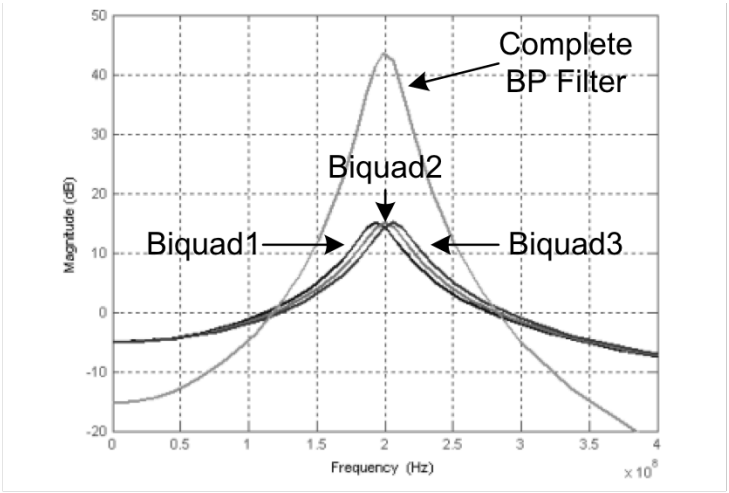


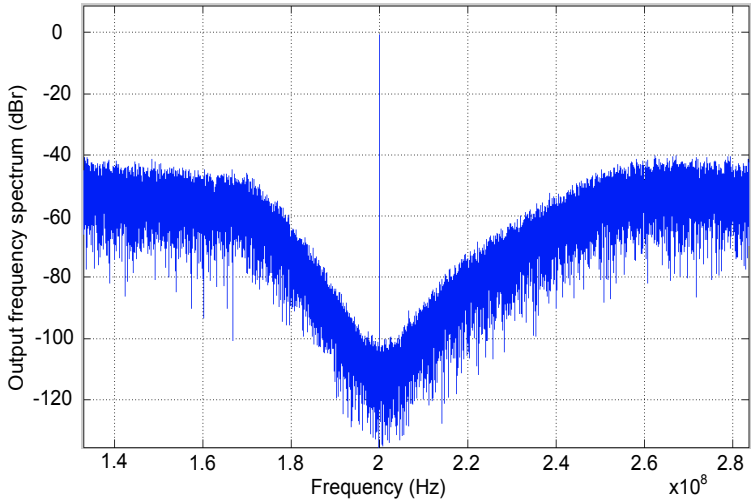

d) Calibration after 20 Iterations. SNR = 82dB

# Experimental Results: 200 MHz Prototype

- **6th-order 2-bit CT BP ΣΔ Modulator**

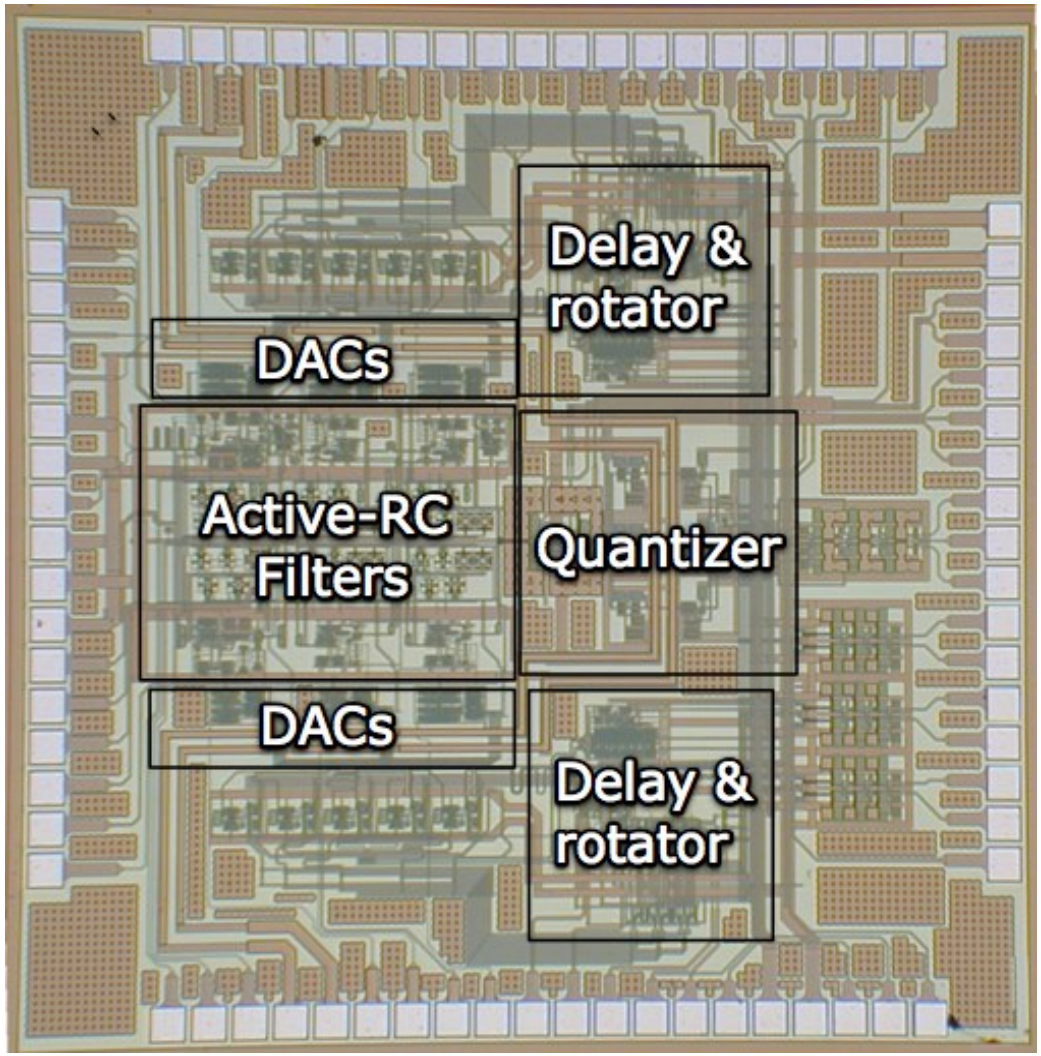



SQNR=77.8dB @10MHz BW

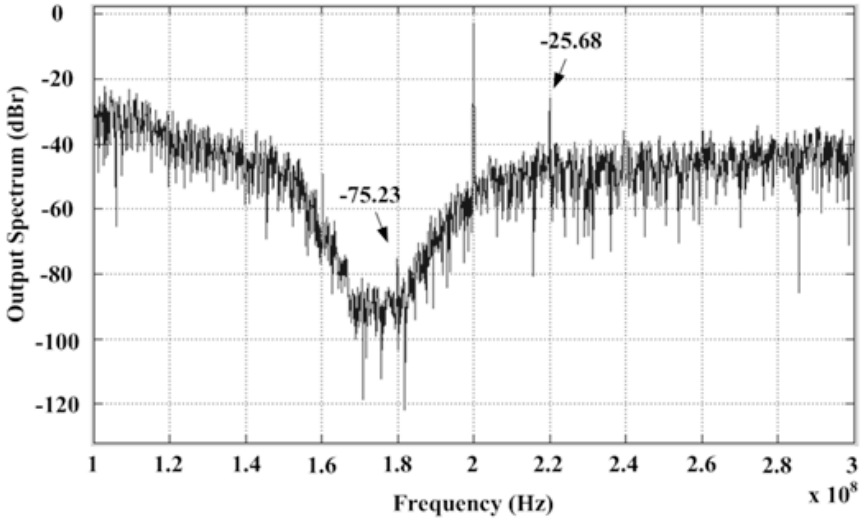
# Chip Prototype: TSMC 0.18um

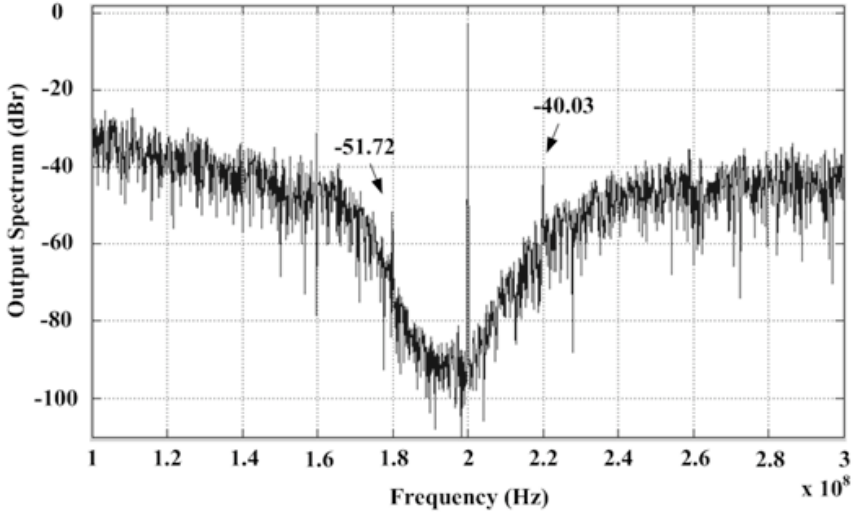


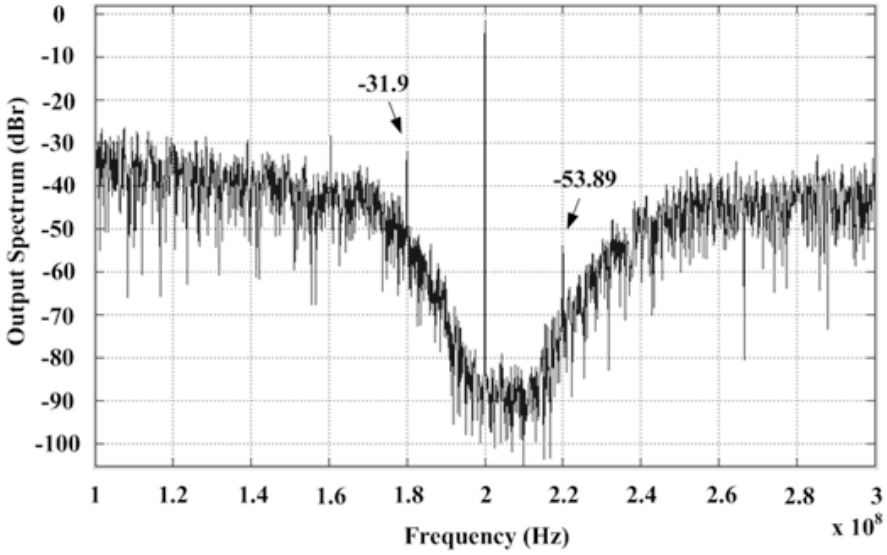

Cho-Ying Lu, et.al.,
June 2010, JSSC

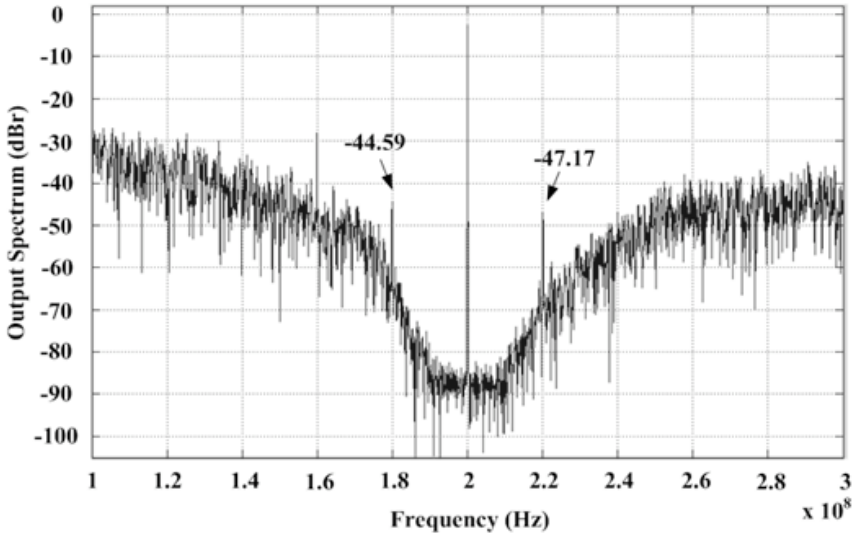
- TSMC 1P6M 0.18um CMOS Technology
- Core area=2.48mm$^2$

# ADC Calibration: Experimental results



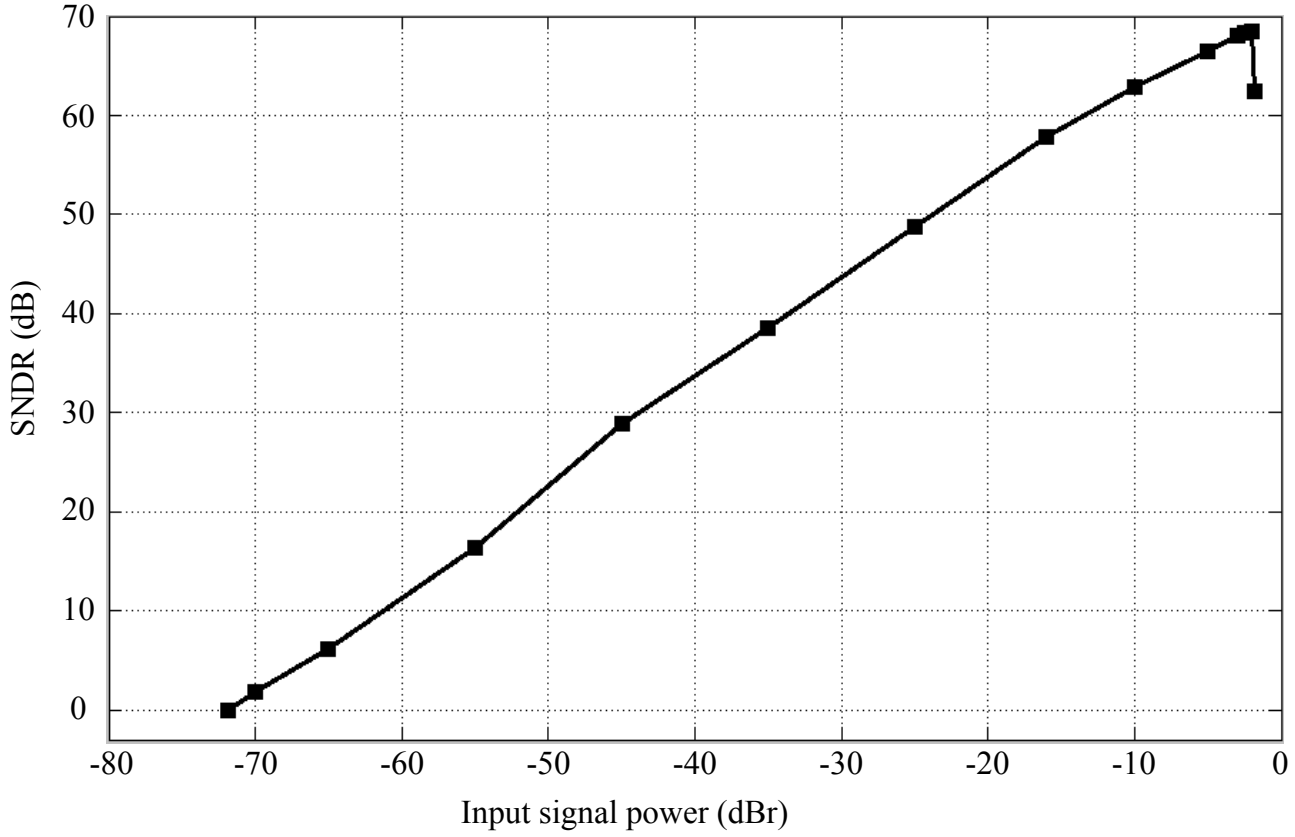



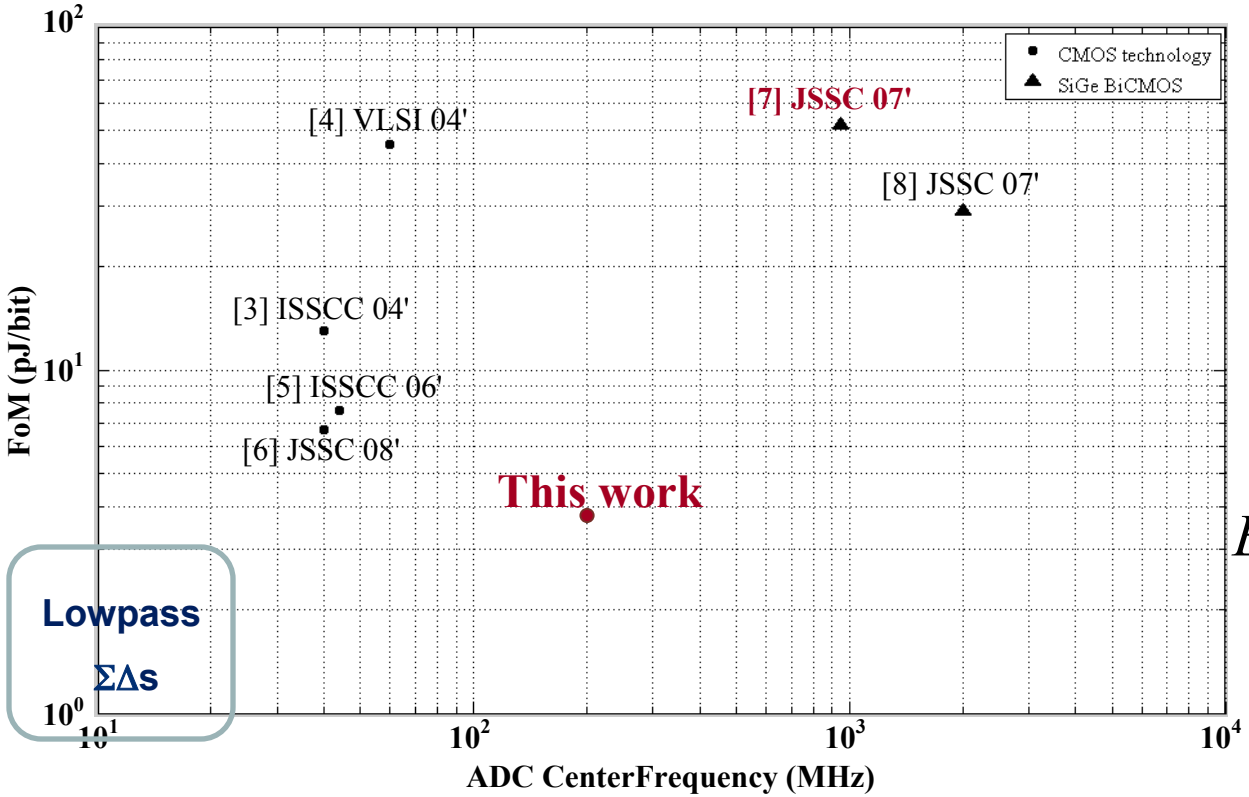



# Measured SNDR: Peak=68.4 dB

$$SNDR = \frac{Power_{input}}{Noise_{in-band} + Power_{third\_intermodulation}}$$



# Figure of Merit versus ADC Frequency




$$FoM = \frac{Power}{2^{ENOB} * 2BW}$$

$$ENOB = \frac{SNDR_{peak} - 1.76}{6.02}$$

# Conclusions

- RF-to-Digital converters are still the big challenge
- Programmability of the filters is quite challenging due to the lack of efficient RF switches
- Efficient frequency synthesizers are possible but..
  - Clock jitter is a major issue
  - Most of the power is dynamic due to the extremely high frequency
- Blocker Rejection is another hurdle
- Currently demonstrated SQNR>60 dB in a 1-5 MHz bandwidth with < 100mW static power consumption. Similar performance is desirable in over 10-20 MHz bandwidth
- System level calibration scheme to obtain maximum SNR is possible; extensive digital signal processing is required
- Still significant design challenges for CMOS RF-ADC's