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Variation-Tolerant Design of Analog CMOS Circuits – Lecture 3

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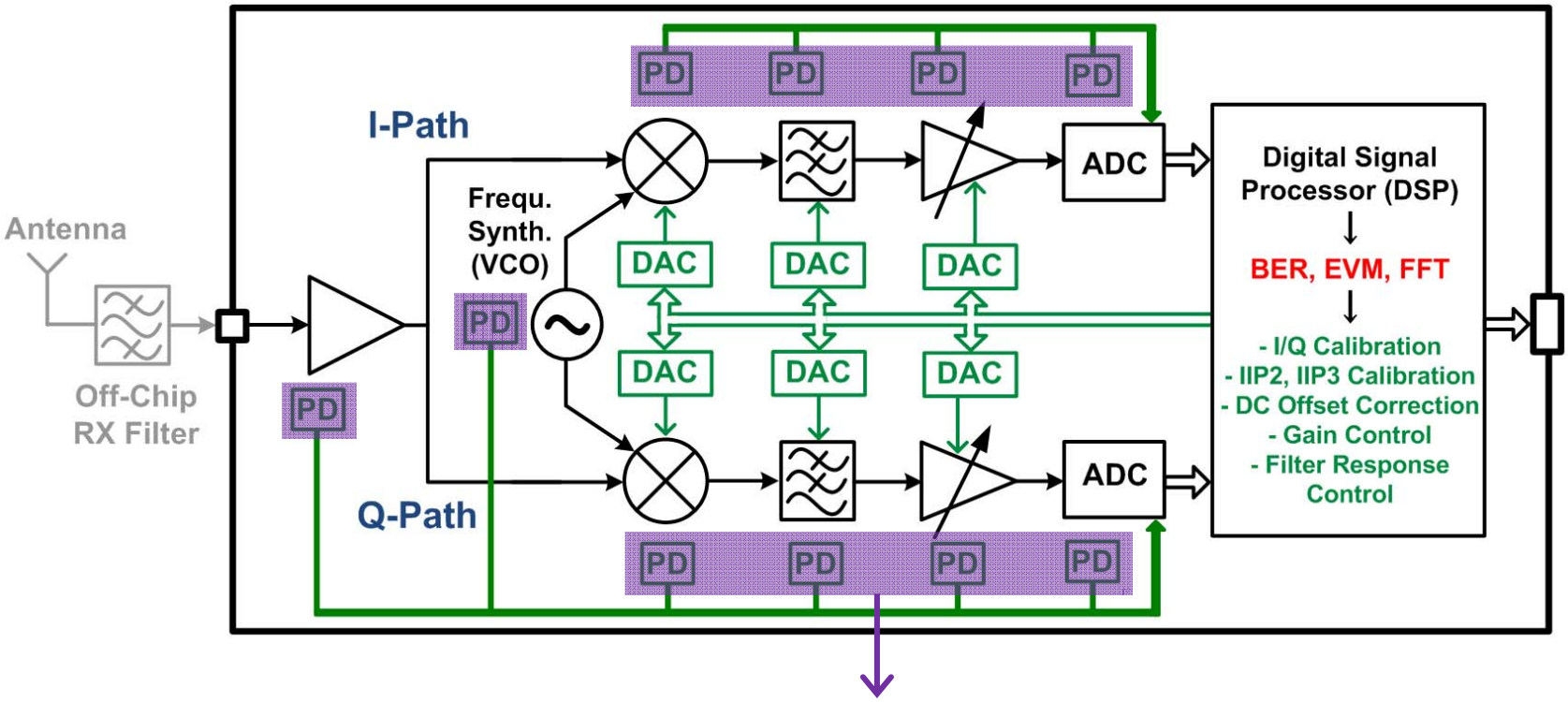
Short Course held at:

Universitat Politècnica de Catalunya
Barcelona, Spain

Outline – Lecture 3

- On-chip DC and RF power measurements with differential temperature sensors
- Case study: differential temperature sensor design
- Temperature sensors as variation monitors
- Mismatch reduction for transistors in high-frequency differential analog signal paths
- Example: mixer design with analog tuning for transistors biased in weak inversion

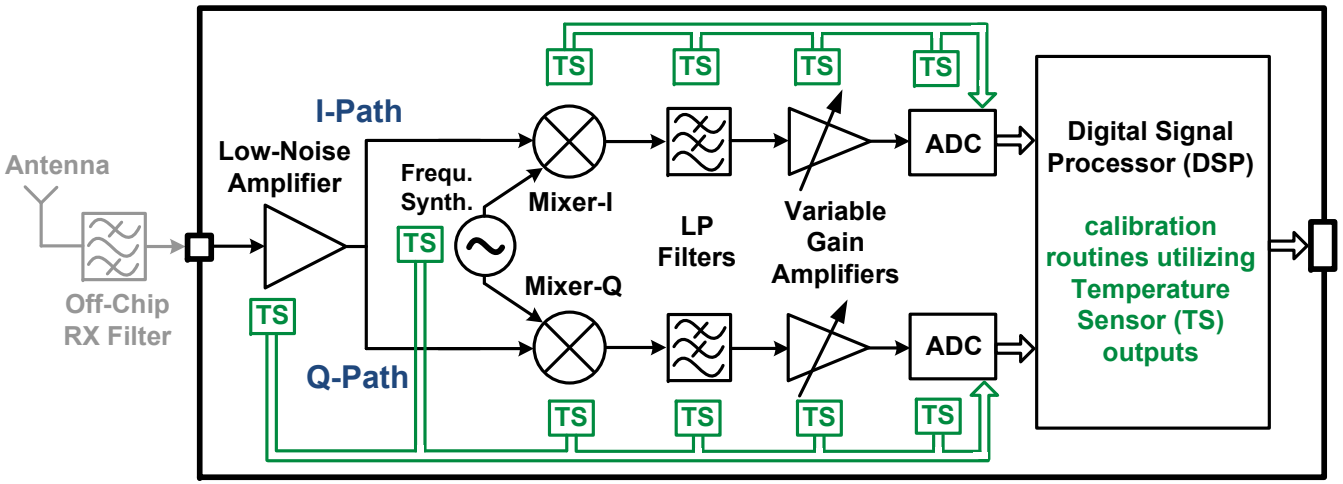
Built-In Receiver Testing and Calibration – Revisited



- Power detectors
  - Main benefit: improved block-level observability
  - Main drawback: loading effects due to connections to signal paths

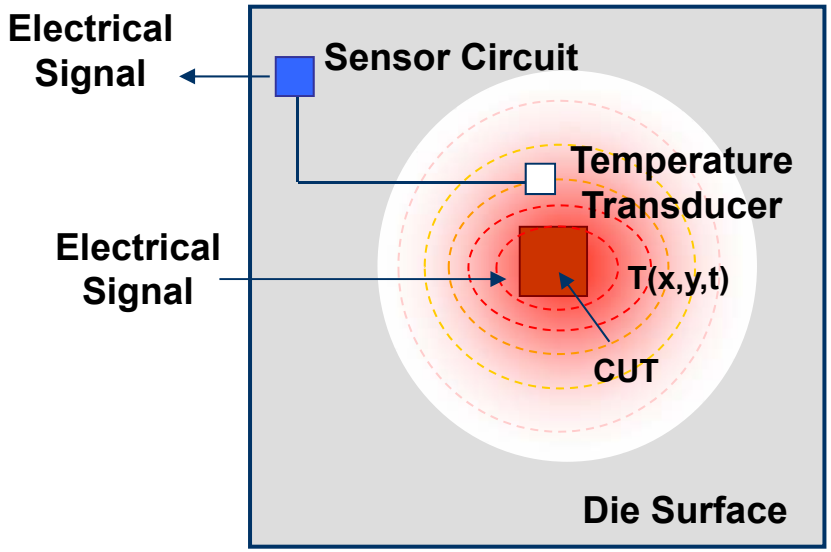
On-Chip Thermal Monitoring

- Motivation for temperature sensing in built-in test (BIT)
  - Thermal coupling: power dissipation → temperature change (near the device)
    - Affects operating parameters
    - Temperature gradients can be used to monitor system performance
  - Measurement without direct contact to the circuit → avoids impact on performance



- Objectives
  - Realization of on-chip temperature sensors for built-in testing applications
  - RF signal power and linearity characterization with temperature sensors

Principle of the Temperature-Sensing Technique



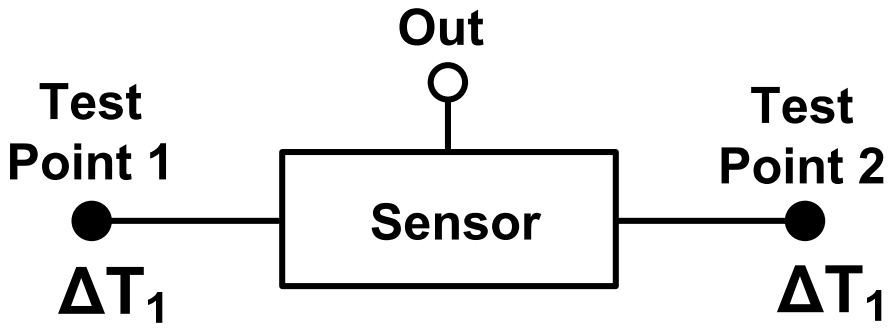
CUT Excitation: Electrical variables Current, Voltage

Joule Effect → Power Dissipation → Thermal Coupling

CUT Measure: Electrical variables Current, Voltage

Temperature Sensor ← Temperature Increase at the Silicon Surface. Thermal Map T(x,y,t)

Differential Temperature Measurements

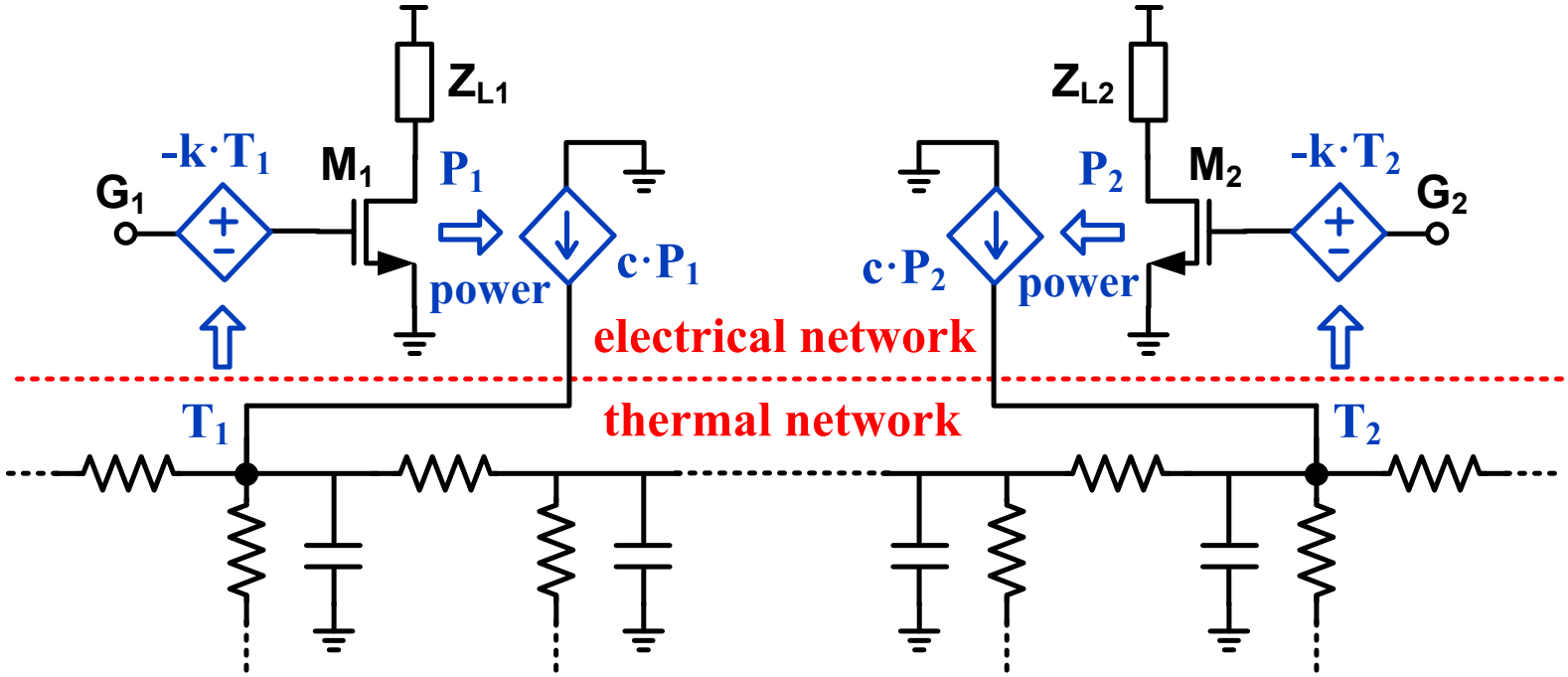


$$\Delta Out = S_{diff}\left(\Delta T_1 - \Delta T_2\right) + S_{cm}\left(T + \frac{\Delta T_1 + \Delta T_2}{2}\right)$$

- Desired on-chip sensor characteristics:
  - High sensitivity (S_{diff}) to differential temperature
  - Low sensitivity (S_{cm}) to common-mode (absolute) temperature

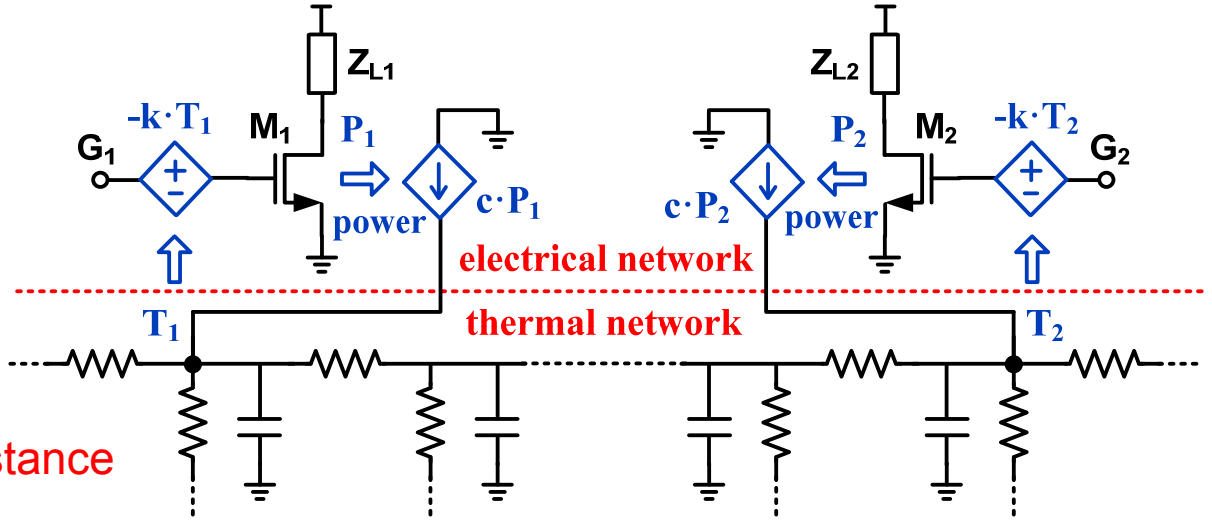
J. Altet, A. Rubio, E. Schaub, S. Dilhaire, and W. Claeys, "Thermal coupling in integrated circuits: application to thermal testing," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 81-91, Jan. 2001.

Modeling of Thermal Coupling



- Equivalence of thermal & electrical domains
  - Temperature ↔ Voltage
  - Power ↔ Current
  - Thermal coupling: based on a discrete RC model from layout dimensions

Key Properties of Thermal Coupling



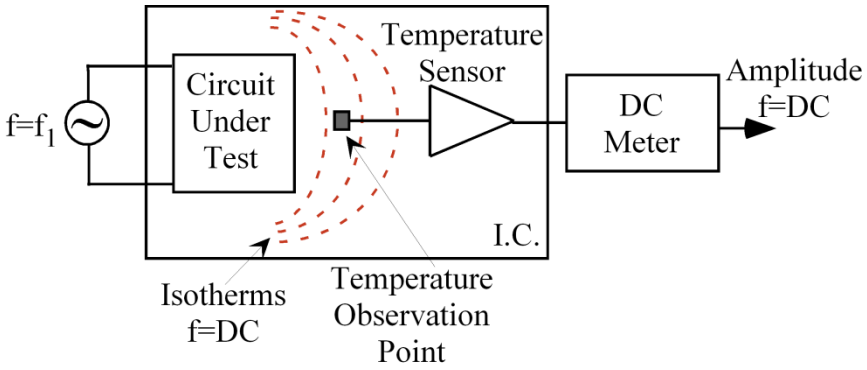
- Thermal diffusion
  - Exponential decay with distance
  - Low-pass frequency response
    (ΔT is dominated by power sources with f < 10kHz)

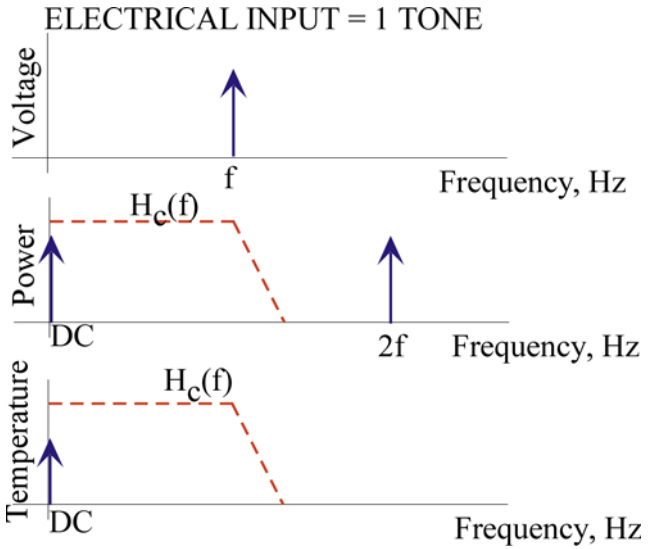
$$T(r,t) = \frac{C}{r}\cdot e^{-r\sqrt{\omega/(2\cdot D)}}\cdot e^{j(\omega t - r\sqrt{\omega/(2\cdot D)})}$$

where : C is a constant
D is the thermal diffusion constant
ω is the frequency of the heat (power) source
r is the radius from the heat source

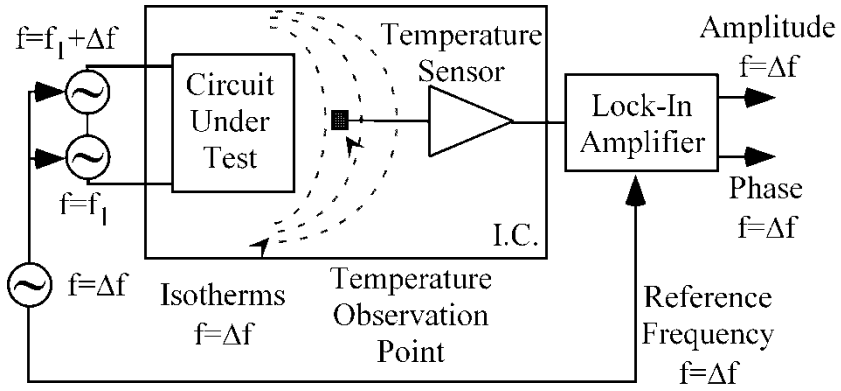
Two Possible Situations

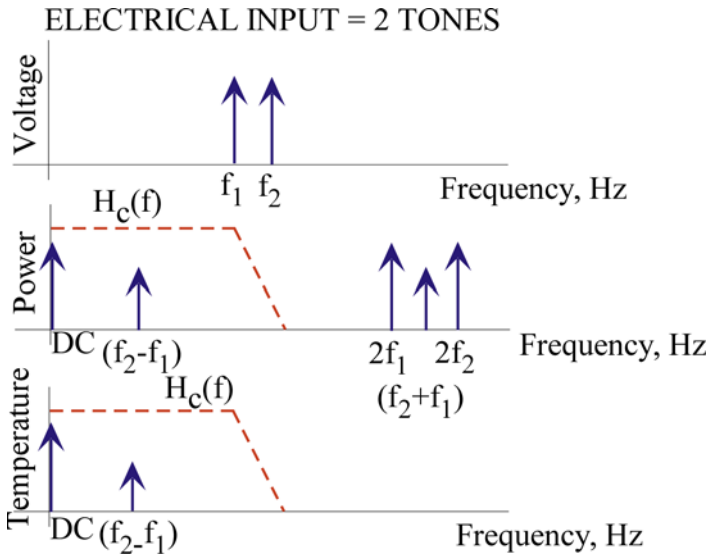
Homodyne Approach:





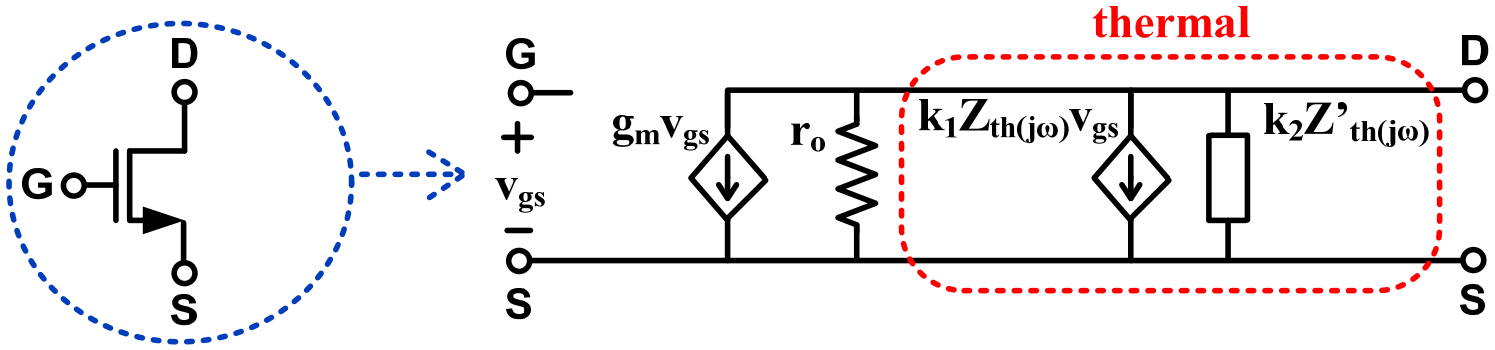
Heterodyne Approach:





Thermal Coupling on the Device Level

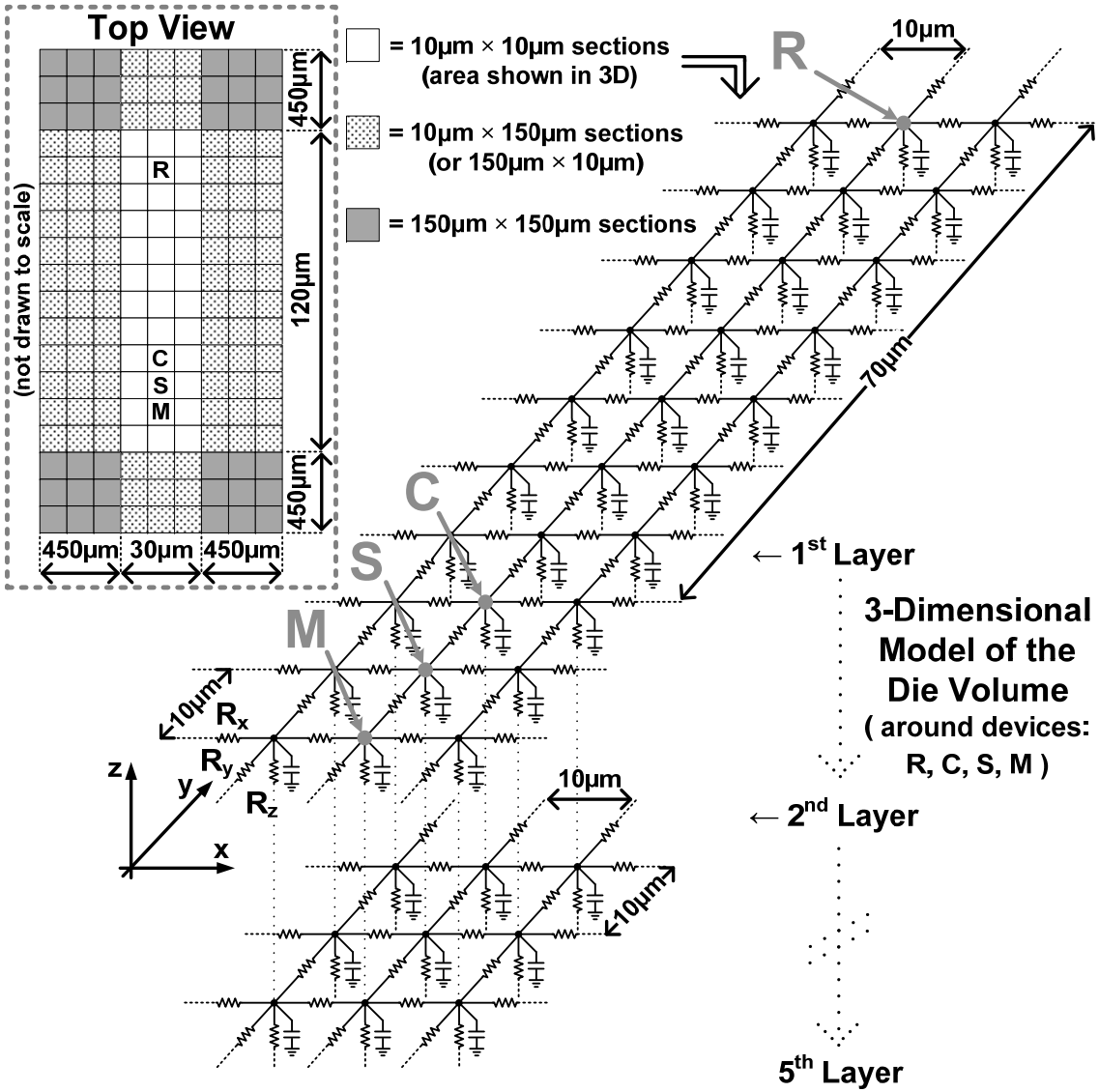
- Example: MOS device model with thermal effects



- $Z_{th(j\omega)}$ = thermal impedance
- $Z'_{th(j\omega)}$ = linearized $Z_{th(j\omega)}$ @ operating point
- From the effect of $Z_{th(j\omega)}$, the typical sensitivity to temperature is:

$$\frac{\Delta V_T}{\Delta T} \approx \frac{-1.8\text{mV}}{\text{K}} \quad , \quad \frac{(\Delta\beta/\beta)}{\Delta T} \approx \frac{-0.5\%}{\text{K}}$$

Modeling the Silicon Die



Unit Elements in the 3-D Model:

$$C = \rho \cdot c \cdot x_u y_u z_u$$

$$R_x = x_u /(\kappa \cdot y_u z_u)$$

$$R_y = y_u /(\kappa \cdot x_u z_u)$$

$$R_z = z_u /(\kappa \cdot x_u y_u)$$

where:
ρ = mass density
c = specific heat capacity
κ = conductivity for silicon

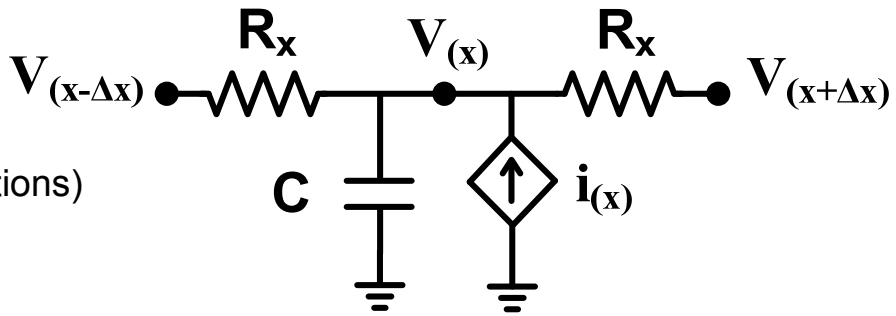
Discrete Thermal Coupling Model

- Partial differential equation to model heat diffusion

$$\rho c \frac{\partial u(x,y,z,t)}{\partial t} = \kappa\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}\right)u(x,y,z,t) + p_d(x,y,z,t)$$

  - where: u is the temperature of the material
    t is time
    x, y, z are the coordinates with respect to the heat source
    for silicon: ρ (mass density) = 2.3 x 10^6 g/m^3
    κ (thermal conductivity) = 120 W/(m x K) at 75ºC
    p_d = rate of heat production (i. e., the dissipated power)
    c (specific heat capacity) = 0.7 J/(g x K)

- Discretized heat diffusion modeling
  - Electrical equivalent circuit →



  - Parameters:
    unit volume ≡ ΔxΔyΔz (small incremental directions)
    C ≡ ΔxΔyΔzρc
    R_x ≡ Δx / (κΔyΔz)
    i ≡ p (power dissipated per unit volume)
    v ≡ u (temperature)

S. Mattisson, H. Hagberg, and P. Andreani, "Sensitivity degradation in a tri-band GSM BiCMOS direct-conversion receiver caused by transient substrate heating," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 486-496, Feb. 2008.

References: Thermal Coupling

D. J. Walkey, T. S. Smy, R. G. Dickson, J. S. Brodsky, D. T. Zweidinger, and R. M. Fox, “Equivalent circuit modeling of static substrate thermal coupling using VCVS representation,” *IEEE J. Solid-State Circuits*, vol. 37, no. 9, pp. 1198-1205, Sep. 2002.

N. Nenadovic, S. Mijalkovic, L. K. Nanver, L. K. J. Vandamme, V. d'Alessandro, H. Schellevis, and J. W. Slotboom, "Extraction and modeling of self-heating and mutual thermal coupling impedance of bipolar transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1764-1772, Oct. 2004.

J. Altet, A. Rubio, E. Schaub, S. Dilahire, and W. Claeys, “Thermal coupling in integrated circuits: application to thermal testing,” *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 81-91, Jan. 2001.

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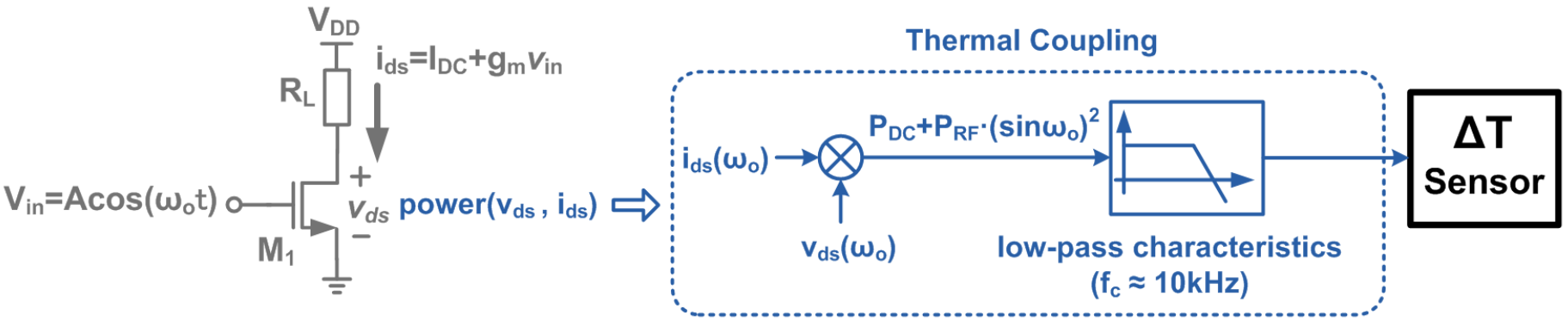
L. Codecasa, D. D'Amore, and P. Maffezzoni, "Modeling the thermal response of semiconductor devices through equivalent electrical networks," *IEEE Trans. Circuits and Systems I: Fund. Theory and Appl.*, vol. 49, no. 8, pp. 1187-1197, Aug. 2002.

V. Szekely, "On the representation of infinite-length distributed RC one-ports," *IEEE Trans. Circuits and Systems*, vol. 38, no. 7, pp. 711-719, July 1991.

S.-S. Lee and D. J. Allstot, “Electrothermal simulations of integrated circuits,” *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1283-1293, Dec. 1993.

W. VanPetegem, B. Geeraerts, W. Sansen, and B. Graindourze, “Electrothermal simulation and design of integrated circuits,” *IEEE J. Solid-State Circuits*, vol. 29, no. 2, pp. 143-146, Feb. 1994.

RF Signal Characterization

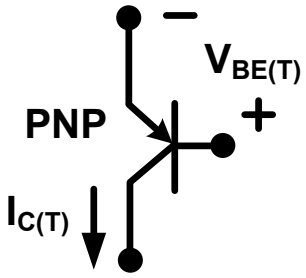


- RF power conversion to low-frequency temperature changes:
  - **Mixing of AC voltage & current at the same frequency**
    → down-conversion (DC power)
- Power components at M_1 that cause low-frequency temperature changes (after low-pass coupling):
  - with single tone $v_{in} = A\cos(\omega t)$
    → at DC: $(V_{DD}I_{DC} - R_L I_{DC}^2)$ **$- \frac{1}{2}R_L(g_m A^2)$**
  - with two tones $v_{in} = A\cos(\omega_1 t) + A\cos(\omega_2 t)$
    → at DC: $(V_{DD}I_{DC} - R_L I_{DC}^2)$ **$- R_L(g_m A)^2$**
    → at $(\omega_1 - \omega_2)$: **$R_L(g_m A)^2$**

Fundamental PNP Temperature Dependence

- Equivalent temperature dependence of $I_{C(T)}$ and $V_{BE(T)}$

$$I_{C(T)} = I_{S(T)} \exp\left(\frac{qV_{BE}}{kT}\right) = A_E C T^{\eta} \exp\left(\frac{q(V_{BE} - V_{g0})}{kT}\right)$$



  - where:
    - $I_{S(T)}$ is the saturation current at temperature T
    - q is the electron charge
    - k is Boltzmann's constant
    - V_{g0} is the extrapolated bandgap voltage at 0K
    - C and η are process-dependent constants
    - A_E is the emitter area

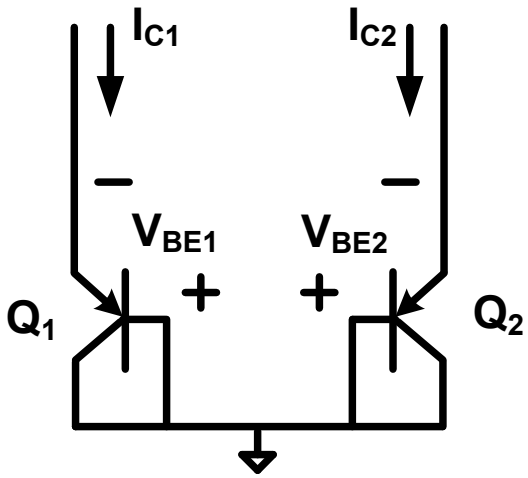
  - From the above expression, the base-emitter voltage was expressed in [1] at reference temperature T_r as:

$$V_{BE(T_r)} = V_{g0} + \frac{kT_r}{q} \ln\left(\frac{I_{C(T_r)}}{A_E C T_r^{\eta}}\right)$$

→ $V_{BE(Tr)}$ typically has a sensitivity of -2mV/K

[1] M. A. P. Pertijs, G. C. M. Meijer, and J. H. Huijsing, "Precision temperature measurement using CMOS substrate pnp transistors," *IEEE Sensors Journal*, vol. 4, no. 3, pp. 294-300, June 2004.

Conventional Temperature Measurements



- Proportional to <u>absolute</u> temperature (PTAT) measurement concept
  - Two substrate PNP transistors with constant collector-current ratio (I_{C2}/I_{C1})
  - Sensitivity of V_{BE} to absolute temperature (T) change ≈ -2mV/K
  - Relative measurement for robustness to process variation:

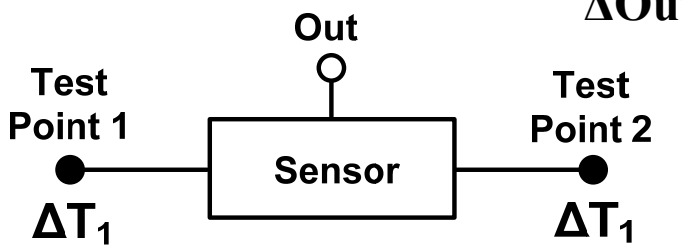
$$\Delta V_{BE(T)} = V_{BE2(T)} - V_{BE1(T)} = n \times \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{C1}}\right)$$

  - n ≈ 1 is the diode ideality factor (minor effect from process variation)
  - Sensitivity of ΔV_{BE} to absolute temperature: k/q ≈ 8.6 x 10^{-5} V/K

Temperature Measurement Sensitivity

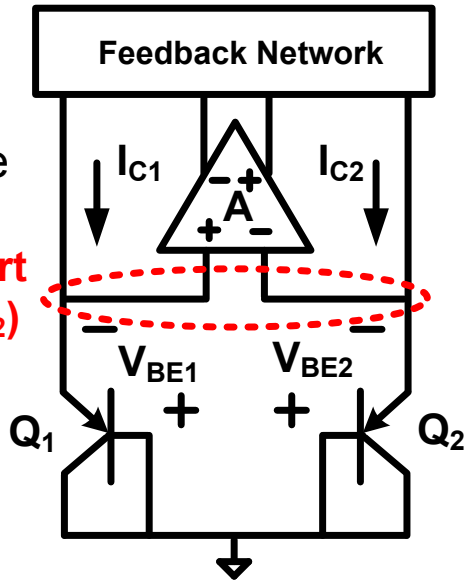
- Differential temperature measurement concept

$$\Delta Out = S_{diff}\left(\Delta T_1 - \Delta T_2\right) + S_{cm}\left(T + \frac{\Delta T_1 + \Delta T_2}{2}\right)$$



  - Desired:
    - High sensitivity (S_{diff}) to differential temperature changes
    - Low sensitivity (S_{cm}) to common-mode (absolute) temperature

→ Achieved by forcing $\Delta V_{BE} = 0$



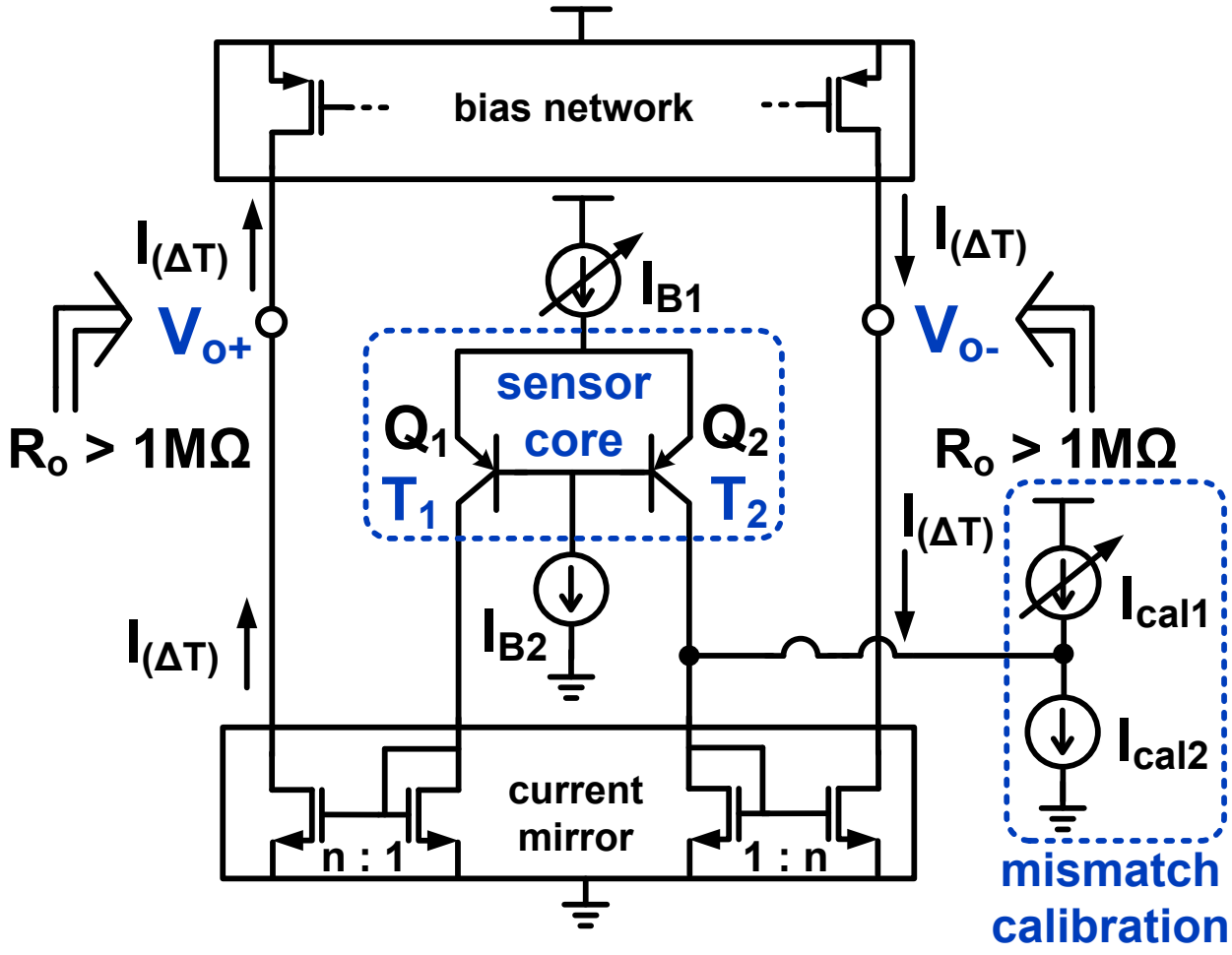
  - Temperature sensitivity is process-dependent
    - Requires calibration

$$S_{diff} = \frac{\partial(I_{C2} - I_{C2})}{\partial T} = 2 \cdot \frac{I_C}{T}\left[\frac{1}{V_t}\left(EG - \frac{V_{BE}}{NF}\right) + XTI\right]$$

    - Example design in 0.18μm CMOS:
      $S_{diff} \approx$ 1-3μA/ºC

where: EG = bandgap energy
XTI = saturation current exponent
NF = forward current emission coefficient
V_t = thermal voltage

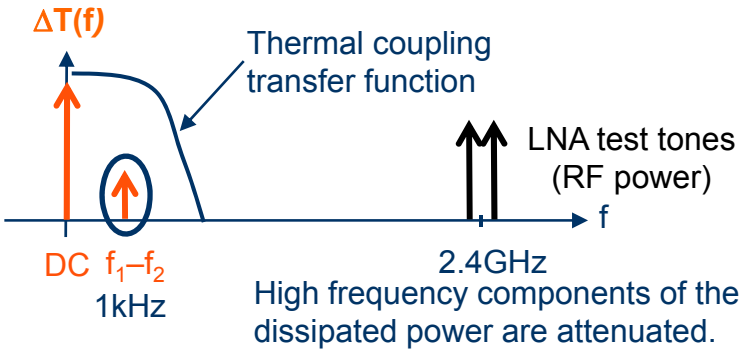
Example Sensor with High Temperature Sensitivity



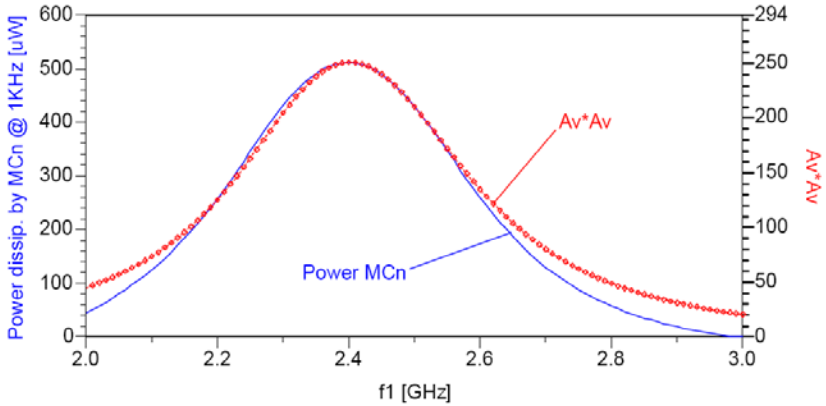
E. Aldrete-Vidrio, D. Mateo, and J. Altet, "Differential temperature sensors fully compatible with a 0.35-µm CMOS process," *IEEE Trans. Components and Packaging Technologies*, vol. 30, no. 4, pp. 618-626, Dec. 2007.

Examples: Low-Noise Amplifier Characterization at UPC

D. Mateo, J. Altet, E. Aldrete-Vidrio, and J. L. Gonzalez, "Frequency characterization of a 2.4 GHz CMOS LNA by thermal measurements," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2006 IEEE , pp. 517-521, June 2006.

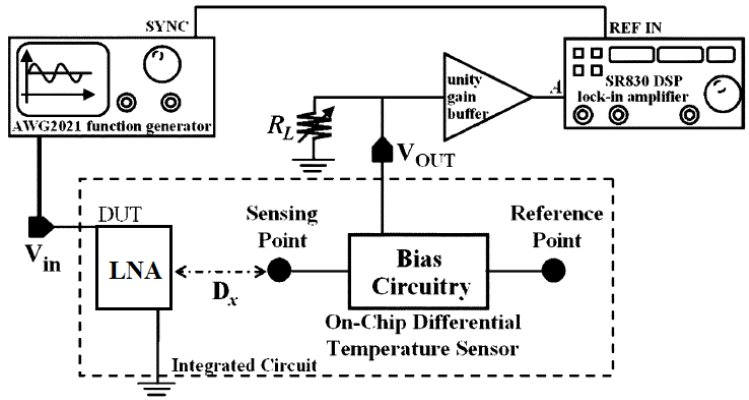


Testing approach exploiting thermal coupling

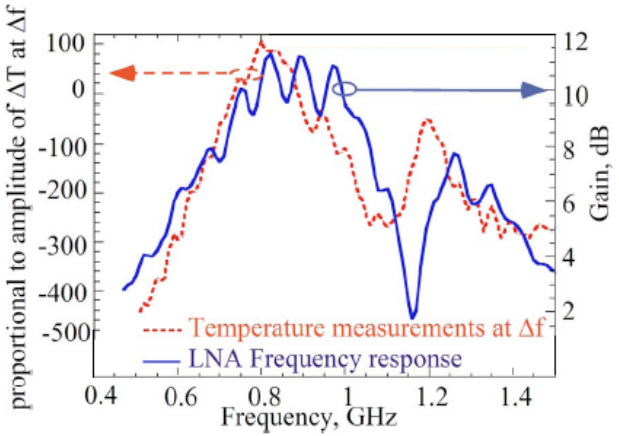


Simulated correlation of power gain (Av^2) and power dissipation (active device at LNA output) vs. frequency

J. Altet, E. Aldrete-Vidrio, D. Mateo, A. Salhi, S. Grauby, W. Claeys, S. Dilhaire, X. Perpiñà, and X. Jordà, "Heterodyne lock-in thermal coupling measurements in integrated circuits: applications to test and characterization," *Review of Scientific Instruments*, vol. 80, no. 2, pp. 026101-1 – 026101-3, Feb. 2009.



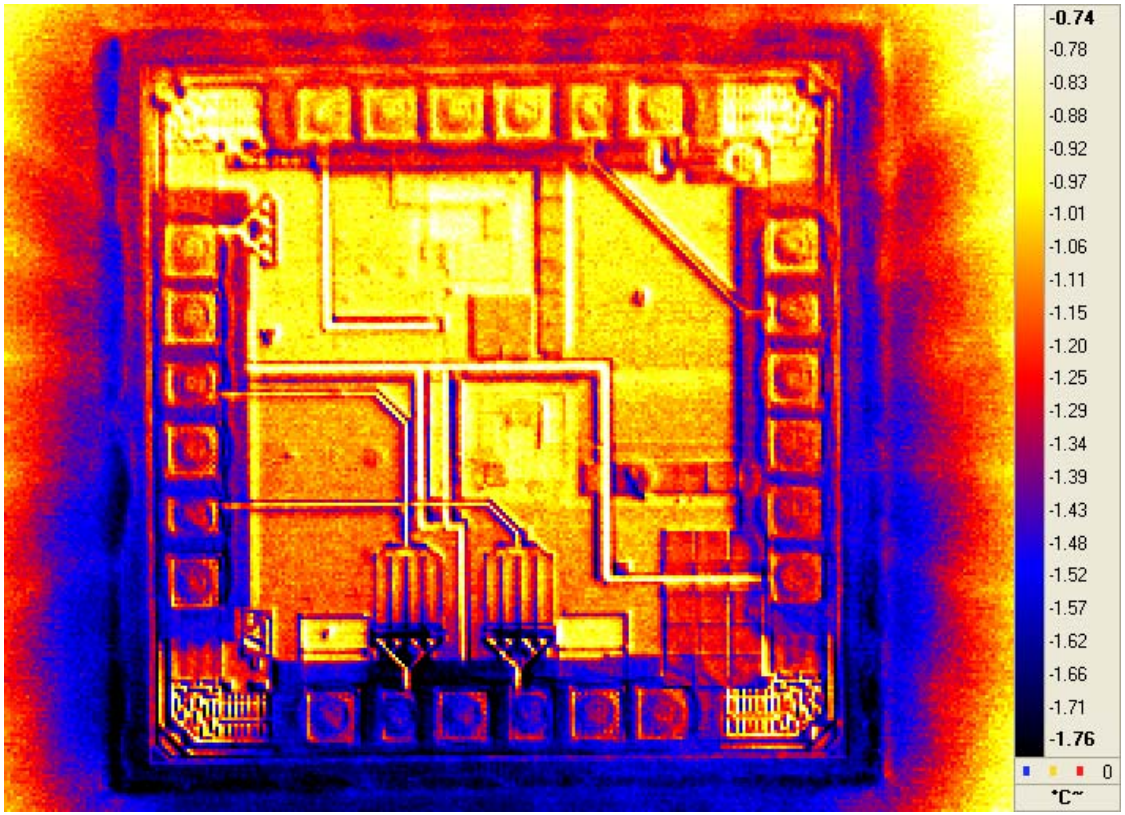
Measurement setup with off-chip lock-in amplifier



Measurement $\Delta T@(f_1\text{-}f_2)$ and LNA gain vs. frequency

On-Chip Heating Example

Thermal map of a power amplifier (PA) with DC bias and 0dBm RF power:

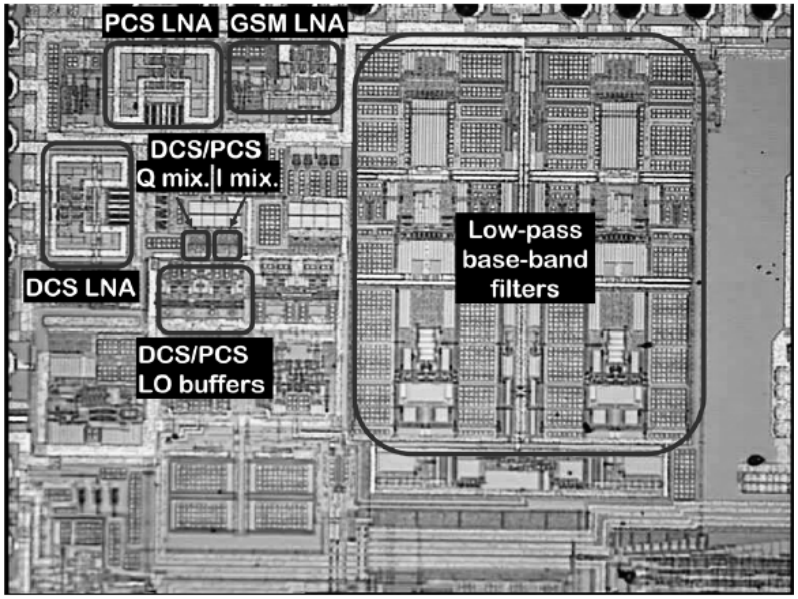


- PA characterization with on-chip temperature sensing
  - 65nm CMOS
  - DC temperature sensor output correlation with the power added efficiency (PAE)
  - Demonstrated with PAs operating at 2GHz and 60GHz

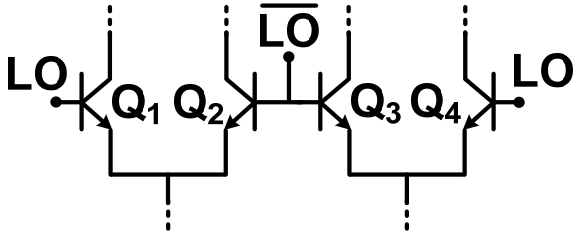
Test chip characterization results can be found in:
J.L. González, B. Martineau, D. Mateo, and J. Altet, “Non-invasive monitoring of CMOS power amplifiers operating at RF and mmW frequencies using an on-chip thermal sensor”, in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, June 2011.

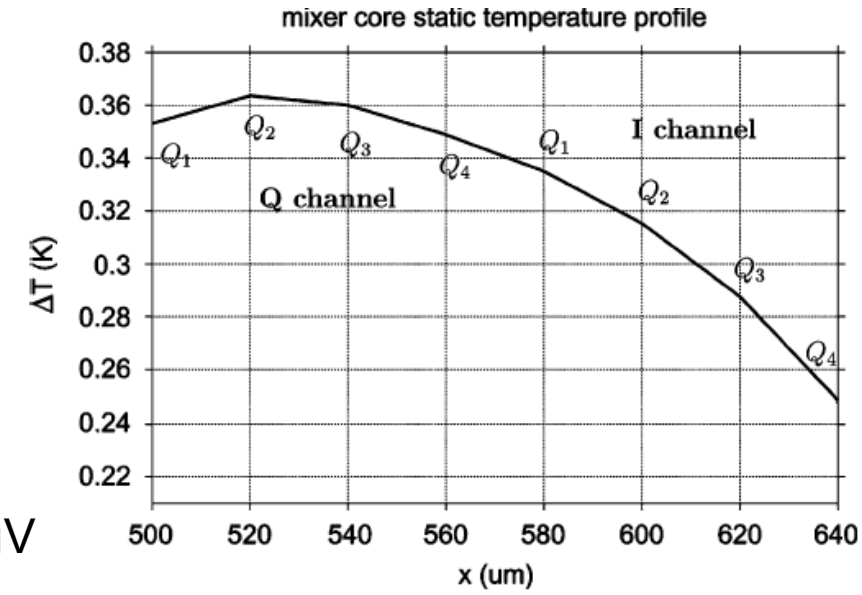
On-Chip Heating Impact on Circuit Performance

Example: GSM Tri-Band BiCMOS Direct Conversion Receiver



mixer core:





- Substrate heating effects
  - Sensitivity degraded by 2-4dB
  - DC offset → I-channel: 620 μV, Q-channel: -340 μV

S. Mattisson, H. Hagberg, and P. Andreani, "Sensitivity degradation in a tri-band GSM BiCMOS direct-conversion receiver caused by transient substrate heating," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 486-496, Feb. 2008.

Outline – Lecture 3

- On-chip DC and RF power measurements with differential temperature sensors
- Case study: differential temperature sensor design
- Temperature sensors as variation monitors
- Mismatch reduction for transistors in high-frequency differential analog signal paths
- Example: mixer design with analog tuning for transistors biased in weak inversion

Differential Temperature Sensor for Built-in Testing

Marvin Onabajo*
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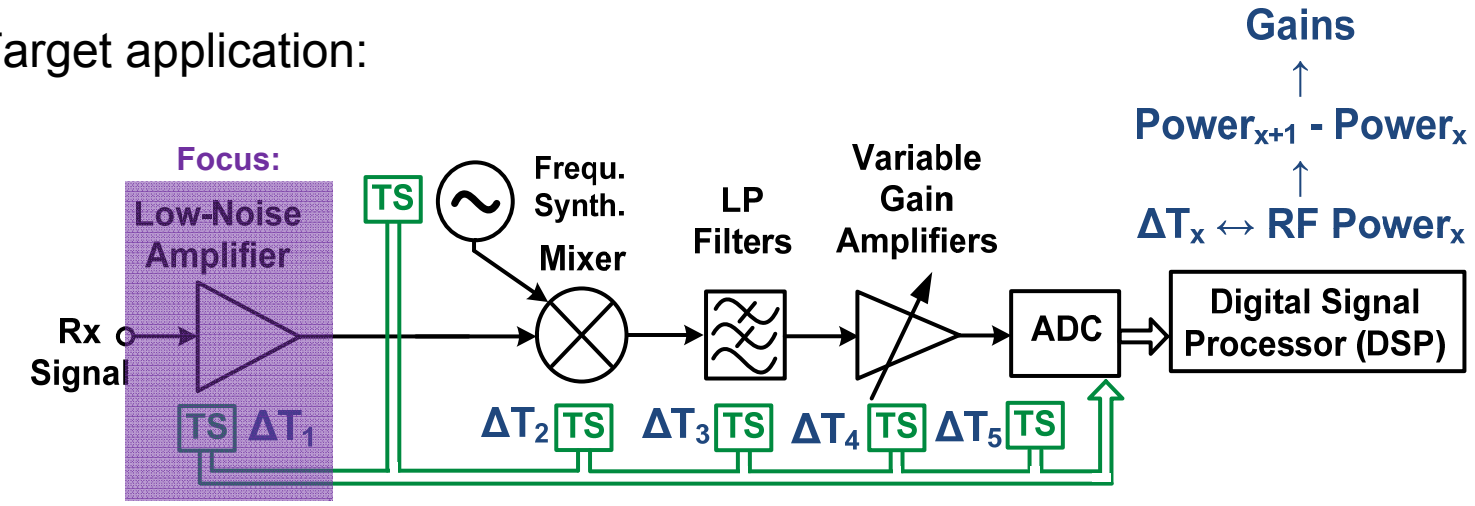
*** Texas A&M University, College Station, USA

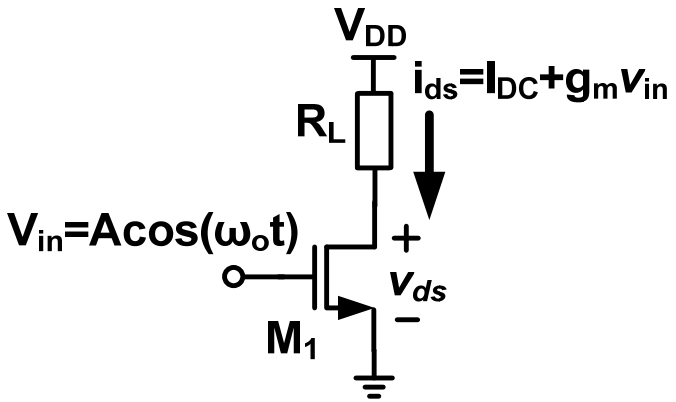
Project-Specific Goals

- Sensor optimization
  - Wide dynamic range
  - Simplicity → homodyne approach → single test tone → DC output
- LNA characterization
  - DC and RF power dissipation measurements through temperature sensing
  - 1-dB compression point estimation
- Target application:

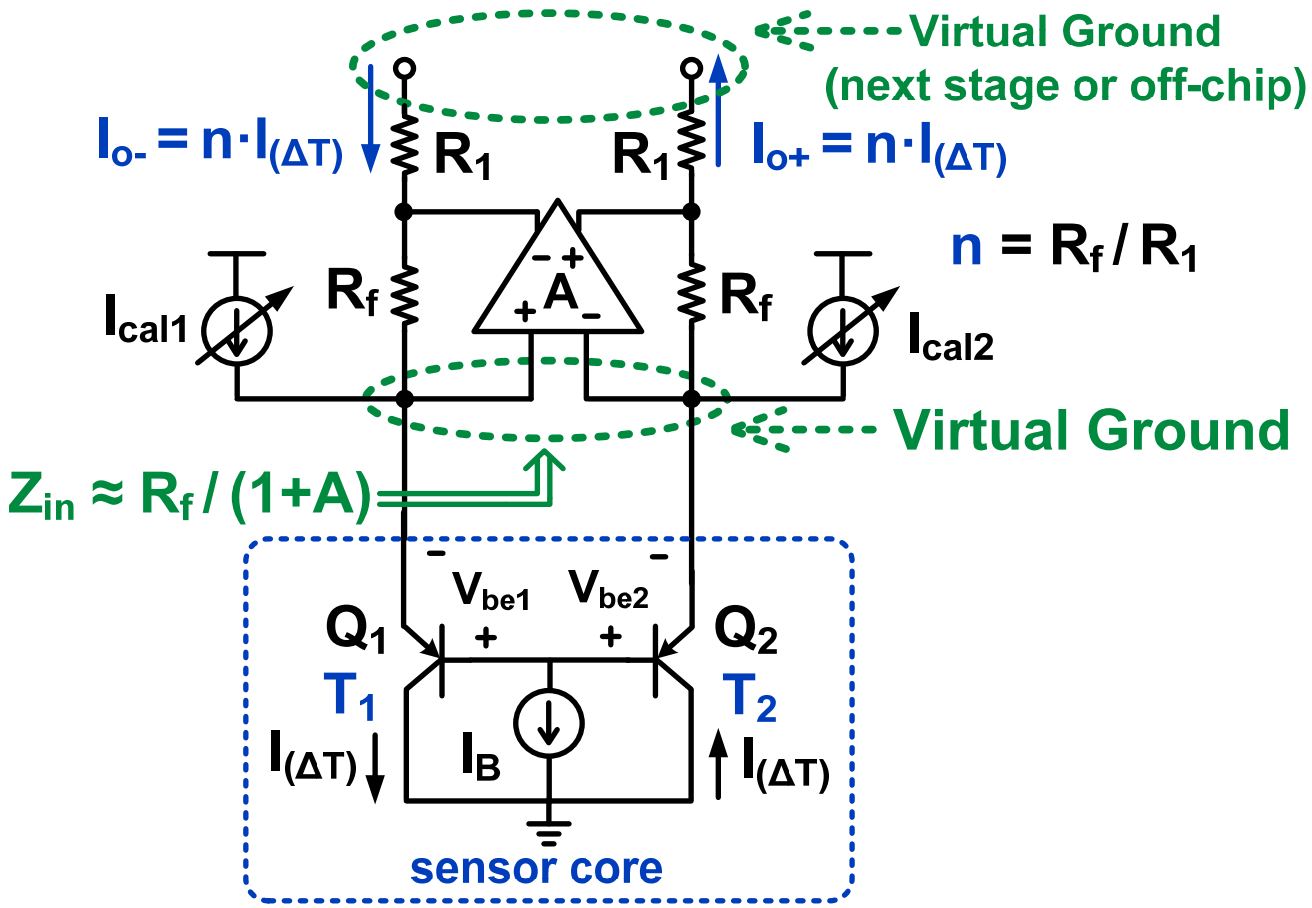


Dynamic Range Extension for DC Measurements

- Temperature measurement sensitivity requirement
  - Worst case due to weak signal: low-noise amplifier (LNA)
  - Typical scenario:
    - DC power of LNA 4-8mW
    - RF power dissipated: 0.5mW - 2mW
    - 0.1mW dissipation → ~4m ºC temperature increase
  - Project goal: improved dynamic range (prevent saturation)
    → DC and RF power measurement: $(V_{DD}I_{DC} - R_L I_{DC}^2) - \frac{1}{2}R_L(g_m A^2)$



Sensor Circuit

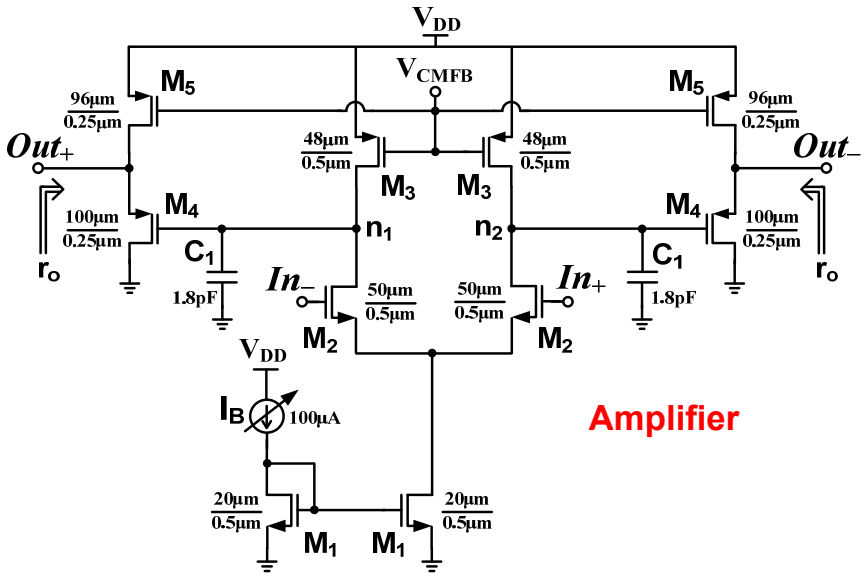


M. Onabajo, J. Altet, E. Aldrete-Vidrio, D. Mateo, and J. Silva-Martinez, "Electro-thermal design procedure to observe RF circuit power and linearity characteristics with a homodyne differential temperature sensor," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 58, no. 3, pp. 458-469, March 2011.

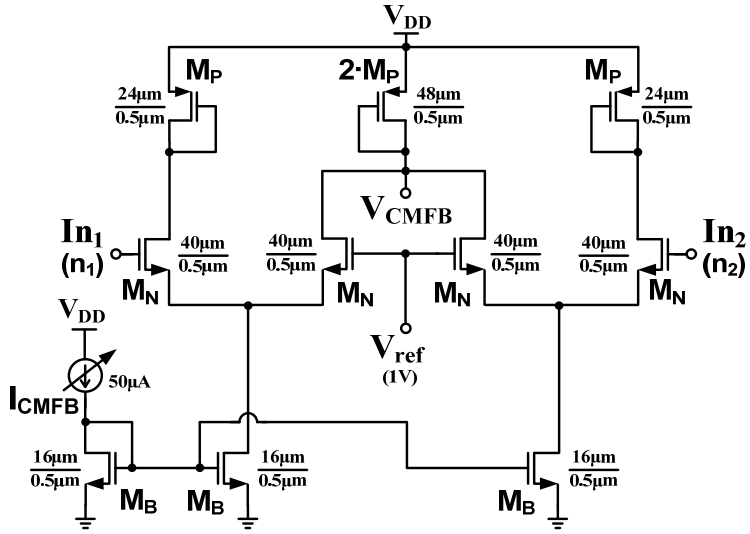
Amplifier in the Temperature Sensor Core

Simulated Amplifier Specifications:

Parameter	Value
DC Gain	30.2dB
f_{3dB}	1.74MHz
Unity Gain Frequency (f_u)	56.9MHz
Phase Margin	89.7°
Integrated Input-Referred Noise (DC - f_u)	55.1μV
Output Resistance	270Ω
5% Settling Time (1mV step input, unloaded)	264ns
CMFB Loop: DC Gain / Phase Margin	35.1dB / 74.4°
Input Offset Voltage (standard deviation)	1.5mV
Technology / V_{DD}	0.18μm CMOS / 1.8V
Power Dissipation (with CMFB)	1.05mW

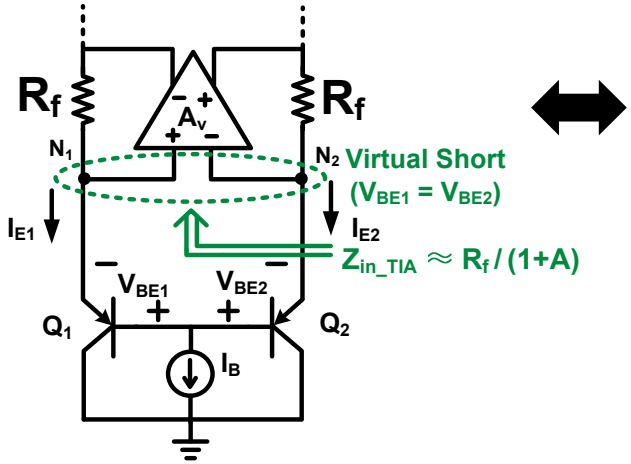


Amplifier

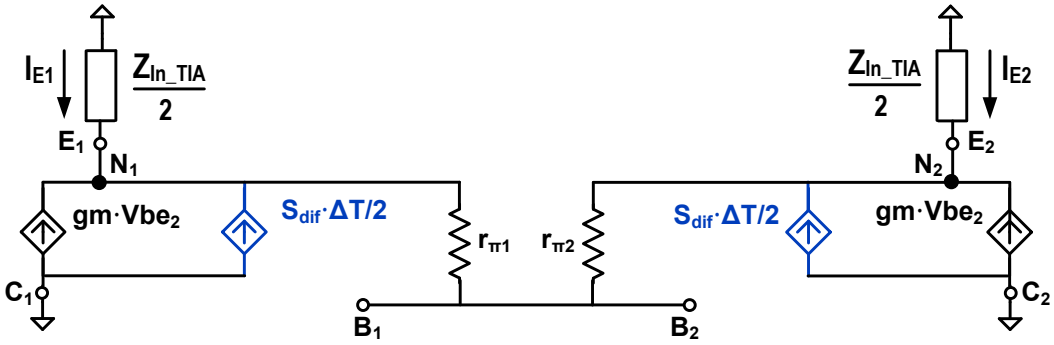


Common-mode feedback circuit

TIA Input Impedance Effect on Sensor Efficiency

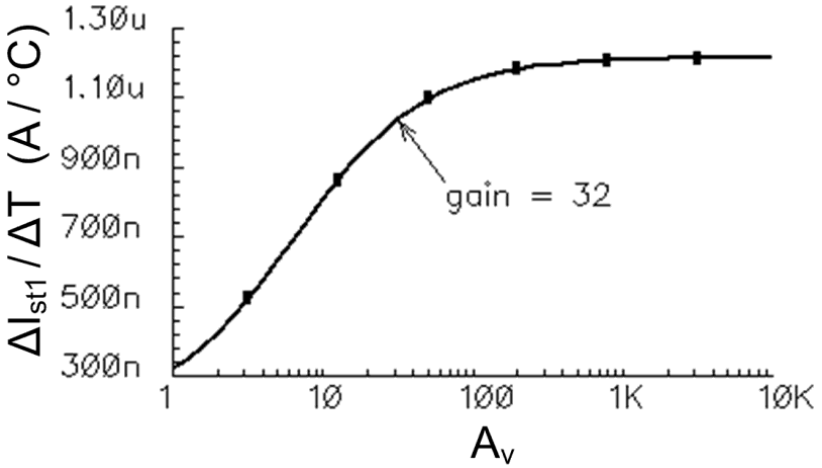


Temperature sensor core with transimpedance amplifier (TIA)



Simplified equivalent circuit of the sensor core (S_{dif} = sensitivity to differential temperature)

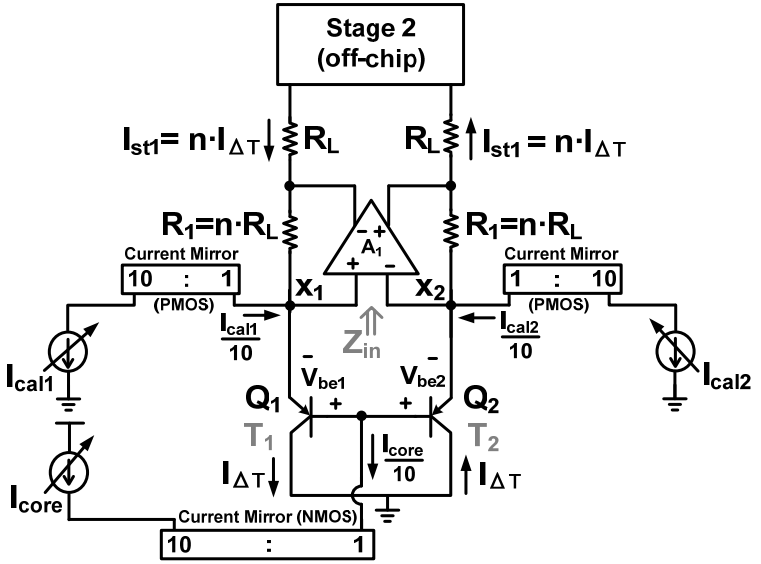
- Current generated by ΔT splits between ½ ·Z_{in_TIA} and r_π
  - Desired: $Z_{in\_TIA} \approx R_f / (1+A) << r_\pi$
  - r_π = kT/q * I_B/2 ≈ 5kΩ in this design depending on sensitivity setting (I_B)
  - The amplifier gain (A) was determined in consideration of the effect on sensitivity →

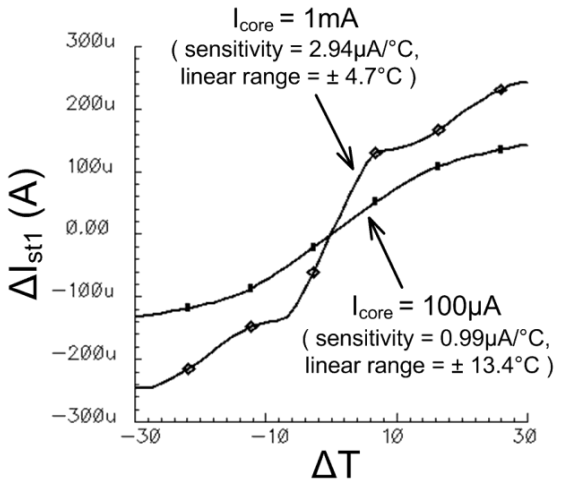


Sensitivity (A/°C) of sensor core (I_B=10µA) vs. amplifier gain (A_v)
Marker A: design point (A = 32 ≈ 30dB)

Temperature Sensor Core Simulations

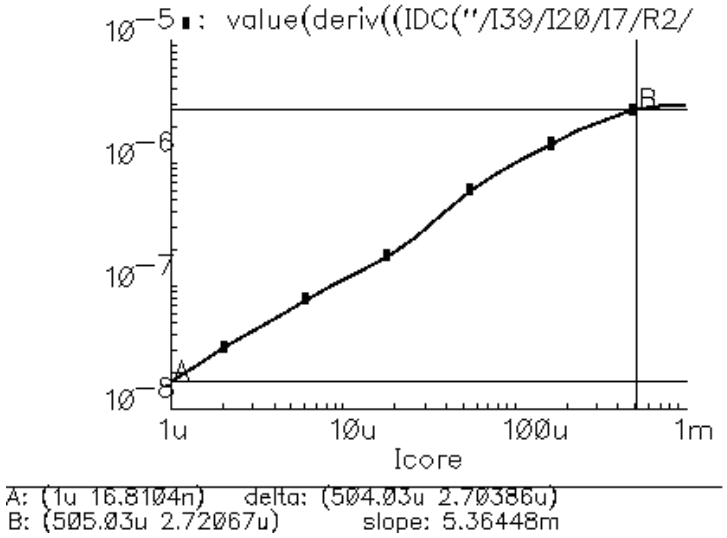
- Design in 0.18µm CMOS
  - **Sensitivity** in the sensor core (stage 1)
    - 0.998µA/ºC – 2.73µA/ºC
    - tunable with I_{core} (100µA - 1mA)
  - **Dynamic range**
    - max. sensitivity setting: 13.5ºC
    - min. sensitivity setting: 28.4ºC
  - **Offset compensation**
    - for process mismatch & temperature gradients
    - by tuning I_{cal1} or I_{cal2} from 0-500µA
    - max. sensitivity setting: ±8.2ºC
    - min. sensitivity setting: ±10.6ºC



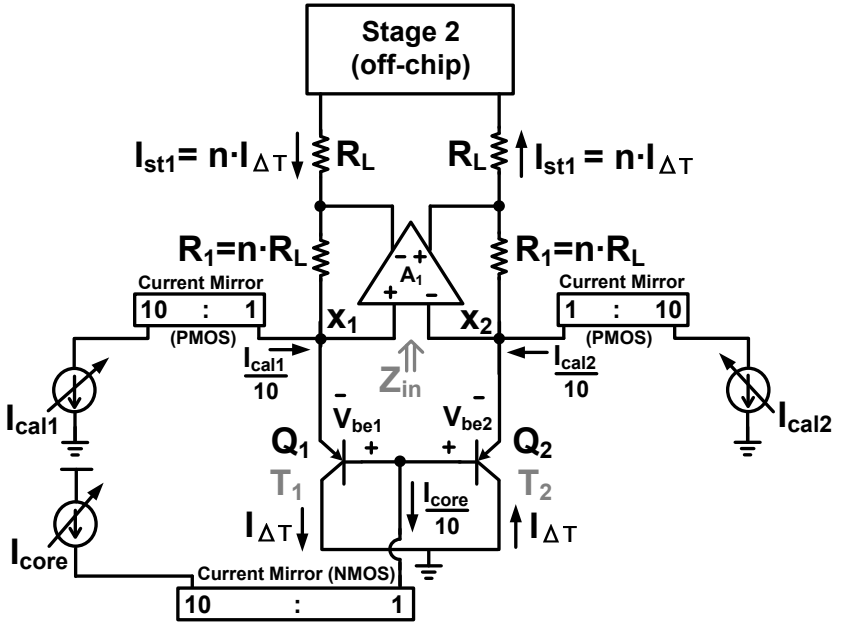


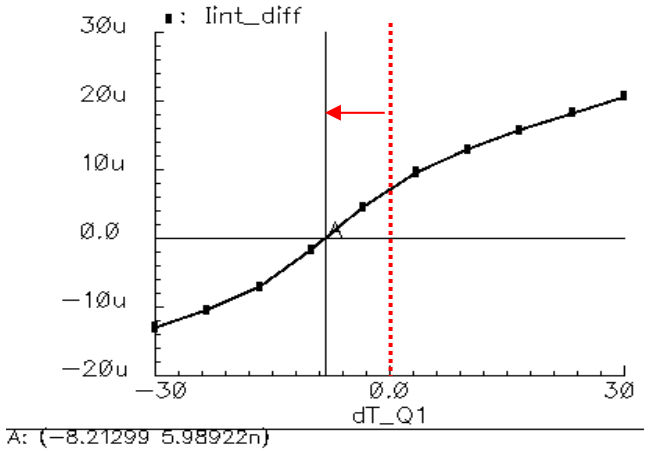
Sensitivity of the sensor core

Temperature Sensor Core Simulations (cont.)

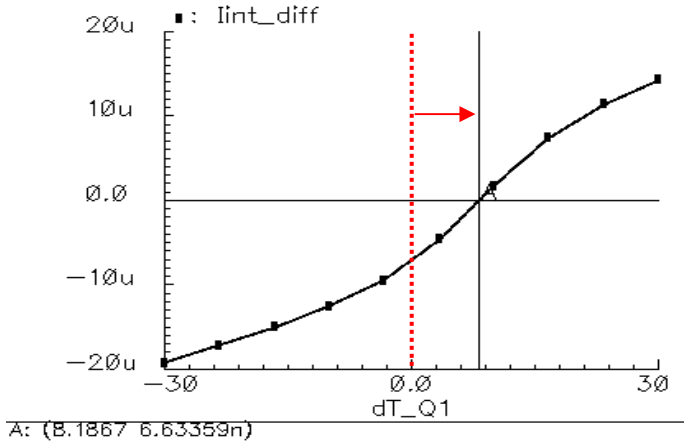


Sensitivity of ΔI_{st1} vs. I_{core} ($I_{core} = 10 \cdot I_{B\_Q1,Q2}$)





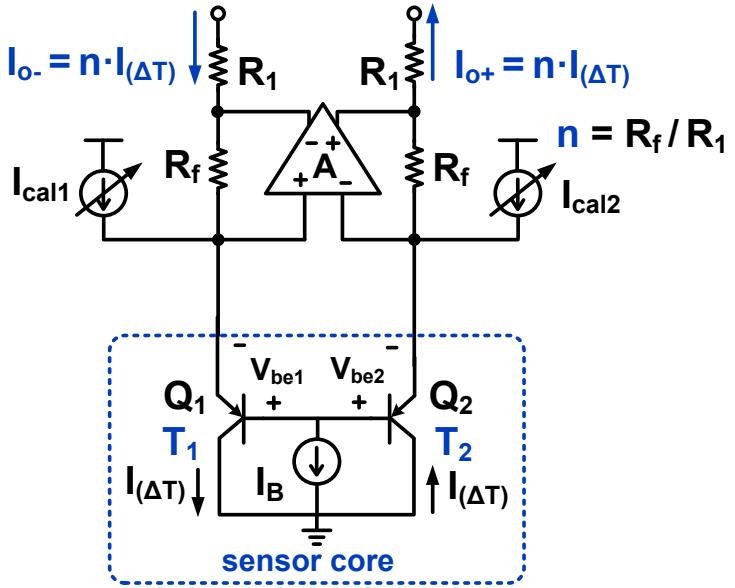
ΔI_o of stage 1 with: I_{cal1} = 100μA , I_{cal2} = 0



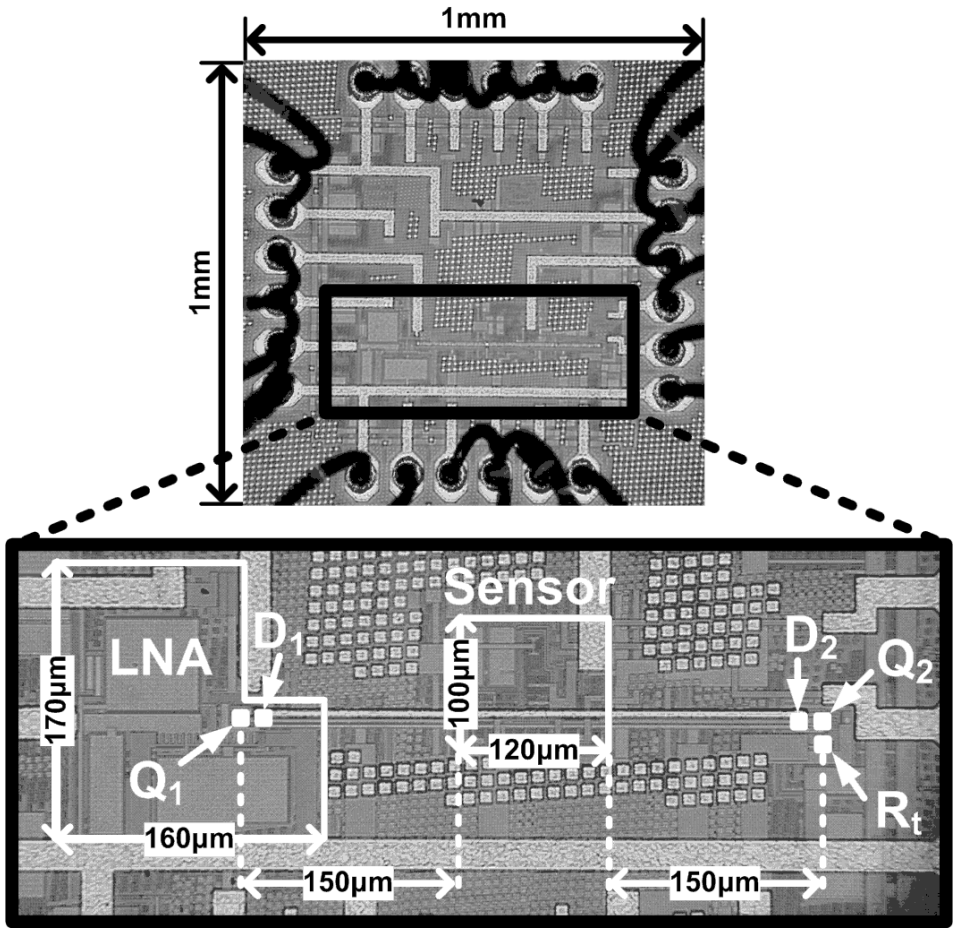
ΔI_o of stage 1 with: I_{cal1} = 0 , I_{cal2} = 100μA

Sensor Specification Overview

- **Sensitivity tuning range**
  - 10mV/mW – 200mV/mW
- **Dynamic range**
  - min. sensitivity setting: 0.2mW to >16mW
  - max. sensitivity setting: 10µW to 12mW
- **Offset compensation**
  - for mismatch & on-chip temperature gradients
  - by tuning I_{cal1} or I_{cal2} from 0-500µA
  - max. sensitivity setting: ±8.2ºC
  - min. sensitivity setting: ±10.6ºC
- **Power consumption** (1.8V supply): 1.1mW



Testchip (0.18µm CMOS)



Layout area:

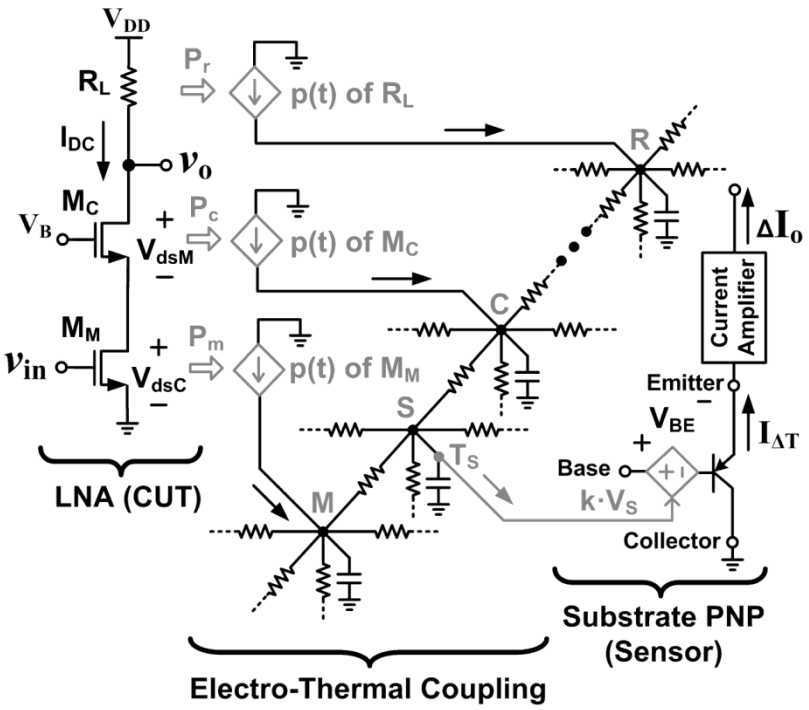
- Sensor circuitry: 0.012mm^2
- Q_1, Q_2: 11µm x 11µm

On-chip low-noise amplifier (LNA):

- Inductor-less (broadband)
- Designed by Mohan Geddada

Broadband LNA on the Testchip

Broadband LNA (Jazz 0.18µm CMOS) designed by Mohan Geddada (Texas A&M University)

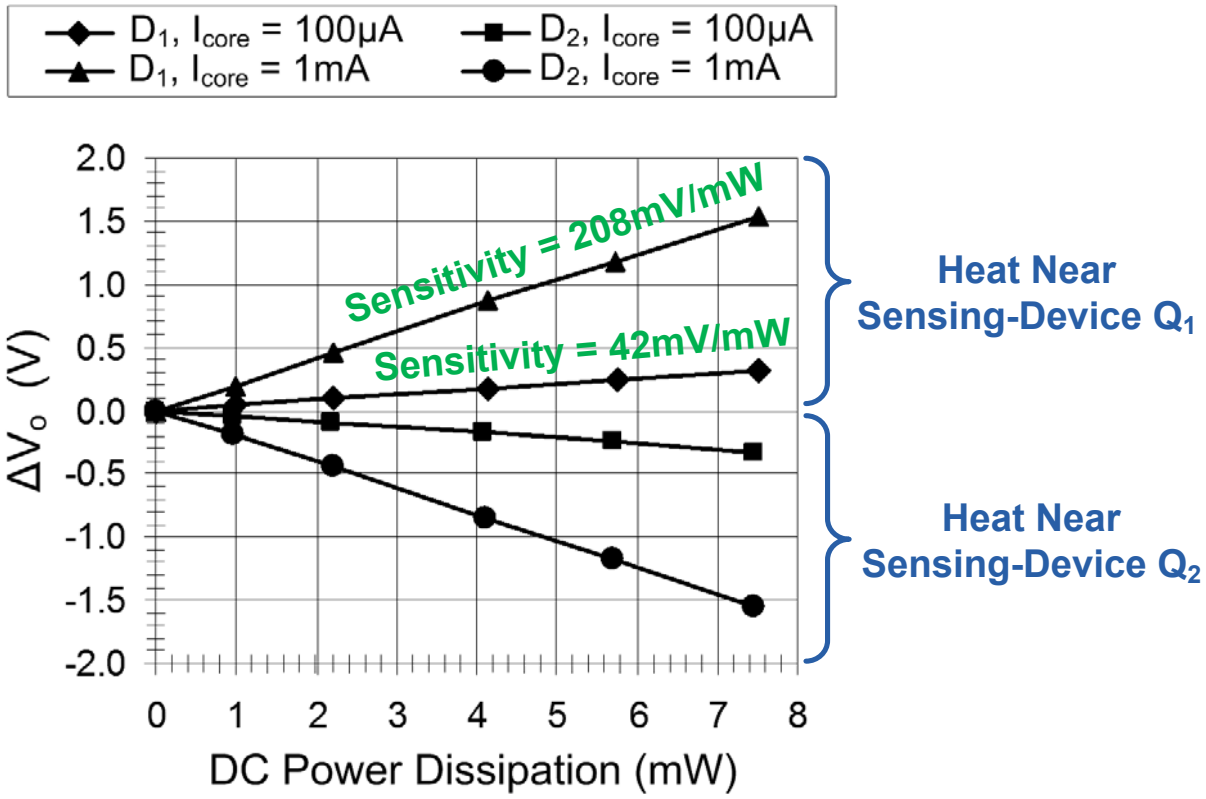


Measured LNA* performance parameters:

Parameter	Value at 1GHz
Gain (S_{21})	-2.3dB**
1-dB Compression Point	0.5dBm
Third-Order Intercept Point (IIP3)	12.0dBm
S_{11}	-6.3dB
S_{22}	-12.7dB
I_{DC}	8.7mA
Technology / V_{DD}	0.18µm CMOS / 2.4V

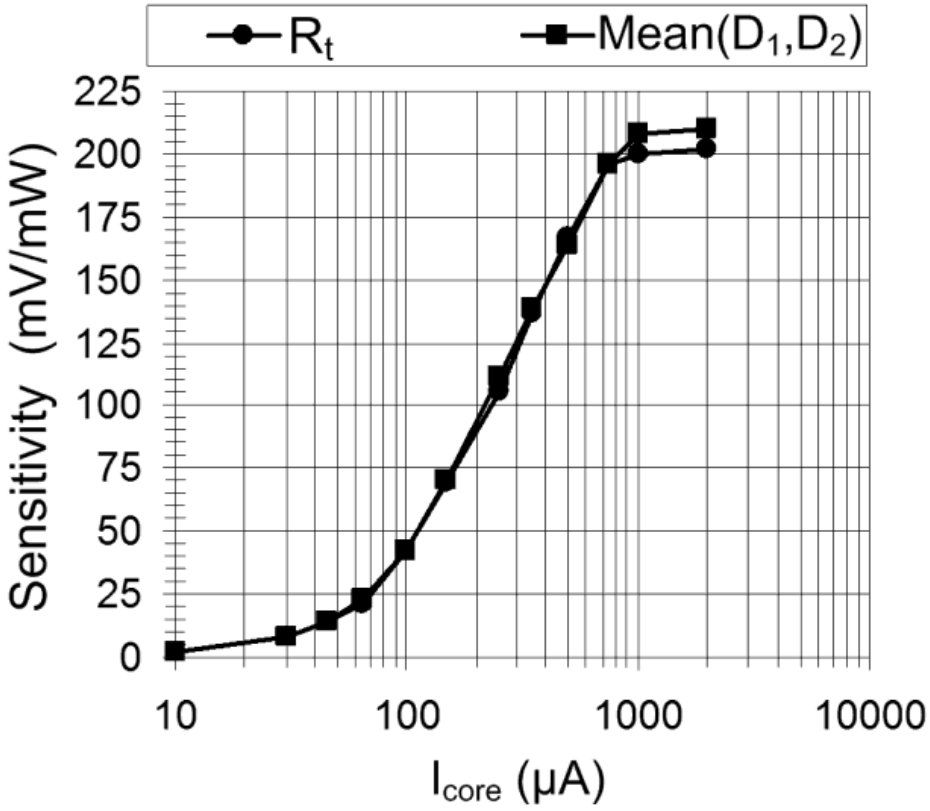
* LNA loaded (without buffer) by a 50Ω analyzer impedance.
** Reduced due to the external 50Ω load in addition to the on-chip load resistor (R_L) and due to S_{11} degradation from packaging/PCB parasitics at 1GHz; S_{21} ≈ 0dB up to 500MHz.

Measurements: Sensor Characterization



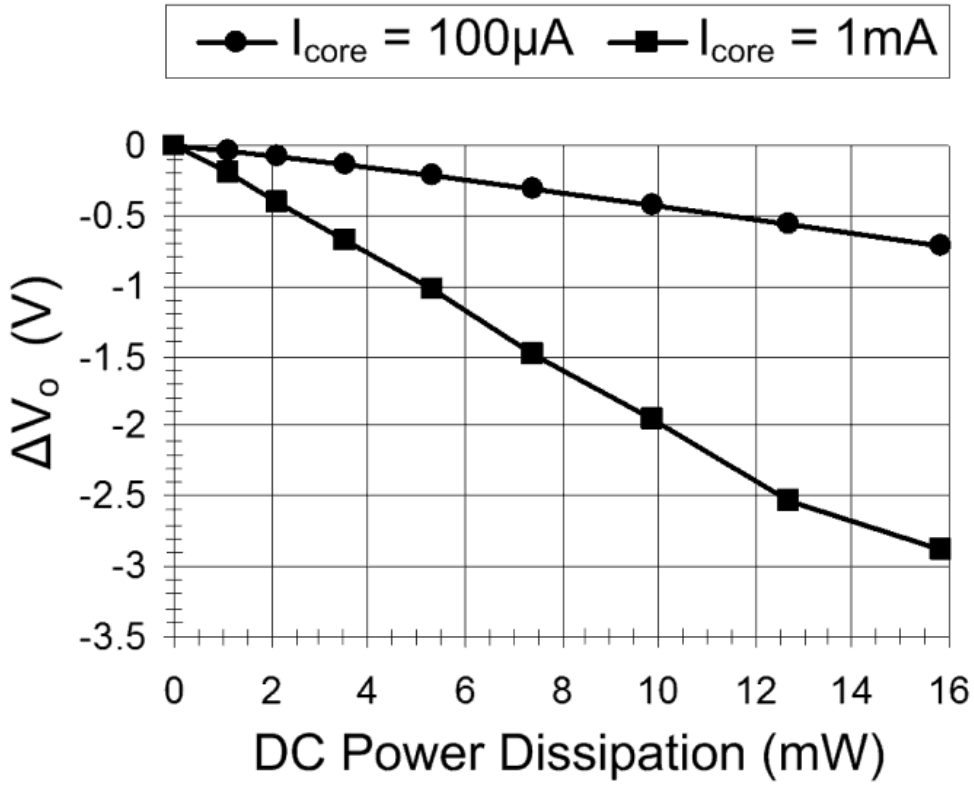
Sensor output vs. power of diode-connected MOS transistors $D_{1,2}$.
Distance between $D_{1,2}$ and $Q_{1,2}$: 4µm.

Measurements: Sensor Characterization (cont.)



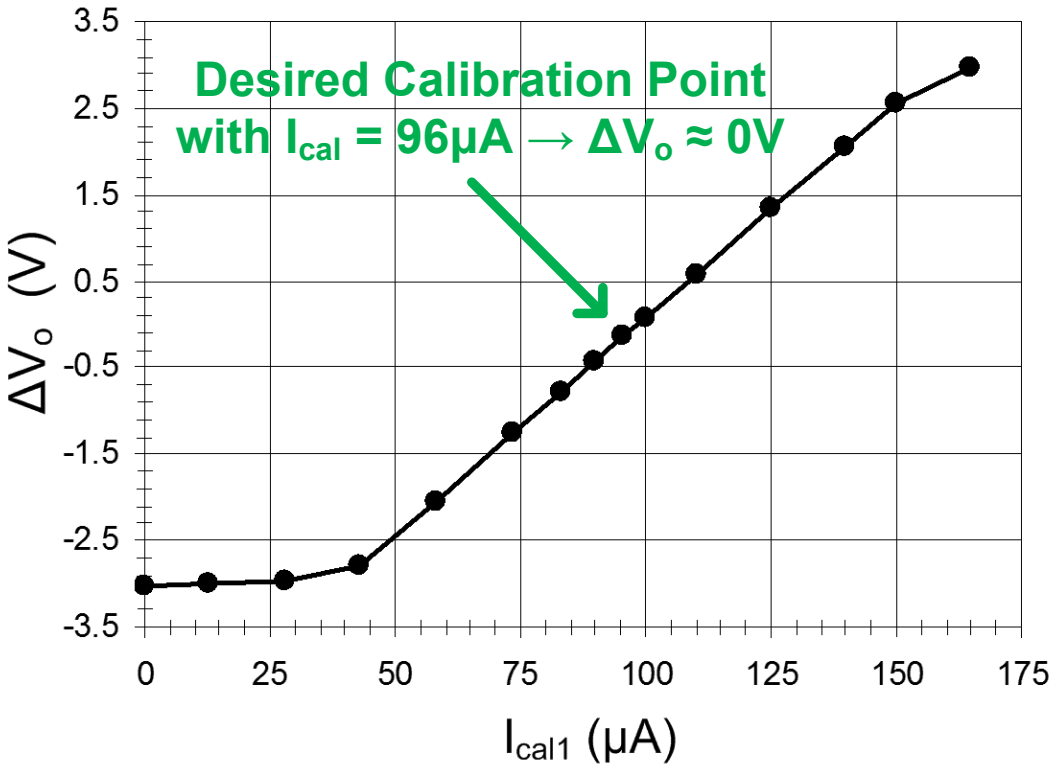
Sensitivity adjustment range: power at R_t and $D_{1,2}$ vs. I_{core}

Measured Dynamic Range



Dynamic Range: sensor output vs. power dissipation
at resistor R_t with I_{core} = 100µA (sensitivity = 41.7mV/mW)
and I_{core} = 1mA (sensitivity = 199.6mV/mW)

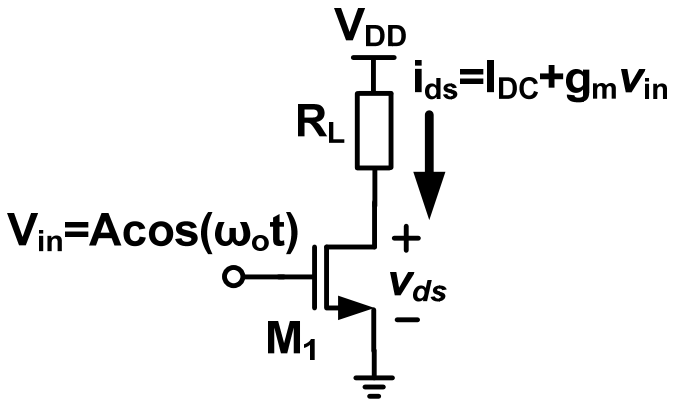
Measurements: Sensor Characterization (cont.)



Offset calibration range

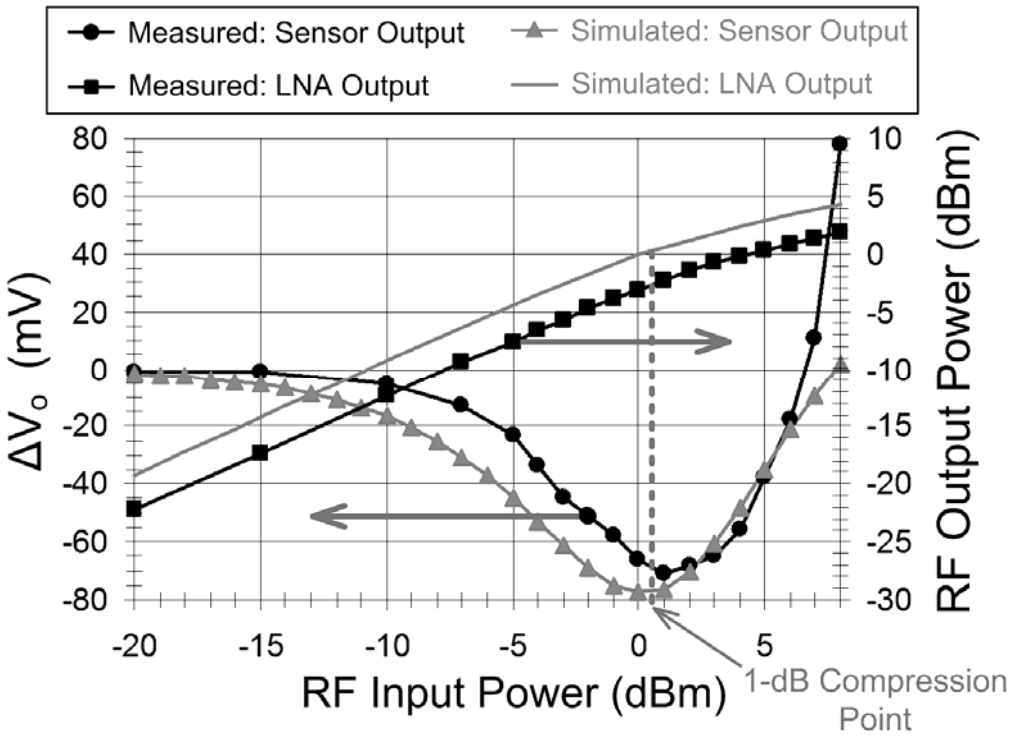
with I_{cal1} (I_{cal2} = 0, I_{core} = 500µA) and 16mW dissipation at resistor R_t
(worst-case imbalance due to process variation and additional temperature gradient)

Practical Calibration Considerations



- Suggested testing sequence:
  1) Sensor calibration → $\Delta V_o = 0V$
  2) Turn-on DC bias of circuits & measure sensor outputs: $(V_{DD}I_{DC} - R_L I_{DC}^2)$
  3) Apply RF signal & measure sensor outputs: $(V_{DD}I_{DC} - R_L I_{DC}^2) - \frac{1}{2}R_L(g_m A^2)$
  4) Extract observables
     - $\frac{1}{2}R_L(g_m A^2)$ from subtraction → RF power gain
     - $(V_{DD}I_{DC} - R_L I_{DC}^2)$ → identify gross failures

Measurements: LNA Testing



1-dB compression point prediction within 1dB error

Measurement vs. simulation comparison:
LNA 1-dB compression point characterization curve
and
DC output voltage of the sensor
(set to 167mV/mW sensitivity)

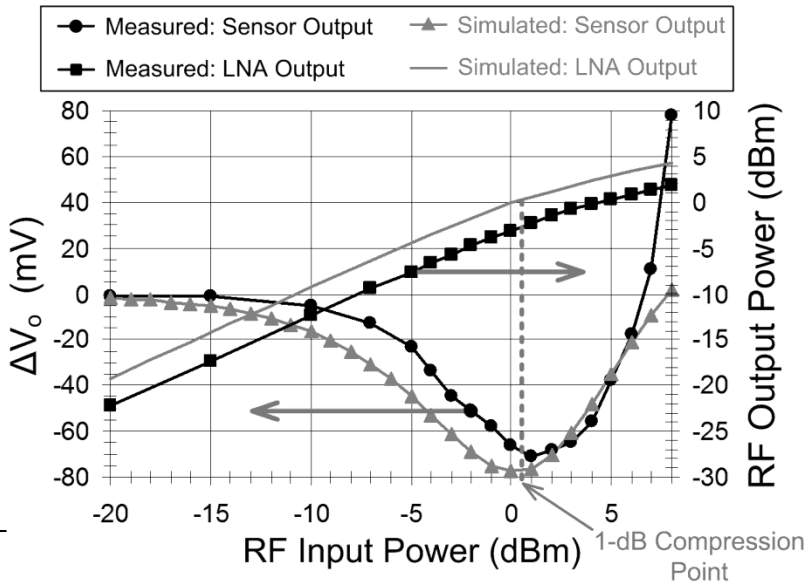
1-dB Compression Point Characterization Details

- The DC temperature change due to the RF signal power depends on non-linearities:

$$P_{DC\rightarrow\Delta T} \approx K_{DC}\cdot\left(\frac{\alpha_2}{2}X^2\right)-\frac{1}{2}K_{AC}\cdot\left(\alpha_1 X-\frac{3}{4}|\alpha_3|X^3\right)$$

where:

- X is the input signal amplitude
- α_1 is the linear transconductance with non-linearity coefficients α_2 and α_3
- K_{DC}, K_{AC} are constants assuming weakly non-linear operation



- The minimum occurs at:

$$X_{min} = \frac{-\alpha_2(K_{DC}/K_{AC})+\sqrt{\alpha_2^2(K_{DC}/K_{AC})^2+\frac{9}{4}\alpha_1|\alpha_3|}}{\frac{9}{4}|\alpha_3|}$$

- Relationship to the 1-dB compression amplitude (x-axis shift):

$$shift_{min[1dB]} = 10\log\left(\frac{X_{min}^2}{X_{1dB}^2}\right)$$

Temperature Sensing: Summary

- Proposed temperature sensor topology for built-in testing
  - Can serve as RF power detector without connection to the signal path
  - Wide dynamic range enables the measurement of RF power components at DC and power dissipation from DC bias circuitry
  - Implemented with substrate PNP devices in standard CMOS technology

- Experimental results (testchip fabricated in 0.18μm CMOS technology)
  - Verified feasibility of RF signal power measurements
  - Demonstrated the capability to measure linearity characteristics (1-dB compression point) of an on-chip RF amplifier

M. Onabajo, J. Altet, E. Aldrete-Vidrio, D. Mateo, and J. Silva-Martinez, "Electro-thermal design procedure to observe RF circuit power and linearity characteristics with a homodyne differential temperature sensor," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 58, no. 3, pp. 458-469, March 2011.

Outline – Lecture 3

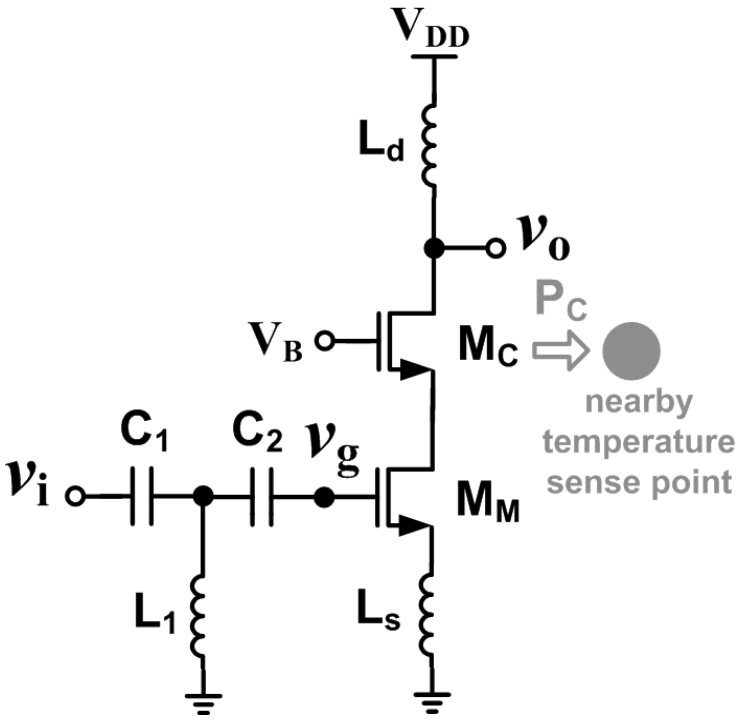
- On-chip DC and RF power measurements with differential temperature sensors
- Case study: differential temperature sensor design
- Temperature sensors as variation monitors
- Mismatch reduction for transistors in high-frequency differential analog signal paths
- Example: mixer design with analog tuning for transistors biased in weak inversion

Variation Monitoring with Temperature Sensors

Acknowledgement:

Thanks to **Didac Gómez**,
Eduardo Aldrete-Vidrio, **Josep Altet**,
and **Diego Mateo** for providing the following
simulation and measurement results.

CUT for Variation-Monitoring Assessments



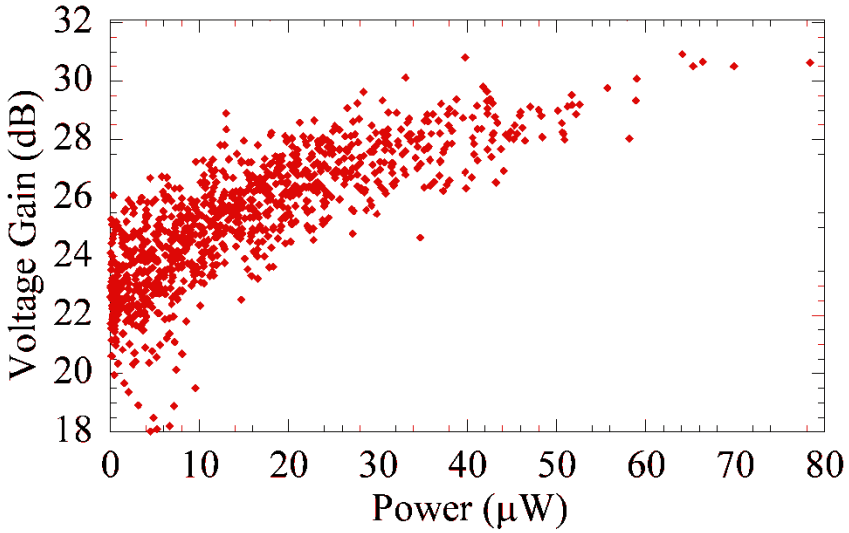
Common-source LNA with T-matching network

Specification	Value at 2.45GHz
Voltage Gain (v_o/v_i)	25.9dB
1-dB Compression Point	-15.4dBm
IIP3	-3.2dBm
S_{11}	-17.6dB
NF	4.5dB
Power	0.42mW
Technology / V_{DD}	65nm CMOS / 1.2V

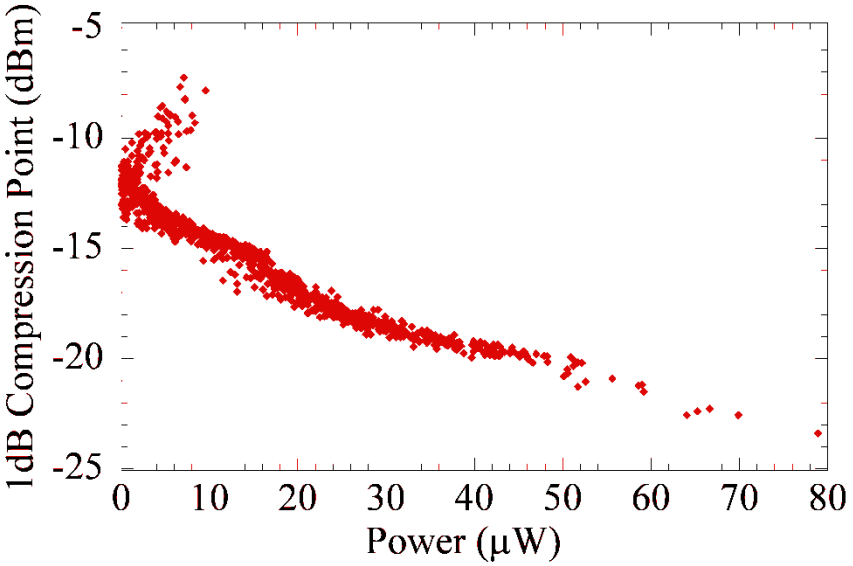
- Power dissipation is monitored at the cascode transistor M_c
  - Larger drain-source voltage swing than transistor M_M, but the same DC and AC current
  - Higher power dissipation at M_C compared to M_M in this CUT

Simulated Correlations betw. Specification and Power

- 1000 Monte Carlo runs
- Gain vs. DC power dissipation at M_C →
  - Due to the RF test signal only
  - DC bias power excluded (assumes completed calibration)



- 1-dB compression point vs. DC power dissipation at M_C →
  - Due to the RF test signal only
  - DC bias power excluded

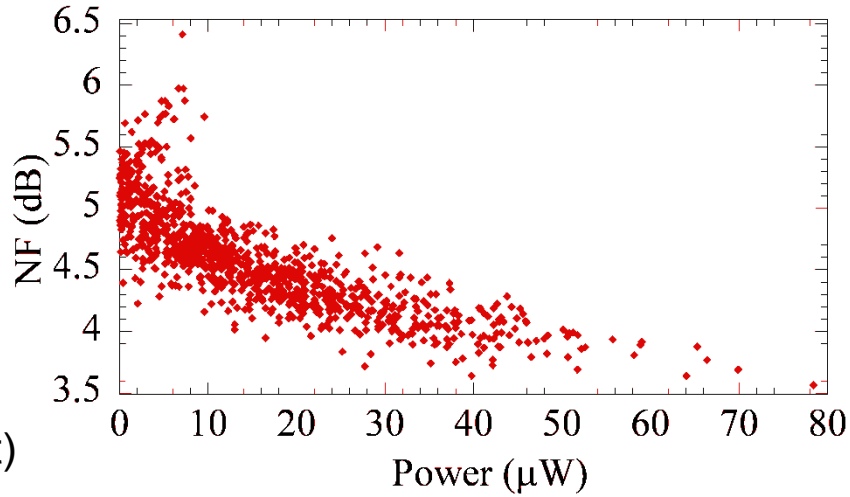


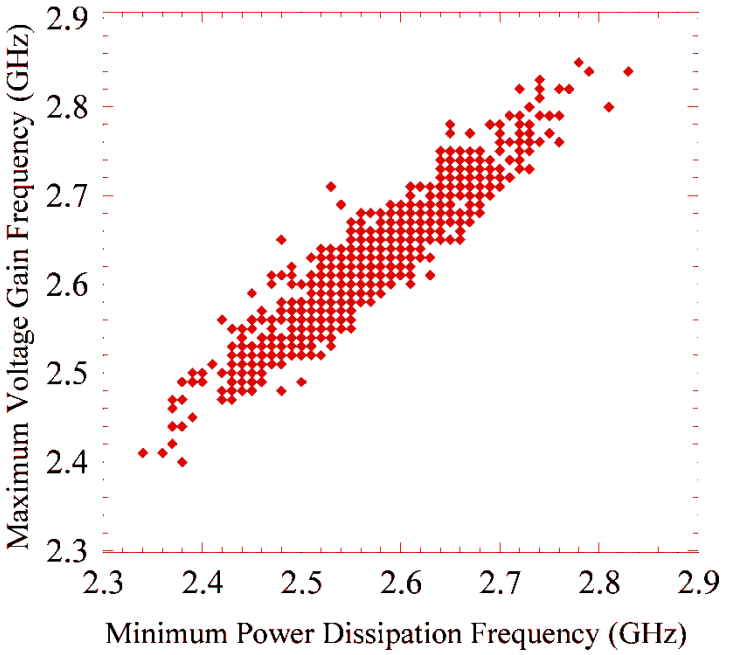
- Required power detection range: 5-80μW
  - Feasible with a diff. temperature sensor

Simulated Correlations betw. Specification and Power

- Noise Figure vs. DC power dissipation at M_C →
  - Due to the RF test signal only
  - DC bias power excluded

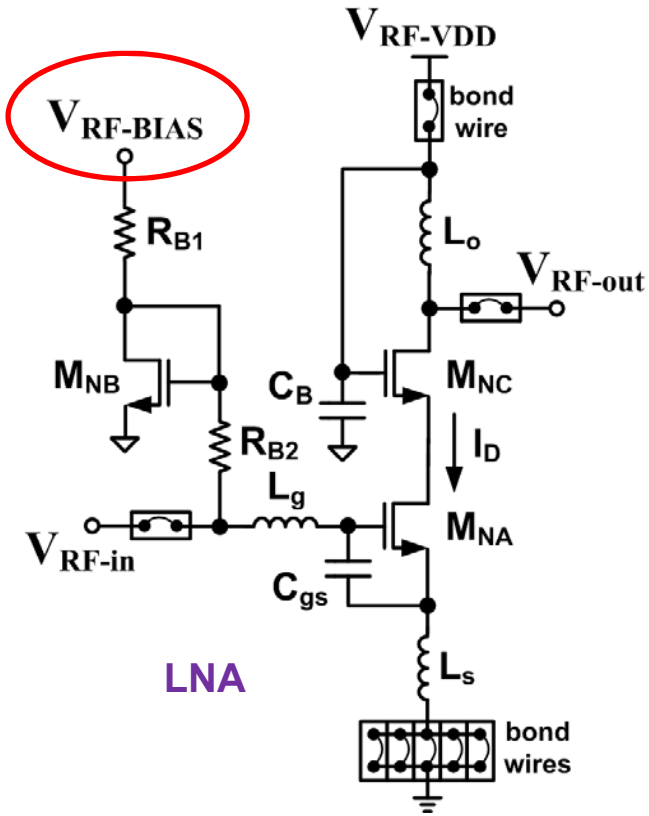
- Thermal tendency analysis
  - Defined as the temperature evolution when a parameter is swept (i.e., frequency of the input)
  - Relative min. or max. temperature point is extracted through multiple measurements
    → exact value of the sensor sensitivity does not have to be known
    → more robust to process variations
  - Relaxes the sensor design requirements
  - Example:
- Simulated LNA center frequency vs. frequency with minimum DC power dissipation →



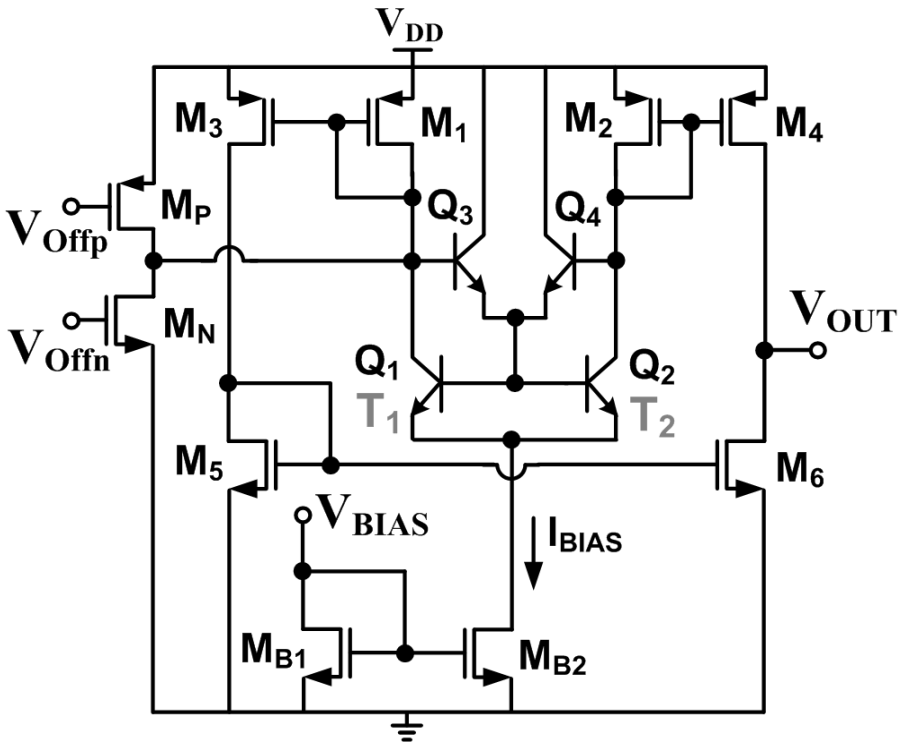


Experimental Evaluation

- LNA with sensor fabricated in 0.25μm CMOS
- Change of DC bias voltage ($V_{RF\text{-}BIAS}$) to induce specification variations due to different bias points: A = 3.3V, B = 2.6V, C = 2.0V



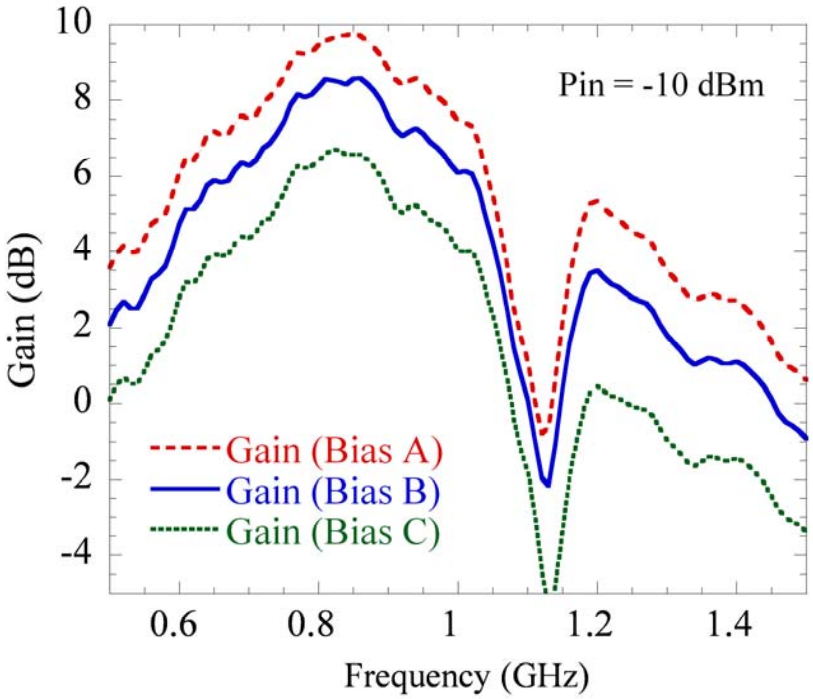
LNA



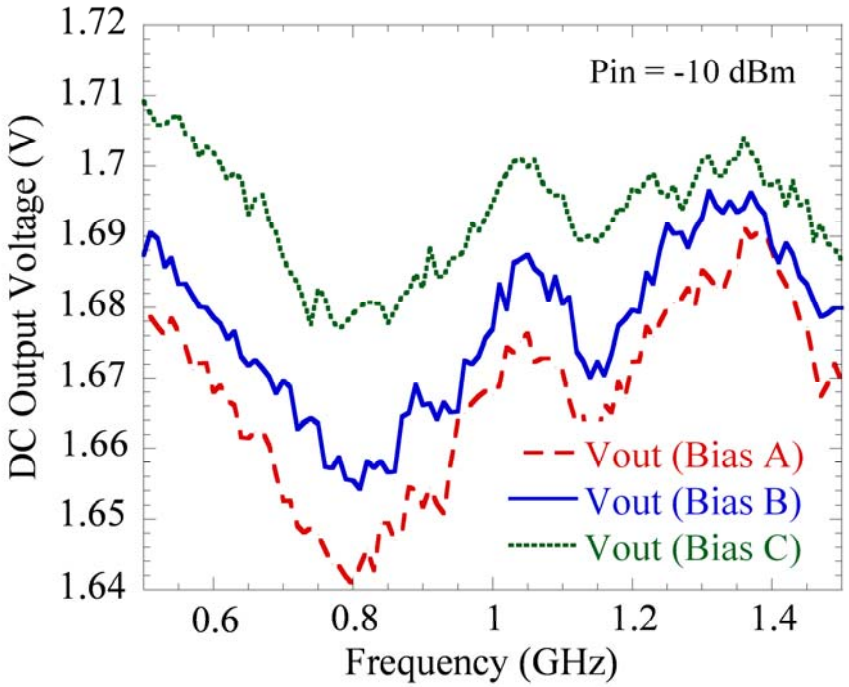
Temperature Sensor

Measured Correlations

- Bias points
  - **A**: I_D = 10.59mA, Gain = 9.79 dB@850 MHz
  - **B**: I_D = 8.05mA, Gain = 8.56 dB@850 MHz
  - **C**: I_D = 5.80mA, Gain = 6.58 dB@850 MHz
- The min. sensor output matches with the max. gain in the LNA's frequency response:

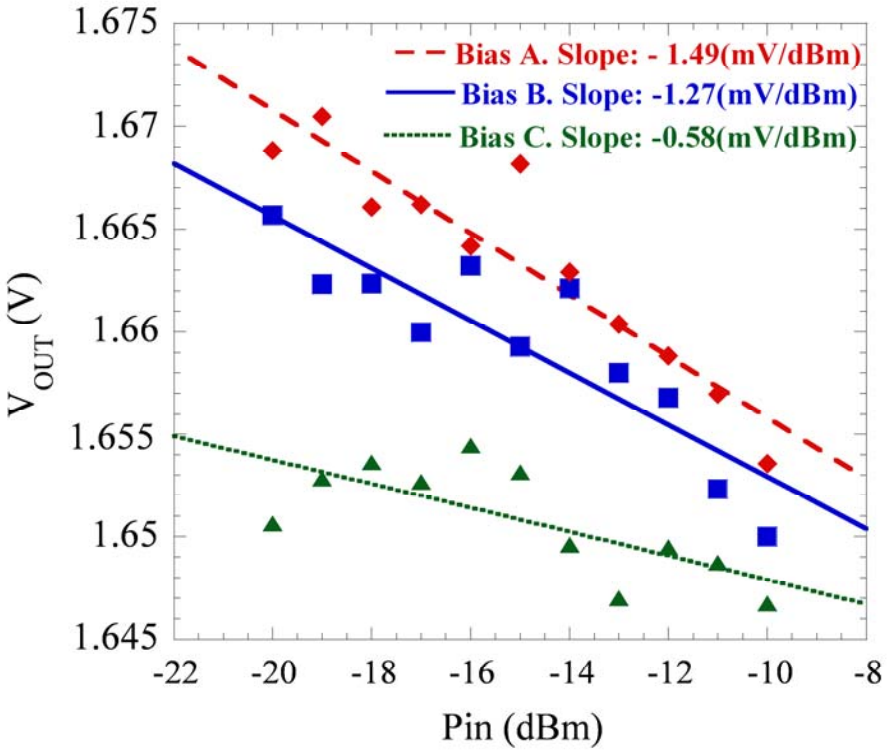


LNA frequency response
(conventional measurement)



DC output of the temperature sensor vs. frequency of the LNA's RF input

Measured Correlations



DC output of the sensor vs. LNA input power
(test tone frequency = 800MHz)

- Gain = slope of the linear approximation for the measured sensor outputs
- Scattering of data points
  - Due to interferences (DC temperature fluctuations)
  - Less severe with higher input power levels
  - Immunity to noises improves with the heterodyne approach

Variation Monitoring: Summary

- Performance variations can be observed with an on-chip temperature sensor
  - Homodyne approach → DC output voltage
  - Voltage gain prediction accuracy ≈ ±2dB
  - Thermal tendency accuracy (e.g., 1dB compression point) ≈ ±1dB
- Thermal sensing is a non-influential variation-monitoring method
  - No connection to the CUT
  - Multiple small substrate PNP devices (sensors) could be multiplexed to a single core to minimize area overhead

M. Onabajo, D. Gómez, E. Aldrete-Vidrio, J. Altet, D. Mateo, and J. Silva-Martinez, "Survey of robustness enhancement techniques for wireless systems-on-a-chip and study of temperature as observable for process variations," *Springer J. Electronic Testing: Theory and Applications*, vol. 27, no. 3, pp. 225-240, June 2011.

Outline – Lecture 3

- On-chip DC and RF power measurements with differential temperature sensors
- Case study: differential temperature sensor design
- Temperature sensors as variation monitors
- Mismatch reduction for transistors in high-frequency differential analog signal paths
- Example: mixer design with analog tuning for transistors biased in weak inversion

Mismatch Reduction for Transistors in High-Frequency Differential Analog Signal Paths

Team at Texas A&M University:

Marvin Onabajo
Jose Silva-Martinez

Transistor Mismatch Reduction

- Target applications
  - Differential RF circuits → mismatch reduction to improve IIP2 performance
    - Examples:
      - Direct down-conversion mixers
      - Differential broadband LNAs
  - Alternative for digitally-assisted approach when:
    - Minimal on-chip digital measurement & calibration resources are available
  - Supplement to digitally-assisted calibration
    - Fast analog coarse calibration at start-up (within microseconds)

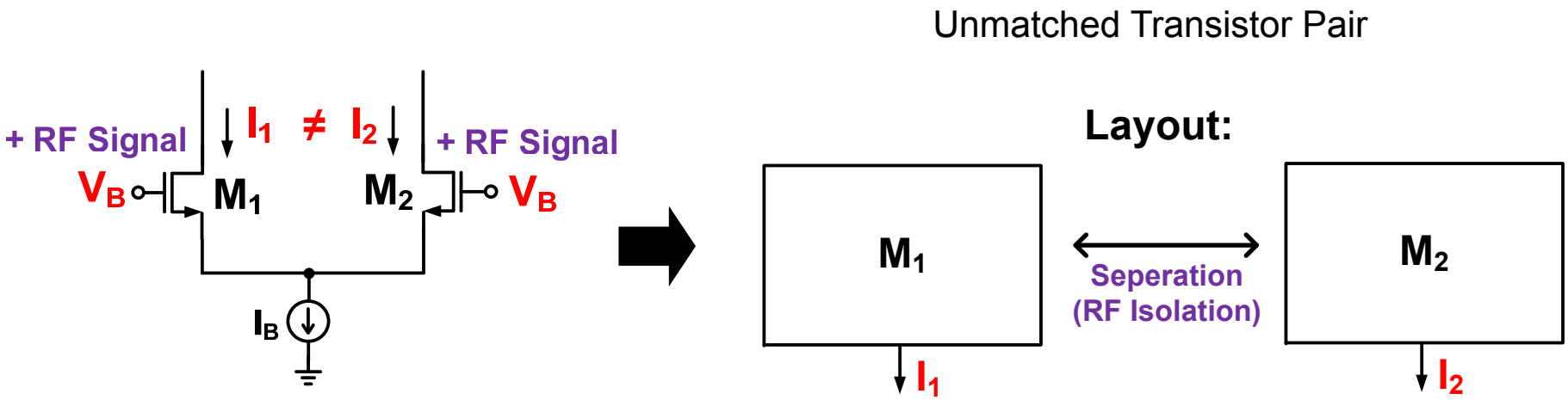
M. Onabajo and J. Silva-Martinez, "Mismatch reduction technique for transistors with minimum channel length," *Analog Integrated Circuits and Signal Processing*, vol. 70, no. 3, pp. 429-435, March 2012.

Mismatch Calibration with an Analog Control Loop

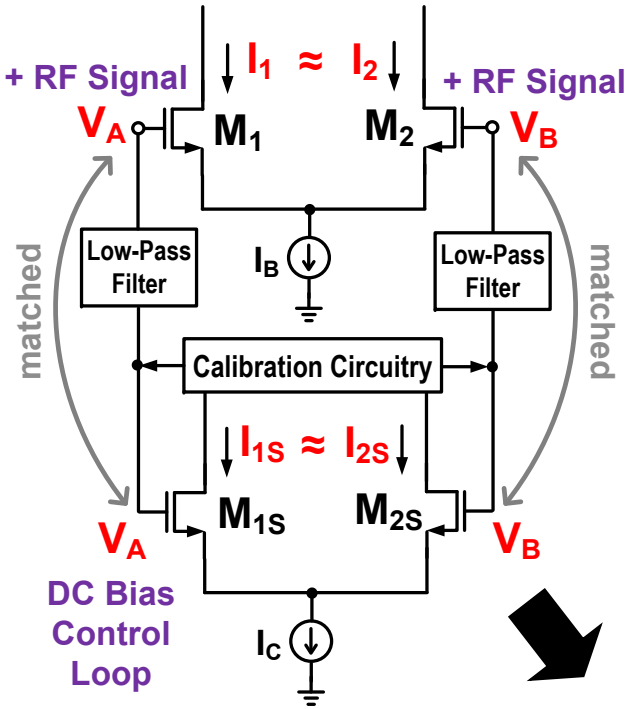
- Conventional approaches to reduce variations are opposing design objectives
  - Increased transistor lengths → Larger parasitic capacitances
    → worse high-frequency operation
  - Layout matching techniques (e.g. interleaved or common-centroid styles)
    → More high-frequency coupling (cross-talk)
    - Parasitic capacitances of crossing metal lines
    - Leakage through the substrate due to the proximity of the devices

- Proposed approach
  - Indirect matching of the transistors under calibration through an analog DC control loop
  - Calibration circuitry is not in the RF signal path
    → Large devices are used to measure the mismatch and to control bias voltages

Typical RF Layout Situation



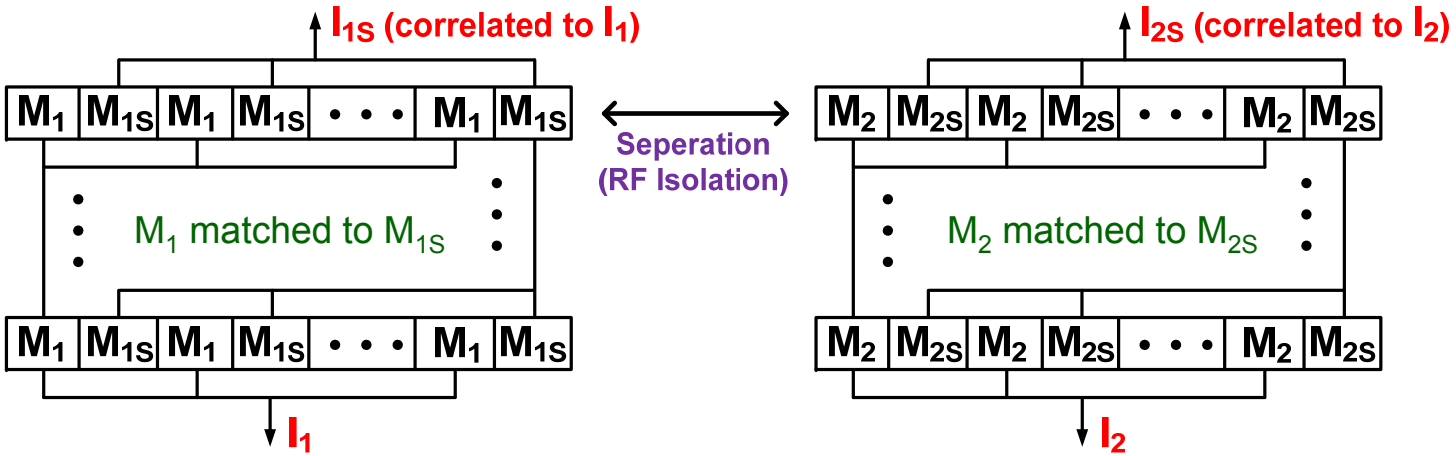
Mismatch Calibration Concept



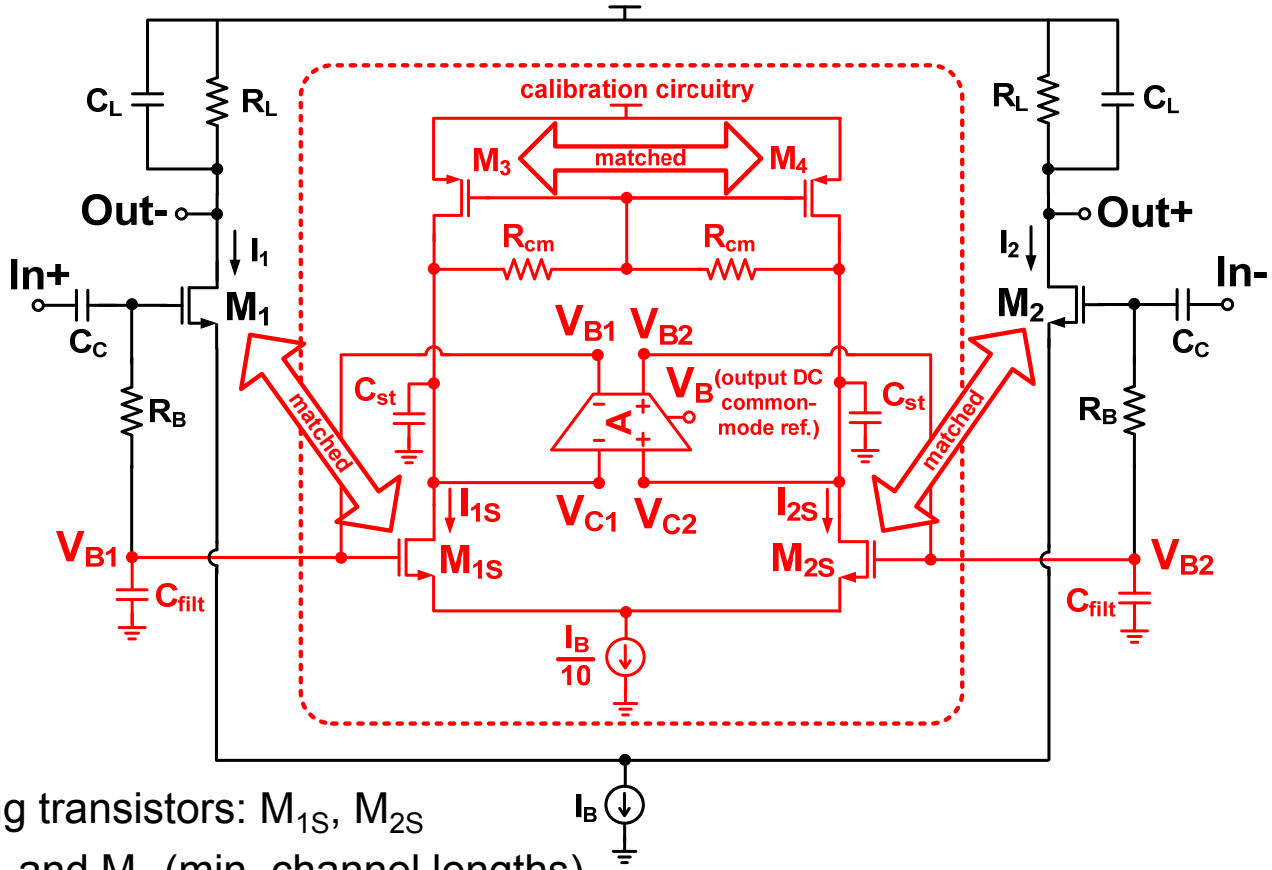
M_1 and M_2 are matched to mismatch-sensing transistors

↓

Layout:



Example: Differential Amplifier



- Mismatch-sensing transistors: M_{1S}, M_{2S}
  - Matched to M_1 and M_2 (min. channel lengths)
    → Coupling through layout parasitics results in small signal loss instead of cross-talk
  - Correlation: $I_1 \leftrightarrow I_{1S}$, $I_2 \leftrightarrow I_{2S}$
    → In a matched pair with N fingers, the standard deviation of the threshold voltage difference ($\sigma_{\Delta Vth}$) decreases: $\sigma_{\Delta Vth(m)} = \sigma_{\Delta Vth}/\sqrt{N}$

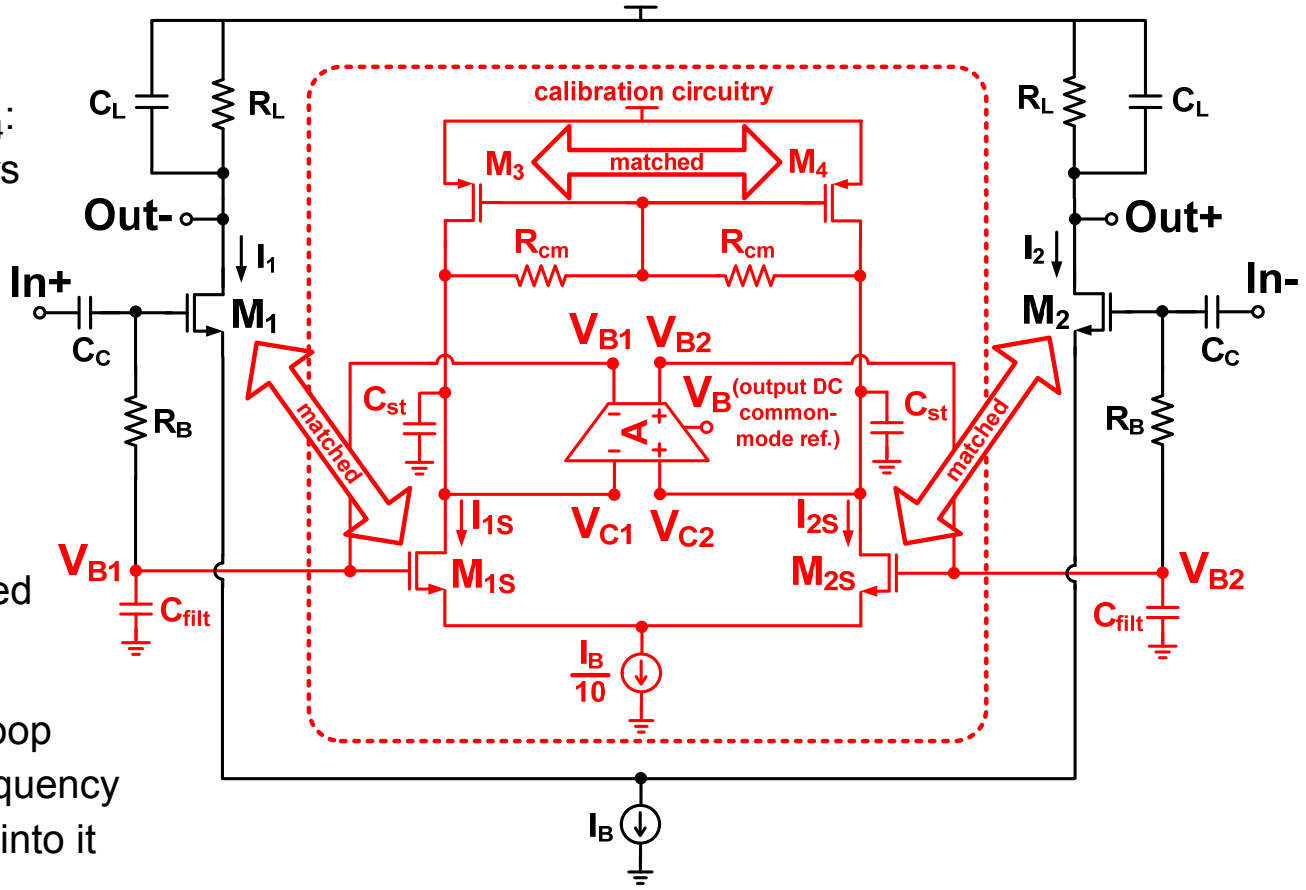
Example: Differential Amplifier (cont.)

- Current I_{S1} and I_{S2} are compared at nodes V_{C1} and V_{C2} to determine mismatch
  - Large transistor dimensions of M_3, M_4, and in the amplifier (A) ensure accurate comparison with low offsets

$$\sigma_{\Delta Vth} \propto 1/\sqrt{W \cdot L}$$

  - Ex.: dimensions of M_3, M_4: width = 6.25µm × 8 fingers length = 3.7µm

- Calibration loop
  - The feedback regulates bias voltages V_{B1} and V_{B2} until the difference of currents I_{S1}/I_{S2} is minimized
  - C_{st} and C_{filt} stabilize the loop and filter out any high-frequency signals that might couple into it

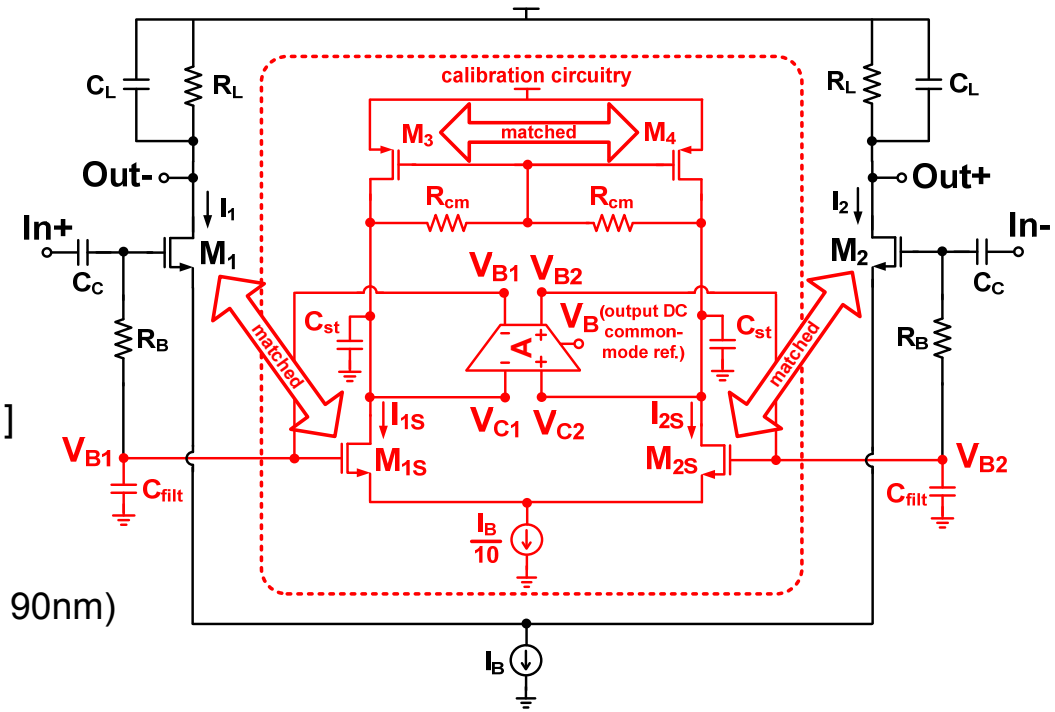


Example: Differential Amplifier Simulation

- Calibration impact on specifications:
  - 15% power increase
  - AC input impedance change < 1%
- Monte Carlo simulations
  - With parameter correlations for matched devices based on the number of fingers [1]

$$1/\sqrt{N} = \sqrt{1 - C_m}$$

  - Ex.: M_1, M_2, M_{1S}, M_{2S} have 20 fingers (L = 90nm) → $C_M = 0.95$

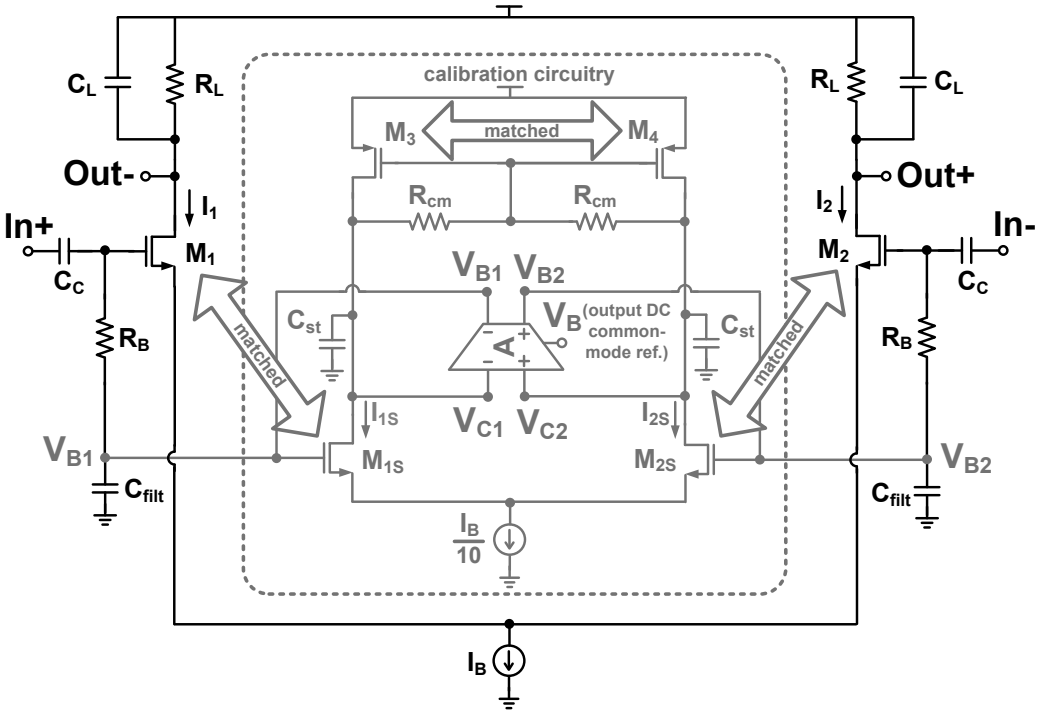


Main Amplifier Parameter	Value
Gain	13dB
-3dB Bandwidth	2.14GHz
AC Input Impedance (over bandwidth)	> 1.77kΩ
Power	1.2mW
Power with Calibration	1.38mW
Technology / Supply	90nm CMOS / 1.2V

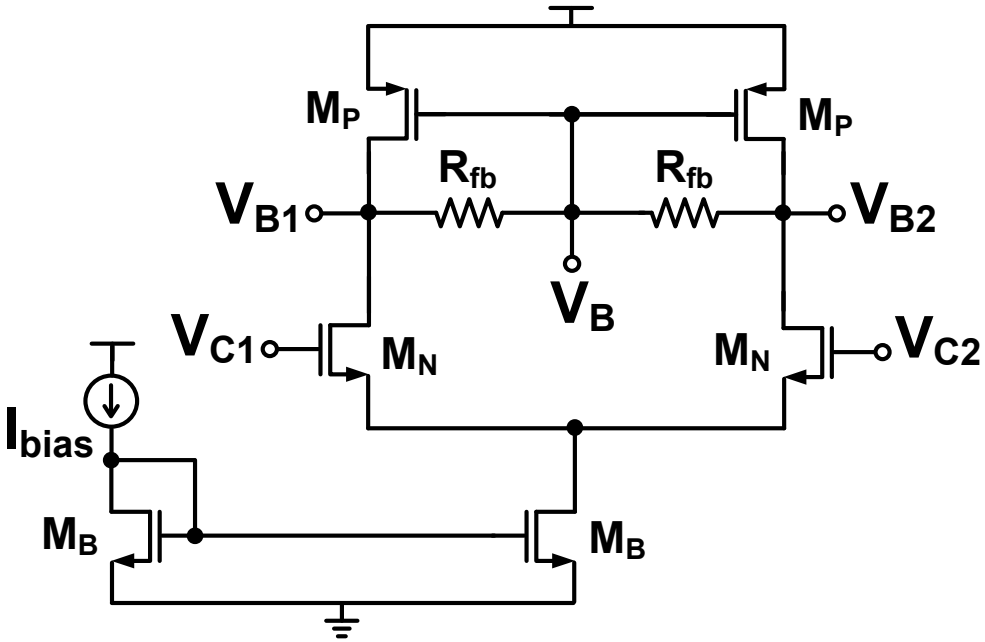
[1] Cadence Design Systems, "Recommended Monte Carlo Modeling Methodology for Virtuoso Spectre Circuit Simulator Application Note", pp. 13-18, Nov. 2003. Available: http://www.cdnusers.org/community/virtuoso/resources/spectre_mcmodelingAN.pdf

Mismatch Reduction: Component Values

Component	Dimensions / Value
M_1, M_2, M_{1S}, M_{2S}	W/L = 90nm × 20 fingers / 90nm
M_3, M_4	W/L = 6.25µm × 8 fingers / 3.7µm
R_L	1.12kΩ (L/W = 9µm / 2µm)
C_L	0.1pF
R_B	100kΩ
C_{filt}	1pF
C_c	5pF
C_{st}	10pF
R_{cm}	100kΩ (L/W = 20 × 10µm / 1µm)
I_B	1mA
Technology	90nm CMOS
Supply Voltage	1.2V



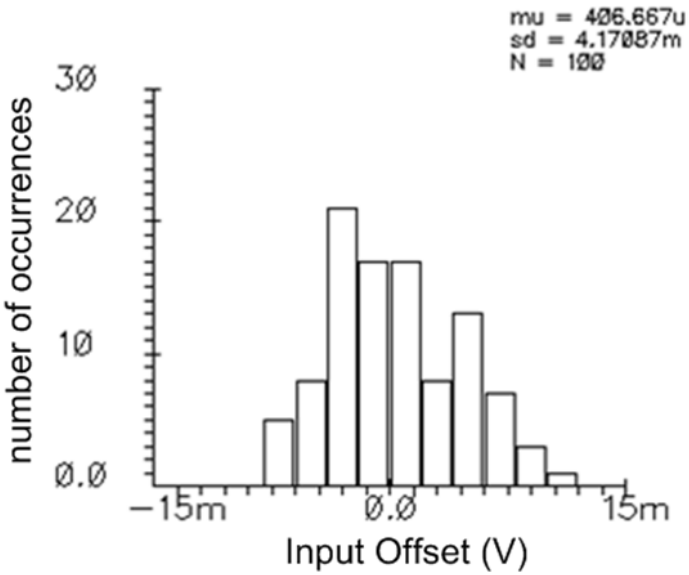
Mismatch Reduction: Amplifier Component Values



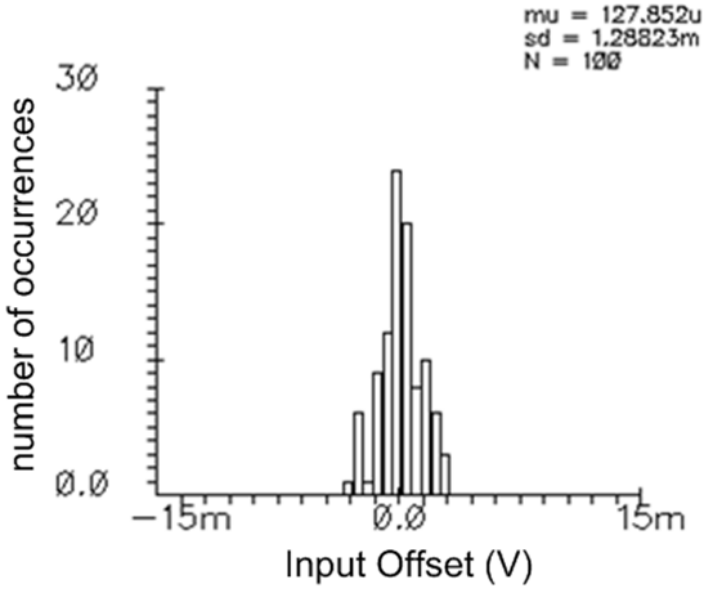
Operational Transconductance Amplifier (A)	
M_N	W/L = 8μm × 4 fingers / 4μm
M_P	W/L = 5μm × 2 fingers / 1.55μm
M_B	W/L = 3μm × 4 fingers / 1μm
R_{fb}	38kΩ (L/W = 8 × 19μm / 1μm)
I_{bias}	50μA

Monte Carlo Simulation Results

- Mismatch reduction with calib. based on M_1/M_{1S} (M_2/M_{2S}) layout with 20 fingers (Cm = 0.95)
  - Input-referred offset voltage reduction: from 4.17mV to 1.29mV
  - Drain current difference (main transistors): 3.1% to 1.0%
- Mismatch reduction if the layout style ensures 1% matching (C_m = 0.99) for M_1/M_{1S} (M_2/M_{2S}) (e.g. common-centroid)
  - Input-referred offset voltage reduction: from 4.17mV to 0.76mV
  - Drain current difference (main transistors): 3.1% to 0.6%



Amplifier input offset
without calibration



Amplifier input offset
with calibration (C_m = 0.95)

Outline – Lecture 3

- On-chip DC and RF power measurements with differential temperature sensors
- Case study: differential temperature sensor design
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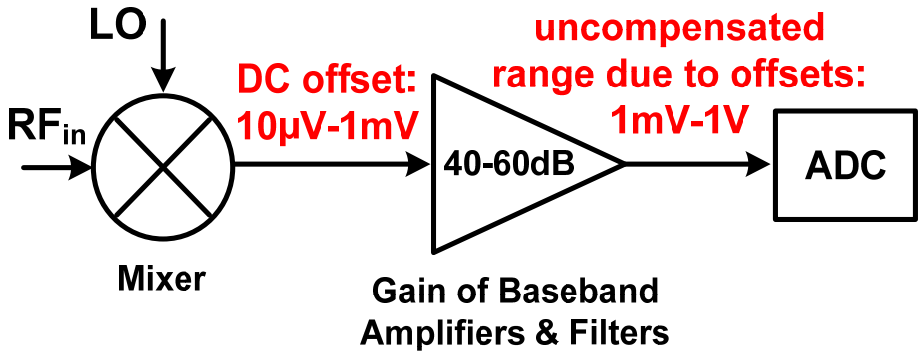
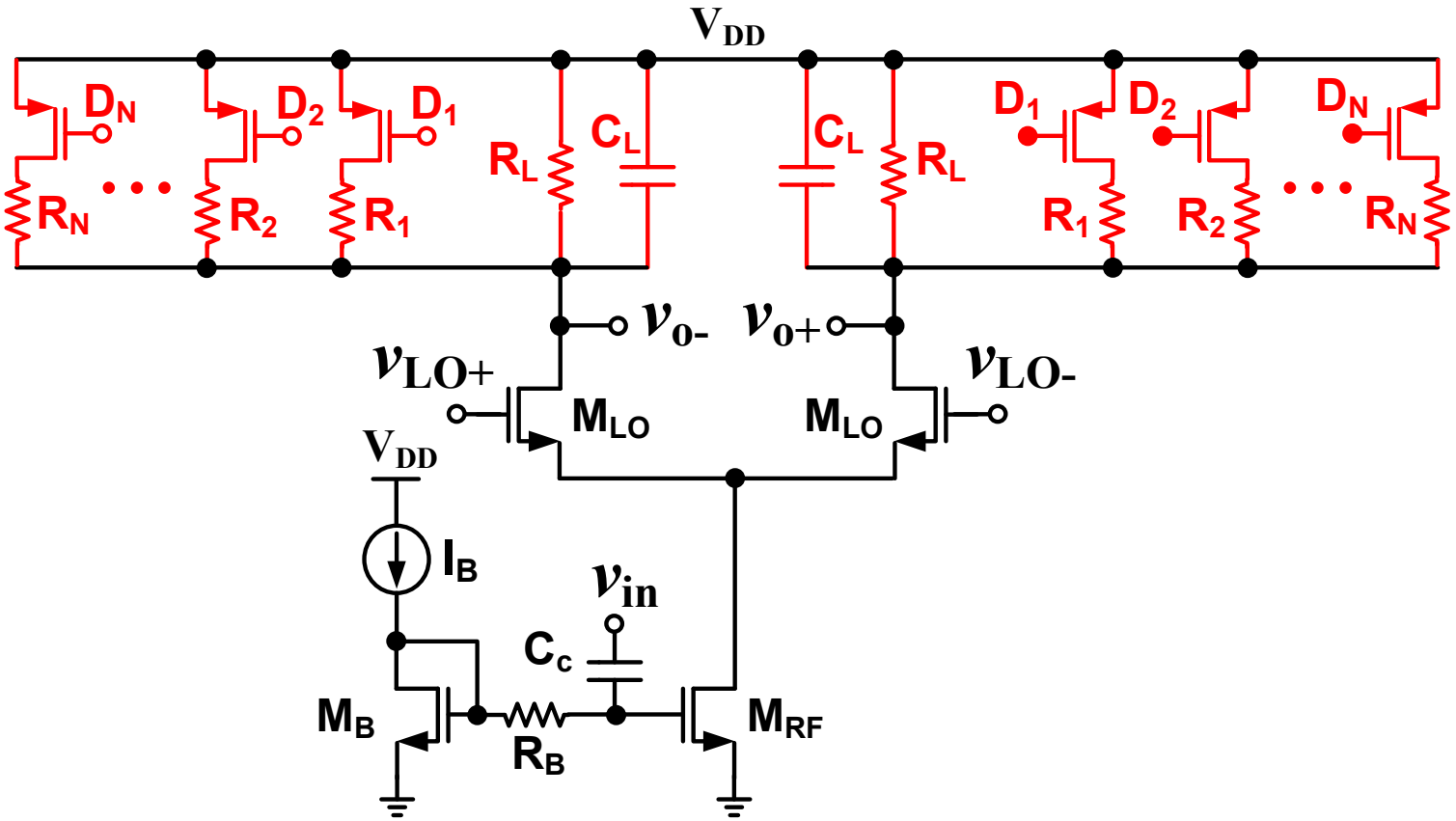
DC Offsets and IIP2



- Mixer 2nd - order intermodulation intercept point (IIP2)
  - Causes:
    - Device mismatches
    - Device non-linearities
    - Self-mixing (coupling between LO and RF ports)
  - Poor IIP2 results in signal distortion and **DC offsets**
    - Offsets after the mixer are amplified by the baseband section
      - Saturation due to limited voltage headroom
      - Increased dynamic range requirements for the baseband circuits and the ADC

Mixer IIP2 Tuning Example



- 5-bit load resistor control with switches D_1-D_N
- Reduced 2nd-order non-linearities due to mismatches
- +60dBm IIP2 (>20dB improvement)

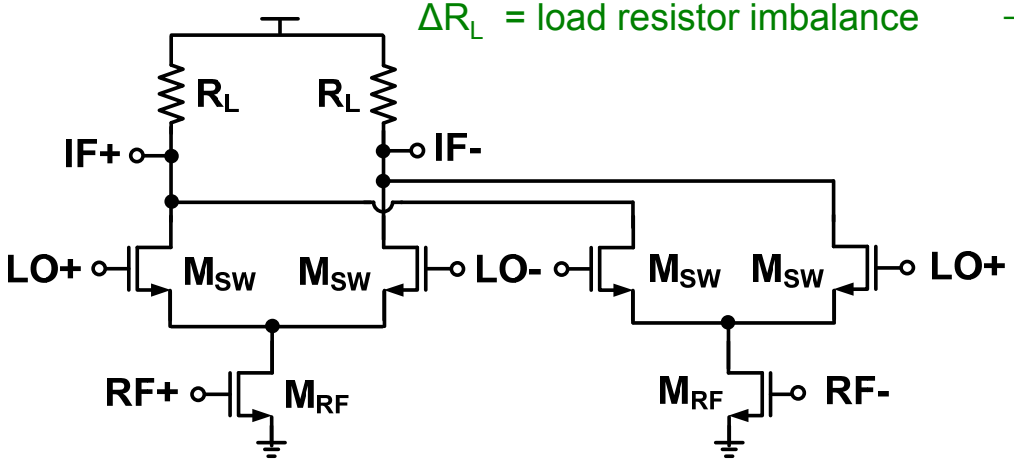
K. Kivekas, A. Parssinen, J. Ryynanen, J. Jussila, and K. Halonen, "Calibration techniques of active BiCMOS mixers," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 766-769, Jun 2002.

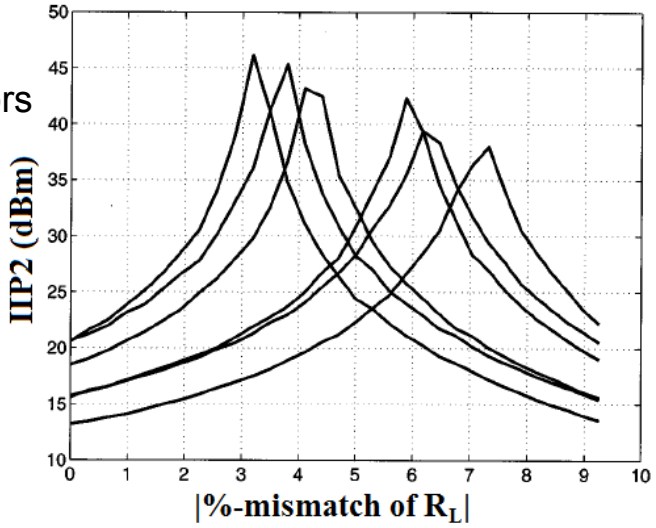
Effects of Device Mismatches on Mixer IIP2 Degradation

- IIP2 of mixers is very sensitive to device mismatches
  → guaranteed IIP2 > 40dBm requires compensation
  - IIP2 for a conventional double-balanced mixer [1]:

$$IIP2 = \frac{\sqrt{2}}{\pi \eta_{nom} \alpha_2} \times \frac{4}{[2 \cdot \Delta\eta(\Delta g_m + \Delta A_{RF})] + \Delta R_L (1+\Delta g_m)(1+\Delta A_{RF})}$$

where: η = LO duty cycle
α_2 = 2nd - order non-linearity coefficient
g_m = transconductance of RF input transistors
ΔA_{RF} = RF amplitude imbalance
ΔR_L = load resistor imbalance →





Example from [2]: measured IIP2 of six receiver samples vs. %-change of mixer load mismatch

[1] M. Hotti, J. Ryynanen, K. Kivekas, and K. Halonen, "An IIP2 calibration technique for direct conversion receivers," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, vol. 4, pp. 257-260, May 2004.

[2] K. Kivekas, A. Parssinen, J. Ryynanen, and J. Jussila, "Calibration techniques of active BiCMOS mixers," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 766-769, June 2002.

IIP2 Degradation with Non-Ideal Switching Transistors

- IIP2 RMS voltage [3]: $$\sigma_{IIP2} = \frac{(2/\pi)\cdot g_m}{\sqrt{L^2\cdot[(\alpha_2^{dif})^2+(\alpha_2^{cm})^2]+(\frac{\Delta R_L}{R_L}\cdot\alpha_2^{cm})^2}}$$

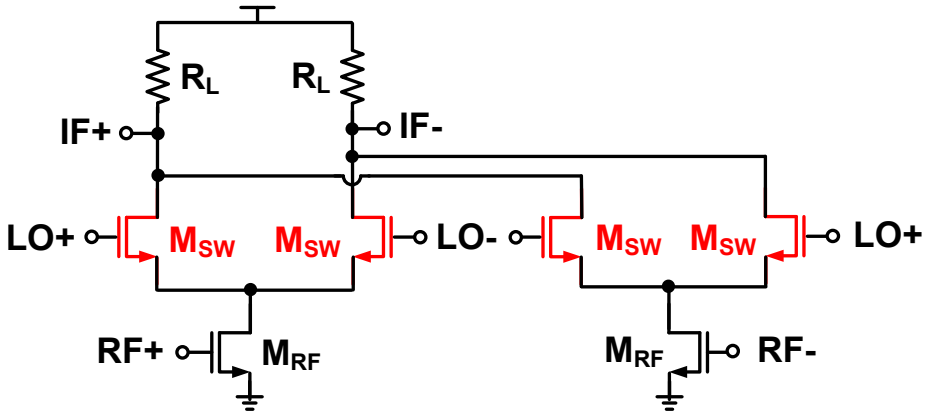
  where: L is a statistically-varying mismatch parameter

  g_m is the transconductance of the RF input transistor M_{RF} with 2nd - order nonlinearity:

  * differential component: α_2^{dif}
  * common-mode component: α_2^{cm}

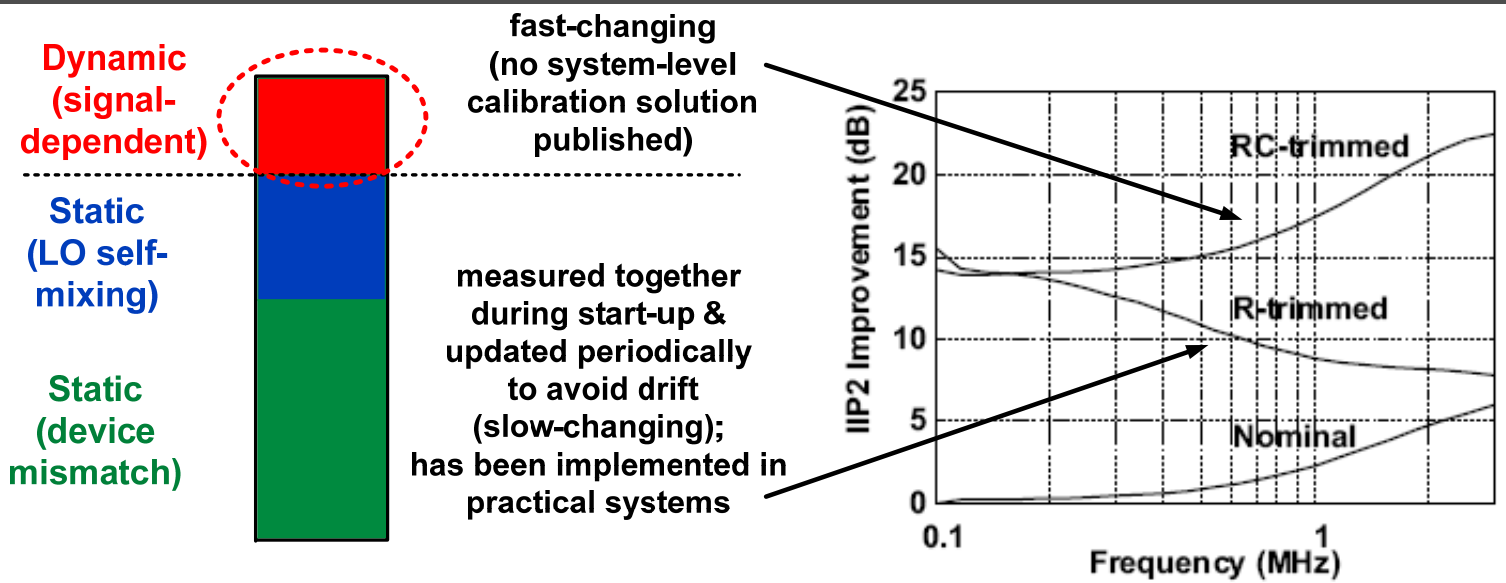
  R_L and ΔR_L are the value of the load resistors and their mismatch

- α_2^{cm} can be suppressed with a common-mode feedback circuit at the IF output
- Mismatch of the LO switching transistors limits the achievable IIP2 through parameter L



[3] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order intermodulation mechanisms in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394- 406, March 2003.

Signal-Dependent DC Offsets in Mixers



Offset contributions and improvement with digital RC-trimming from manually adjusting the load of a standalone mixer (programmable load resistors and capacitors)

- DC offset contributors
  - Static:
    - Device mismatch
    - LO signal imbalance
  - Dynamic:
    - Input signal power and modulation format
    - Frequency-dependent
    - Interference-dependent

Figure from: M. Hotti, J. Ryynanen, K. Kivekas, and K. Halonen, "An IIP2 calibration technique for direct conversion receivers," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, vol. 4, pp. 257-260, May 2004.

Mixer DC Offset Cancellation Considerations

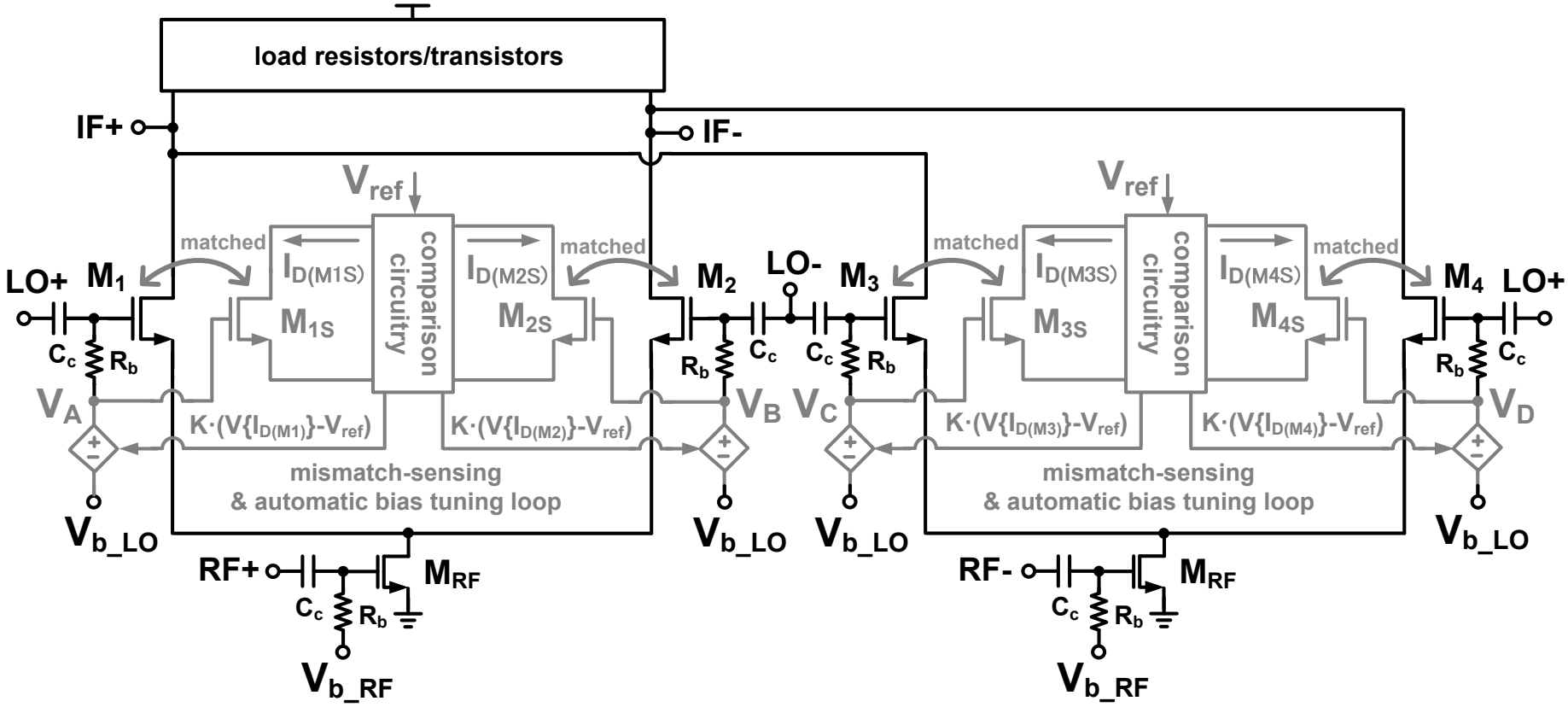
- Complications in wideband multi-standard receivers with dynamic offset cancellation
  - Optimum performance would require digital mixer compensation trimming codes to be updated frequently to cancel dynamic DC offsets
  - Each new DAC setting (e.g. 5-bit trimming codes) will require a new digital performance measurement (BER, FFT, etc.) until the optimum settings have been determined

  → would require much longer & more frequency training sequences than static offset cancellation

- Anticipated improvements/challenges with automatic analog calibration
  - Fast analog feedback loop to cancel dynamic offsets

    → delay will depend only on the loop bandwidth/settling time, not on digital signal processing
  - Must ensure sufficient accuracy (μA-range currents) with PVT variations in the sensing devices

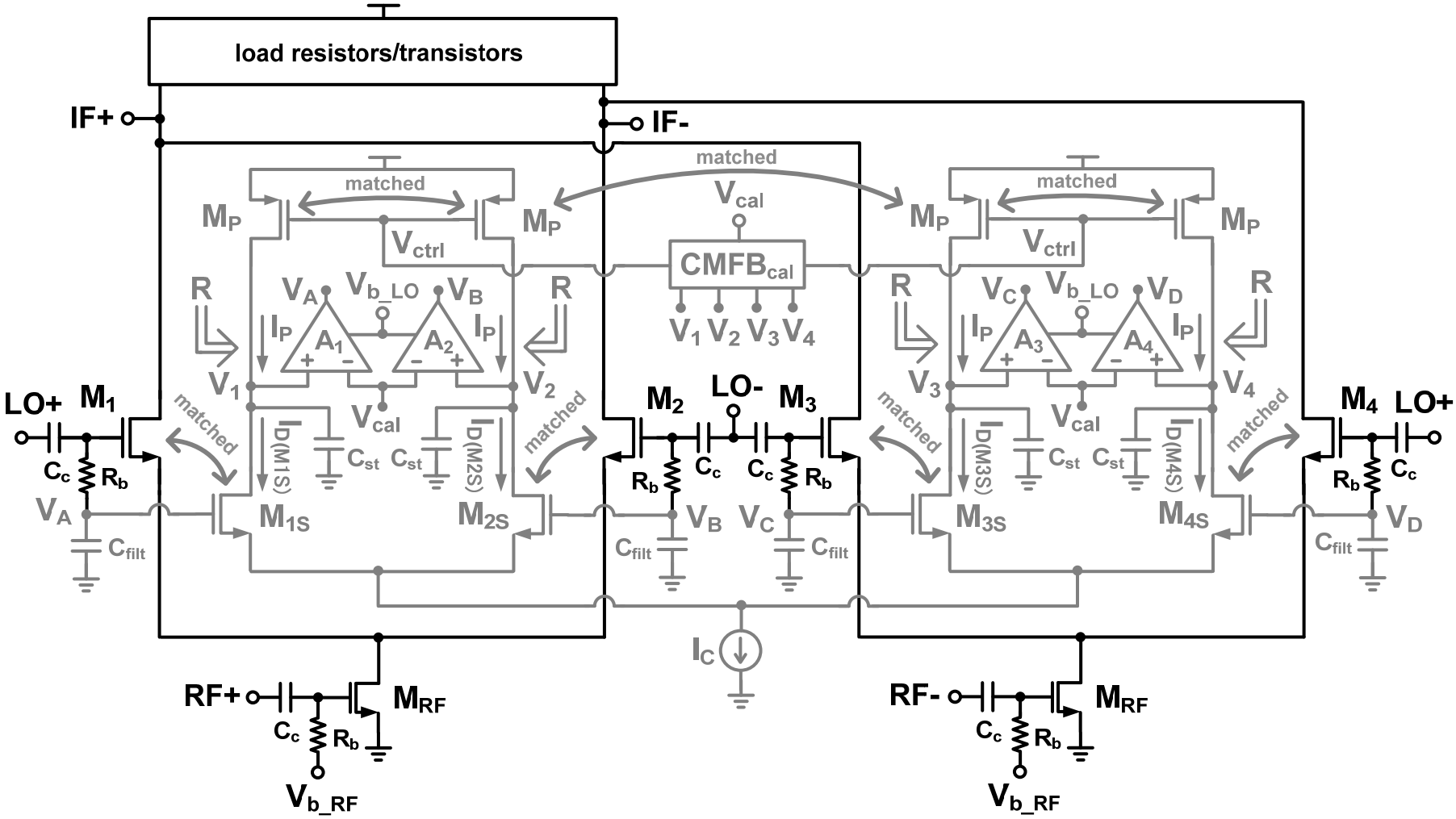
Mismatch Reduction: Application to Mixers



Double-balanced down-conversion mixer with mismatch reduction loops – conceptual view

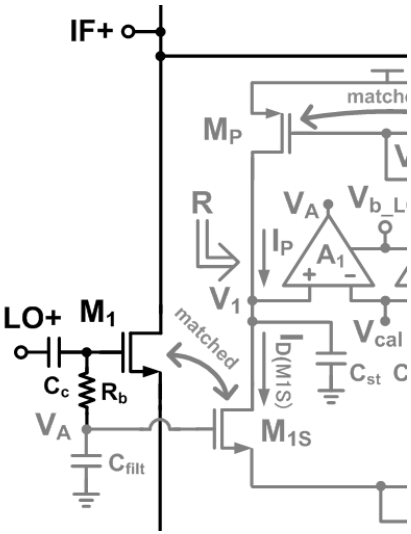
(DC loop gain per branch ≈ 42dB)

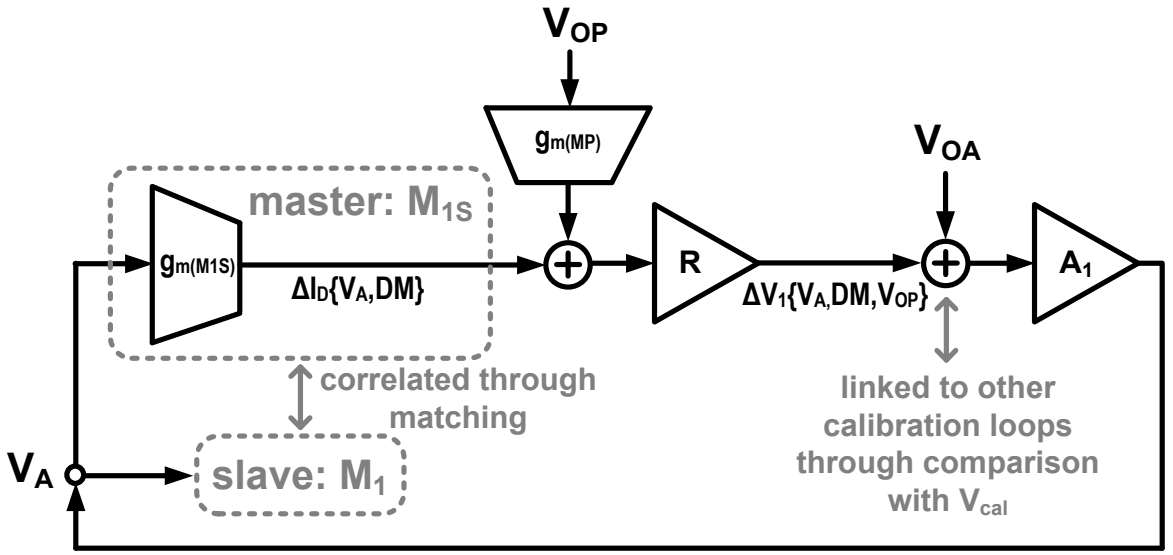
Mismatch Reduction: Application to Mixers (cont.)



Double-balanced down-conversion mixer with mismatch reduction loops – detailed view

Calibration Loop Offsets & Mismatches





DC signal flow diagram for one calibration loop with offsets

- Parasitic capacitances from the large devices are not critical in this DC calibration loop

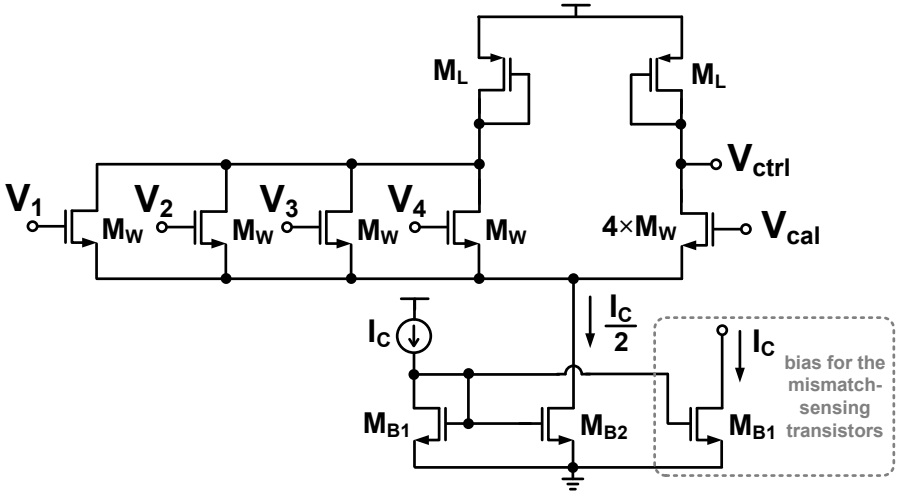
→ Device dimensions can be increased until the simulated offsets are negligible

- Conditions to be met:

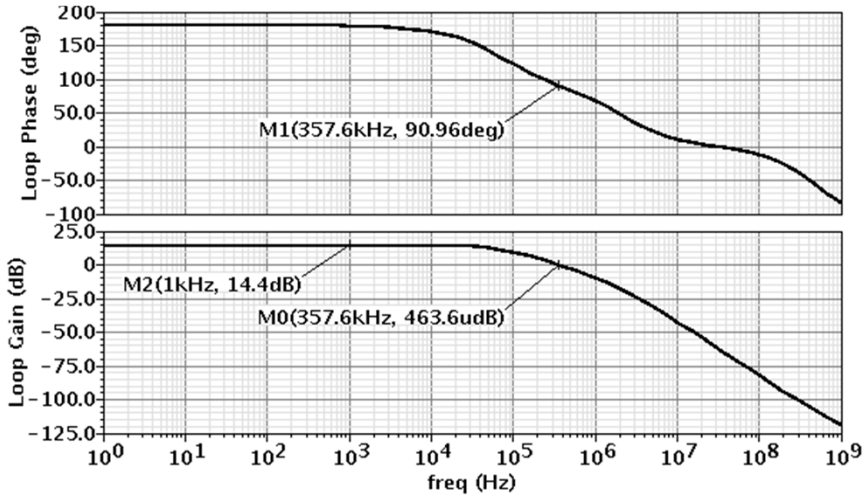
$$V_{OP} << \frac{\Delta I_D\{V_A, DM\}}{g_{m(MP)}} \qquad V_{OA} << \Delta I_D\{V_A, DM\} \times R$$

* $g_{m(M1S)}$ and $g_{m(MP)}$ are representing the transconductance parameters of M_{1S} and M_P
* V_{OP} is the gate-referred offset voltage of M_P, V_{OA} is input-referred offset voltage of amplifier A_1
* Current $\Delta I_{D\{VA, DM\}}$ is the difference of the sensing transistor's drain-source current relative to the mean of the same current in the other branches, which depends on control voltage V_A and the device mismatches (DM)
* R represents the resistance looking into the node at the drains of M_{1S} and M_P

Mixer Calibration Loop Circuits

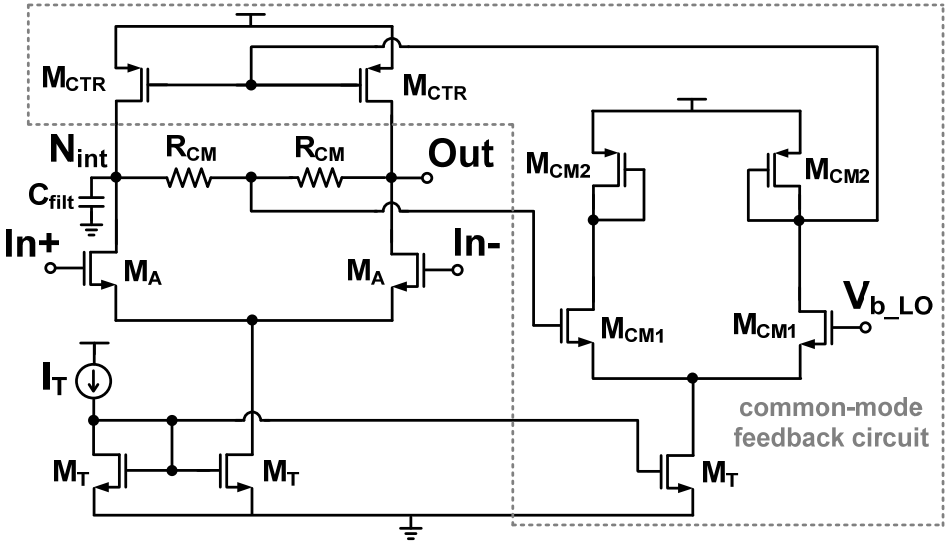


Common-mode feedback circuit (CMFB) for the calibration loop

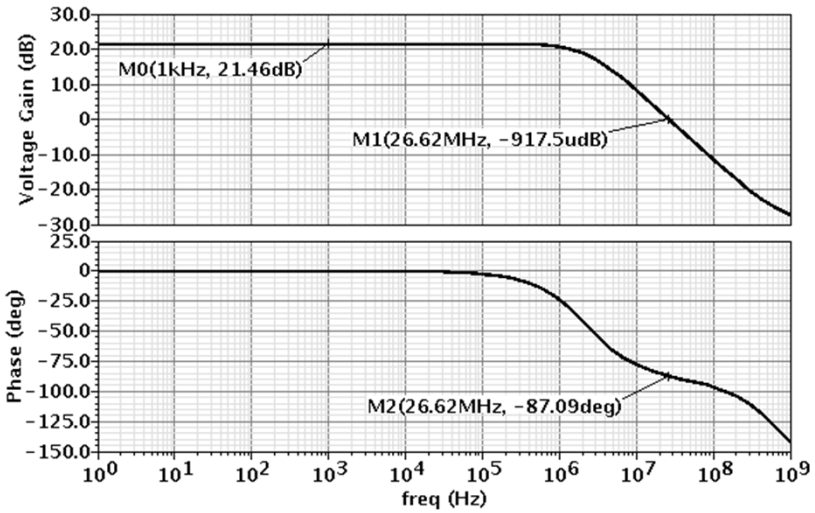


Frequency response of the main CMFB circuit

Mixer Calibration Loop Circuits (cont.)

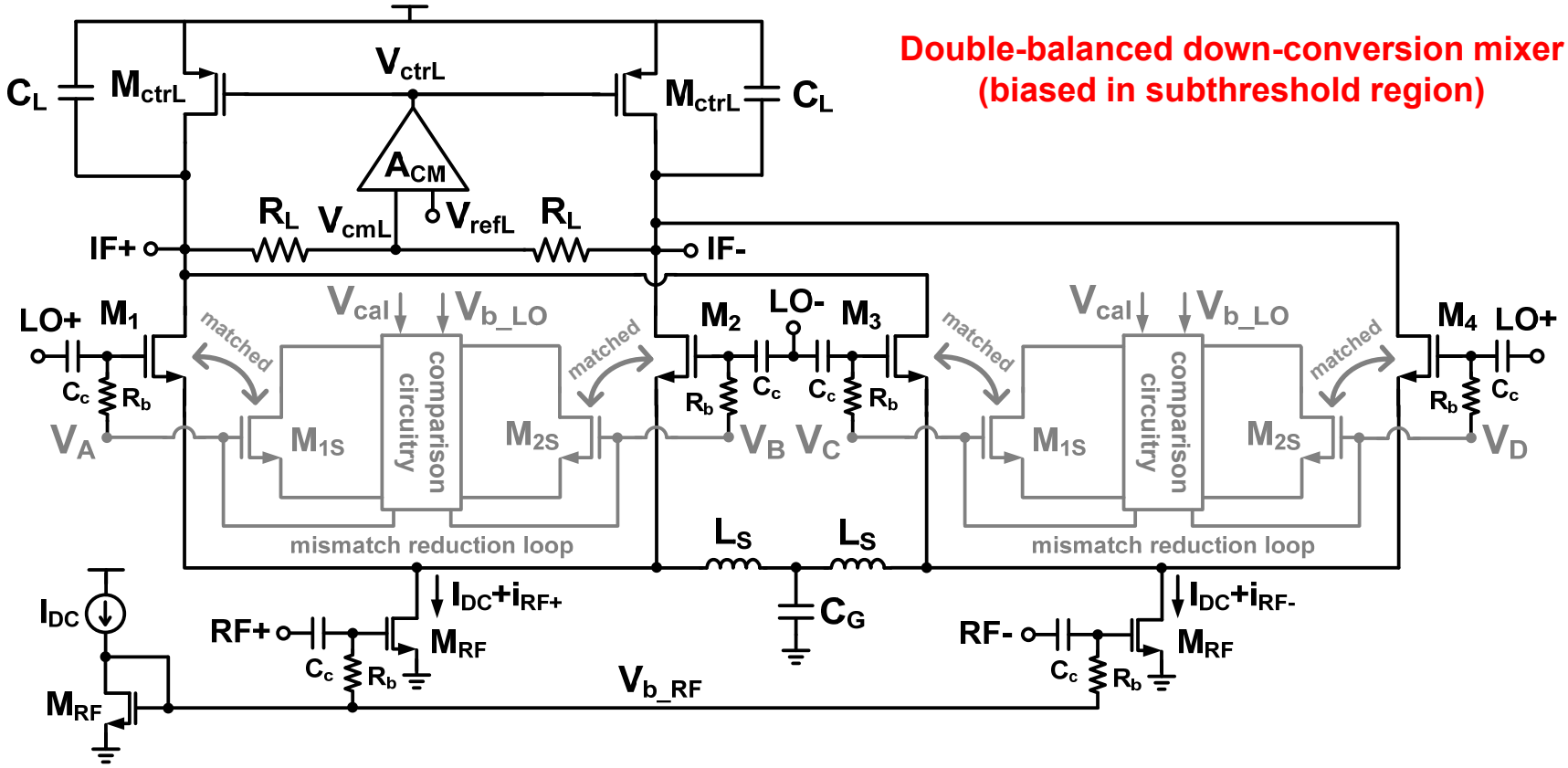


Schematic of amplifiers A_1-A_4 in the calibration loop



Frequency response of the amplifiers

Mixer Design Considerations

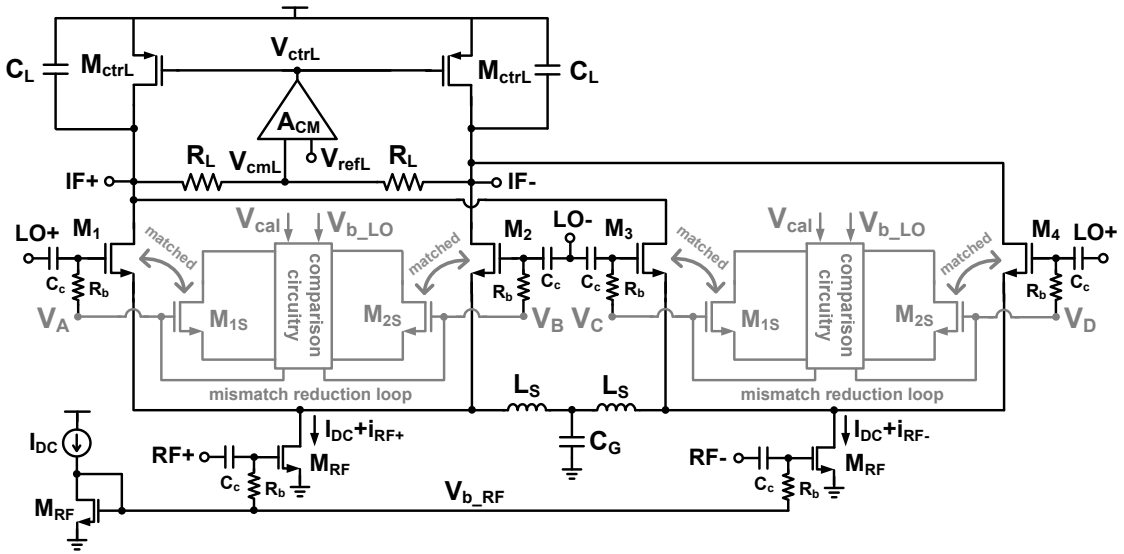


- Inductors (L_S) resonate with parasitic capacitances to improve the IIP2 performance [1]
- Common-mode feedback at the mixer output suppresses the common-mode IM2 components [2]

[1] M. Brandolini, P. Rossi, D. Sanzogni, and F. Svelto, "A +78 dBm IIP2 CMOS direct downconversion mixer for fully integrated UMTS receivers," IEEE *J. Solid-State Circuits*, vol. 41, no. 3, pp. 552- 559, March 2006.

[2] M. Brandolini, M. Sosio, and F. Svelto, "A 750 mV fully integrated direct conversion receiver front-end for GSM in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1310-1317, June 2007.

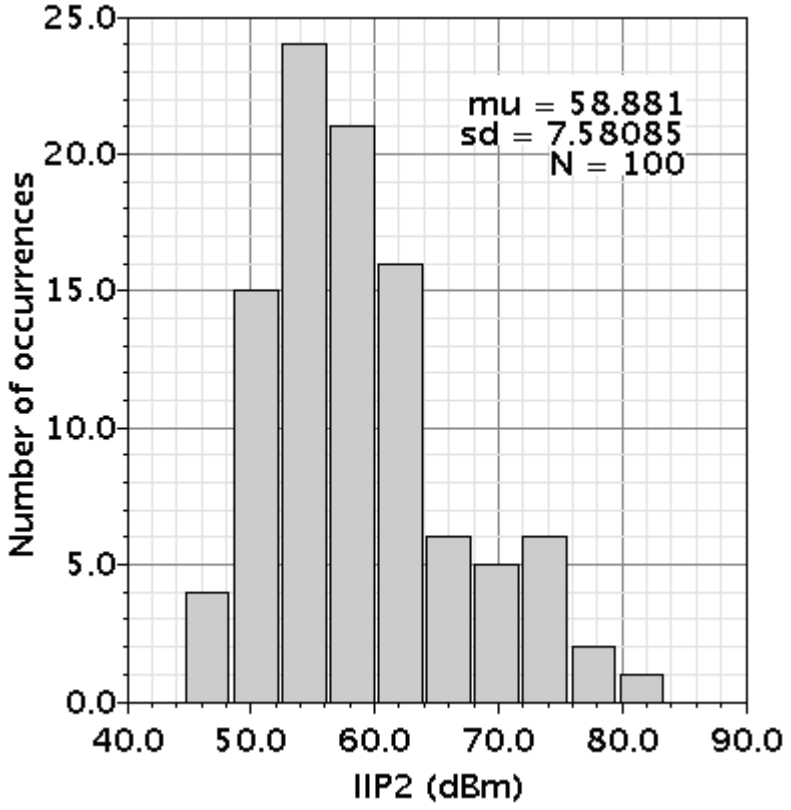
Mixer Component Values



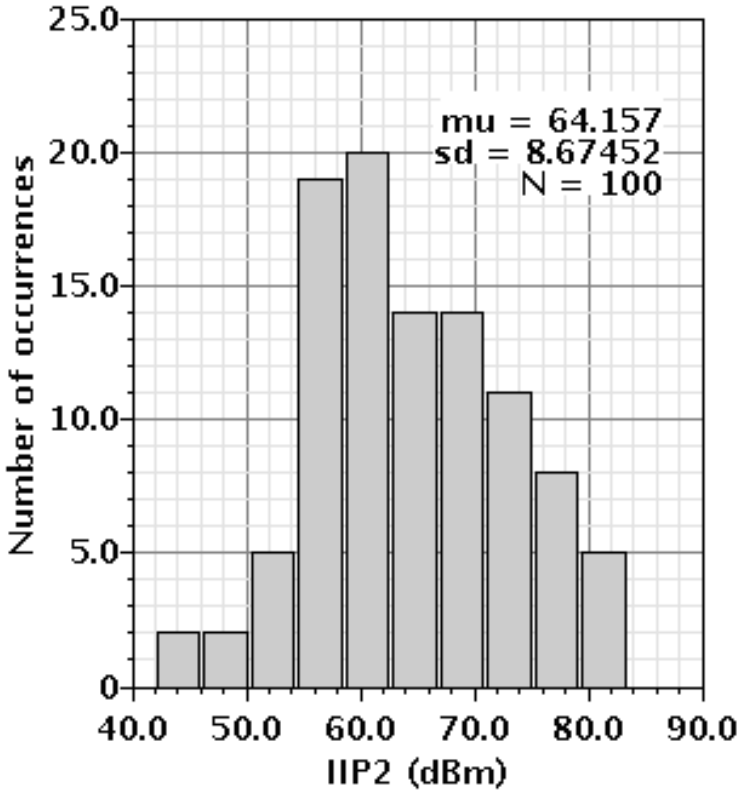
M_1, M_2, M_3, M_4	W/L = 2μm × 40 fingers / 0.13μm
M_{RF}	W/L = 10μm × 40 fingers / 0.13μm
M_{ctrL}	W/L = 1.2μm × 26 fingers / 0.25μm
R_L	3kΩ (L/W = 10 × 8.87μm / 8μm)
C_L	0.15pF
L_S	7nH
C_c	1pF
R_b	100kΩ (L/W = 6 × 15.8μm / 1μm)
V_{b_LO} (nominal values of V_A, V_B, V_C, V_D)	0.665V
V_{refL}	0.565V
I_{DC}	200μA

Monte Carlo Simulations: Mixer IIP2

Without calibration circuitry:



With calibration circuitry:



LO frequency: 1.985GHz, RF test tones: 2GHz, 2.005GHz, IM2 frequency: 5MHz

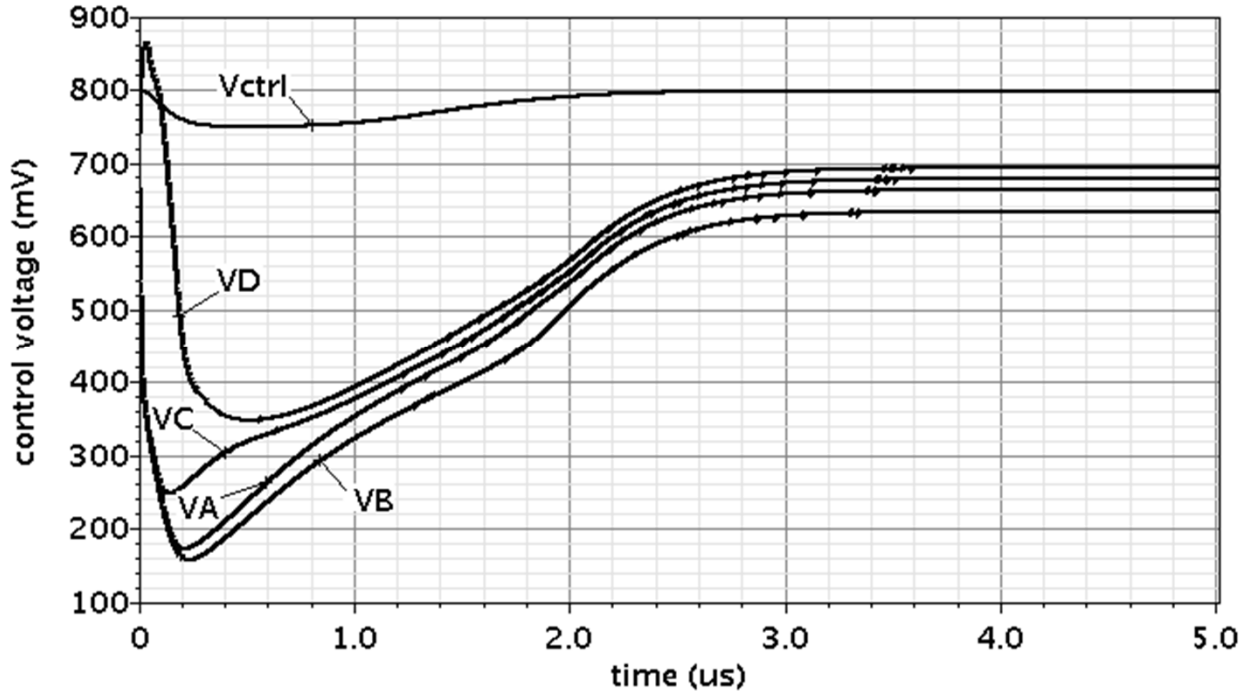
Simulated Mixer Specifications with/without Calibration

0.13μm CMOS Technology with 1.2V Supply

	Without Calibration Circuitry	With Calibration Circuitry
RF Frequency	2GHz	2GHz
IF Bandwidth	< 124.9MHz	< 124.3MHz
Conversion Gain	11.5dB	11.5dB
IIP3	7.3dBm	7.3dBm
1-dB Compression Point	-7.7dBm	-7.8dBm
IIP2 (With 0.5% R_L Mismatch)	62.9dBm	63.0dBm
Avg. IIP2* (100 Monte Carlo runs)	**58.9dBm**	**64.2dBm**
Yield (for IIP2 > 54dBm)**	**75%**	**91%**
DSB Noise Figure	13.2dB	13.2dB
Flicker Noise Corner	266KHz	274KHz
LO-RF Isolation (2-2.3GHz)	> 110dB	> 110dB
LO-IF Isolation (2-2.3GHz)	> 185dB	> 182dB
RF-IF Isolation (2-2.3GHz)	> 80dB	> 79dB
Power (with auxiliary circuits)	**0.68mW**	**0.97mW**

*** With foundry-supplied statistical models (process & mismatch) for all devices in the mixer and calibration circuits.**
**** Defined as the percentage of the Monte Carlo simulation outcomes that meet the IIP2 target.**

Mixer Calibration: Settling Time



Transient settling behavior of critical control voltages

[offset voltages at the gates of (M_2, M_3, M_4) changed from 0V to (30mV, -15mV, -30mV) at time = 0s]

Mismatch Reduction: Summary & Conclusions

- Automatic analog calibration loop for transistor mismatch reduction
  - Intended for short-channel transistors in the differential RF signal path
  - Mismatch reduction by a factor of 3-4 times, depending on the layout configuration of the mismatch-sensing transistors
  - Loop converges within microseconds → suitable for fast coarse calibration (before system-level digital calibrations with convergence times in the milliseconds)
- 1st Application: active double-balanced mixer
  - Mismatch reduction loops enhance second-order linearity (IIP2) performance
  - From Monte Carlo simulations: IIP2 improvement of 5-10dB
  - Trade-offs:
    - 30% power increase
    - Estimated mixer layout area increase due to calibration circuitry: 2x
- Room for future research
  - Experimental verification: layout, fabrication, testing

M. Onabajo, D. Gómez, E. Aldrete-Vidrio, J. Altet, D. Mateo, and J. Silva-Martinez, "Survey of robustness enhancement techniques for wireless systems-on-a-chip and study of temperature as observable for process variations," *Springer J. Electronic Testing: Theory and Applications*, vol. 27, no. 3, pp. 225-240, June 2011.

Course Summary

- Main incentives for on-chip built-in test and calibration schemes
  - Increasing complexity of SoCs and worsening CMOS process variations
  - Improved fabrication yields and extended product reliability
  - Production test cost reduction
- Trend: system-level calibration strategies
  - Digital performance monitoring & calibration control
  - Digital and analog correction
  - Requires “knobs” to tune analog circuits
- Circuit-level features for performance enhancements
  - Demonstrated with examples
  - Alternative on-chip sensors for variation monitoring (e.g., thermal sensing)

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Thank You.