Outline – Lecture 2

• Digitally-assisted analog circuit design & performance tuning
  ▪ LNAs
  ▪ Mixers
  ▪ Filters
  ▪ Example: subthreshold LNA design techniques

▪ Case study:
  Digitally-assisted linearization of operational transconductance amplifiers

▪ Case study:
  Variation-aware continuous-time $\Delta \Sigma$ analog-to-digital converter design
Example Application: Digitally-Assisted Analog Blocks

- Digitally-assisted receiver calibration
  - Analog tuning with digital-to-analog converters (DACs)
  - Digital correction and control
  - Requires programmable analog circuits for performance tuning
• Auxiliary transistor $M_T$ (variable resistor) diverts signal current to the AC ground → Gain control (range: 3.6-12.5dB)

• $C_B$ ensures that the DC bias remains unaffected

• Linearity could be affected

LNA Center Frequency Tuning Example

- Example application: WLAN (2.4GHz, 5GHz)

- 4-bit resolution for $C_{var}$
  $\rightarrow <0.4$dB gain error due to center frequency shift from process variations

• **S\(_{11}\) tuning**
  - \(L_g\) is tapped at 5 points in the outermost turn
  - Control: switches \(S_1-S_N\)

• **With automatic cal. loop**
  - Aux. amplifier, peak detector, digital logic
  - Converges within 30\(\mu\)s

• ~0.4dB lower NF (due to switches)

---

LNA Linearity

• Linearity Tuning
  ▪ MT Operates in triode region
  ▪ MS is biased in subthreshold
  ▪ Non-linearities of the main transistor M0 are canceled

• >10dB IM3 improvement

• With tuning knobs
  ▪ LNA linearity could be monitored in DSP or through power detectors
  ▪ More robust against PVT variations

• NF increases <0.25dB and power increases by 5%

Mixer IIP2 Tuning Example

- 5-bit load resistor control with switches D1-DN
- Reduced 2\textsuperscript{nd}-order non-linearities due to mismatches
- +60dBm IIP2 (>20dB improvement)

• 4-bit bias current control with switches $B_1$-$B_N$
• Less I/Q gain error: $0.1$-$0.2$dB → $0.05$dB ($\Delta \theta_{I/Q} < 3.5^\circ$)
• 1.5dB gain tuning range (steps = $0.09$-$0.13$dB)

- Reconfigurable: Chebyshev/Inv. Chebyshev, order: 1,3,5
- Continuously tunable: 1-20MHz cutoff frequency
- Power-adjustable: 3-7.5mW

Cutoff frequency tuning with adjustable elements in the filter sections

Coarse tuning with capacitors

Fine tuning with continuous impedance multipliers

Subthreshold Low-Noise Amplifier Design Techniques

Chun-hsiang Chang
Marvin Onabajo

Northeastern University
Low-Power Low-Noise Amplifier

- Motivation for biasing RF circuits in the subthreshold (weak inversion) region
  - High transition frequencies \( f_t \) of newer CMOS technologies enable subthreshold RF circuit design (< 3GHz) with sufficiently high transistor transconductance (gain)
  - **5-10 times less power consumption**

- Subthreshold design challenges
  - Degraded linearity & noise performance → for applications with relaxed requirements [wireless personal area network (WPAN), global positioning system (GPS), and wireless medical monitoring]
  - Larger devices → increased parasitic capacitances
Example: Input Impedance Matching

• Typical matching: $Z_{in} = 50\Omega$
  - $S_{11}(\text{dB}) = -\infty$ (ideal)
  - In practice: $-20\text{dB} < S_{11} < -10\text{dB}$

• Conventional approximation:

$$Z_{in} = L_s \frac{g_{m1}}{C_{gs1}} + j \left[ \omega (L_s + L_g) - \frac{1}{\omega C_{gs1}} \right]$$
Issues with Subthreshold Biasing

• Larger parasitic capacitances
  - \( C_{gg} = C_{gs} + C_{gd} + C_{gb} \)
  - Inaccurate \( Z_{in} \) approximation with the conventional equation

• Different contributions to the total gate capacitance \( (C_{gg}) \):

![Diagram showing contributions of parasitics to \( C_{gg} \) vs \( V_{ov} \) in subthreshold and strong inversion regions.](image)
Improved $Z_{in}$ Estimation

- Equations include the effects of $C_{gs}$, $C_{gd}$, $C_{gb}$
- Impact of $M_2$ (load) is considered
- Simplified calculations with a Matlab script

\[ Z_{in} = sL_g + r_{g1} + Z'_{in} \parallel \frac{1}{sC_{MF}} \]

where:
- $r_{g1}$ is the small-signal gate resistance of $M_1$
- $C_{MF}$ is the effective input Miller capacitance
- $Z'_{in}$ is the impedance looking into the gate (without $r_{g1}$) → very long equation
Simulation Results

- Desired matching frequency: 2.4 GHz
- 0.18 µm CMOS technology
- Comparison with different operating regions:

![Graph showing matching frequency and S11 minimum](image)

- Matching frequency (at which the S11 minimum occurs)
- Minimum S11

Super-threshold → Subthreshold

- Proposed (Matlab script)
- Conventional equation

![Graph showing g_m/I_D vs. frequency and S11](image)

- g_m/I_D [S/A]
- Frequency [GHz]
- S11 at the matching frequency [dB]
Simulation Results

- Desired matching frequency: 2.4 GHz
- 0.18 µm CMOS technology
- Comparison with transconductance values:

- Matching frequency (at which the $S_{11}$ minimum occurs)
- Minimum $S_{11}$
Digitally-Controllable Tuning

- Allows digitally-assisted enhancement of $S_{11}$ to compensate for process variations
- Based on newly proposed equations
- Programmable bank of metal-insulator-metal (MIM) capacitors
## Performance with Tuning

<table>
<thead>
<tr>
<th>Condition 1: TT models, 27°C, V_{dd}</th>
<th>Reference LNA</th>
<th>Tunable LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>S11 [dB]</td>
<td>-32.1</td>
<td>-26.4 [00111]</td>
</tr>
<tr>
<td>S21 [dB]</td>
<td>14.1</td>
<td>14.0</td>
</tr>
<tr>
<td>NF [dB]</td>
<td>4.9</td>
<td>5.1</td>
</tr>
<tr>
<td>P1dB [dBm]*</td>
<td>-19.0</td>
<td>-17.6</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>-11.4</td>
<td>-9.5</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Condition 2: FF models, 85°C, +20% V_{dd}</th>
<th>Reference LNA</th>
<th>Tunable LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>S11 [dB]</td>
<td>-14.4</td>
<td>-27.0 [01010]</td>
</tr>
<tr>
<td>S21 [dB]</td>
<td>13.7</td>
<td>13.2</td>
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<tr>
<td>NF [dB]</td>
<td>4.6</td>
<td>5.0</td>
</tr>
<tr>
<td>P1dB [dBm]*</td>
<td>-15.2</td>
<td>-13.4</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>-8.7</td>
<td>-6.0</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Condition 3: FF models, 85°C, +20% V_{dd}, -15% L, -15% Lp</th>
<th>Reference LNA</th>
<th>Tunable LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>S11 [dB]</td>
<td>-9.4</td>
<td>-19.5 [10000]</td>
</tr>
<tr>
<td>S21 [dB]</td>
<td>13.8</td>
<td>12.4</td>
</tr>
<tr>
<td>NF [dB]</td>
<td>4.5</td>
<td>5.6</td>
</tr>
<tr>
<td>P1dB [dBm]*</td>
<td>-15.7</td>
<td>-12.6</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>-8.8</td>
<td>-5.1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Condition 4: SS models, -40°C, -20% V_{dd}</th>
<th>Reference LNA</th>
<th>Tunable LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>S11 [dB]</td>
<td>-15.6</td>
<td>-32.8 [00011]</td>
</tr>
<tr>
<td>S21 [dB]</td>
<td>12.6</td>
<td>13.1</td>
</tr>
<tr>
<td>NF [dB]</td>
<td>4.5</td>
<td>4.4</td>
</tr>
<tr>
<td>P1dB [dBm]*</td>
<td>-20.4</td>
<td>-19.4</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>-12.6</td>
<td>-11.6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Condition 5: SS models, -40°C, -20% V_{dd}, -15% L, +15% Lp</th>
<th>Reference LNA</th>
<th>Tunable LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>S11 [dB]</td>
<td>-8.2</td>
<td>-18.8 [00000]</td>
</tr>
<tr>
<td>S21 [dB]</td>
<td>12.2</td>
<td>13.4</td>
</tr>
<tr>
<td>NF [dB]</td>
<td>4.9</td>
<td>4.4</td>
</tr>
<tr>
<td>P1dB [dBm]*</td>
<td>-20.5</td>
<td>-20.4</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>-12.5</td>
<td>-12.4</td>
</tr>
</tbody>
</table>

- Tunable LNA design with almost identical specifications as the reference LNA
- S11 improvement: >10dB
- The tuning has small impact on other performance parameters
- Next step: Linearity improvement and tuning
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▪ Case study:
  Digitally-assisted linearization of operational transconductance amplifiers

▪ Case study:
  Variation-aware continuous-time ΔΣ analog-to-digital converter design
Digitally-Assisted Receiver Calibration – Revisited

- Next case study: baseband filter
  - High linearity over wide frequency range
  - Digital programmability
Motivation for OTA Linearization

- Applications with operational transconductance amplifiers (OTAs)
  - On-chip filters in the 100-200MHz frequency range
    - In the intermediate frequency stage of wireless receivers
    - Continuous-time $\Sigma\Delta$ analog-to-digital converters
  - Transconductance-capacitor baseband filters
    - Baseband frequency < 50MHz
    - (ex. comm. standards: WiMAX, WLAN, WCDMA, UMTS)
    - Third-order intermodulation distortion (IM3) < -60dB

- Project objectives
  - Cancellation of OTA non-linearities (signal distortion reduction)
  - Robustness of the linearization to process variations
  - Compensation for frequency-dependent linearity degradation
The Problem of Limited Linearity

- Mathematical representation of non-linear behavior
  - Amplitude of a sinusoidal input signal: $V_{in}$
  - Output current ($i_{out}$) can be expressed as:
    - **Linear**: $i_{lin}\{V_{in}\} = Gm \times V_{in}$
    - **Non-linear**: $i_{non-lin}\{V_{in}\} = g_{m2} \times V_{in}^2 + g_{m3} \times V_{in}^3 + \ldots$
      where $g_{m2}, g_{m3}, \ldots$ are Taylor series coefficients

- Practical issues
  - Distorted output current
    - Undesired spectral components at multiples of the frequency $f_0$ →
    - Typical limit without linearization: HD3 is 50-60dB below the fundamental
  - Frequency dependence: worse linearity at high frequencies
Linearization Basics

- Linearity Improvement Concepts
  - Harmonics can be reduced by:
    - Signal attenuation
    - Cancellation
    - Feedback
  - Even-order harmonics are suppressed in fully-differential circuits

Spectrum for a fully-differential OTA without odd-order cancellation
Proposed Linearization

• Concept
  ▪ Identical auxiliary path generates the same distortion as in the main path
  ▪ The predistorted signal is subtracted at the input of the OTA in the main path
  ▪ Result: cancellation of distortion

• Effective transconductance
  ▪ \( G_{\text{m eff}} = \frac{1}{2} G_m \) of non-linearized OTA with input-attenuation factor of 0.5
  ▪ Same dimensions & operating conditions in both paths

• Conditions for cancellation
  ▪ \( G_m \times R = 1 \) in aux. path
  ▪ \( R_c \approx R \) for optimum cancellation
  ▪ \( R_c \) & \( C_i \) provide phase shift → 1st-order frequency compensation

\[
\begin{align*}
  i_{\text{aux}} &= G_m V_{\text{in}}/2 + i_{\text{non-lin}}(V_{\text{in}}/2) \\
  V_x &= V_{\text{in}}/2 + i_{\text{non-lin}}(V_{\text{in}}/2) \times R \\
  V_{\text{diff}} &= V_{\text{in}}/2 - i_{\text{non-lin}}(V_{\text{in}}/2) / G_m \\
  i_{\text{out}} &\approx G_m V_{\text{in}}/2 + i_{\text{non-lin}}(V_{\text{in}}/2) - i_{\text{non-lin}}(V_{\text{in}}/2) \approx G_m V_{\text{in}}/2
\end{align*}
\]

* \( i_{\text{non-lin}}(V_m) \) represents the distortion components of the current generated by \( G_m \) with input voltage amplitude \( V_m \)
Single-Ended OTA for High-Frequencies

• Topology modified from the typical 3-current mirror OTA
  • Source degeneration resistors (Rd) in the output stage
    • Similar output resistance as a cascode stage with minimum-length transistors in 0.13μm technology
    • High linearity with large signal swings
  • Minimum length transistors (min. parasitic capacitances) for 100MHz operation

• Key component values
  • \( R = 1.28k\Omega \approx 1/Gm \)
  • \( R_c = 1.28k\Omega, C_i = 240fF \)

• Basic specifications →
  (0.13μm CMOS, 1.2V supply)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gm</td>
<td>776μA/V</td>
</tr>
<tr>
<td>Excess Phase</td>
<td>2.6° at 100MHz</td>
</tr>
<tr>
<td>( R_o )</td>
<td>13kΩ</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>622MHz</td>
</tr>
<tr>
<td>Power</td>
<td>2.4mW</td>
</tr>
</tbody>
</table>
Simulations: Single-Ended OTA

- Output current spectra from IM3 tests
  - $V_{\text{in}_{\text{peak-peak}}} = 200\text{mV}$, test tones at 100MHz and 105MHz
  - Linearity improvements
    - IM3: 19dB, HD2: 28dB, HD3: 30dB
    - THD: 29dB (20dB in a 2nd-order bandpass filter)
  - Trade-offs
    - Noise increase (~1.6x), power consumption (2x), area (2x)

**OTA with input-attenuation factor of 0.5**
IM3 = -42.8dB at 100MHz

**Linearized OTA (attenuation-predistortion)**
IM3 = -61.8dB at 100MHz
Variation of Resistor $R$ & Calibration

- $\Delta THD < 5.4$dB requires accuracy of $R$ within 4%

- Some form of calibration is necessary
  - Digital (implemented):
    R can be adjusted with discrete steps until $Gm \times R = 1$
  - Analog tuning also a possibility:
    comparison of $V_{in}$ and $V_x$ with an error amplifier
    ($V_{peak}$, $V_{rms}$, etc. should be identical), automatic
    adjustment of $R$ (transistor biased in triode region)

THD vs. %-variation of resistor $R$

$$\begin{align*}
A &\approx \{0 - 88.117\%\} \\
B &\approx \{4 - 62.713\%\} \\
\text{slope} &\approx 1.35098
\end{align*}$$

Auxiliary OTA:

Total $R_c = 1.28k\Omega$ (this design)
Variation of Resistor Rc & Calibration

ΔTHD < 6dB requires accuracy of Rc within 4%

Requires same calibration approach as for resistor R
  ▪ Simplest: cycling through switch combinations until optimum linearity
  ▪ Options to assess performance in the digital domain:
    ▪ Monitor HD3 or THD (if A/D, DSP are available)
    ▪ In receivers: monitor bit error rate

THD vs. %-variation of resistor Rc

Total Rc = 1.28kΩ (this design)
Single-Ended OTA: Schematic Simulations

Comparison with $V_{\text{in}_{\text{p-p}}} = 200\text{mV}$ @ 100MHz:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Reference OTA</th>
<th>Linearized OTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_{m_{\text{effective}}}$</td>
<td>$G_{m}/2$</td>
<td>$G_{m}/2$</td>
</tr>
<tr>
<td>THD</td>
<td>1.32% (-37.6dB)</td>
<td>0.048% (-66.8dB)</td>
</tr>
<tr>
<td>HD2 (below fundamental)</td>
<td>37.68dB</td>
<td>66.68dB</td>
</tr>
<tr>
<td>HD3 (below fundamental)</td>
<td>54.35dB</td>
<td>84.26dB</td>
</tr>
<tr>
<td>IM3, $\Delta f=5\text{MHz}$ (below fundamental)</td>
<td>42.8dB</td>
<td>61.9dB</td>
</tr>
<tr>
<td>Input-referred noise</td>
<td>17.3nV/$\sqrt{\text{Hz}}$</td>
<td>27.7nV/$\sqrt{\text{Hz}}$</td>
</tr>
</tbody>
</table>

Comparison with $V_{\text{in}_{\text{p-p}}} = 200\text{mV}$ @ 10MHz:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Reference OTA</th>
<th>Linearized OTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_{m_{\text{effective}}}$</td>
<td>$G_{m}/2$</td>
<td>$G_{m}/2$</td>
</tr>
<tr>
<td>THD</td>
<td>1.31% (-37.7dB)</td>
<td>0.021% (-73.6dB)</td>
</tr>
<tr>
<td>HD2 (below fundamental)</td>
<td>37.78dB</td>
<td>73.49dB</td>
</tr>
<tr>
<td>HD3 (below fundamental)</td>
<td>53.88dB</td>
<td>93.03dB</td>
</tr>
<tr>
<td>IM3, $\Delta f=0.5\text{MHz}$ (below fundamental)</td>
<td>42.8dB</td>
<td>67.2dB</td>
</tr>
<tr>
<td>Input-referred noise</td>
<td>18.7nV/$\sqrt{\text{Hz}}$</td>
<td>29.1nV/$\sqrt{\text{Hz}}$</td>
</tr>
</tbody>
</table>
Fully-Differential OTA Linearization

- Design for high performance
  - High-frequency operation
  - Common-mode noise rejection
  - Differential signal swing (2x larger)
  - Floating-gate transistors as attenuators

- Generalized conditions for attenuation-predistortion linearization
  - Weakly non-linear operation: \( k_2 G_m R \leq 1 \)
  - Non-linearity cancellation:
    \[
    (1 - k_1) G_m R = 1, \quad k_2 = k_1 / 2
    \]
  - Effective transconductance: \( G_{m_{\text{eff}}} = k_2 G_m \)

- To ensure IM3 \( \approx 0 \) based on Volterra series analysis to take high-frequency effects of capacitors into account:
  \[
  R_c \approx \frac{(1 - k_1) + 2C_o / C}{2k_1} R
  \]

- This design: \( k_1 = 2/3, \quad k_2 = 1/3 \)
  \[ R_c = (R/4)(1+6C_o / C) \]
**Fully-Differential OTA**

- **Folded-cascode OTA** (implements $G_m$ in main and auxiliary paths)

  - Error amplifier compensation with resistor $R_z$ in CMFB extends the bandwidth of the common-mode rejection:

    $$GBW \approx \sqrt{A_0 \cdot \omega_p \cdot \omega_3} \approx \sqrt{A_0 \cdot \omega_p \cdot \frac{2}{R_z (C_{gs} / 2 + (g_{mL} R_L / 2) C_{dg})}}$$

  - Affect of $R_z$ on stability according to phase margin (PM):

    $$PM \approx \tan^{-1}\left(\frac{2 R_z C_{dg}^2}{C_{gs} / 2 + (g_{mL} R_L / 2) C_{dg}}\right)$$

---

**Error amplifier circuit in the common-mode feedback (CMFB) loop**

**Parameter** | **Measurement**
---|---
Transconductance ($G_m$) | 510 μA/V
IM3 @ 50MHz (Vin = 0.2 Vp-p) | -55.3 dB
Noise (input-referred) | 13.3 nV/√Hz
Power with CMFB | 2.6 mW
PSRR @ 50MHz | 48.9 dB
Supply | 1.2 V
High-Frequency Effects & Process Variation

- Theoretical IM3 higher than 70dBc with up to ±10% variation of Gm and ±5% of Rc
  - Not always ensured by matching devices in the layout → programmable resistors for tuning
  - Robustness was verified with schematic corner and component mismatch simulations
- Sensitivity of IM3 (in dBc) to component mismatches:

10MHz signal frequency

200MHz signal frequency
Simulated Fully-Diff. OTA: Resistor Variations

- IM3 better than 71dBc for ±7.5% Rc-variation
- IM3 better than 71dBc for ±3.3% R-variation in the presence of 10% Gm-mismatch
- Reference OTA has IM3 of 51dBc

Theoretical IM3:

\[
i_{IM3} \approx g_m^3 \left( \frac{k_1 / 2}{1 + 2C_p / C} \right)^3 \left( 3V_{in1}V_{in2} / 4 \right) \left( \frac{1 + j\omega C((1 - k_1)R - k_1 R_c) + 2j\omega C_o R}{1 + j\omega b - c\omega^2} \right) \left( \frac{1 - j\omega C((1 - k_1)R - k_1 R_c) - 2j\omega C_o R}{1 - j\omega b - c\omega^2} \right)
\]

\[
- g_m^3 \left( \frac{k_1 / 2}{1 + 2C_p / C} \right)^3 \left( 3V_{in1}V_{in2} / 4 \right) \left( \frac{1 + j\omega Ck_1 R_c}{1 + j\omega b - c\omega^2} \right)
\]
Measurements: Standalone OTAs

- 0.13μm CMOS Testchip
- Reference OTAs & linearized OTAs (fully-differential → input attenuation = 1/3)

<table>
<thead>
<tr>
<th>OTA Type</th>
<th>Input-referred Noise</th>
<th>IM3 (V_{in} = 0.2 V_{p-p})</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>50 MHz</td>
</tr>
<tr>
<td>Reference (input attenuation = 1/3)</td>
<td>13.3 nV/√Hz</td>
<td>-55.3 dB</td>
</tr>
<tr>
<td>Linearized (attenuation = 1/3)</td>
<td>21.8 nV/√Hz</td>
<td>-77.3 dB</td>
</tr>
</tbody>
</table>
Measurements: Standalone OTAs (cont.)

**IM3 vs. input voltage for reference OTA and linearized OTA**
(two test tones having 100kHz separation around 350MHz)

**IM3 dependence of the linearized OTA on phase shift at 350MHz.**
(The least significant bit of the digital control code changes the value of phase shift resistor $R_c$ by $\sim$3%)
Fully-Differential OTA Comparison With Previous Works

- Figure of Merit [1]:
  - FOM = NSNR + 10log( f/1MHz ) where:
    - NSNR = SNR\(_{\text{dB}}\) + 10log[ ( IM3\(_N\) / IM3 ) ( BW / BW\(_N\) ) ( P\(_N\) / P\(_{\text{dis}}\) ) ] from [2]
    - Normalizations:  
      SNR integrated over 1MHz, IM3\(_N\) = 1\%, bandwidth BW\(_N\) = 1Hz , power P\(_N\) = 1mW

- Competitive performance with respect to the state of the art
  - Effective trade-offs between linearity, power, noise

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</thead>
<tbody>
<tr>
<td>IM3</td>
<td>-</td>
<td>-47 dB</td>
<td>-70 dB</td>
<td>-60 dB</td>
<td>-</td>
<td>-74.2 dB</td>
</tr>
<tr>
<td>IIP3</td>
<td>-12.5 dBV</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>7 dBV</td>
<td>7.6 dBV</td>
</tr>
<tr>
<td>f</td>
<td>275 MHz</td>
<td>10 MHz</td>
<td>20 MHz</td>
<td>40 MHz</td>
<td>184 MHz</td>
<td>350 MHz</td>
</tr>
<tr>
<td>Input voltage</td>
<td>-</td>
<td>0.2 V(_p-p)</td>
<td>1.0 V(_p-p)</td>
<td>0.9 V(_p-p)</td>
<td>-</td>
<td>0.2 V(_p-p)</td>
</tr>
<tr>
<td>Power / transconductor</td>
<td>4.5 mW</td>
<td>1.0 mW</td>
<td>4 mW</td>
<td>9.5 mW</td>
<td>1.26 mW</td>
<td>5.2 mW</td>
</tr>
<tr>
<td>Input-referred noise</td>
<td>7.8 nV/\sqrt{Hz}</td>
<td>7.5 nV/\sqrt{Hz}</td>
<td>70.0 nV/\sqrt{Hz}</td>
<td>23.0 nV/\sqrt{Hz}</td>
<td>53.7 nV/\sqrt{Hz}</td>
<td>21.8 nV/\sqrt{Hz}</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.2 V</td>
<td>1.8 V</td>
<td>3.3 V</td>
<td>1.5 V</td>
<td>1.8 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
<td>0.18(\mu)m CMOS</td>
<td>0.5(\mu)m CMOS</td>
<td>0.18(\mu)m CMOS</td>
<td>0.18(\mu)m CMOS</td>
<td>0.13(\mu)m CMOS</td>
</tr>
<tr>
<td>FOM(_{\text{dB}})</td>
<td>87.5</td>
<td>92.9</td>
<td>96.1</td>
<td>99.1</td>
<td>100</td>
<td>105.6</td>
</tr>
</tbody>
</table>

* Power/transconductor calculated from filter power. Individual OTA characterization results not reported in full.
OTA Linearization References

• Cited on the previous slide:


OTA Linearization without Increased Power

- Requires redesign of the OTA with 50% of the initial bias current
  - Increased W/L ratio to maintain the same transconductance value
  - Parasitic capacitances of the larger devices lead to bandwidth ($f_{3dB}$) reduction
  - Gate-source overdrive (saturation) voltage is approximately 50% less

- Trade-off to maintain similar transconductance and +20dB linearity enhancement without power increase: Bandwidth reduction

- Example – Comparison after linearization (redesign of the fully-differential OTA) with the same power consumption as the non-linearized reference OTA:

| OTA type                  | $V_{DSAT}$ of input diff. pair | $f_{3db}$ with 50Ω load | Input-referred noise | Power | $IM3$ ($V_{in} = 0.2 \ V_{p-p}$) | Normalized $|FOM|$ (at $f_{max}$) |
|---------------------------|--------------------------------|------------------------|----------------------|-------|---------------------------------|----------------------------------|
| Reference (input attenuation = 1/3) | 90 mV                         | 2.49 GHz               | 9.7 nV/√Hz          | 2.6 mW | -53.1 dB at $f_{max} = 350MHz$ (-53.2 dB at 100MHz) | 57.2                             |
| Linearized (attenuation = 1/3 & compensation) | 54 mV                         | 1.09 GHz               | 14.3 nV/√Hz         | 2.6 mW | -77.1 dB at $f_{max} = 100MHz$ | 119.2                            |
Measurements: Filter with Linearized OTAs

- IM3 ≈ -70dB up to 150MHz (with 0.2V_{p-p} input)
- Broadband linearity thanks to the phase shifter (IM3 = -66.1dB at 200MHz, filter corner frequ. = 194.7MHz)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Corner frequency (f_{3db})</td>
<td>194.7 MHz</td>
</tr>
<tr>
<td>Passband gain</td>
<td>0 dB</td>
</tr>
<tr>
<td>Quality factor</td>
<td>1</td>
</tr>
<tr>
<td>Gm_{1,2,3,4}</td>
<td>510 \mu A/V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Linearized Filter</th>
<th>IM3 (V_{in} = 0.2 V_{p-p})</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>50 MHz</td>
</tr>
<tr>
<td></td>
<td>-73.9 dB</td>
</tr>
</tbody>
</table>

IM3 with compensated OTAs (input: 0.2V_{p-p}@150MHz)
Measurements: Filter with Fully-Differential OTAs

Frequency response of the 2nd - order low-pass filter

IM3 vs. input peak-peak voltage (two test tones having 100kHz separation around 150MHz)

IIP3 = 14.0dBm
(two tones, Δf = 100kHz around 150MHz)

IIP2 = 13.4dBm
(two tones, Δf = 100kHz around 2MHz)
## Wideband $G_m$-C Low-Pass Filter Comparison

<table>
<thead>
<tr>
<th>Filter order</th>
<th>[A]</th>
<th>[B]</th>
<th>[C]</th>
<th>[D]</th>
<th>[E]</th>
<th>[F]</th>
<th>[G]</th>
<th>presented work</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_c$ (max.)</td>
<td>275MHz</td>
<td>184MHz</td>
<td>120MHz</td>
<td>200MHz</td>
<td>200MHz</td>
<td>500MHz</td>
<td>300MHz</td>
<td>200MHz</td>
</tr>
<tr>
<td>Signal swing</td>
<td>-</td>
<td>0.30V$_{pp}$</td>
<td>0.20V$_{pp}$</td>
<td>0.88V$_{pp}$</td>
<td>0.80V$_{pp}$</td>
<td>0.50V$_{pp}$</td>
<td>-</td>
<td>0.75V$_{pp}$</td>
</tr>
<tr>
<td>Linearity with max. Vin$_{pp}$</td>
<td>-</td>
<td>HD3, HD5: &lt; -45dB</td>
<td>THD: -50dB @ 120MHz</td>
<td>THD: -40dB @ 20MHz</td>
<td>THD: -42dB @ 200MHz</td>
<td>THD: &lt; -40dB @ 70MHz</td>
<td>-</td>
<td>THD &lt; -40dB @ 150MHz</td>
</tr>
<tr>
<td>In-band IIP3</td>
<td>-12.5dBV (0.5dBm)</td>
<td>7dBV (20dBm)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>3.9dBV (16.9dBm)</td>
<td>1.0dBV (14.0dBm)</td>
</tr>
<tr>
<td>In-band IIP2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Out-of-band IIP3</td>
<td>-8dBV (5dBm)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Out-of-band IIP2</td>
<td>15dBV (28dBm)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Power</td>
<td>36mW</td>
<td>12.6mW</td>
<td>120mW</td>
<td>48mW</td>
<td>210mW</td>
<td>100mW</td>
<td>72mW</td>
<td>20.8mW</td>
</tr>
<tr>
<td>Power per pole</td>
<td>7.2mW</td>
<td>2.5mW</td>
<td>15mW</td>
<td>12mW</td>
<td>30mW</td>
<td>20mW</td>
<td>24mW</td>
<td>10.4mW</td>
</tr>
<tr>
<td>Input-referred noise</td>
<td>7.8nV/√Hz</td>
<td>53.7nV/√Hz</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>5nV/√Hz</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>44dB</td>
<td>43.3dB</td>
<td>45dB</td>
<td>58dB</td>
<td>-</td>
<td>52dB</td>
<td>-</td>
<td>54.5dB</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.2V</td>
<td>1.8V</td>
<td>2.5V</td>
<td>2V</td>
<td>3V</td>
<td>3.3V</td>
<td>1.8V</td>
<td>1.2V</td>
</tr>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
<td>180nm CMOS</td>
<td>250nm CMOS</td>
<td>350nm CMOS</td>
<td>350nm CMOS</td>
<td>250nm CMOS</td>
<td>350nm CMOS</td>
<td>180nm CMOS</td>
</tr>
</tbody>
</table>


OTA Linearization: Summary & Conclusions

• Proposed linearization technique
  ▪ For OTAs in transconductance-C filter applications
  ▪ Independent of the OTA circuit topology
  ▪ Allows linearity, noise, power design trade-offs

• Measured performance
  ▪ IM3 improvement of up to 22dB
  ▪ Performance meets state-of-the-art requirements

• Compensation for PVT variations and high-frequency effects
  ▪ Based on digital adjustment of resistors
  ▪ Main amplifier can be optimized for its target application
    (no internal circuit design change due to the linearization scheme)

Outline – Lecture 2

• Digitally-assisted analog circuit design & performance tuning
  ▪ LNAs
  ▪ Mixers
  ▪ Filters
  ▪ Example: subthreshold LNA design techniques

▪ Case study: Digitally-assisted linearization of operational transconductance amplifiers

▪ Case study: Variation-aware continuous-time ΔΣ analog-to-digital converter design
Digitally-Assisted Receiver Calibration – Revisited

- Next case study: continuous-time $\Delta \Sigma$ analog-to-digital converter design
  - High Signal-to-noise-and-distortion ratio (SNDR) over wide bandwidth
  - Robustness to performance degradation from component mismatches

![Diagram of a receiver system with I-Path and Q-Path, including components like mixer, filter, DACs, and ADCs.](image-url)
Variation-Aware Continuous-Time ΔΣ Analog-to-Digital Converter Design

Team at Texas A&M University:

Cho-Ying Lu, Marvin Onabajo, Venkata Gadde, Yung-Chung Lo, Hsien-Pu Chen, Vijay Periasamy, Jose Silva-Martinez
Specific Quantizer Application Overview

• Analog-to-digital converter (ADC) group project
  ▪ Continuous-time low-pass $\Sigma\Delta$ modulator with competitive specifications
    ▪ 25MHz bandwidth, sampling frequency = 400MHz
    ▪ Signal-to-noise-and-distortion ratio (SNDR) = 67.7dB
    ▪ Power consumption = 48mW
  ▪ Robustness to performance degradation from component mismatches
    ▪ Device mismatches → non-linearities (signal distortion) → SNDR degradation
    ▪ Novel multi-bit feedback with a single-element digital-analog-converter (DAC) using pulse width modulation (PWM)
      → Avoids non-linearities from unit element mismatches
        (encountered in conventional multi-bit DACs)

• Presentation focus: 3-bit quantizer
  ▪ Proposed topology is optimized for the PWM DAC approach (multiple clock phases)
  ▪ Option for adjusting quantization levels to compensate for process variations
Basic $\Sigma\Delta$ Modulation Concepts

- Highlights of relevant multi-bit DAC/quantizer effects:
  - Reduced quantization noise $\rightarrow \sigma_{\text{quant. noise}} = \frac{V_{\text{full-swing}}}{2^{\text{bits}} \cdot \sqrt{12}}$
  - Improved stability
  - DAC non-linearity at $V_{\text{in}}$ is not suppressed by the feedback loop! $\rightarrow$ More sensitivity to mismatches from process variations!
Conventional 3-Bit Flash Quantizer
Two-Step ADC Principle

- Subranging
  - Most-significant bit(s) (MSB) are resolved first (fixed reference $V_{ref1}$)
  - Least-significant bit(s) (LSB) are quantized with variable references $V_{ref2a}$ and $V_{ref2b}$
    - $V_{ref2a}$ and $V_{ref2b}$ depend on the MSB value
- Multi-step quantization can reduce area and power consumption when a delay of multiple clock cycles is acceptable

Modern “Flash-like” ADC Examples

• Alternative architectures take advantage of technology scaling (fast switching)
  ▪ Enhanced performance at higher conversion speeds
  ▪ Reduced power consumption
  ▪ Improving compatibility with digital CMOS processes

• Folding flash ADC
  ▪ Comprised of 16 instead of 31 (conventional flash) comparators for 5-bit resolution
  ▪ 1.75 GS/s in 90nm CMOS, 2.2mW, 5-bit res.

• Asynchronous ADC
  ▪ Asynchronous successive approximations performed with a single comparator
  ▪ Input is weighted against a reference that is changed with a switchable capacitor array
  ▪ 600-MS/s in 0.13µm CMOS, 5.3-mW
More Modern “Flash-like” ADC Examples

• Two-step ADC
  ▪ MSB is quantized first
  ▪ LSBs are determined with an asynchronous binary-search procedure
  ▪ 150MS/s in 90nm CMOS, 133µW, 7-bit res.

• Other related references:


Taking Advantage of Fast-Switching

- Multi-phase digital-analog-converter (DAC) & quantizer approach
  - Exploits the inherent linearity of the single-element DAC
  - Same charge injected into the filter as with the conventional multi-bit feedback DAC
  - Multi-bit feedback with a single-element DAC
    - No element mismatch, low layout complexity, low power
    - 7 clock phases → accurate low-jitter phases from an injection-locked frequency divider

- Requirement trade-offs (conventional vs. multi-phase):
  - Good device matching → accurate low-jitter clock generation
  - Large device dimensions (older CMOS) → fast-switching transistors (modern CMOS)
Low-Jitter Clock Generation

- Generation of 7 low-jitter clock phases at 400MHz
  - 2.8GHz inductor-capacitor (LC) tank voltage-controlled oscillator (VCO)
    * Improves phase noise (jitter) of the locked ring oscillator
  - Ring oscillator output phases control the timing of the quantizer & DAC logic circuits

3-Bit Successive Approximation Quantizer

- 2-step current-mode quantization
  - 1\textsuperscript{st}: Most significant bit (MSB) decision
  - 2\textsuperscript{nd}: Successive comparisons of the sampled input with three reference levels

- Clocking
  - Sampling at 400MHz
  - Timing signals derived from the 7-phase clock generation for the DAC

- Current-mode comparison
  - Matched transconductors ($G_m$)
  - Reference currents are switched and compared to $I_{in}$
  - Fast low-voltage differential signaling configuration ($R_{cmp} < 500\Omega$)
  - Ref. voltages can be un-buffered (a low source output impedance is not required)

Simplified single-ended equivalent circuit
Quantizer Operation

- Fully-differential circuit
- Matched branches \((M_p, M_{sw}, M_n)\)
- Currents driven into low impedance nodes for fast decisions \((T/7 \approx 360\text{ps})\)
Quantizer Simulations

- Implementation in 0.18μm CMOS with 1.8V supply
  - 24mW power consumption
  - 5mV resolution
  - Tunability to allow for PVT variations
    - Quantization levels can be shifted up to 30mV
    - Reference voltages are not in the direct signal path
  - Layout area of quantizer & timing circuitry: 750μm x 520 μm

Differential Input MSB B2 B1 B0

<table>
<thead>
<tr>
<th>Range</th>
<th>MSB</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>150mV to 200mV</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>100mV to 150mV</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>50mV to 100mV</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0 to 50mV</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-50mV to 0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>-100mV to -50mV</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>-150mV to -100mV</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-200mV to -150mV</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Ramp test: output bits for -200mV < V_{in} < 200mV
### CT $\Sigma\Delta$ Modulators: State of the Art

<table>
<thead>
<tr>
<th></th>
<th>[A]</th>
<th>[B]</th>
<th>[C]</th>
<th>[D]</th>
<th>[E]</th>
<th>[F]</th>
<th>[G]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak SNDR</td>
<td>72dB</td>
<td>82dB</td>
<td>60dB</td>
<td>69dB</td>
<td>70dB</td>
<td>74dB</td>
<td>78.1dB</td>
<td>67.7dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>10MHz</td>
<td>10MHz</td>
<td>20MHz</td>
<td>20MHz</td>
<td>20MHz</td>
<td>20MHz</td>
<td>20MHz</td>
<td>25MHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>40mW</td>
<td>100mW</td>
<td>10.5mW</td>
<td>56mW</td>
<td>28mW</td>
<td>20mW</td>
<td>87mW</td>
<td>48mW</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>950MHz</td>
<td>640MHz</td>
<td>250MHz</td>
<td>340MHz</td>
<td>420MHz</td>
<td>640MHz</td>
<td>900MHz</td>
<td>400MHz</td>
</tr>
<tr>
<td>Technology</td>
<td>130nm CMOS</td>
<td>180nm CMOS</td>
<td>65nm CMOS</td>
<td>90nm CMOS</td>
<td>90nm CMOS</td>
<td>130nm CMOS</td>
<td>130nm CMOS</td>
<td>180nm CMOS</td>
</tr>
</tbody>
</table>


Quantizer: Process Variation Compensation

- Adjustable reference voltages
  - Quantization levels can be shifted up to 30mV
  - Do not have to be buffered
    (current-mode comparison → ref. voltages not in direct signal path)

- Example: shift of quantization level for bit 2
  - Schematic simulation with modeled pad/package parasitics
  - Nominal: transition at -153.6mV with $V_{\text{ref3}} = 150$ mV

Bit transition at -187.4mV with $V_{\text{ref3}} = 180$ mV

Bit transition at -122.5mV with $V_{\text{ref3}} = 120$ mV
Quantizer: Technology Scaling & Process Variation

Key quantizer performance differences due to design scaling:

<table>
<thead>
<tr>
<th></th>
<th>Jazz 0.18μm CMOS</th>
<th>UMC 90nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>+/-5mV</td>
<td>+/-7mV</td>
</tr>
<tr>
<td>(nominal corner, no jitter)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Static power: quantizer core</td>
<td>6.8mW</td>
<td>0.5mW</td>
</tr>
<tr>
<td>Static power: diff. amp. &amp; latch</td>
<td>4 x 4.3mW</td>
<td>4 x 0.3mW</td>
</tr>
<tr>
<td>Layout area</td>
<td>750μm x 520μm</td>
<td>estimate: ~500μm x 500μm</td>
</tr>
<tr>
<td>(actual area for core, logic, routing)</td>
<td></td>
<td>(~1/3 of active area, but similar passive device sizes &amp; routing)</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>400MHz</td>
<td>400MHz</td>
</tr>
<tr>
<td>(7 phases with equal spacing and 50% duty cycle)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Histograms of the 1st reference level (-150mV) from Monte Carlo simulations with 100 runs:

0.18μm CMOS

90nm CMOS
Quantizer: Summary & Conclusions

• Functionality verified through measurements
  ▪ Quantizer operated within a ΣΔ ADC prototype (0.18μm CMOS technology)

• Quantization with multi-phase clocks provides a viable alternative to typical flash quantizers in ΣΔ modulators
  ▪ Optimized for combination with a single-element PWM DAC that avoids unit element mismatch problems due to process variations
  ▪ Benefits from fast-switching transistors in modern CMOS technologies
    • For the same specifications: power of 90nm design < 10% power of 0.18μm design

• Tuning “knobs” are available to compensate for PVT variations
  ▪ Quantization levels can be shifted individually via reference voltage adjustments

• A low-jitter clock source is mandatory
  ▪ < 50ps RMS period jitter is required for the standalone 3-bit quantizer operation

Thank You.