Outline – Lecture 1

• Introduction
  ▪ Course overview
  ▪ Greetings from Northeastern University

• CMOS process variation
  ▪ Trends
  ▪ Impacts

• System-level calibration trends
  ▪ Systems-on-a-chip examples (receivers, transceivers)

• Production test simplification and cost reduction
  ▪ Example: loopback testing

• Built-in testing of analog circuits
  ▪ Introduction
  ▪ On-chip power detection
  ▪ RF LNA built-in testing example
Course Overview

• Lecture 1 – June 5, 2012
  ▪ CMOS process variation challenges
  ▪ System-level calibration trends (transceiver systems-on-a-chip examples)
  ▪ Production test simplification and cost reduction (example: loopback testing)
  ▪ Built-in testing of analog circuits

• Lecture 2 – June 6, 2012
  ▪ Digitally-assisted analog circuit design and performance tuning
  ▪ Case study: digitally-assisted linearization of operational transconductance amplifiers
  ▪ Case study: variation-aware continuous-time $\Delta\Sigma$ analog-to-digital converter design

• Lecture 3 – June 7, 2012
  ▪ On-chip DC and RF power measurements with differential temperature sensors
  ▪ Case study: differential temperature sensor design
  ▪ Temperature sensors as variation monitors
  ▪ Mismatch reduction for transistors in high-frequency differential analog signal paths
  ▪ Example: mixer design with analog tuning for transistors biased in weak inversion
Reference Book


• Includes descriptions of many concepts and projects discussed in this course
Greetings from Northeastern University

- Location: Boston, Massachusetts, USA
- Web: www.northeastern.edu
- Student population
  - Undergraduate: ~16,000
  - Graduate: ~5000
  - International: 15% (125 countries)
- Colleges and schools
  - College of Arts, Media, and Design
  - College of Business Administration
  - **College of Computer and Information Science!!!**
  - **College of Engineering!!!**
  - Bouvé College of Health Sciences
  - College of Professional Studies
  - College of Science
  - College of Social Sciences and Humanities
  - School of Law
Electrical & Computer Eng. Graduate Program

• Programs Offered (full time & part time):
  ▪ M.S. in ECE
  ▪ Ph.D. in EE and CE

• Faculty:
  ▪ 48 regular faculty members
  ▪ 11 IEEE Fellows (including 2 Life Fellows)
  ▪ 1 member of NAE
  ▪ 7 recipients of NSF/CAREER awards
  ▪ 1 recipient of Presidential Early Career Award for Scientists and Engineers

• Looking for motivated, hard-working, and well-prepared graduate students → www.ece.neu.edu
Concentrations and Research Programs

- Communication and Signal Processing
- Computer Engineering
- Control and Signal Processing
- Electromagnetics, Plasma, and Optics
- Electronic Circuits, Semiconductor Devices, and Micro-fabrication
- Power Systems, Power Electronics, and Motion Control
Research Centers and Institutes

- Bernard M. Gordon Center for Subsurface Sensing & Imaging Systems (CenSSIS)
- Center for Awareness and Localization of Explosive-Related Threats (ALERT)
- Center for Communication and Digital Signal Processing (CDSP)
- Northeastern University Center for Electrical Energy Research (NUCEER)
- Center for High-Rate Nanomanufacturing (CHN)
- Center for Microwave Magnetic Materials and Integrated Circuits (CM^3IC)
- Institute for Information Assurance (IIA)
- Institute for Complex Scientific Software (ICSS)
- Center for Ultra-wide-area Resilient Electric Energy Transmission Network (CURENT)
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Wireless Product Trends

- Support of multiple communication standards and more features
- Increasing circuit integration and system complexity per chip
- Technology optimizations for digital circuits
  → Create analog design challenges
- Increasing process-voltage-temperature (PVT) variations
  → Lower manufacturing yield and reduced reliability
Design Objectives

• Development of analog & mixed-signal circuits with extra features for integration into reliable single-chip systems
  ▪ Digitally assisted analog design
  ▪ On-chip calibration to improve performance and yield

• New built-in test capabilities with on-chip measurement circuits

• “Self-healing” integrated systems
  ▪ On-chip adjustment of parameters to maintain high performance despite of environmental changes and aging effects
  ▪ For future medical and military devices that require high reliability
“Digital intensive” System-on-Chip (SoC)
- Shrinking of transistor dimensions in complementary metal-oxide-semiconductor (CMOS) technologies
- Process variations and interferences have more impact on analog circuits
- Reduced access to internal blocks for testing
- Increased test cost
Process Variation Problems

Example: Intra-die threshold voltage variability vs. technology node

<table>
<thead>
<tr>
<th>CMOS Techn.</th>
<th>250nm</th>
<th>180nm</th>
<th>130nm</th>
<th>90nm</th>
<th>65nm</th>
<th>45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma{V_{th}} / V_{th}$</td>
<td>4.7%</td>
<td>5.8%</td>
<td>8.2%</td>
<td>9.3%</td>
<td>10.7%</td>
<td>16%</td>
</tr>
</tbody>
</table>

- Defect densities are higher in newer technologies → lower yield
- Increased intra-die variability from device scaling & dopant fluctuations
  - Yield impact on analog specifications:

Variation-Aware Design Approaches

• Based on device corner models
  ▪ Allows for analog parameter variations
  ▪ Leads to overdesign [1]

• Statistical design
  ▪ Yield estimation based on Monte Carlo simulations
  ▪ Long simulation times

• Less reliance on device matching
  ▪ Random dopant fluctuations cause threshold voltage mismatch in neighboring devices, especially below the 65nm node [2]
  ▪ On-chip variation sensing becomes more important

Larger SoC Sizes $\rightarrow$ Lower Yields

- Yields decrease as SoC integration levels increase
- Defect densities become worse with technology nodes and larger chip sizes:

Figures from:
Larger SoC Sizes $\rightarrow$ Lower Yields

- Manufacturing defects are more concentrated at the wafer edge

Figures from:
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**Image-Rejection Receivers**

- Image-rejection ratio (IRR) depends on:
  - I/Q amplitude mismatch ($\Delta A$)
  - Phase mismatch ($\Delta \theta$)

$$IRR_{(dB)} \approx 10 \cdot \log \left( \frac{4}{(\Delta \theta)^2 + (\Delta A)^2} \right)$$

- Typical IRR performance
  - Almost 60dB are required for acceptable BER performance
  - Often limited to 25dB-40dB due to mismatches
Analog DC voltage ($V_{cal}$) can be directly used to tune the bias voltages of analog circuits for mismatch compensation, resulting in high IRR (e.g. 57dB in [1]).

- I/Q mismatch compensation follows anti-aliasing rate change filter (AARCF) in this low-IF receiver example
  - Gain mismatch appears as difference in auto-correlation between I and Q
  - Phase mismatch appears as nonzero cross-correlation between I and Q
  - **Adaptive decorrelator** drives auto-correlation and cross-correlation between I and Q outputs towards zero by adjusting the correction coefficients:

\[
\omega_{I(n+1)} = \omega_{I(n)} + \mu \cdot [ u_{I(n)} u_{I(n)} - u_{Q(n)} u_{Q(n)} ] \\
\omega_{Q(n+1)} = \omega_{Q(n)} + 2 \mu \cdot u_{I(n)} u_{Q(n)}
\]

* \( \mu \) is the adaptation step size, which is inversely proportional to the signal energy

→ periodic training sequences (preambles) are required
Digital I/Q Correction Example (cont.)


- 15-20dB IRR improvement
- Convergence times in the milliseconds range

<table>
<thead>
<tr>
<th>Temperature °C</th>
<th>Phase Mismatch (degrees)</th>
<th>Gain Mismatch (Percentage)</th>
<th>Raw IRR (dB)</th>
<th>IRR after IQMC with fixed coefficients (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40</td>
<td>0.458</td>
<td>-7.83</td>
<td>27.76</td>
<td>42.3</td>
</tr>
<tr>
<td>-20</td>
<td>0.247</td>
<td>-8.2</td>
<td>27.37</td>
<td>40.3</td>
</tr>
<tr>
<td>25</td>
<td>1.037</td>
<td>-7.24</td>
<td>28.26</td>
<td>55.0</td>
</tr>
<tr>
<td>85</td>
<td>0.257</td>
<td>-7.6</td>
<td>28.05</td>
<td>41.7</td>
</tr>
</tbody>
</table>
Another Digital Receiver Calibration Example

• General calibration effectiveness
  ▪ Typical I/Q mismatch accuracy after calibration: $\Delta$gain < 0.1dB, $\Delta$phase < 1°
  ▪ Received constellation improvement to guarantee the specified bit error rate

• Reference:

64-QAM constellations with I/Q imbalance
($\Delta$phase = 10°, $\Delta$gain = 20%)

before calibration
after calibration
Loopback

- Dedicated test signal generation and true self-test
- System-level BER/EVM testing or local loopback
- Cannot be executed on-line
- Limited information regarding failure causes and fault locations
Digitally Assisted Receiver Calibration

- Emerging system-level approach
  - Analog tuning with digital-to-analog converters (DACs) → wide range, coarse
  - Digital correction → accurate
- Focus of the presented research efforts:
  - Performance adjustment features for analog circuits
  - Enable system-level calibration (self-healing) during testing and/or normal operation

higher yield & reliability
More Considerations: Digitally Assisted Calibration

- Calibration optimization
  - System-level metrics: bit error rate (BER), error vector magnitude (EVM)
  - On-chip DSP: Fast Fourier Transform (FFT)
    → enables determination of non-linearities
  - Typical limitation: no observability for individual blocks
    → unknown fault causes/locations
Transceiver Calibration: Industry Examples

- 5.2-5.8GHz 802.11a WLAN transceiver (0.18μm CMOS) – Athena Semiconductor
  - Digital I/Q mismatch correction
  - Multiple internal loopback switches for self-calibration in test mode
  - 8-bit DACs for DC offset minimization after mixers and filters

- 2.4GHz Bluetooth radio (0.35μm CMOS) – Broadcom
  - Bias networks with digital settings for LNA, mixer, filter
  - Direct tuning patent (US 7,149,488 B2) with 2 RSSIs and digital block-level bias trimming

- 2.4GHz 802.11g WLAN transceiver (0.25μm CMOS) – MuChip
  - Baseband I/Q gain and phase calibration
  - Extra analog mixer & peak detector

- Single-chip GSM/WCDMA transceiver (90nm CMOS) – Freescale Semiconductor
  - DC offset, I/Q gain & phase, IIP2 calibration in the digital signal processor
  - 6-bit DACs for analog compensation
Calibration with Enhanced Fault Coverage

- Power detectors (PDs) for built-in testing
  - Block-level fault and performance identification
  - Localized analog tuning (coarse but fast)
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Conceptual Test Economics

- Characterization phase
  - Design debug → comprehensive testing to obtain product specifications

- Production testing
  - Screening out of faulty devices based on specified limits (pass/fail)
  - Quick functionality checks with sufficient accuracy

- The commonly mentioned “Rule of Ten” for testing
  - Defect detection cost increases ~10 times at each stage of the chip assembly
  - Common practice: selective (sampled) verification at each stage
    - More economical
    - General need: improve test coverage at wafer test or enable recovery from faults/variations with calibration
Conceptual Test Economics (cont.)

• Relative test cost increase
  - Up to 40-50% of total cost for complex mixed-signal chips

• Cost reduction efforts
  - Earlier fault detection
  - Test time reduction
  - Sampled testing (high-yield products)

• Potential savings with built-in testing
  - Less inputs/outputs → lower pin count
    - ATE pin cost: $200/pin - $10,000/pin
  - Minimization of wafer test time cost
    - Range: 0.03¢/sec. (digital) - 0.07¢/sec. (analog)
  - Elimination of external RF measurement equipment → multi-site testing
    - Parallel testing of multiple dies on wafer with digital resources

Silicon Cost vs. Test Cost
Technical Manufacturing Test Issues

• System-on-chip complexity
  ▪ Verification of all functions is impractical in production testing
  ▪ Coupling and interference effects → block-level tests less reliable

• Limited access to internal nodes
  ▪ Solutions: on-chip power detectors, multiplexed outputs (low-frequency)

• Process variations
  ▪ Necessitates tuning or calibration
  ▪ Requires: measurement/estimation of critical parameters
    → analog/digital compensation

• RF test interfaces
  ▪ Sensitive to impedance matching → costly interface hardware
  ▪ Avoid RF signal capture → dedicated equipment and/or long processing times
Conventional RF Transceiver Testing

• Block-level characterization
  ▪ Design debug & characterization test phases

• System-level verification in production
  ▪ Transmitter (TX): digital baseband input (1) → RF output capture (2)
    • Basic measures: Output power (spectrum), TX gain
  ▪ Receiver (RX): RF source (3) → digital baseband output (1)
    • Basic measures: bit error rate (BER), error vector magnitude (EVM)
Conventional RF Transceiver Testing (cont.)

• Common performance tests [1]
  ▪ Test selection during production testing depends on:
    product / manufacturer / application
  ▪ TX/RX gain, RX noise figure, RX dynamic range, TX adjacent channel power ratio (ACPR), RX I/Q amplitude/phase mismatch, local oscillator rejection,…

• Higher-level tests (BER, EVM) reduce test time & cost [2], [3]
  ▪ A system-level functional test can replace:
    ◆ several lower-level tests
    ◆ block-level characterization
  ▪ BER/EVM are affected by noise figure, I/Q mismatch, etc.

• RF ATE cost
  ▪ RF measurements raise equipment and test development cost
  ▪ In terms of dollars [4]:
    ◆ Range: $100K/tester (low-speed digital) - $2M/tester (RF)
    ◆ High-volume products can require up to 20 ATE platforms
RF Transceiver Testing References

• Cited on the previous slide:


• Other useful sources:


The Loopback Method

- System-level approach
  - Only low-frequency inputs/outputs at point 1
  - Transceiver resources used for RF signal generation & modulation operations
  - ATE calculations reduced to digital comparisons

- Loopback circuitry
  - Required to match the conditions of transmitter output and receiver input

- Testing algorithms
  - Propositions based on BER calculations and spectral analysis (ref.: [A]-[G])
  - Verified with simulations or discrete components (off-chip loopback)

- On-chip loopback has further benefits
  - No high-frequency signals routed off-chip
  - Potential for transceiver self-test & calibration in the field
On-Chip Loopback Implementation

- **Basic requirements**
  - Input impedance matching
  - Attenuation
  - Frequency translation (if $f_{RX}$ ≠ $f_{TX}$)
  - Switches with high isolation

- **First switch/attenuator for loopback application [H]**
  - Switches optimized for compactness and insertion loss
  - Fixed resistive attenuator (no tuning)

- **First offset mixer [I]**
  - Optimized for suppression of unwanted RF mixing by-products
  - Quadrature mixing → single-ended PA cannot be included in test loop
  - Passive topology → max. output power -20dBm
Loopback References

• Cited on the previous slides:


• Other useful sources:


RF Front-End with On-Chip Loopback

Team at Texas A&M University:

Marvin Onabajo
Felix Fernandez
Edgar Sánchez-Sinencio
Jose Silva-Martinez
Loopback Project Overview

- Proof-of-concept RF front-end

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx frequency</td>
<td>2GHz</td>
</tr>
<tr>
<td>PA output power</td>
<td>0dBm</td>
</tr>
<tr>
<td>Rx frequency</td>
<td>2.1GHz</td>
</tr>
<tr>
<td>LNA gain</td>
<td>21dB</td>
</tr>
<tr>
<td>Mixer gain</td>
<td>6.9dB</td>
</tr>
</tbody>
</table>

- Root-mean-square (RMS) power detectors
  - To measure gains and 1-dB compression points of the RF blocks
  - To improve the test coverage and identification of fault locations

- Test coverage
  - Project focus: front-end circuits
  - In case of a fully integrated transceiver: system-level BER
Proposed Loopback Block: Overview

• Design challenges
  • Linearity (up to 0.7V swing at input)
  • Avoiding excessive mixer loss
  • Low impedance at the LNA gate node
    • This case: ~150Ω
    • High load-driving capability needed
  • Minimum die area/complexity

• Reconfigurability
  • Specs ensure compatibility with multiple standards (1.9-2.4GHz)
  • Offset mixing required if \( f_{RX} \neq f_{TX} \) (ex.: W-CDMA, CDMA2000)

Target Specifications:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input impedance</td>
<td>50Ω (matched to PA)</td>
</tr>
<tr>
<td>Tx/Rx offset frequency range</td>
<td>40-200MHz</td>
</tr>
<tr>
<td>Attenuation range (continuous)</td>
<td>10-25dB</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>&lt; 2.5GHz</td>
</tr>
<tr>
<td>Tx/Rx isolation (loopback deactivated)</td>
<td>&gt; 80dB</td>
</tr>
</tbody>
</table>

Output noise: depends on communication standard and power level
Input Stage: Switch/Fixed Attenuator

- **Switch**
  - $M_1$: low insertion loss/high linearity (large W/L) vs. high isolation (small W/L)
  - $R_G$: improves linearity (1-dB comp. pt. increase: ~4dB) & high-frequency performance
  - $M_2$: ~10dB more isolation in off-state

- **Fixed attenuator ($R_{att1}$, $R_{att2}$)**
  - Decreases signal level at mixer input → relaxed mixer linearity

![Diagram](image)
Offset Mixing with a Switching Mixer

• Goals
  ▪ Allow single-ended input from transmitter → inclusion of PA in the loop
  ▪ Digital rail-to-rail signal can be used to provide the offset signal
    (simple to generate with low-cost ATE)
  ▪ Avoid complexity → more robust

• Mixing scheme:

output components (DC removed by a blocking capacitor):

\[ A_1 \cos(\omega_{TX} t) + A_2 \cos(\omega_{TX} \pm \omega_{off} t) - A_3 \cos(\omega_{TX} \pm 3 \omega_{off} t) + ... \]

on/off switching represented with Fourier series:

\[ \frac{1}{2} + \frac{2}{\pi} \cos(\omega_{off} t) - \frac{2}{3\pi} \cos(3\omega_{off} t) + \frac{2}{5\pi} \cos(5\omega_{off} t) - ... \]
Suppression of Undesired Spectral Components

- RF feedthrough at $f_{RFin} = f_{TX}$
  - Appears as common-mode signal
  - Attenuated by the common-mode rejection property of the differential output stage in the mixer
- Unwanted components at the receiver input
  - Located $\geq 2 \times f_{offset}$ (80-400MHz) away from desired signal
  - Equal or lower power than the desired signal
  - Must be suppressed according to communication standards

**Example:** W-CDMA blocker template (tolerable interference at 10MHz offset is $>50$dB above the desired signal)
Offset Mixer Topology Development

- Simple single-balanced mixer =>
  - Differential offset signal (LO+/-)
  - Problem: voltage fluctuation from switching (at nodes x and y)

- Modified mixer core =>
  - Auxiliary branch for DC stabilization
  - M3=M1, M4=M2
  - Reversed LO+/ phase in aux. branch
Proposed Offset Mixer Topology

- 2 gain settings in the mixer core
  - $R_{L2}/R_{L3}$ activated to reduce gain
  - Range: ~14dB

- Coupling capacitor $C_{c4}$
  - Prevents DC operating point changes at nodes x/y
  - Allows use of NMOS switch instead of PMOS (lower on-resistance for same size/parasitics)

- Conversion gain

$$G_{mix\_diff} = \frac{2g_m R_L[setting]}{\pi}$$
Offset Mixer Output Stage

• Continuous gain tuning
  ▪ Load transistor \((M_L)\) is biased in triode region
  ▪ Range with \(V_{att_{ctrl}}\): \(~6\text{dB}\)

• Load-driving improvement

\[
G_{out} = \frac{g_{m6}R_{ON}(ML)}{2}
\]

• Output switch
  ▪ To disconnect loopback: \(V_{att_{ctrl}}\) high, \(V_{B3}/V_{B2}\) low

• Common-mode attenuation of RF feedthrough

\[
A_v(\omega_{RFin}) = A_{v_{cm}} = \frac{g_{m6}R_{ON}(ML)}{1 + 2g_{m6}(r_{ds}5||\frac{1}{j\omega C_p})}
\]
• UMC 0.13μm CMOS technology

• Loopback block die area
  ▪ 0.052mm²
  ▪ 40% of the combined PA, LNA, and down-conversion mixer area
  ▪ Roughly 1-4% overhead for a transceiver
Measurement Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Target</th>
<th>Simulation</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input impedance</td>
<td>50Ω</td>
<td>50Ω</td>
<td>50Ω*</td>
</tr>
<tr>
<td>Tx/Rx offset frequency range</td>
<td>40-200MHz</td>
<td>40-200MHz</td>
<td>40-200MHz</td>
</tr>
<tr>
<td>Attenuation range**</td>
<td>10-25dB</td>
<td>10.9-27.3dB</td>
<td>25.8-41.5dB</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>&lt; 2.4GHz</td>
<td>&lt; 2.4GHz</td>
<td>&lt; 2.4GHz</td>
</tr>
<tr>
<td>Tx/Rx isolation (deactivated)</td>
<td>&gt; 80dB</td>
<td>&gt; 89dB**</td>
<td>&gt; 27.4dB***</td>
</tr>
</tbody>
</table>

* On-chip resistor (subject to PVT variations)

** Not accounting for RF feedthrough via substrate, mutual inductance between bonding wires, and PCB.

*** Measurement setup does not permit verification of isolation with more certainty. (Coupling between nearby traces on the PCB: measured isolation between pins ranged from 30dB to 50dB)

• Fabrication-specific comments
  ▪ Strong PVT variations
    ♦ Gain degradation up to 10dB implied from reductions of:
      - 20% for effective RF transconductances
      - 10% for polysilicon resistors
        (in each of the two offset mixer stages)
  ▪ Coupling losses
    ♦ At the input attenuator
    ♦ Capacitors in the offset mixer

• General suggestions
  ▪ Avoid MOS capacitors
    (signal leakage to ground through parasitic capacitances)
  ▪ Design with ~10dB more gain in the loopback
    ♦ To provide sufficient margin for worst-case PVT conditions
    ♦ To allow 1-dB compression point testing for the LNA
Measured Loopback Output Spectrum

- $P_{in} = -3.5\text{dBm}$ at 2GHz
- $f_{\text{offset}} = 100\text{MHz}$ → $f_{\text{out}} = 2.1\text{GHz}$
- 25.8dB attenuation setting
- -9.9dB from buffer/cable losses
- $P_{out} = -39.2\text{dBm}$
Tuning and Frequency-Dependence

• Attenuation vs. RF frequency →
  - $\Delta$attenuation $\approx 4$dB (1.9-2.4GHz)

• Tuning range

<table>
<thead>
<tr>
<th>Control Mechanism</th>
<th>Attenuation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Discrete setting 1 (switched resistance value)</td>
<td>25.8dB</td>
</tr>
<tr>
<td>Discrete setting 2 (switched resistance value)</td>
<td>28.6dB</td>
</tr>
<tr>
<td>Discrete setting 3 (switched resistance value)</td>
<td>30.2dB</td>
</tr>
<tr>
<td>Control voltage (load transistor in triode region)</td>
<td>$+ (0$dB-$11.3$dB)</td>
</tr>
<tr>
<td>Combined</td>
<td>25.8dB-41.5dB</td>
</tr>
</tbody>
</table>

Continuous attenuation vs. control voltage ($P_{in}=-12.5$dBm, $f_{RFout}=2.1$GHz)
Summary: On-Chip Loopback Method

• Application-specific design constraints for the offset mixer
  ▪ Location between PA and LNA
  ▪ Low-frequency digital offset signal
  ▪ Minimal complexity
    → Influenced the construction of the topology

• The proposed loopback topology provides continuous attenuation control and offset mixing for transceivers in the 1.9-2.4GHz range

• Design margin for gain discrepancies due to PVT variations is critical
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Analog Built-In Testing

- Goal: on-chip extraction of performance parameters
  - Improved fault coverage
  - Enables tuning

- Benefits
  - Performance and yield improvement
  - Manufacturing test time and cost reduction

- Trade-offs
  - Possible loading effects on circuit under test (CUT)
  - Die area requirement
  - Power dissipation (particularly critical in online testing)
Built-In Test (BIT) Approaches

- Supply current sensing

- Oscillation-based testing

- Use of on-chip peak/power/RMS detectors

- Spectral analysis (on-chip FFT in DSP)

- Analog instrumentation (e.g., on-chip analog spectrum analyzer)

- ...

→ **Commonality**: BIT results must be correlated with specifications!
Envisioned On-Chip Calibration Example

- Based on on-chip FFT engine and digitally tunable analog blocks
- Project started at Northeastern University
- For low-frequency (<50MHz) appl.
- Focus: FFT area and power minimization
On-Chip Peak/Power/RMS Detectors

- Applications
  - Built-in testing
  - Received signal strength indicators (RSSIs)

- Design consideration
  - Gain
    - Linearity (1dB compression)
    - Input impedance matching

- Often used at RF frequencies when direct digitization of the signals is not feasible
• Benefits
  ▪ On-chip block-level characterization information
  ▪ Analog local tuning loops for fast coarse calibration
  ▪ Direct RF signal measurements without DSP
    (avoiding difficult high-speed digitization)
Desired power detector characteristics:

- High input impedance
- Small die area
- Large dynamic range
- Wide input frequency range
Input Impedance Considerations

\[ Z_{in} = \frac{1}{sC_c} + R_B \left[ \frac{1}{sC_{gs}} + \frac{R_{in}}{1 + sR_{in}C_{in}} \left( 1 + \frac{g_m}{sC_{gs}} \right) \right] \]

- \( Z_{in} \) reduction at RF frequencies
  - Due to input device capacitances
- Input transistor dimensions should be minimized
RMS Detector Example Circuit

Figure from:
Example RMS Detector Characteristics

- Conversion gain: 50mV/dBm
- Settling time: 40ns
- Dynamic range: 30dB

Measured DC output voltage vs. RF input power at several frequencies

Gain & 1dB-Compression Measurements

**Measured response of the RF detectors at the input and output of the LNA**

## Detector Performance Examples

### Reported Measurement Results:

<table>
<thead>
<tr>
<th>Reference</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.25μm BiCMOS</td>
<td>0.35μm CMOS</td>
<td>0.18μm CMOS</td>
<td>0.18μm CMOS</td>
</tr>
<tr>
<td>Area</td>
<td>-</td>
<td>0.031mm²</td>
<td>0.06mm²</td>
<td>-</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>40dB</td>
<td>&gt; 30dB</td>
<td>&gt; 25dB</td>
<td>~10dB</td>
</tr>
<tr>
<td>Min. Detectable Signal</td>
<td>~ -40dBm</td>
<td>-25dBm</td>
<td>-15dBm</td>
<td>50mV</td>
</tr>
<tr>
<td>Operating Frequency</td>
<td>1.3GHz</td>
<td>0.9 – 2.4GHz</td>
<td>5.2GHz</td>
<td>2.5GHz</td>
</tr>
<tr>
<td>Power</td>
<td>&lt; 1mW</td>
<td>8.6mW</td>
<td>3.5mW</td>
<td>-</td>
</tr>
</tbody>
</table>


RF Built-In Testing with Current Injection

Team at Texas A&M University:

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RF LNA Built-In Testing Example

- Input impedance measurements with on-chip power detectors
  - Detection of faults in the off-chip matching network
  - Suitable for final in-package/board-level test stages

• Voltage gain determination with sensitivity to $R_s/L_g$
  - part of the test interface hardware
    → well-controlled variation, or:
  - under test (external matching network)
    → sensitivity allows fault detection

\[
G = \frac{v_{out}}{v_{in}} = \left(\frac{1}{R_s + j\omega L_g}\right)\left(\frac{v_{out}}{i_{test}}\right)
\]
Current Injection Test Example

- To avoid impact on impedance matching:
  \[ Z_{\text{test}} \gg Z_{\text{gate}} \]

- Measurement with power detectors:
  \[ |Z_M| = \left| \frac{v_{\text{out}}}{i_{\text{test}}} \right| \]

Transimpedance gain:

\[
|Z_M| = \left| \frac{v_{\text{out}}}{i_{\text{test}}} \right| = \frac{\frac{1}{\omega C_{gs}} \left( R_s^2 + (\omega L_g)^2 \right) (g_{m1} |Z_o|)}{\sqrt{(R_s + g_{m1} \frac{L_s}{C_{gs}})^2 + (\omega(L_g + L_s) - \frac{1}{\omega C_{gs}})^2}}
\]

Voltage gain estimation:

\[
|G| = \left| \frac{v_{\text{out}}}{v_{\text{in}}} \right| = \frac{|Z_M|}{\sqrt{R_s^2 + (\omega L_g)^2}}
\]
Current Generator Circuit

- Designed with:
  - \( C_1 = m \cdot C_2 \)
  - \( |1/j\omega C_2| >> Z_{gate} \)
  - \( i_m/i_{test} \approx m \)

- Indirect measurement of \( i_{test} \) with \( R_1 \) and \( i_m \)

Layout area (without PD\(_m\)): 0.002mm\(^2\)

\[
\frac{i_m}{i_{test}} = \frac{Z_{gate} + \frac{1}{j\omega C_2}}{R_1 + \frac{1}{j\omega C_1}} = m \times \left( \frac{Z_{gate} + \frac{1}{j\omega C_2}}{mR + \frac{1}{j\omega C_2}} \right)
\]

- \( Z_{test} >> Z_{gate} \) avoids loading (\( Z_{test} > 1.1k\Omega \) for \( f < 2.4\text{GHz} \))
Post-Layout Simulation Results

Voltage-mode gain estimation:

\[ G_{V, dB} = 20 \log \left( \frac{V_{out\_rms}}{V_{g\_rms}} \times \sqrt{\frac{50^2 + (\omega \times 8.1 \times 10^{-9})^2}{2 \times 50}} \right) + 6 \]

Current-mode gain estimation (error < 1dB):

\[ G_{I, dB} = 20 \log \left( 250 \frac{V_{out\_rms}}{V_{m\_rms}} \right) - 10 \log (50^2 + (\omega \times 8.1 \times 10^{-9})^2) + 6 \]

Simulated comparison of \( S_{21} \) with \( G_v \) and \( G_i \)
Thank You.