June 5, 2012

Variation-Tolerant Design of Analog CMOS Circuits – Lecture 1

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Short Course held at:

Universitat Politècnica de Catalunya
Barcelona, Spain

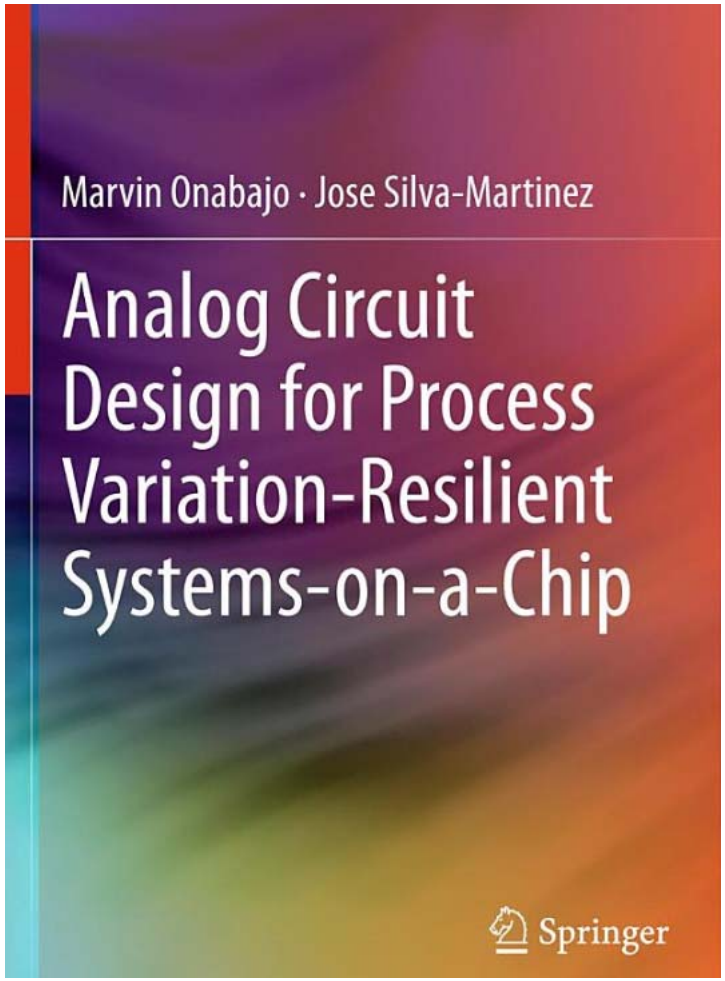
Outline – Lecture 1

- Introduction
  - Course overview
  - Greetings from Northeastern University
- CMOS process variation
  - Trends
  - Impacts
- System-level calibration trends
  - Systems-on-a-chip examples (receivers, transceivers)
- Production test simplification and cost reduction
  - Example: loopback testing
- Built-in testing of analog circuits
  - Introduction
  - On-chip power detection
  - RF LNA built-in testing example

Course Overview

- Lecture 1 – June 5, 2012
  - CMOS process variation challenges
  - System-level calibration trends (transceiver systems-on-a-chip examples)
  - Production test simplification and cost reduction (example: loopback testing)
  - Built-in testing of analog circuits
- Lecture 2 – June 6, 2012
  - Digitally-assisted analog circuit design and performance tuning
  - Case study: digitally-assisted linearization of operational transconductance amplifiers
  - Case study: variation-aware continuous-time ΔΣ analog-to-digital converter design
- Lecture 3 – June 7, 2012
  - On-chip DC and RF power measurements with differential temperature sensors
  - Case study: differential temperature sensor design
  - Temperature sensors as variation monitors
  - Mismatch reduction for transistors in high-frequency differential analog signal paths
  - Example: mixer design with analog tuning for transistors biased in weak inversion

Reference Book



- M. Onabajo and J. Silva-Martinez, Analog Circuit Design for Process Variation-Resilient Systems-on-a-Chip, Springer (**ISBN: 978-1-4614-2295-2**).

- Includes descriptions of many concepts and projects discussed in this course

Greetings from Northeastern University

- Location: Boston, Massachusetts, USA
- Web: www.northeastern.edu
- Student population
  - Undergraduate: ~16,000
  - Graduate: ~5000
  - International: 15% (125 countries)
- Colleges and schools
  - College of Arts, Media, and Design
  - College of Business Administration
  - **College of Computer and Information Science!!!**
  - **College of Engineering!!!**
  - Bouvé College of Health Sciences
  - College of Professional Studies
  - College of Science
  - College of Social Sciences and Humanities
  - School of Law

Electrical & Computer Eng. Graduate Program

- Programs Offered (full time & part time):
  - M.S. in ECE
  - Ph.D. in EE and CE

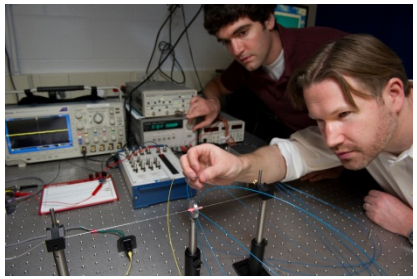
- Faculty:
  - 48 regular faculty members
  - 11 IEEE Fellows (including 2 Life Fellows)
  - 1 member of NAE
  - 7 recipients of NSF/CAREER awards
  - 1 recipient of Presidential Early Career Award for Scientists and Engineers

- Looking for motivated, hard-working, and well-prepared graduate students → www.ece.neu.edu

Concentrations and Research Programs

- Communication and Signal Processing

- Computer Engineering
- Control and Signal Processing



- Electromagnetics, Plasma, and Optics
- Electronic Circuits, Semiconductor Devices, and Micro-fabrication
- Power Systems, Power Electronics, and Motion Control

Research Centers and Institutes

- Bernard M. Gordon Center for Subsurface Sensing & Imaging Systems (CenSSIS)
- Center for Awareness and Localization of Explosive-Related Threats (ALERT)
- Center for Communication and Digital Signal Processing (CDSP)
- Northeastern University Center for Electrical Energy Research (NUCEER)
- Center for High-Rate Nanomanufacturing (CHN)
- Center for Microwave Magnetic Materials and Integrated Circuits (CM^3IC)
- Institute for Information Assurance (IIA)
- Institute for Complex Scientific Software (ICSS)
- Center for Ultra-wide-area Resilient Electric Energy Transmission Network (CURENT)

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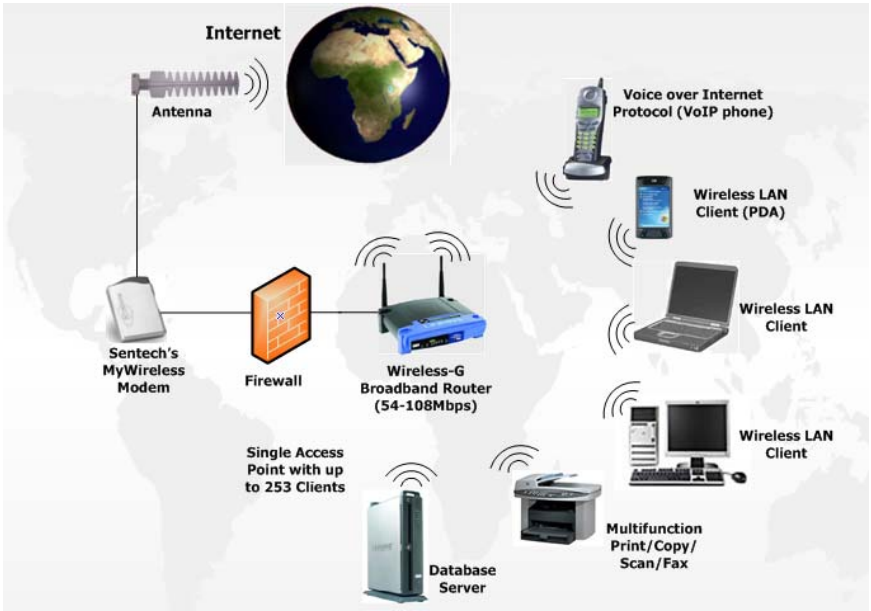
Wireless Product Trends

- Support of multiple communication standards and more features
- Increasing circuit integration and system complexity per chip
- Technology optimizations for digital circuits

  → Create analog design challenges
- Increasing process-voltage-temperature (PVT) variations

  → Lower manufacturing yield and reduced reliability

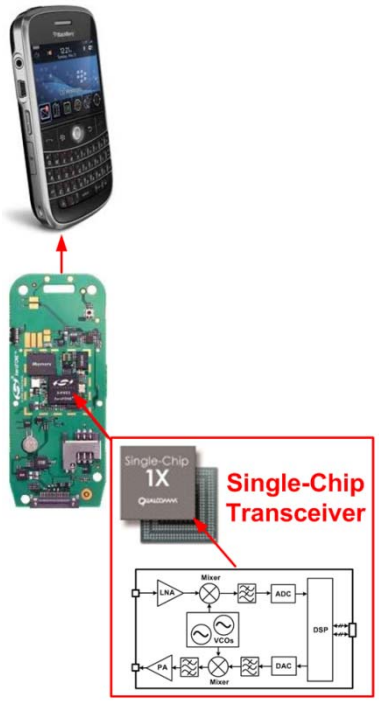


Design Objectives

- Development of analog & mixed-signal circuits with extra features for integration into reliable single-chip systems
  - Digitally assisted analog design
  - On-chip calibration to improve performance and yield
- New built-in test capabilities with on-chip measurement circuits
- “Self-healing” integrated systems
  - On-chip adjustment of parameters to maintain high performance despite of environmental changes and aging effects
  - For future medical and military devices that require high reliability

The Single-Chip Transceiver as Paradigm

- "Digital intensive" System-on-Chip (SoC)
  - Shrinking of transistor dimensions in complementary metal-oxide-semiconductor (CMOS) technologies
  - Process variations and interferences have more impact on analog circuits
  - Reduced access to internal blocks for testing
  - Increased test cost

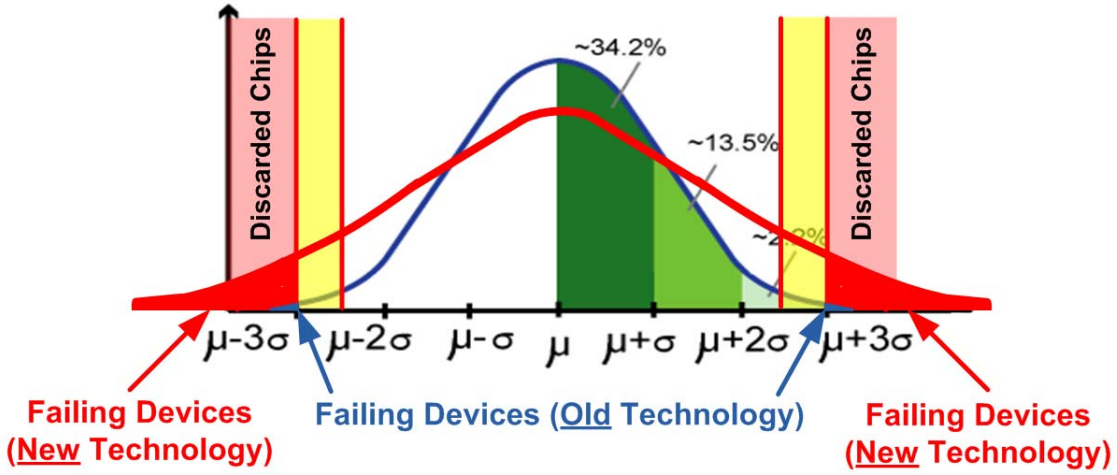


Process Variation Problems

Example: Intra-die threshold voltage variability vs. technology node

CMOS Techn.	250nm	180nm	130nm	90nm	65nm	45nm
$\sigma\{V_{th}\} / V_{th}$	4.7%	5.8%	8.2%	9.3%	10.7%	16%

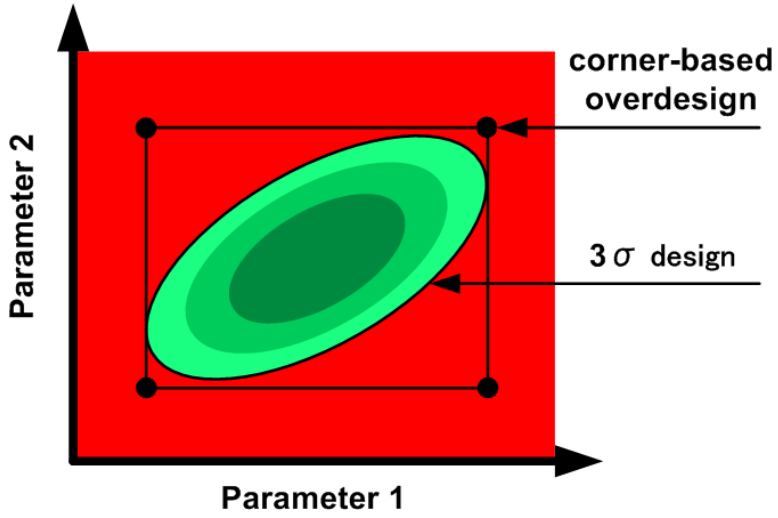
- Defect densities are higher in newer technologies → lower yield
- Increased intra-die variability from device scaling & dopant fluctuations
  - Yield impact on analog specifications:



M. Onabajo, D. Gómez, E. Aldrete-Vidrio, J. Altet, D. Mateo, and J. Silva-Martinez, "Survey of robustness enhancement techniques for wireless systems-on-a-chip and study of temperature as observable for process variations," *Springer J. Electronic Testing: Theory and Applications*, vol. 27, no. 3, pp. 225-240, June 2011.

Variation-Aware Design Approaches

- Based on device corner models
  - Allows for analog parameter variations
  - Leads to overdesign [1]
- Statistical design
  - Yield estimation based on Monte Carlo simulations
  - Long simulation times



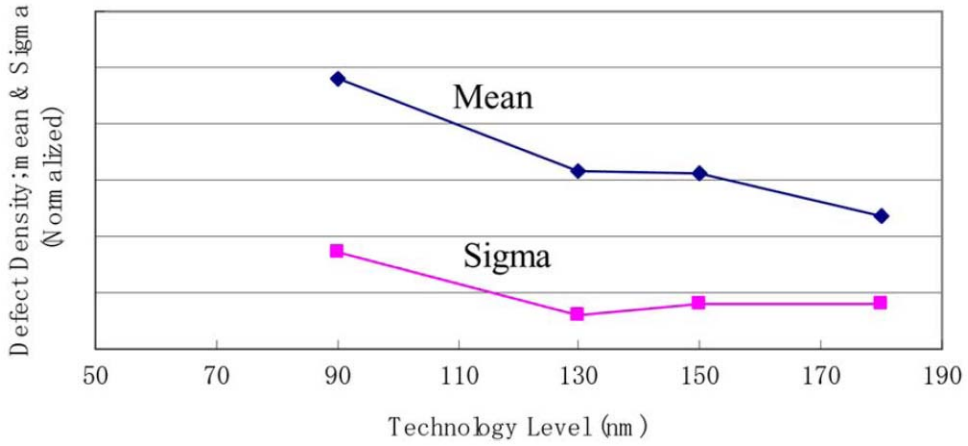
- Less reliance on device matching
  - Random dopant fluctuations cause threshold voltage mismatch in neighboring devices, especially below the 65nm node [2]
  - On-chip variation sensing becomes more important

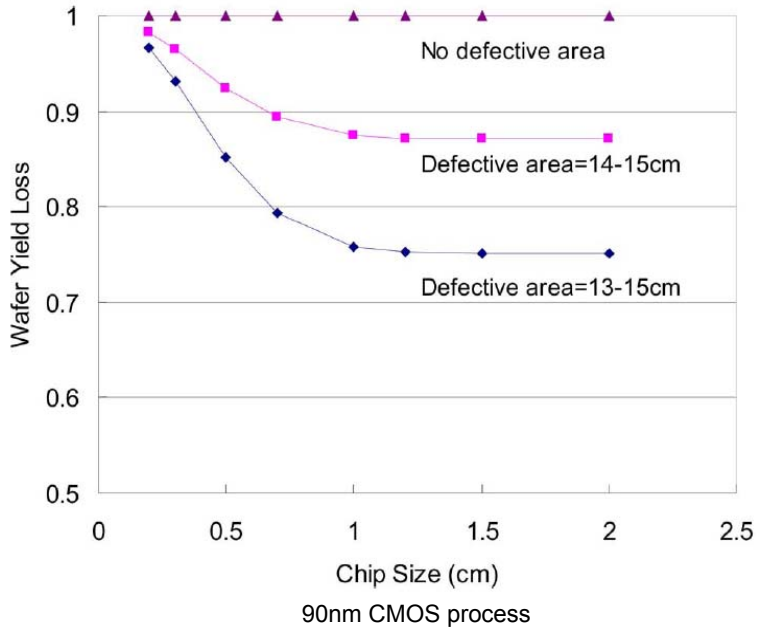
[1] G. G. E. Gielen, "Design methodologies and tools for circuit design in CMOS nanometer technologies," in *Proc. 36th European Solid-State Device Research Conference (ESSDERC)*, pp. 21-32, Sept. 2006.
[2] K. Agarwal, J. Hayes, and S. Nassif, "Fast characterization of threshold voltage fluctuation in MOS devices," *IEEE Trans. Semiconductor Manufacturing*, vol. 21, no. 4, pp. 526-533, Nov. 2008.

Larger SoC Sizes → Lower Yields

- Yields decrease as SoC integration levels increase

- Defect densities become worse with technology nodes and larger chip sizes:



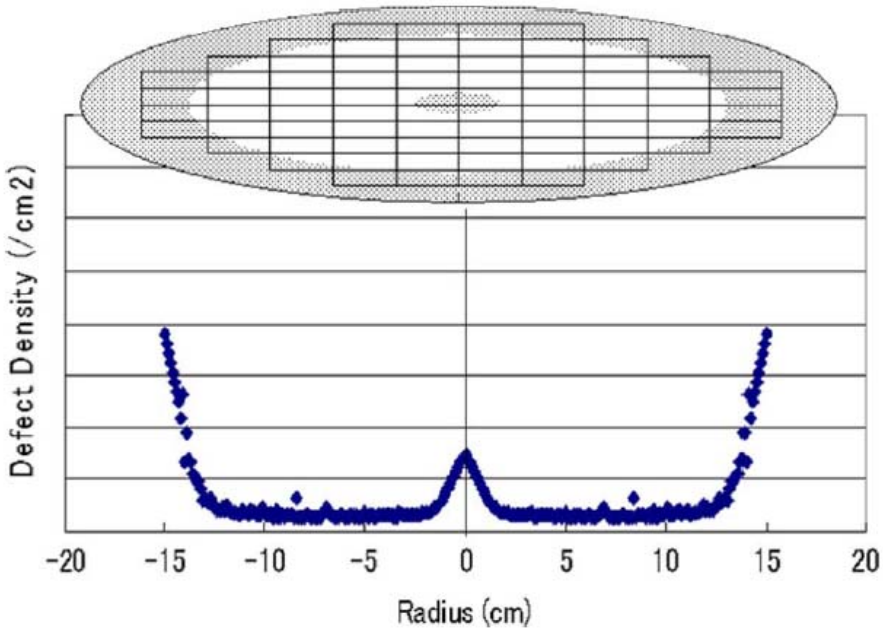


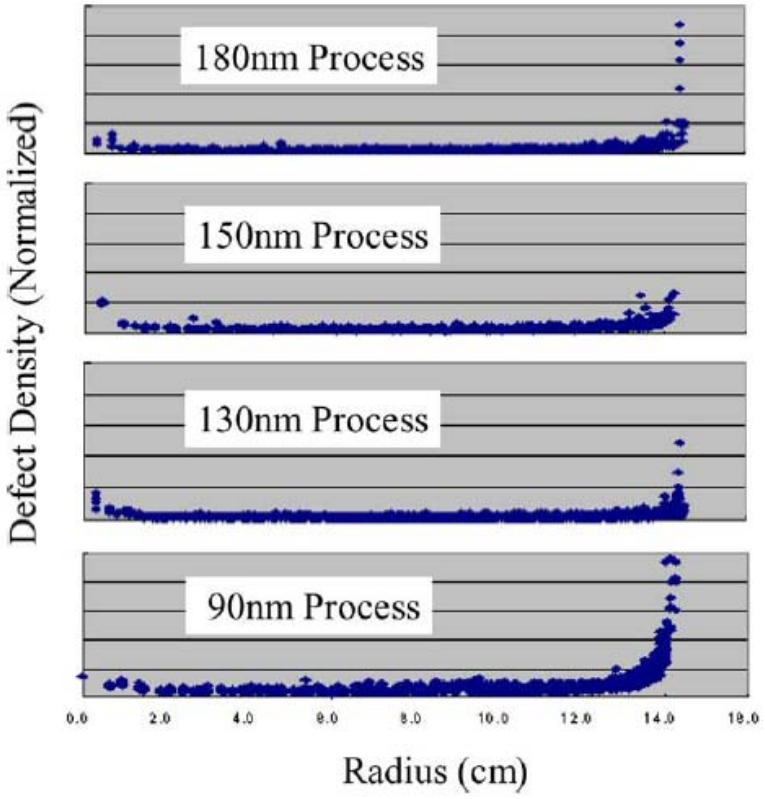
90nm CMOS process

Figures from:
H. Masuda, M. Tsunozaki, T. Tsutsui, H. Nunogami, A. Uchida, and K. Tsunokuni, "A Novel Wafer-Yield PDF Model and Verification With 90-180nm SOC Chips," *IEEE Trans. Semiconductor Manuf.*, vol. 21, no. 4, pp. 585-591, Nov. 2008.

Larger SoC Sizes → Lower Yields

- Manufacturing defects are more concentrated at the wafer edge





Figures from:
H. Masuda, M. Tsunozaki, T. Tsutsui, H. Nunogami, A. Uchida, and K. Tsunokuni, "A Novel Wafer-Yield PDF Model and Verification With 90-180nm SOC Chips," *IEEE Trans. Semiconductor Manuf.*, vol. 21, no. 4, pp. 585-591, Nov. 2008.

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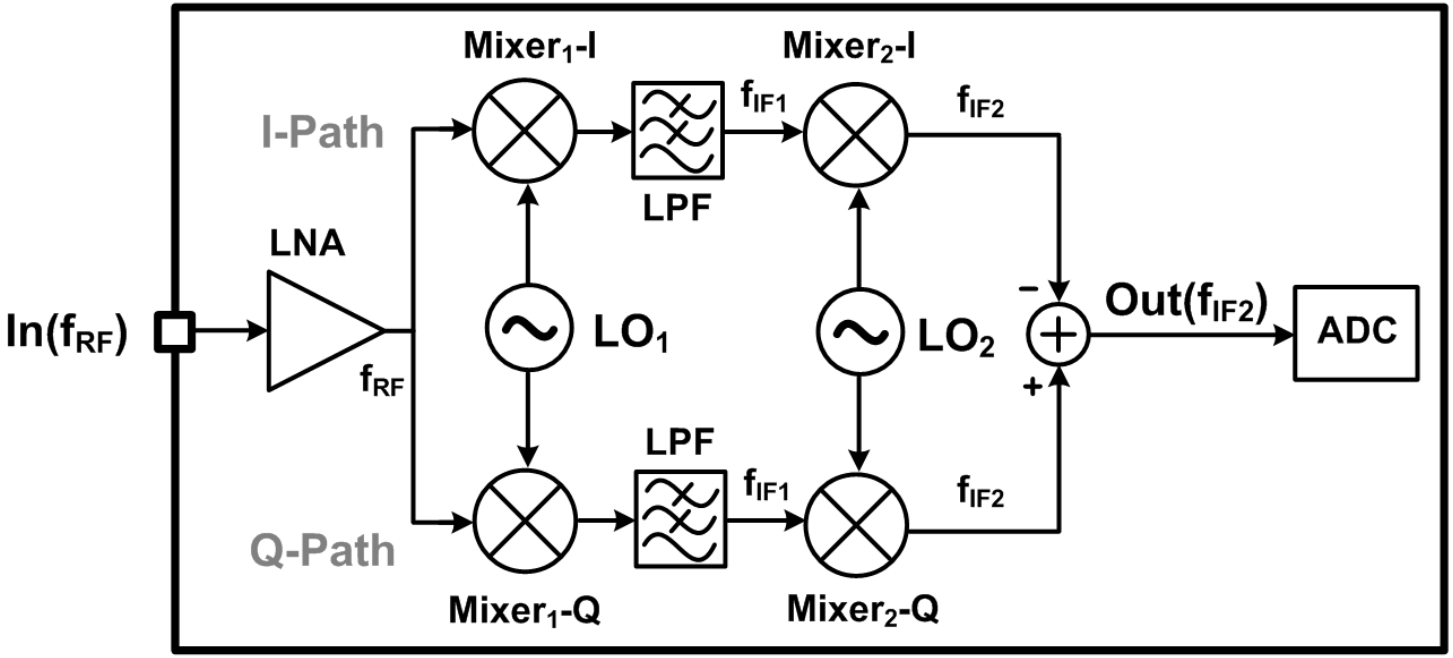
Image-Rejection Receivers



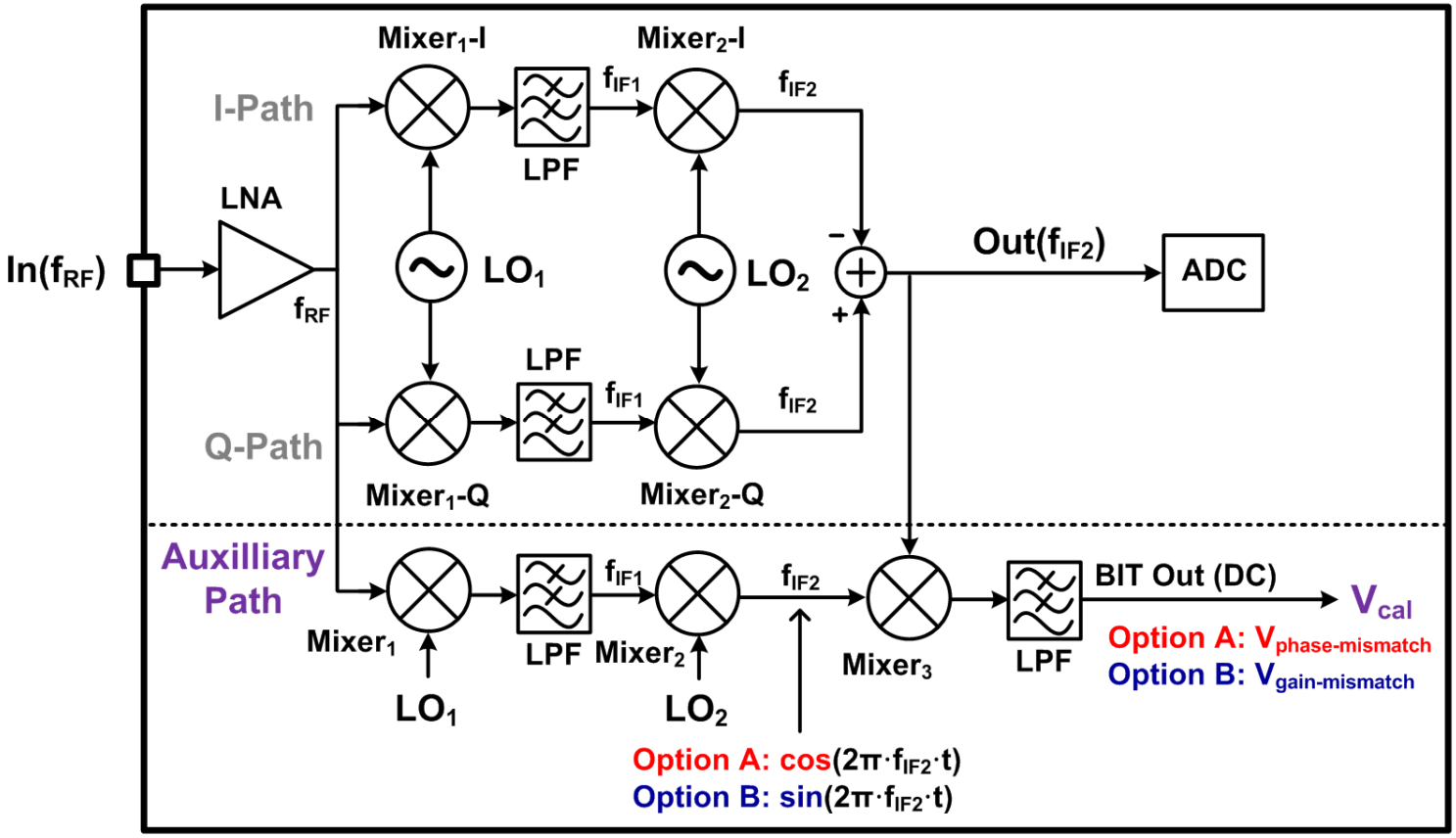
- Image-rejection ratio (IRR) depends on:
  - I/Q amplitude mismatch (ΔA)
  - Phase mismatch (Δθ)

$$IRR_{(dB)} \approx 10 \cdot \log\left(\frac{4}{(\Delta\theta)^2 + (\Delta A)^2}\right)$$

- Typical IRR performance
  - Almost 60dB are required for acceptable BER performance
  - Often limited to 25dB-40dB due to mismatches

Analog I/Q Calibration for Image-Rejection Receivers

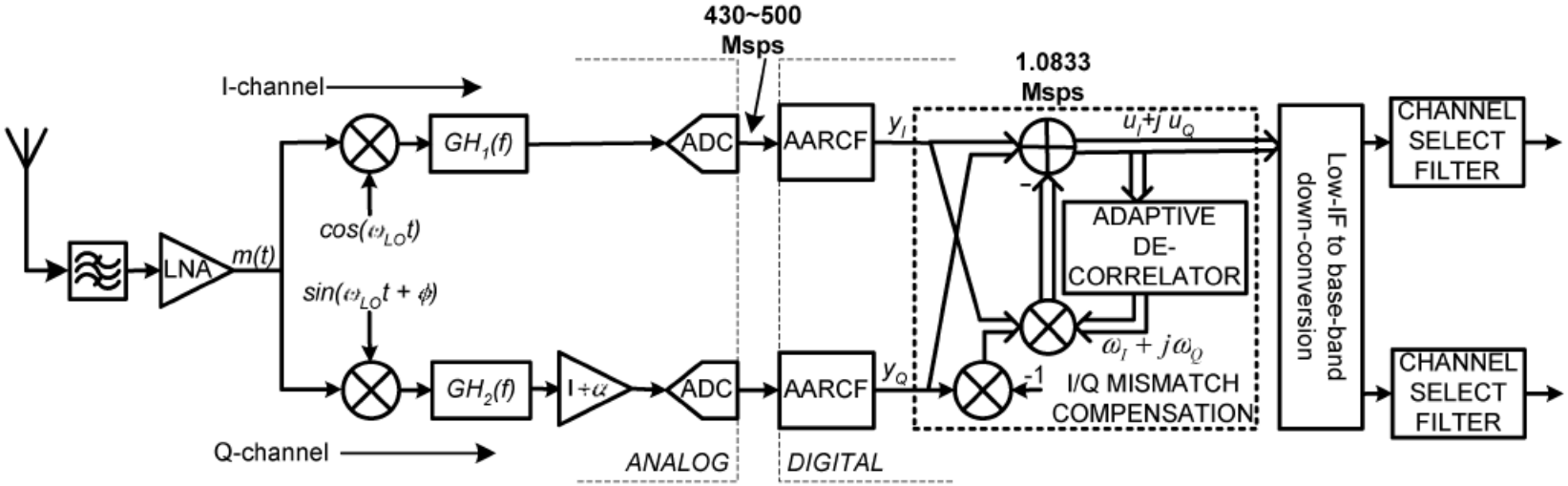
[1] R. Montemayor and B. Razavi, "A self-calibrating 900-MHz CMOS image-reject receiver," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sept. 2000, pp. 320-323.



- Analog DC voltage (V_{cal}) can be directly used to tune the bias voltages of analog circuits for mismatch compensation, resulting in high IRR (e.g. 57dB in [1])

Digital I/Q Correction Example

I. Elahi, K. Muhammad, and P. T. Balsara, "I/Q mismatch compensation using adaptive decorrelation in a low-IF receiver in 90-nm CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 395-404, Feb. 2006.



- I/Q mismatch compensation follows anti-aliasing rate change filter (AARCF) in this low-IF receiver example
  - Gain mismatch appears as difference in auto-correlation between I and Q
  - Phase mismatch appears as nonzero cross-correlation between I and Q
  - **Adaptive decorrelator** drives auto-correlation and cross-correlation between I and Q outputs towards zero by adjusting the correction coefficients:

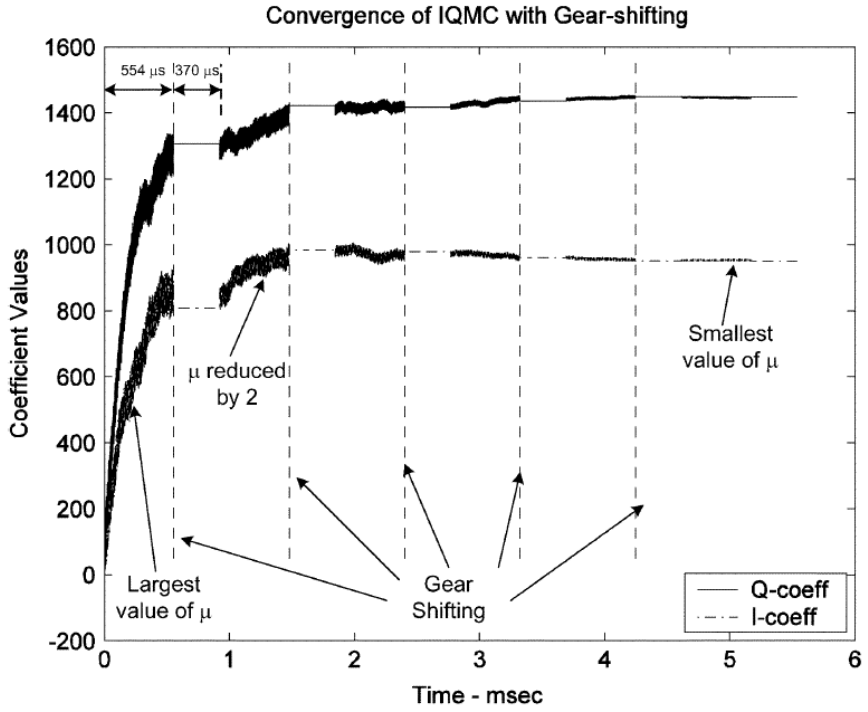
$$\omega_{I(n+1)} = \omega_{I(n)} + \mu\cdot[\, u_{I(n)}\, u_{I(n)} - u_{Q(n)}\, u_{Q(n)}\,]$$
$$\omega_{Q(n+1)} = \omega_{Q(n)} + 2\,\mu \cdot u_{I(n)}\, u_{Q(n)}$$

  * μ is the adaptation step size, which is inversely proportional to the signal energy
    → periodic training sequences (preambles) are required

Digital I/Q Correction Example (cont.)

I. Elahi, K. Muhammad, and P. T. Balsara, "I/Q mismatch compensation using adaptive decorrelation in a low-IF receiver in 90-nm CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 395-404, Feb. 2006.

- 15-20dB IRR improvement
- Convergence times in the milliseconds range



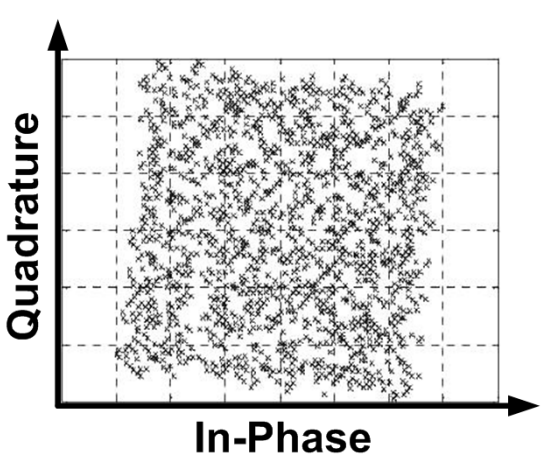
Temperature °C	Phase Mismatch degrees	Gain Mismatch (Percentage)	Raw IRR (dB)	IRR after IQMC with fixed coefficients (dB)
-40	0.458	-7.83	27.76	42.3
-20	0.247	-8.2	27.37	40.3
25	1.037	-7.24	28.26	55.0
85	0.257	-7.6	28.05	41.7

Another Digital Receiver Calibration Example

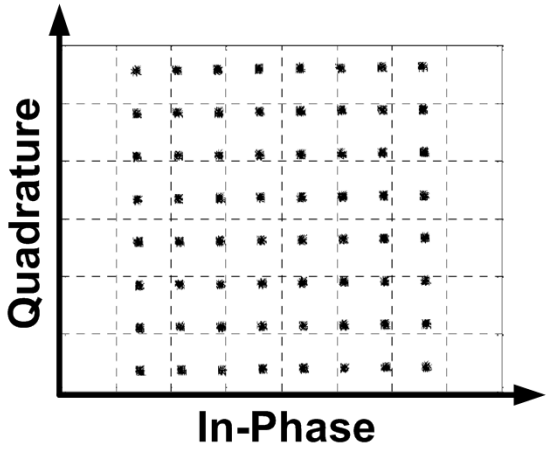
- General calibration effectiveness
  - Typical I/Q mismatch accuracy after calibration: Δgain < 0.1dB , Δphase < 1º
  - Received constellation improvement to guarantee the specified bit error rate

- Reference:
  - K.-H. Lin, H.-L. Lin, S.-M. Wang, R. C. Chang, "Implementation of digital IQ imbalance compensation in OFDM WLAN receivers," in *Proc. IEEE Intl. Symp. on Circuits and Systems*, pp. 3534-3537, 2006.

64-QAM constellations with I/Q imbalance
(Δphase = 10º, Δgain = 20%)

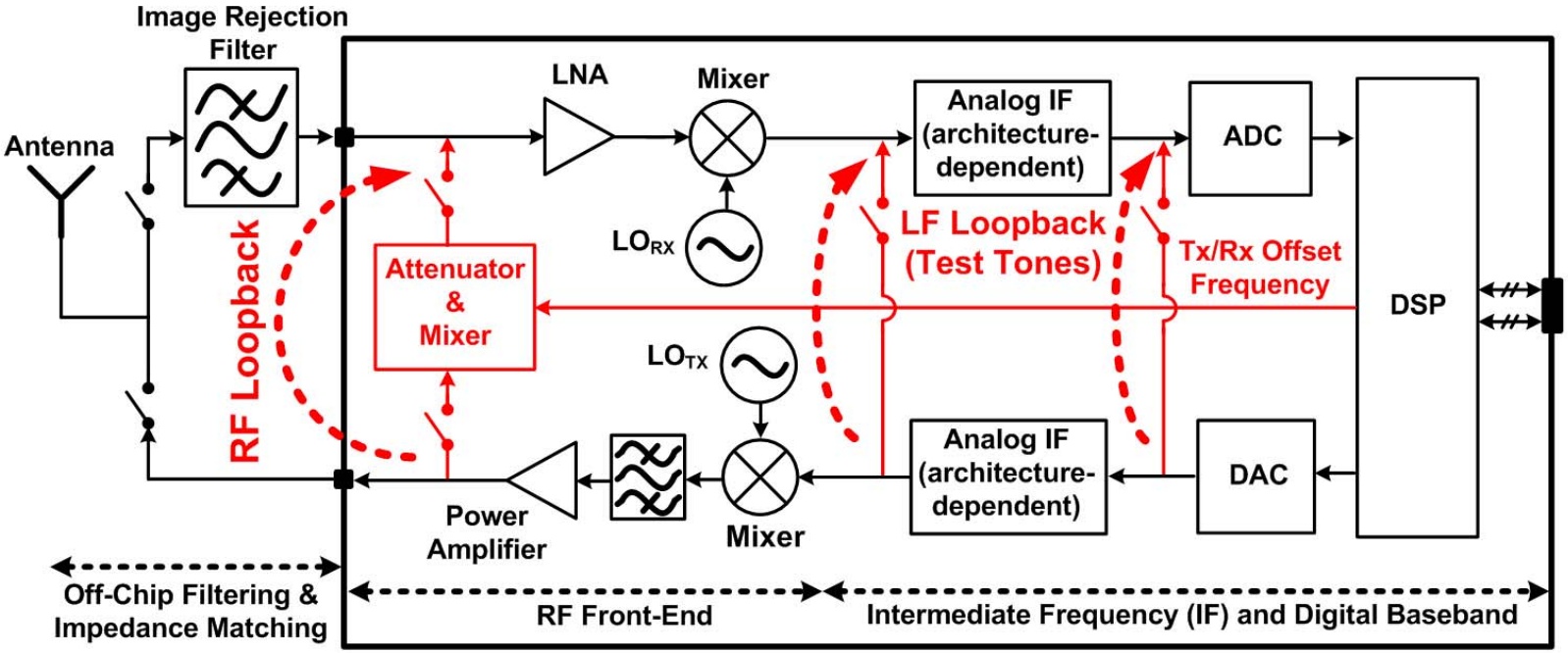


before calibration



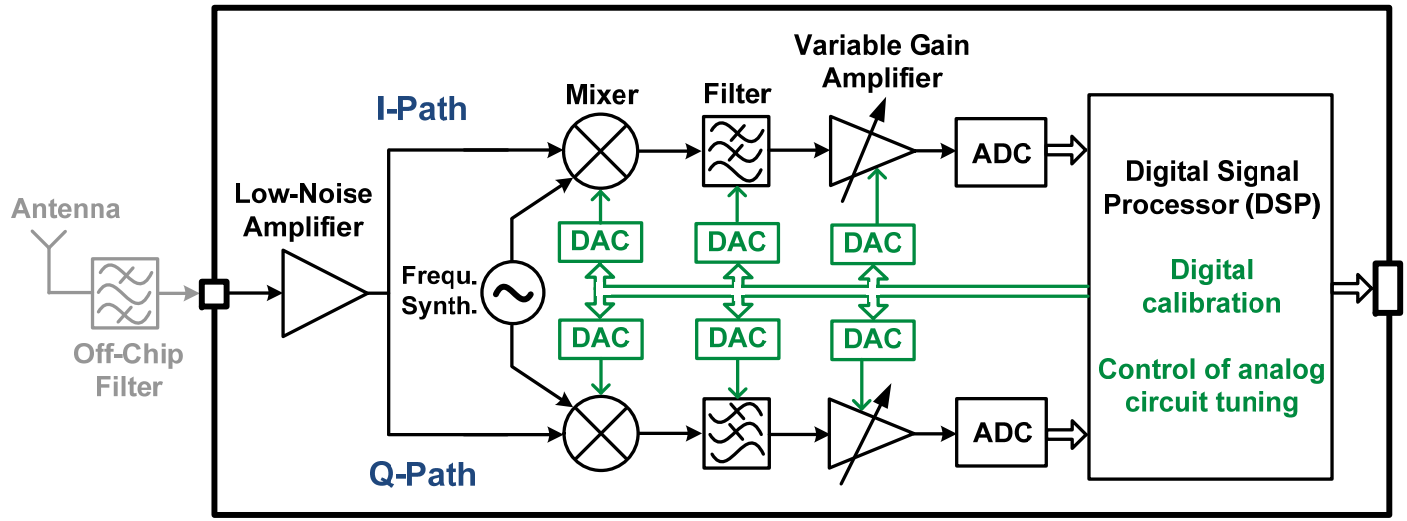
after calibration

Loopback



- Dedicated test signal generation and true self-test
- System-level BER/EVM testing or local loopback
- Cannot be executed on-line
- Limited information regarding failure causes and fault locations

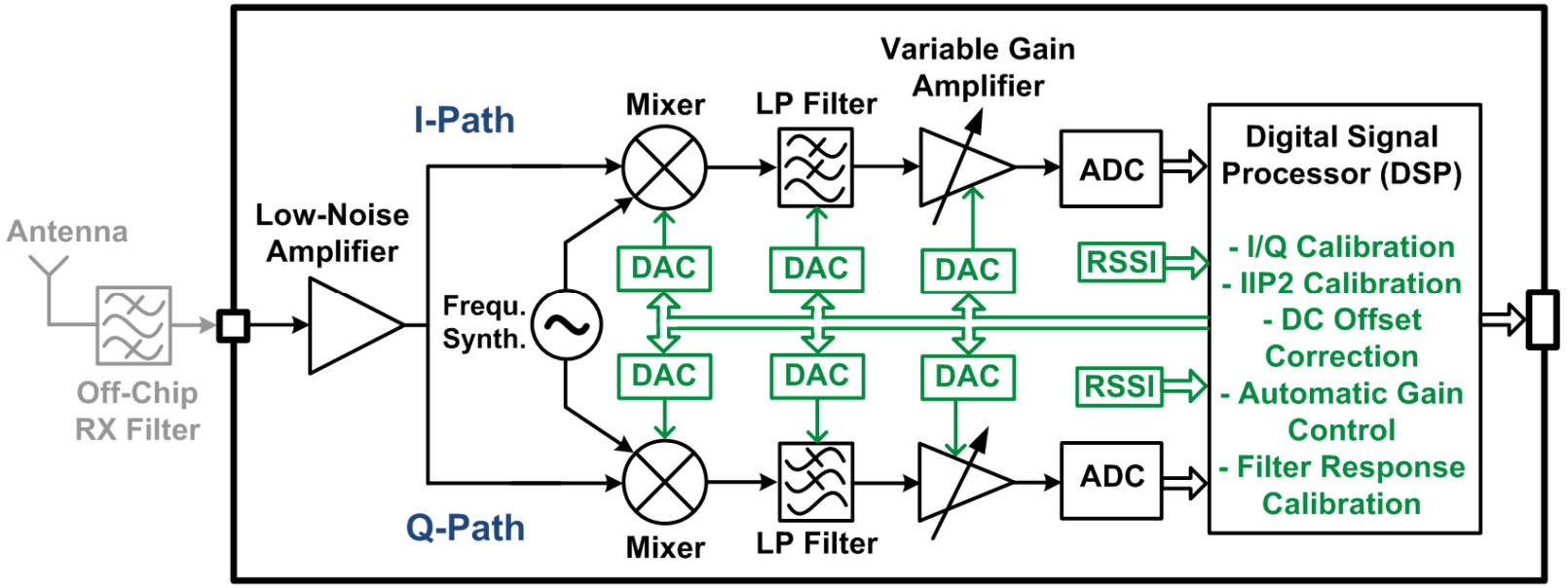
Digitally Assisted Receiver Calibration



- Emerging system-level approach
  - Analog tuning with digital-to-analog converters (DACs) → wide range, coarse
  - Digital correction → accurate
- Focus of the presented research efforts:
  - Performance adjustment features for analog circuits
  - Enable system-level calibration (self-healing) during testing and/or normal operation

} higher yield & reliability

More Considerations: Digitally Assisted Calibration



- Calibration optimization
  - System-level metrics: bit error rate (BER), error vector magnitude (EVM)
  - On-chip DSP: Fast Fourier Transform (FFT)

    → enables determination of non-linearities
  - Typical limitation: no observability for individual blocks

    → unknown fault causes/locations

Transceiver Calibration: Industry Examples

- 5.2-5.8GHz 802.11a WLAN transceiver (0.18µm CMOS) – Athena Semiconductor
  - Digital I/Q mismatch correction
  - Multiple internal loopback switches for self-calibration in test mode
  - 8-bit DACs for DC offset minimization after mixers and filters

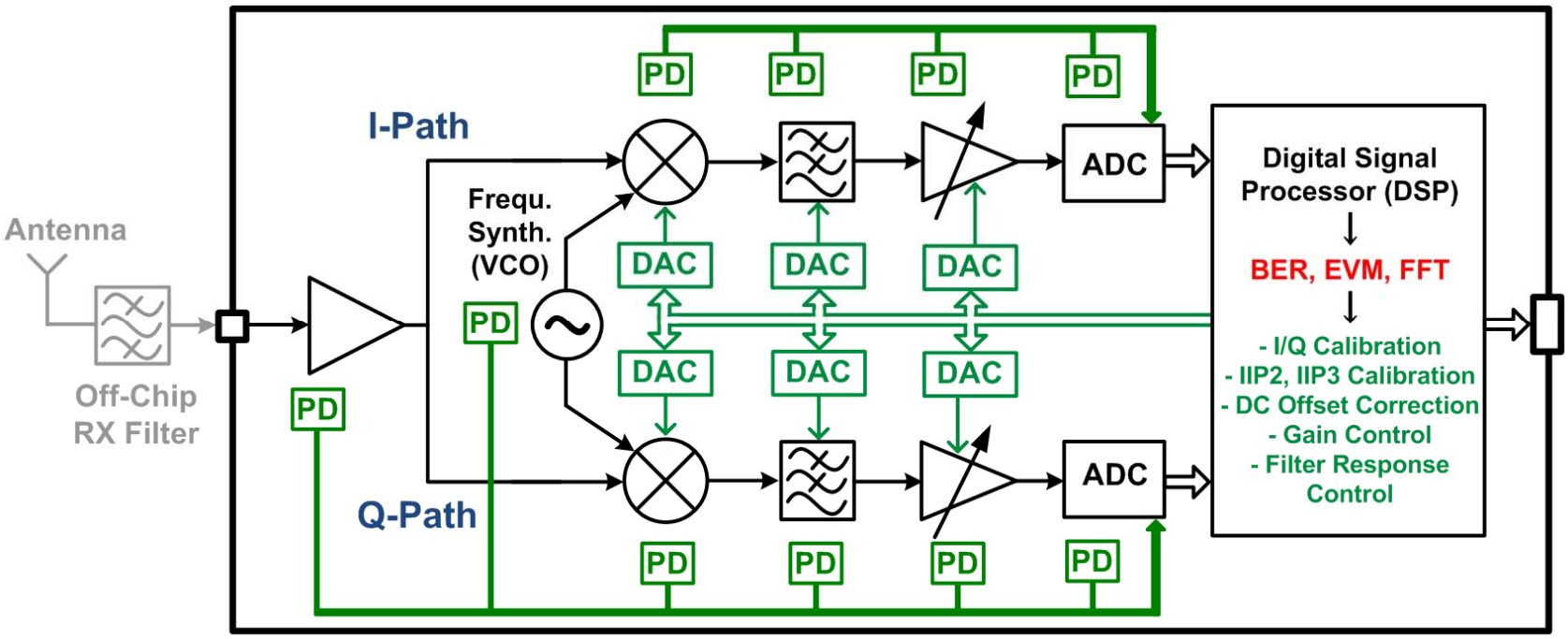
  I. Vassiliou, et. al., "A single-chip digitally calibrated 5.15-5.825-GHz 0.18-µm CMOS transceiver for 802.11a wireless LAN," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2221-2231, Dec. 2003.
- 2.4GHz Bluetooth radio (0.35µm CMOS) – Broadcom
  - Bias networks with digital settings for LNA, mixer, filter
  - Direct tuning patent (US 7,149,488 B2) with 2 RSSIs and digital block-level bias trimming

  H. Darabi, et. al., "A dual-mode 802.11b/bluetooth radio in 0.35-µm CMOS," Solid-State Circuits, *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 698-706, March 2005.
- 2.4GHz 802.11g WLAN transceiver (0.25µm CMOS) – MuChip
  - Baseband I/Q gain and phase calibration
  - Extra analog mixer & peak detector

  Y.-H. Hsieh, et. al., "An auto-I/Q calibrated CMOS transceiver for 802.11g," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2187-2192, Nov. 2005.
- Single-chip GSM/WCDMA transceiver (90nm CMOS) – Freescale Semiconductor
  - DC offset, I/Q gain & phase, IIP2 calibration in the digital signal processor
  - 6-bit DACs for analog compensation

  D. Kaczman, et. al., “A Single-Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver With DigRF 3G Interface and +90 dBm IIP2,” *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 718-739, March 2009.

Calibration with Enhanced Fault Coverage



- Power detectors (PDs) for built-in testing
  - Block-level fault and performance identification
  - Localized analog tuning (coarse but fast)

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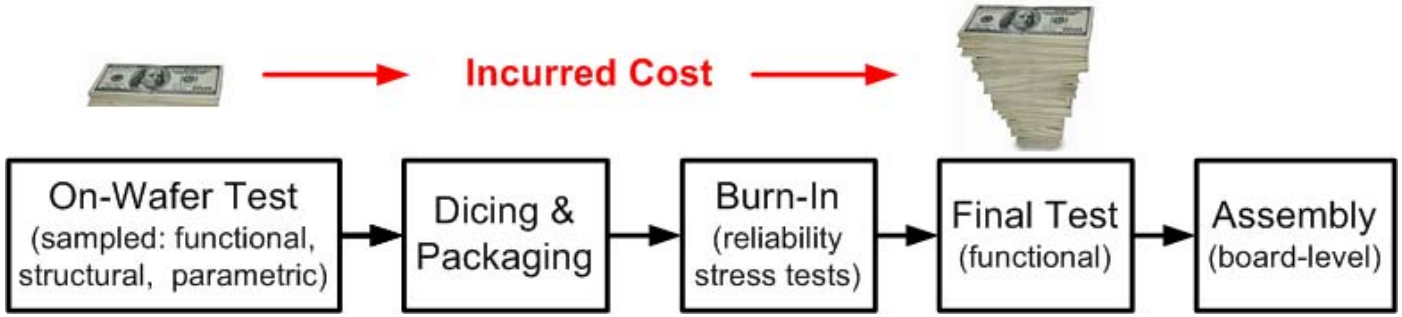
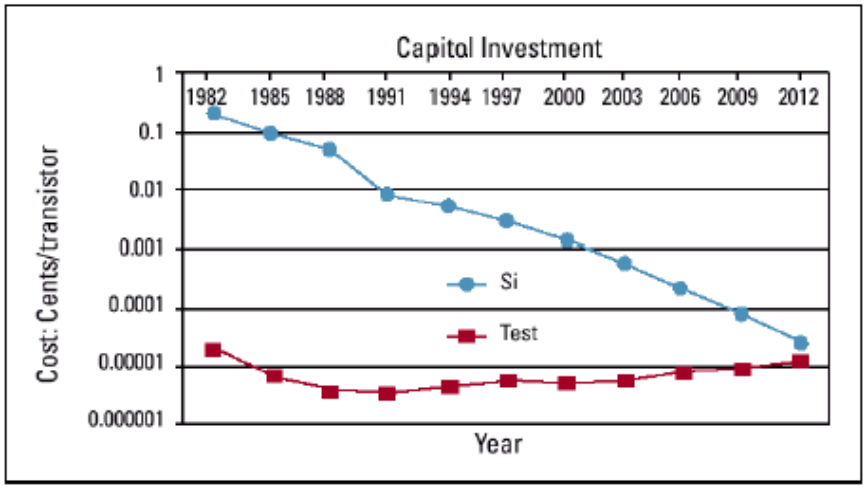
Conceptual Test Economics

- Characterization phase
  - Design debug → comprehensive testing to obtain product specifications
- Production testing
  - Screening out of faulty devices based on specified limits (pass/fail)
  - Quick functionality checks with sufficient accuracy
- The commonly mentioned “Rule of Ten” for testing
  - Defect detection cost increases ~10 times at each stage of the chip assembly
  - Common practice: selective (sampled) verification at each stage
    - More economical
    - General need: improve test coverage at wafer test or enable recovery from faults/variations with calibration



Conceptual Test Economics (cont.)

- Relative test cost increase
  - Up to 40-50% of total cost for complex mixed-signal chips
- Cost reduction efforts
  - Earlier fault detection
  - Test time reduction
  - Sampled testing (high-yield products)
- Potential savings with built-in testing
  - Less inputs/outputs → lower pin count
    - ATE pin cost: $200/pin - $10,000/pin
  - Minimization of wafer test time cost
    - Range: 0.03¢/sec. (digital) - 0.07¢/sec. (analog)
  - Elimination of external RF measurement equipment → multi-site testing
    - Parallel testing of multiple dies on wafer with digital resources



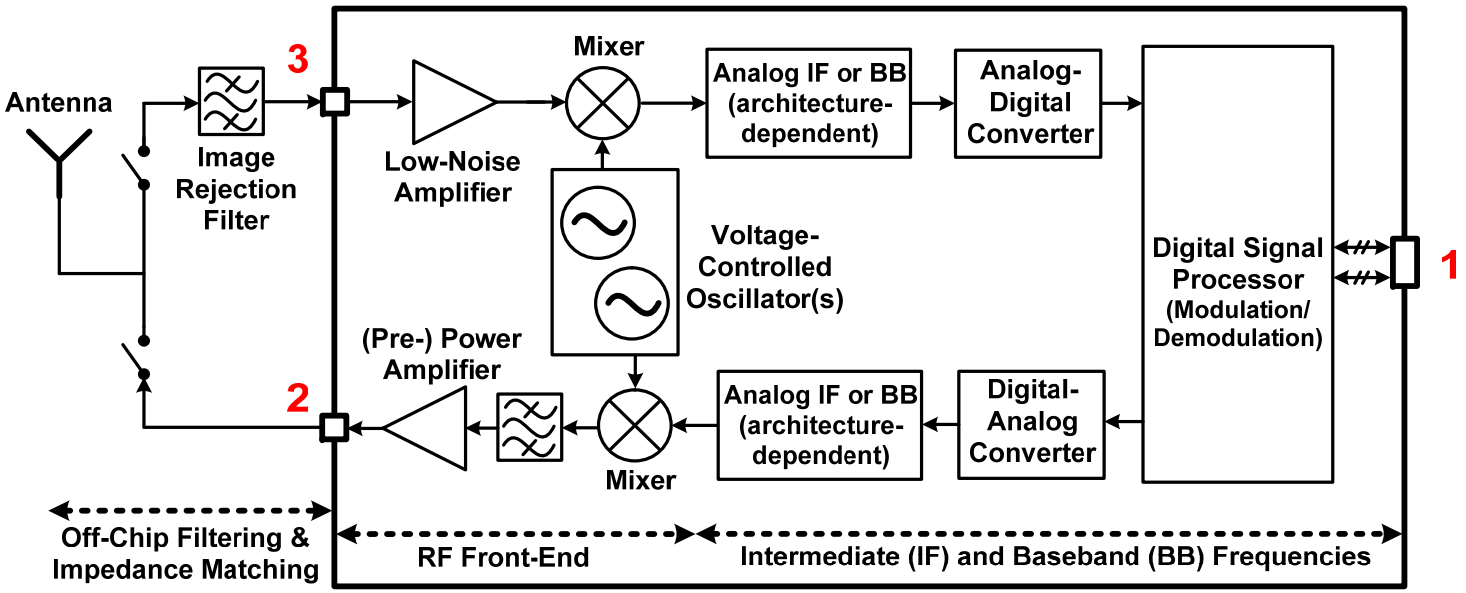
Silicon Cost vs. Test Cost
(source: National Instruments Corp., http://zone.ni.com/devzone/cda/tut/p/id/2869)

Technical Manufacturing Test Issues

- System-on-chip complexity
  - Verification of all functions is impractical in production testing
  - Coupling and interference effects → block-level tests less reliable
- Limited access to internal nodes
  - Solutions: on-chip power detectors, multiplexed outputs (low-frequency)
- Process variations
  - Necessitates tuning or calibration
  - Requires: measurement/estimation of critical parameters
    → analog/digital compensation
- RF test interfaces
  - Sensitive to impedance matching → costly interface hardware
  - Avoid RF signal capture → dedicated equipment and/or long processing times

Conventional RF Transceiver Testing

- Block-level characterization
  - Design debug & characterization test phases
- System-level verification in production
  - Transmitter (TX): digital baseband input (1) → RF output capture (2)
    - Basic measures: Output power (spectrum), TX gain
  - Receiver (RX): RF source (3) → digital baseband output (1)
    - Basic measures: bit error rate (BER), error vector magnitude (EVM)



Conventional RF Transceiver Testing (cont.)

- Common performance tests [1]
  - Test selection during production testing depends on:
    product / manufacturer / application
  - TX/RX gain, RX noise figure, RX dynamic range, TX adjacent channel power ratio (ACPR), RX I/Q amplitude/phase mismatch, local oscillator rejection,…
- Higher-level tests (BER, EVM) reduce test time & cost [2], [3]
  - A system-level functional test can replace:
    - several lower-level tests
    - block-level characterization
  - BER/EVM are affected by noise figure, I/Q mismatch, etc.
- RF ATE cost
  - RF measurements raise equipment and test development cost
  - In terms of dollars [4]:
    - Range: $100K/tester (low-speed digital) - $2M/tester (RF)
    - High-volume products can require up to 20 ATE platforms

RF Transceiver Testing References

- Cited on the previous slide:

[1] K. B. Schaub, J. Kelly, *Production Testing of RF and System-on-a-Chip Devices for Wireless Communications*, Boston, MA: Artech House, 2004.

[2] E. Lowery, "Integrated Cellular Transceivers: Challenging Traditional Test Philosophies," *Proc. of the 28th Annual IEEE/SEMI International Electronics Manufacturing Tech. Symposium*, pp. 427-436, July 2003.

[3] A. Halder and A. Chatterjee, "Low-Cost Alternate EVM Test for Wireless Receiver Systems," *Proc. of the 23rd VLSI Test Symposium*, pp. 255-260, May 2005.

[4] J. Ferrario, R. Wolf, S. Moss, "Architecting Millisecond Test Solutions for Wireless Phone RFIC's," *Proc. of the International Test Conference*, vol. 1, pp. 1325-1332, October 2003.

- Other useful sources:

[5] M. Burns, G. W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*, New York, NY: Oxford University Press, 2001.

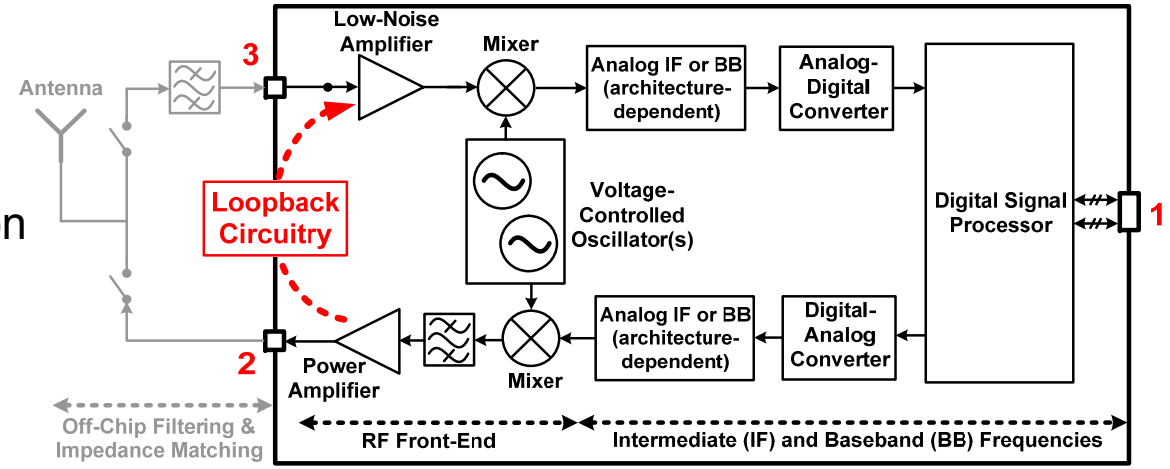
[6] M. Jarwala, D. Le, M. S. Heutmaker, "End-to-End Test Strategy for Wireless Systems", *Proc. of the International Test Conference*, pp. 940-946, October 1995.

[7] M. Onabajo, F. Fernandez, J. Silva-Martinez, and E. Sánchez-Sinencio, "Strategic test cost reduction with on-chip measurement circuitry for RF transceiver front-ends – an overview," in *Proc. 49th IEEE Intl. Midwest Symp. on Circuits and Systems*, vol. 2, pp. 643-647, Aug. 2006.

[8] O. Eliezer, R. B. Staszewski, and D. Mannath, "A statistical approach for design and testing of analog circuitry in low-cost SoCs." in *Proc. IEEE Intl. Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2010, pp. 461-464.

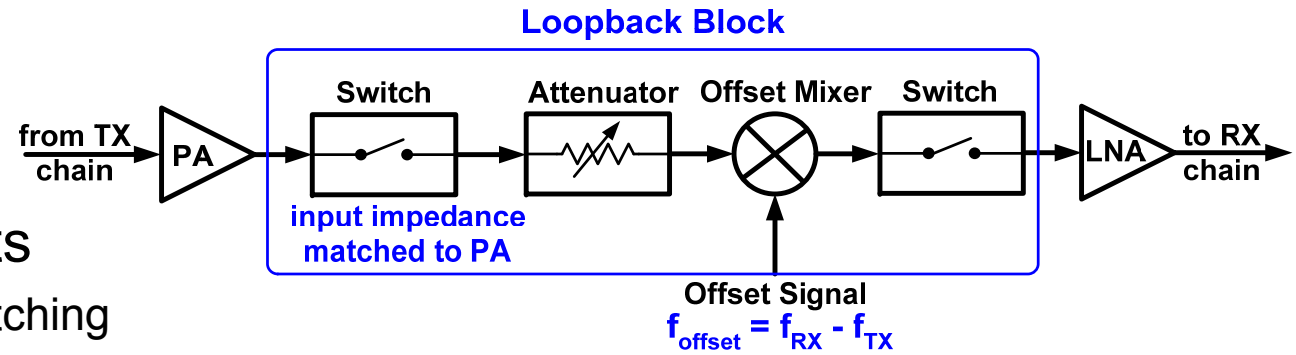
The Loopback Method

- System-level approach
  - Only low-frequency inputs/outputs at point 1
  - Transceiver resources used for RF signal generation & modulation operations
  - ATE calculations reduced to digital comparisons



- Loopback circuitry
  - Required to match the conditions of transmitter output and receiver input
- Testing algorithms
  - Propositions based on BER calculations and spectral analysis (ref.: [A]-[G])
  - Verified with simulations or discrete components (off-chip loopback)
- On-chip loopback has further benefits
  - No high-frequency signals routed off-chip
  - Potential for transceiver self-test & calibration in the field

On-Chip Loopback Implementation



- Basic requirements
  - Input impedance matching
  - Attenuation
  - Frequency translation (if $f_{RX} \neq f_{TX}$)
  - Switches with high isolation
- First switch/attenuator for loopback application [H]
  - Switches optimized for compactness and insertion loss
  - Fixed resistive attenuator (no tuning)
- First offset mixer [I]
  - Optimized for suppression of unwanted RF mixing by-products
  - Quadrature mixing → single-ended PA cannot be included in test loop
  - Passive topology → max. output power -20dBm

Loopback References

- Cited on the previous slides:

[A] M. Jarwala, D. Le, M. S. Heutmaker, "End-to-End Test Strategy for Wireless Systems", *Proc. of the International Test Conference*, pp. 940-946, October 1995.

[B] B. R. Veillette, G. W. Roberts, "A built-in self-test strategy for wireless communication systems", *Proc. of the International Test Conference*, pp. 930-939, October 1995.

[C] J. Dabrowski, "Loopback BIST for RF front-ends in digital transceivers", *Proc. of the Intl. Symposium for System-on-Chip*, pp. 143-146, November 2003.

[D] D. Lupea, U. Pursche, and H.-J. Jentschel, "RF-BIST: Loopback Spectral Signature Analysis," *Proc. of the Design, Automation, and Test in Europe Conference and Exhibition*, pp. 478-483, 2003.

[E] A. Haider, S. Bhattacharya, G. Srinivasan, and A. Chatterjee, "A system-level alternate test approach for specification test of RF transceivers in loopback mode," *Proc. of the 18th International Conference on VLSI Design*, pp. 289-294, January 2005.

[F] M. Negreiros, L. Carro, A. A. Susin, "An Improved RF Loopback for Test Time Reduction", *Proc. of the Design, Automation, and Test in Europe Conference and Exhibition*, March 2006.

[G] G. Srinivasan, A. Chatterjee, F. Taenzler, "Alternate loop-back diagnostic tests for wafer-level diagnosis of modern wireless transceivers using spectral signatures", *Proc. of the 24th VLSI Test Symposium*, May 2006.

[H] J.-S. Yoon and W. R. Eisenstadt, "Embedded loopback test for RF ICs," *IEEE Transactions on Instrumentation and Measurement*, pp. 1715-1720, Oct. 2005.

[I] S. Bota, E. Garcia-Moreno, E. Isern, R. Picos, M. Roca, K. Suenaga, "Compact Frequency Offset Circuit for Testing IC RF Transceivers," *Proc. of the 8th International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 2125-2128, October 2006.

- Other useful sources:

[J] J. J. Dabrowski and R. M. Ramzan, "Built-in loopback test for IC RF transceivers," IEEE. Trans. Very Large Scale Integration (VLSI) Systems, vol. 18, no. 6, pp. 933-946, June 2010.

[K] H. Shin, J. Park, J. A. Abraham, "Spectral prediction for specification-based loopback test of embedded mixed-signal circuits," *Springer J. Electronic Testing*, vol. 26, no. 1, pp. 73-86, Jan. 2010.

RF Front-End with On-Chip Loopback

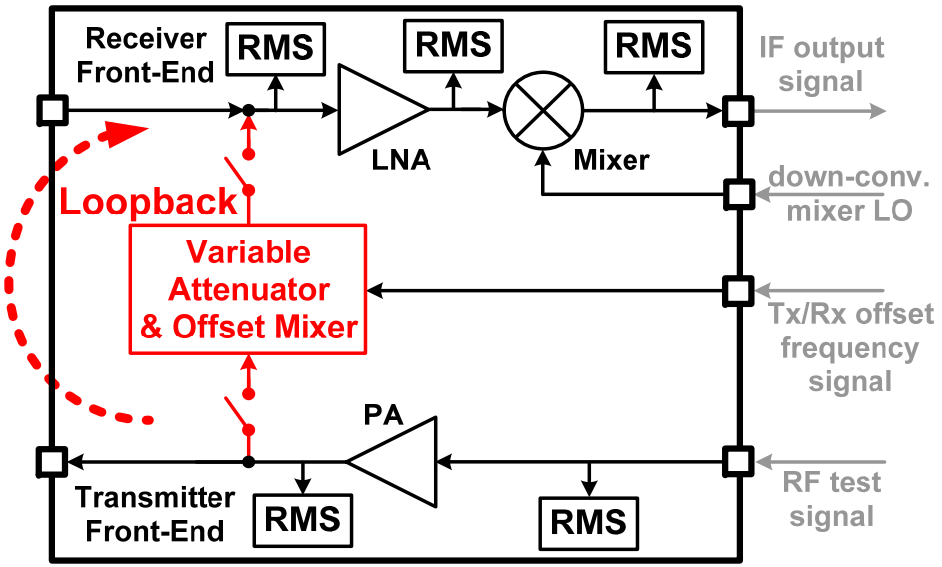
Team at Texas A&M University:

Marvin Onabajo
Felix Fernandez
Edgar Sánchez-Sinencio
Jose Silva-Martinez

Loopback Project Overview

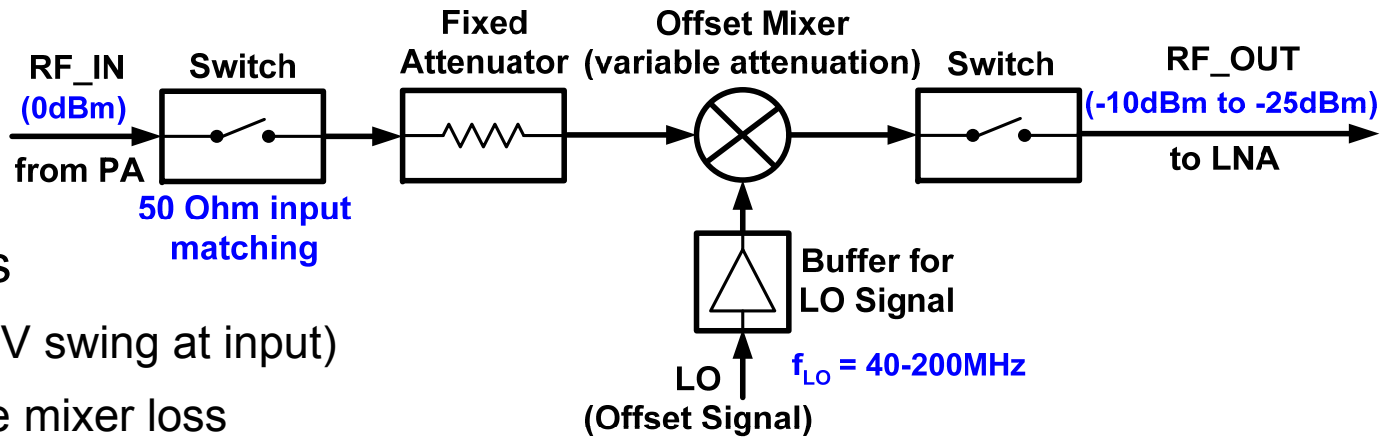
- Proof-of-concept RF front-end

Parameter	Value
Tx frequency	2GHz
PA output power	0dBm
Rx frequency	2.1GHz
LNA gain	21dB
Mixer gain	6.9dB



- Root-mean-square (RMS) power detectors
  - To measure gains and 1-dB compression points of the RF blocks
  - To improve the test coverage and identification of fault locations
- Test coverage
  - Project focus: front-end circuits
  - In case of a fully integrated transceiver: system-level BER

Proposed Loopback Block: Overview



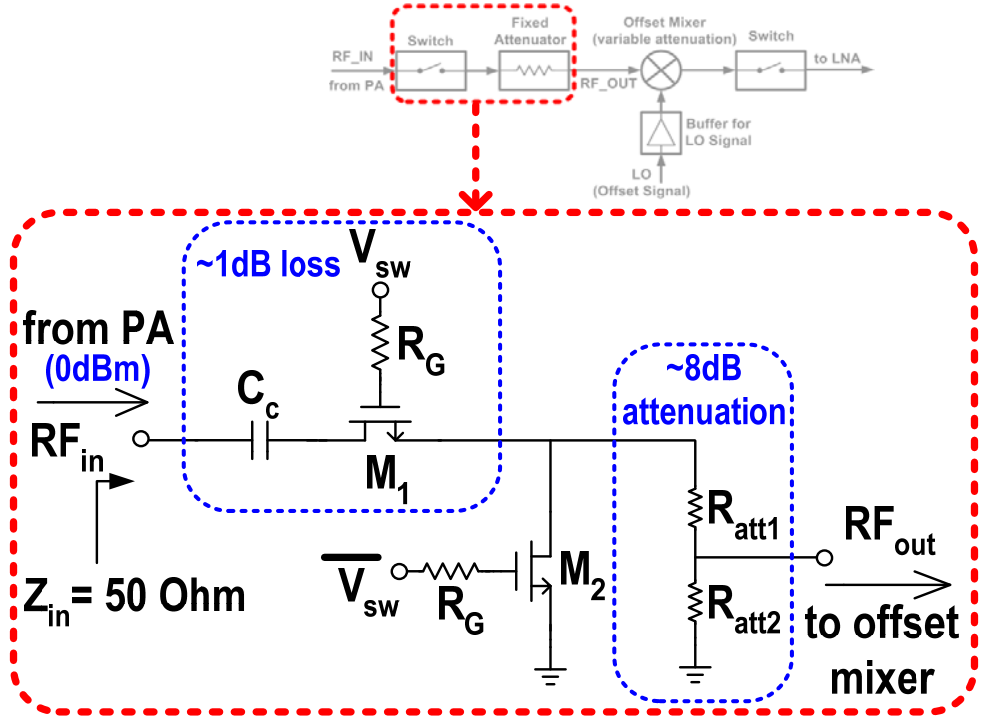
- Design challenges
  - Linearity (up to 0.7V swing at input)
  - Avoiding excessive mixer loss
  - Low impedance at the LNA gate node
    - This case: ~150Ω
    - High load-driving capability needed
  - Minimum die area/complexity
- Reconfigurability
  - Specs ensure compatibility with multiple standards (1.9-2.4GHz)
  - Offset mixing required if $f_{RX} \neq f_{TX}$ (ex.: W-CDMA, CDMA2000)

Target Specifications:

Parameter	Value
Input impedance	50Ω (matched to PA)
Tx/Rx offset frequency range	40-200MHz
Attenuation range (continuous)	10-25dB
Operating frequency	< 2.5GHz
Tx/Rx isolation (loopback deactivated)	> 80dB
Output noise: depends on communication standard and power level	

Input Stage: Switch/Fixed Attenuator

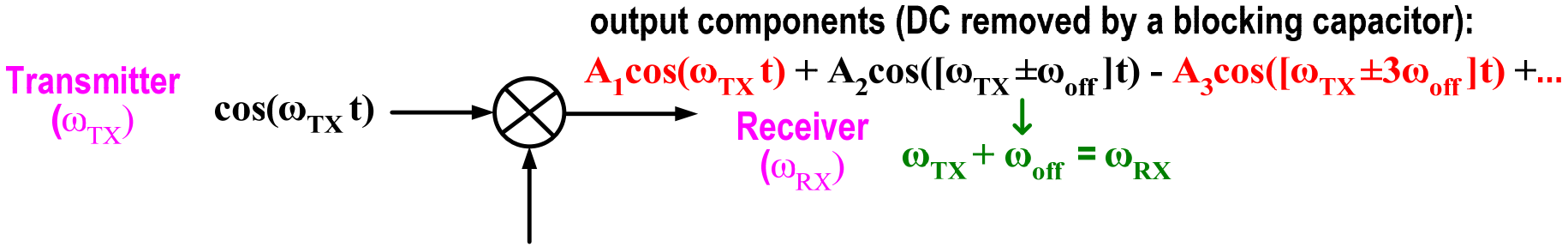
- Switch
  - M_1: low insertion loss/high linearity (large W/L) vs. high isolation (small W/L)
  - R_G: improves linearity (1-dB comp. pt. increase: ~4dB) & high-frequency performance
  - M_2: ~10dB more isolation in off-state
- Fixed attenuator (R_{att1}, R_{att2})
  - Decreases signal level at mixer input → relaxed mixer linearity



Offset Mixing with a Switching Mixer

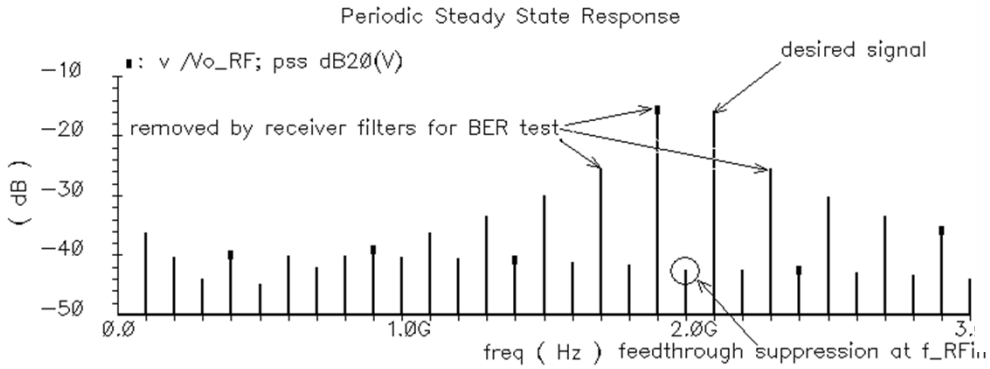
- Goals
  - Allow single-ended input from transmitter → inclusion of PA in the loop
  - Digital rail-to-rail signal can be used to provide the offset signal (simple to generate with low-cost ATE)
  - Avoid complexity → more robust

- Mixing scheme:

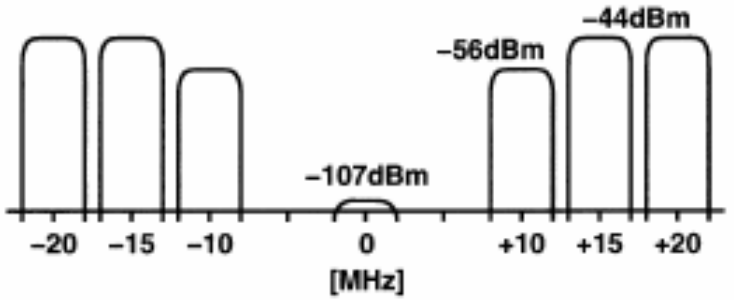


Suppression of Undesired Spectral Components

- RF feedthrough at $f_{RFin} = f_{TX}$
  - Appears as common-mode signal
  - Attenuated by the common-mode rejection property of the differential output stage in the mixer
  - Unwanted components at the receiver input
    - Located ≥ $2 \times f_{offset}$ (80-400MHz) away from desired signal
    - Equal or lower power than the desired signal
    - Must be suppressed according to communication standards



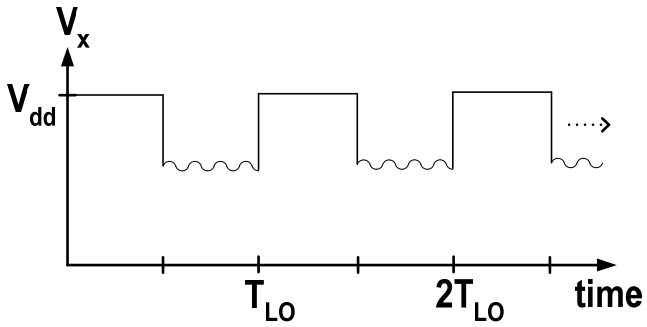
Output spectrum of second mixer stage

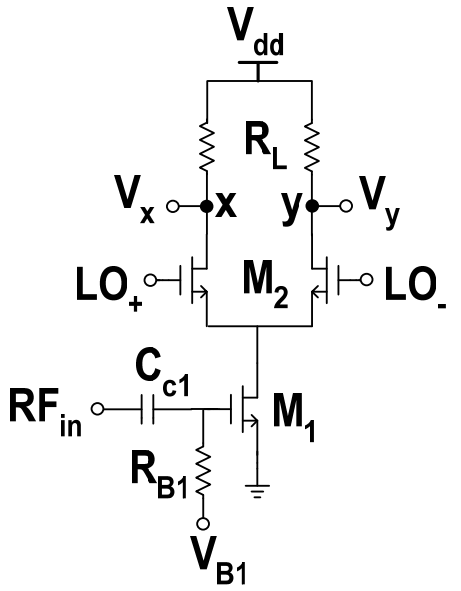


Example: W-CDMA blocker template (tolerable interference at 10MHz offset is >50dB above the desired signal)

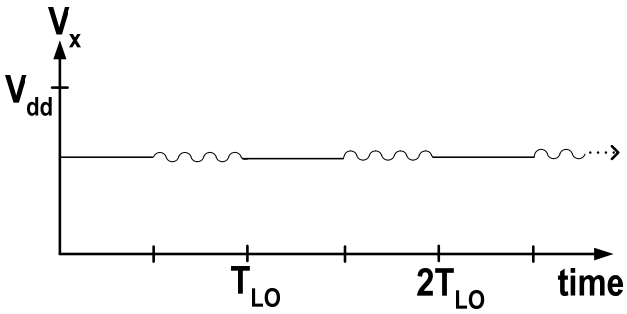
Offset Mixer Topology Development

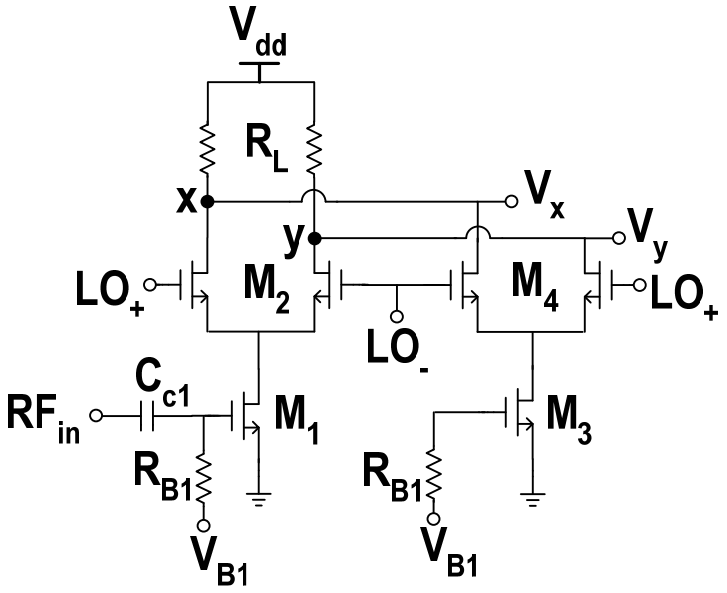
- Simple single-balanced mixer =>
  - Differential offset signal ($LO_{+/-}$)
  - Problem: voltage fluctuation from switching (at nodes x and y)





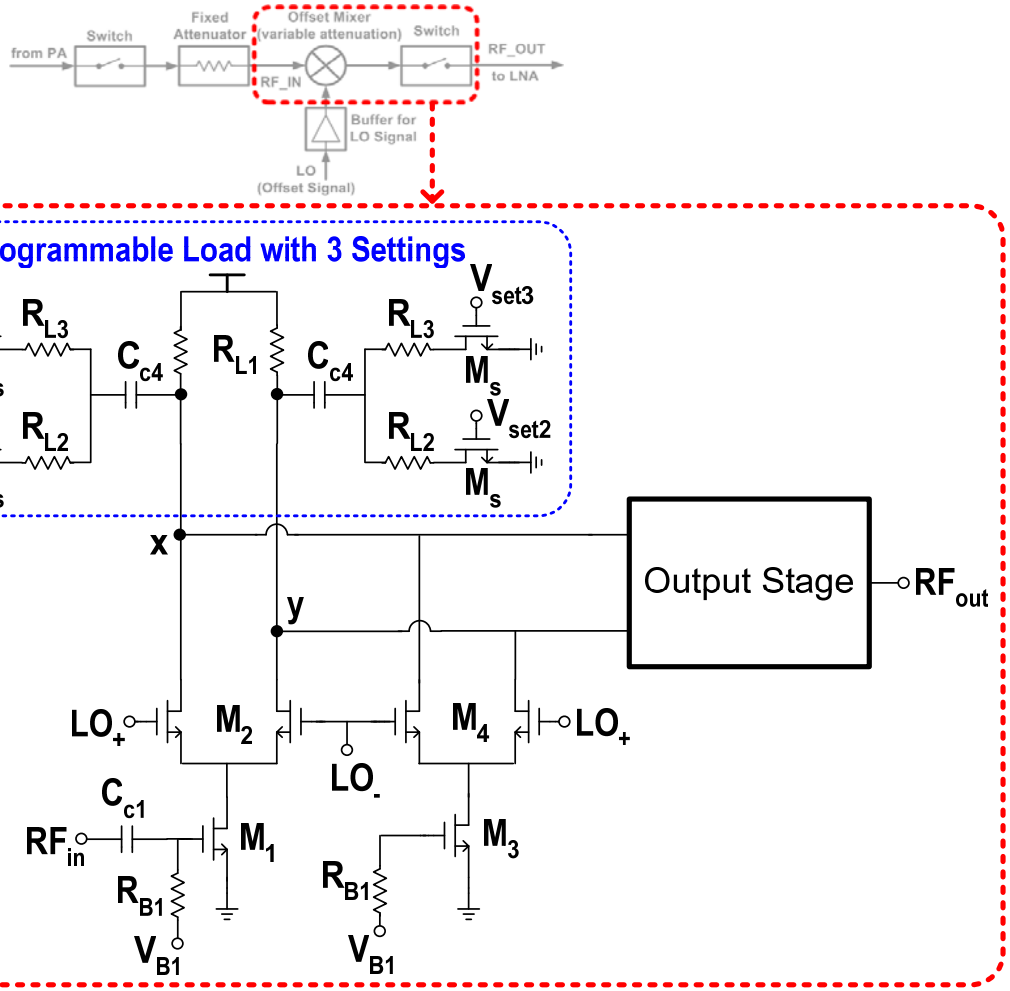
- Modified mixer core =>
  - Auxiliary branch for DC stabilization
  - $M_3=M_1$, $M_4=M_2$
  - Reversed $LO_{+/-}$ phase in aux. branch





Proposed Offset Mixer Topology

- 2 gain settings in the mixer core
  - R_{L2}/R_{L3} activated to reduce gain
  - Range: ~14dB



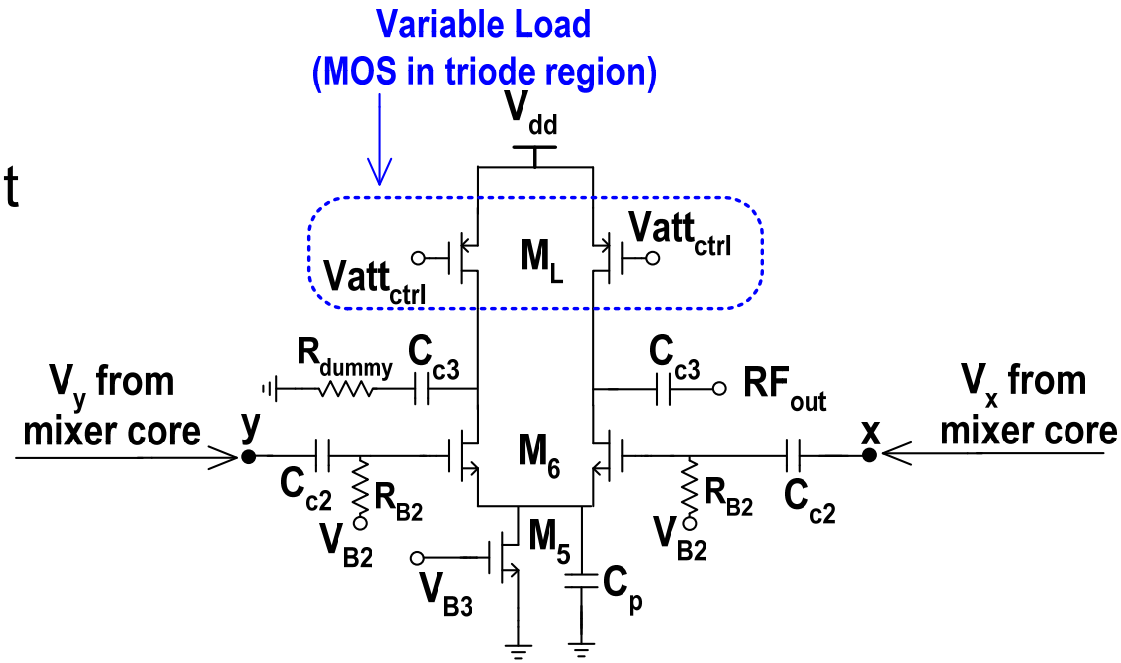
- Coupling capacitor C_{c4}
  - Prevents DC operating point changes at nodes x/y
  - Allows use of NMOS switch instead of PMOS (lower on-resistance for same size/parasitics)

- Conversion gain

$$G_{mix\_diff} = \frac{2g_{m1}R_{L[setting]}}{\pi}$$

Offset Mixer Output Stage

- Continuous gain tuning
  - Load transistor (M_L) is biased in triode region
  - Range with $Vatt_{ctrl}$: ~6dB



- Load-driving improvement

$$G_{out} = \frac{g_{m6} R_{ON(ML)}}{2}$$

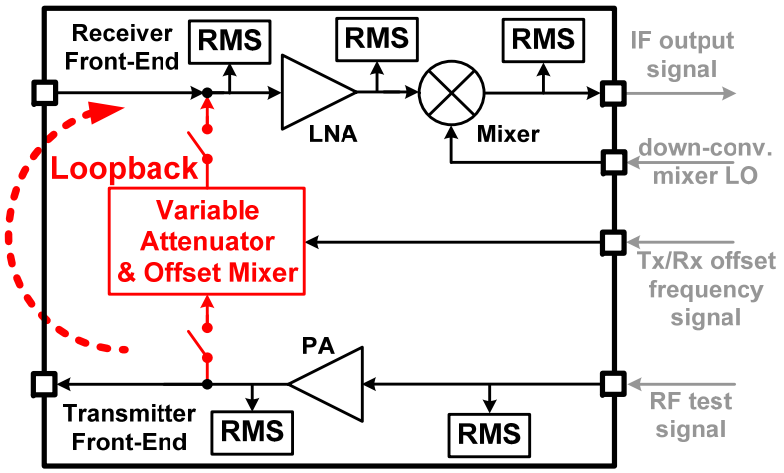
- Output switch
  - To disconnect loopback: $Vatt_{ctrl}$ high, V_{B3}/V_{B2} low

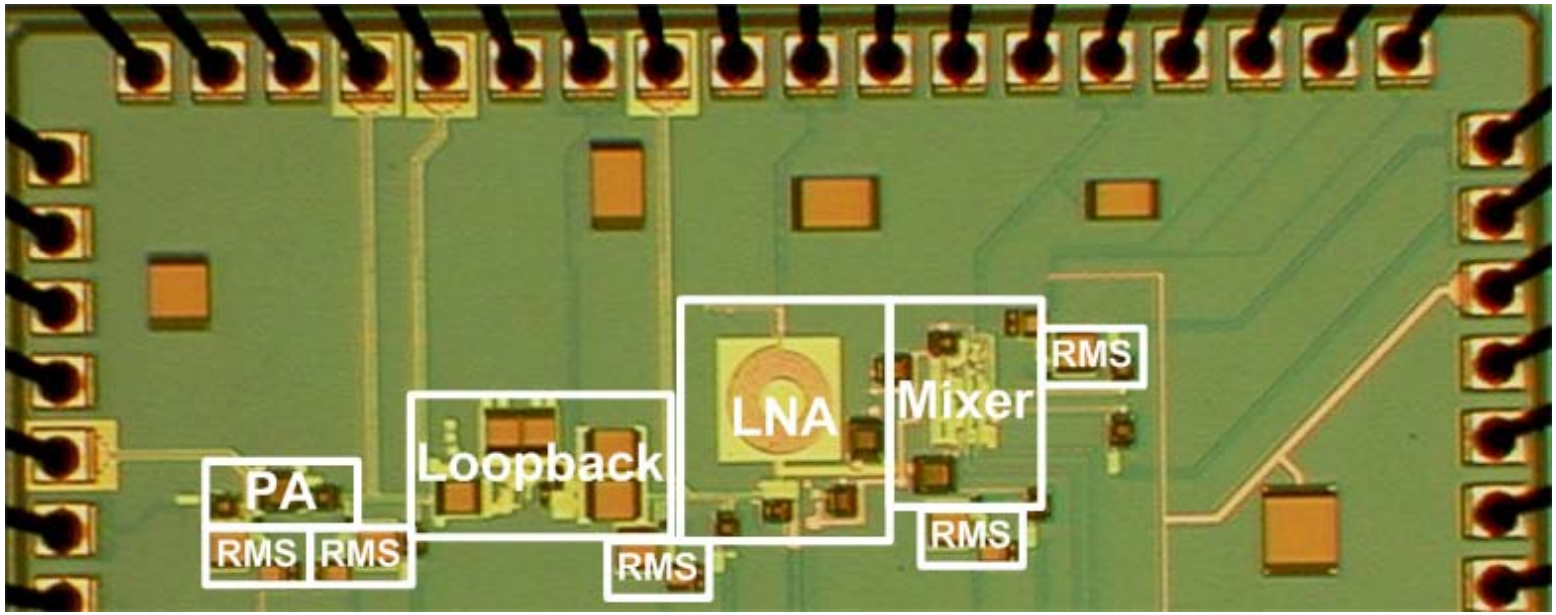
- Common-mode attenuation of RF feedthrough

$$A_{v(\omega_{RFin})} = A_{v\_cm} = \frac{g_{m6} R_{ON(ML)}}{1 + 2 g_{m6} (r_{ds5} \| \frac{1}{j\omega C_p})}$$

Testchip with the Prototype Front-End

- UMC 0.13μm CMOS technology
- Loopback block die area
  - 0.052mm^2
  - 40% of the combined PA, LNA, and down-conversion mixer area
  - Roughly 1-4% overhead for a transceiver





Measurement Results

Parameter	Target	Simulation	Measurement
Input impedance	50Ω	50Ω	50Ω*
Tx/Rx offset frequency range	40-200MHz	40-200MHz	40-200MHz
Attenuation range**	10-25dB	10.9-27.3dB	25.8-41.5dB
Operating frequency	< 2.4GHz	< 2.4GHz	< 2.4GHz
Tx/Rx isolation (deactivated)	> 80dB	> 89dB**	> 27.4dB***

* On-chip resistor (subject to PVT variations)

** Not accounting for RF feedthrough via substrate, mutual inductance between bonding wires, and PCB.

*** Measurement setup does not permit verification of isolation with more certainty. (Coupling between nearby traces on the PCB: measured isolation between pins ranged from 30dB to 50dB)

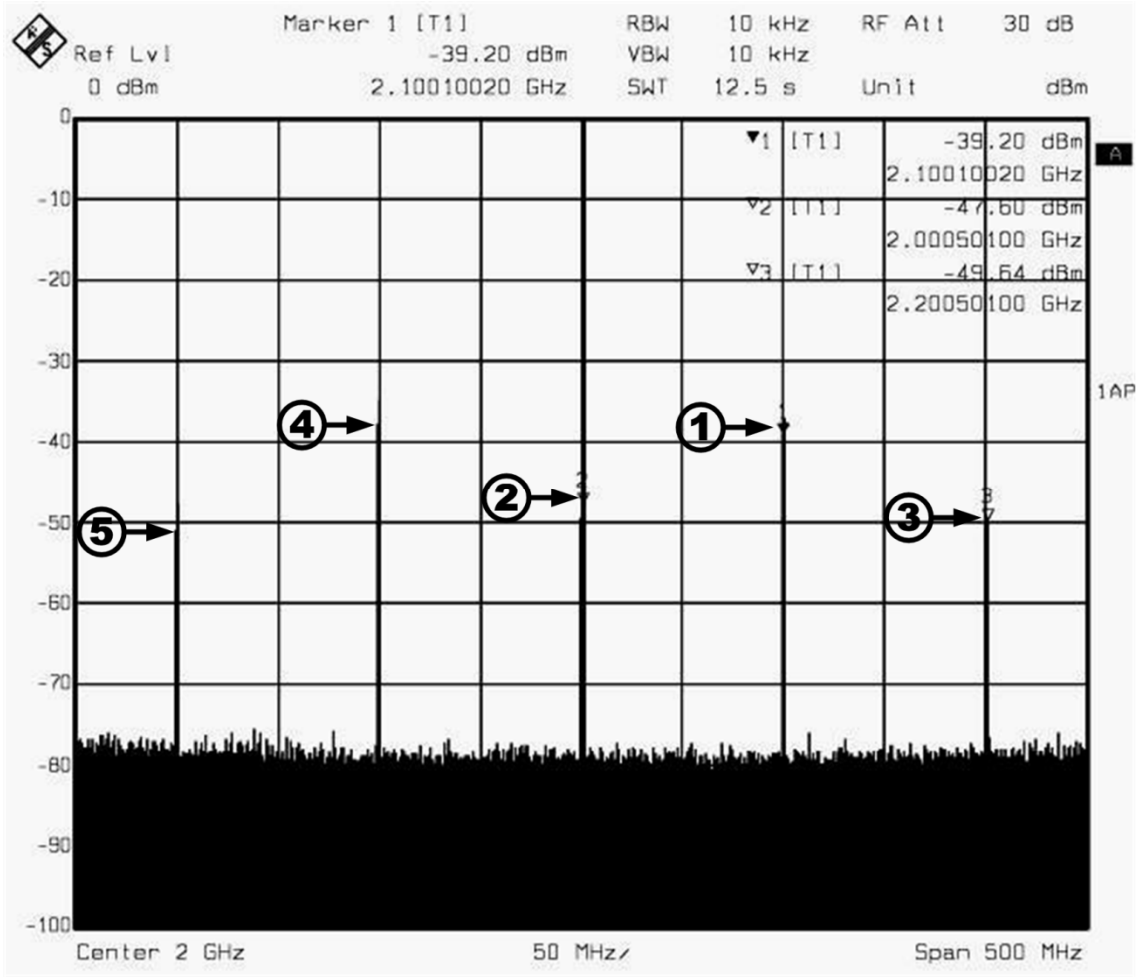
M. Onabajo, J. Silva-Martinez, F. Fernandez, and E. Sánchez-Sinencio, “An on-chip loopback block for RF transceiver built-in test,” *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 56, no. 6, pp. 444-448, June 2009.

Measurement Results (cont.)

- Fabrication-specific comments
  - Strong PVT variations
    - Gain degradation up to 10dB implied from reductions of:
      - 20% for effective RF transconductances
      - 10% for polysilicon resistors
      (in each of the two offset mixer stages)
  - Coupling losses
    - At the input attenuator
    - Capacitors in the offset mixer
- General suggestions
  - Avoid MOS capacitors
    (signal leakage to ground through parasitic capacitances)
  - Design with ~10dB more gain in the loopback
    - To provide sufficient margin for worst-case PVT conditions
    - To allow 1-dB compression point testing for the LNA

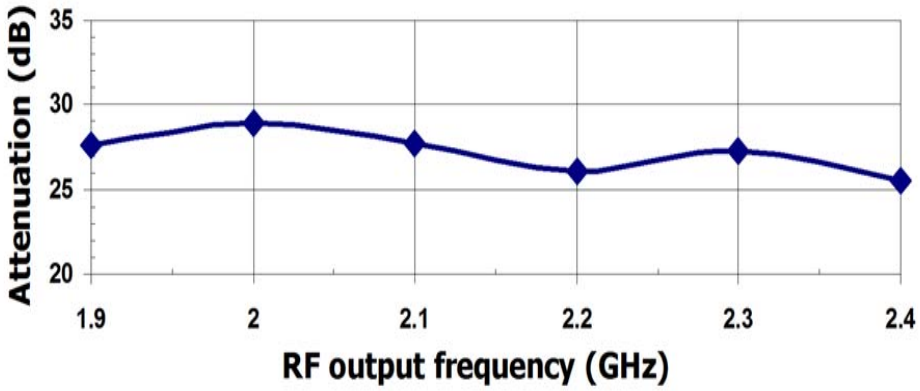
Measured Loopback Output Spectrum

- P_{in} = -3.5dBm at 2GHz
- f_{offset} = 100MHz
  → f_{out} = 2.1GHz
- 25.8dB attenuation setting
- -9.9dB from buffer/cable losses
- P_{out} = -39.2dBm



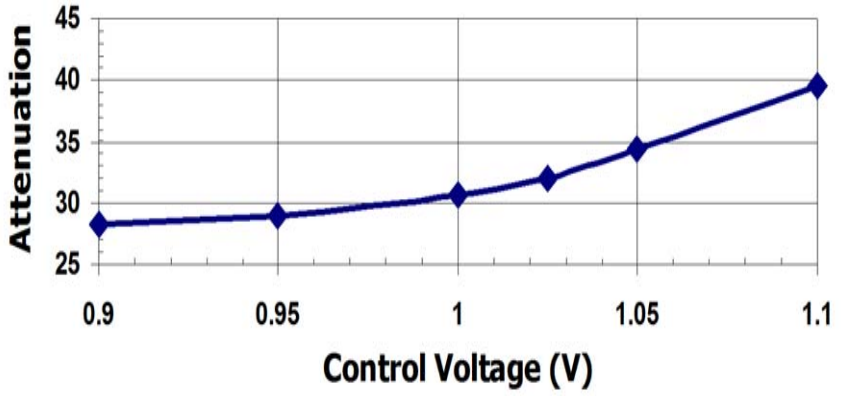
Tuning and Frequency-Dependence

- Attenuation vs. RF frequency →
  - Δattenuation ≈ 4dB (1.9- 2.4GHz)



- Tuning range

Control Mechanism	Attenuation
Discrete setting 1 (switched resistance value)	25.8dB
Discrete setting 2 (switched resistance value)	28.6dB
Discrete setting 3 (switched resistance value)	30.2dB
Control voltage (load transistor in triode region)	+ (0dB-11.3dB)
Combined	25.8dB-41.5dB



Continuous attenuation vs. control voltage (P_{in}=-12.5dBm, f_{RFout}=2.1GHz)

Summary: On-Chip Loopback Method

- Application-specific design constraints for the offset mixer
  - Location between PA and LNA
  - Low-frequency digital offset signal
  - Minimal complexity

  → Influenced the construction of the topology

- The proposed loopback topology provides continuous attenuation control and offset mixing for transceivers in the 1.9-2.4GHz range

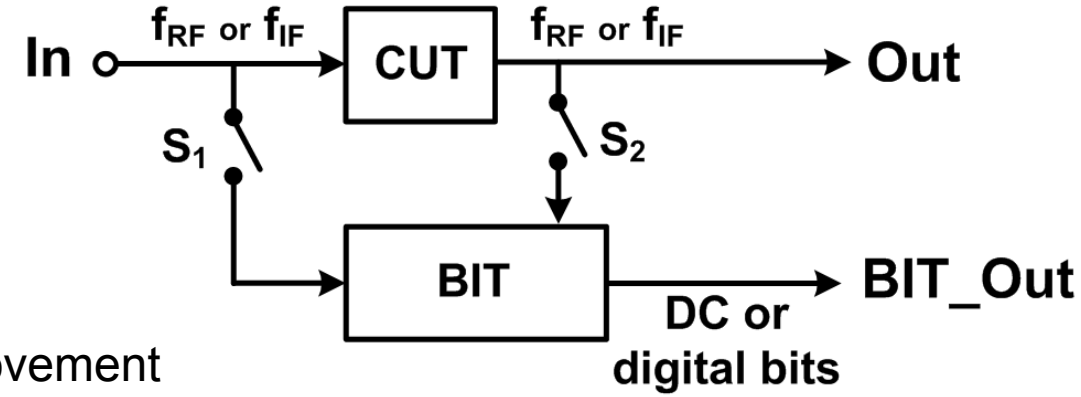
- Design margin for gain discrepancies due to PVT variations is critical

Outline – Lecture 1

- Introduction
  - Course overview
  - Greetings from Northeastern University
- CMOS process variation
  - Trends
  - Impacts
- System-level calibration trends
  - Systems-on-a-chip examples (receivers, transceivers)
- Production test simplification and cost reduction
  - Example: loopback testing
- Built-in testing of analog circuits
  - Introduction
  - On-chip power detection
  - RF LNA built-in testing example

Analog Built-In Testing

- Goal: on-chip extraction of performance parameters
  - Improved fault coverage
  - Enables tuning



- Benefits
  - Performance and yield improvement
  - Manufacturing test time and cost reduction

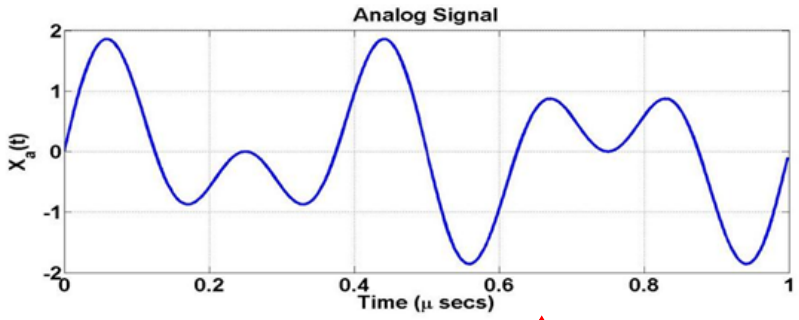
- Trade-offs
  - Possible loading effects on circuit under test (CUT)
  - Die area requirement
  - Power dissipation (particularly critical in online testing)

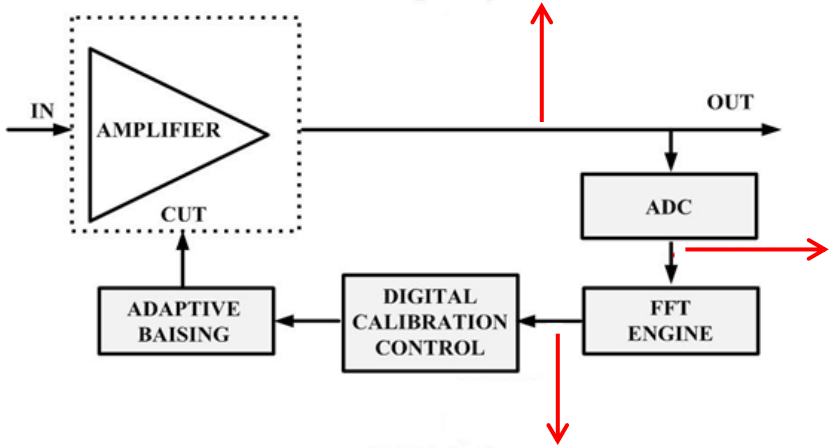
Built-In Test (BIT) Approaches

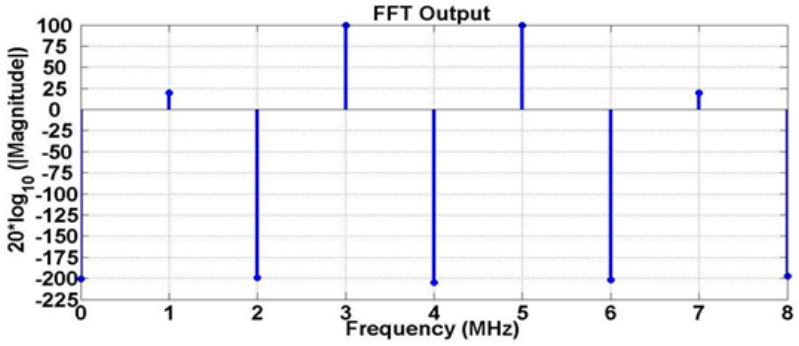
- Supply current sensing
- Oscillation-based testing
- Use of on-chip peak/power/RMS detectors
- Spectral analysis (on-chip FFT in DSP)
- Analog instrumentation (e.g., on-chip analog spectrum analyzer)
- …

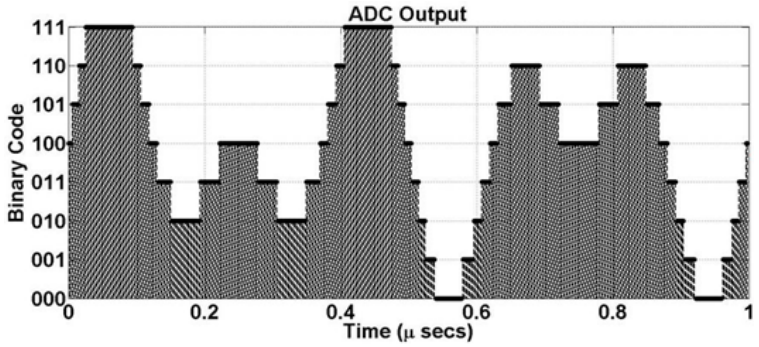
→ Commonality: BIT results must be correlated with specifications!

Envisioned On-Chip Calibration Example



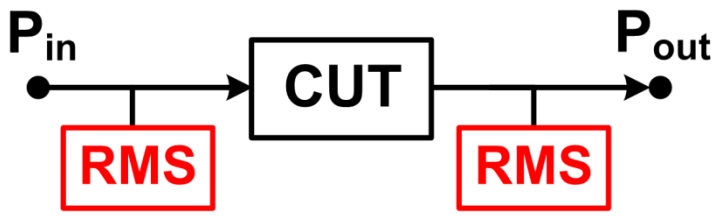






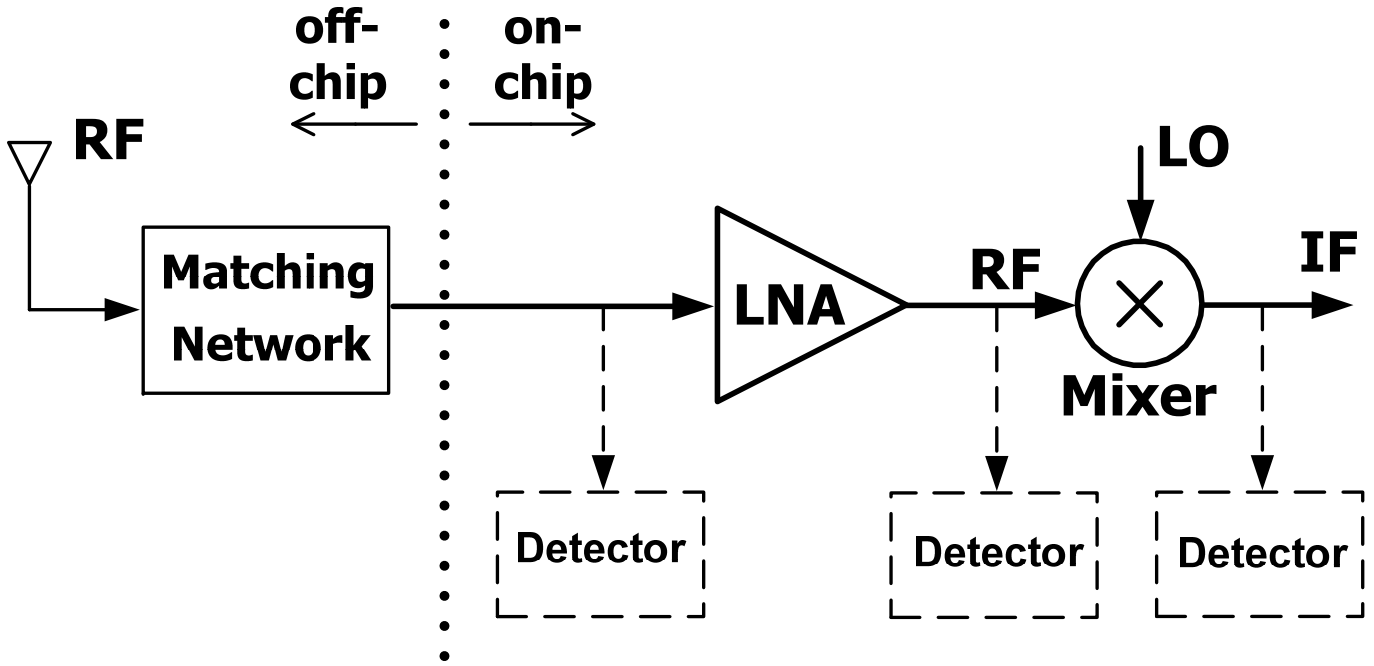
- Based on on-chip FFT engine and digitally tunable analog blocks
- Project started at Northeastern University
- For low-frequency (<50MHz) appl.
- Focus: FFT area and power minimization

On-Chip Peak/Power/RMS Detectors



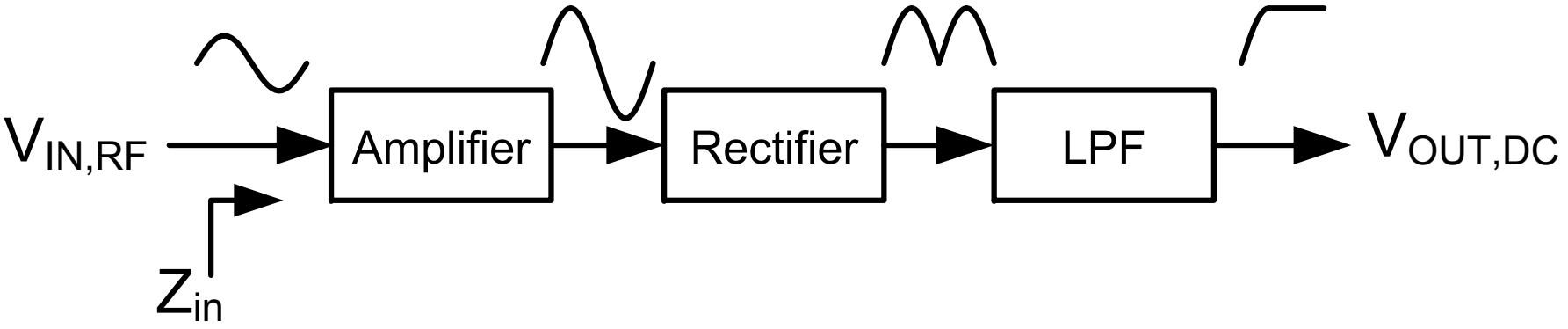
- Applications
  - Built-in testing
  - Received signal strength indicators (RSSIs)
- Design consideration
  - Gain
  - Linearity (1dB compression)
  - Input impedance matching
- Often used at RF frequencies when direct digitization of the signals is not feasible

Power Detectors for RF Built-In Testing



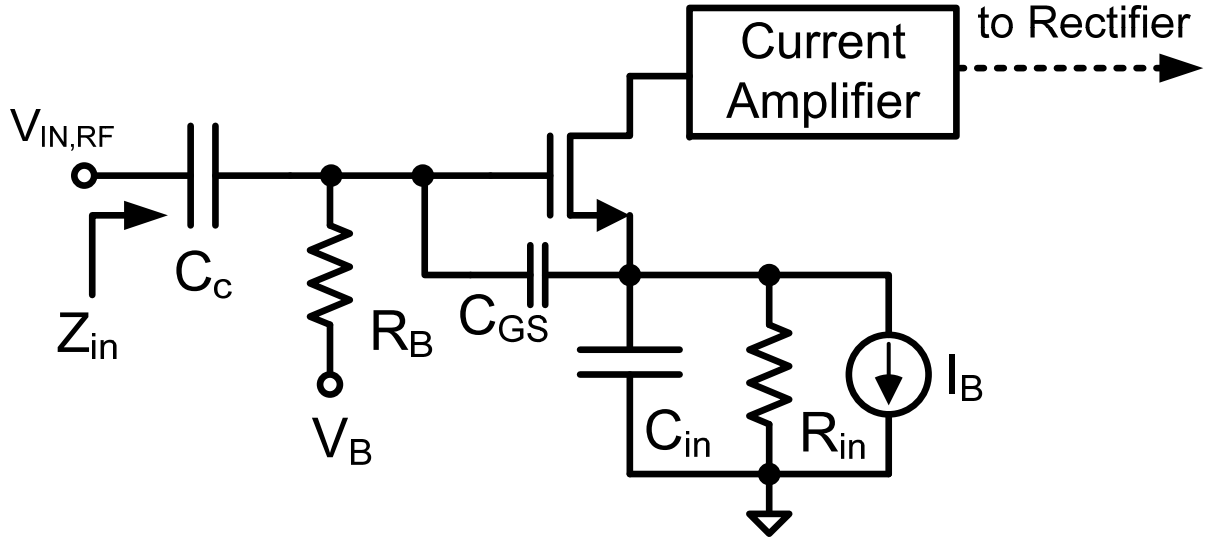
- Benefits
  - On-chip block-level characterization information
  - Analog local tuning loops for fast coarse calibration
  - Direct RF signal measurements without DSP (avoiding difficult high-speed digitization)

Basic Root-Mean-Square (RMS) Detection Concept



- Desired power detector characteristics:
  - High input impedance
  - Small die area
  - Large dynamic range
  - Wide input frequency range

Input Impedance Considerations



$$Z_{in} = \frac{1}{sC_c} + R_B \left\| \left[\frac{1}{sC_{gs}} + \frac{R_{in}}{1 + sR_{in}C_{in}} \left(1 + \frac{g_m}{sC_{gs}} \right) \right] \right.$$

- Z_{in} reduction at RF frequencies
  - Due to input device capacitances
- Input transistor dimensions should be minimized

RMS Detector Example Circuit

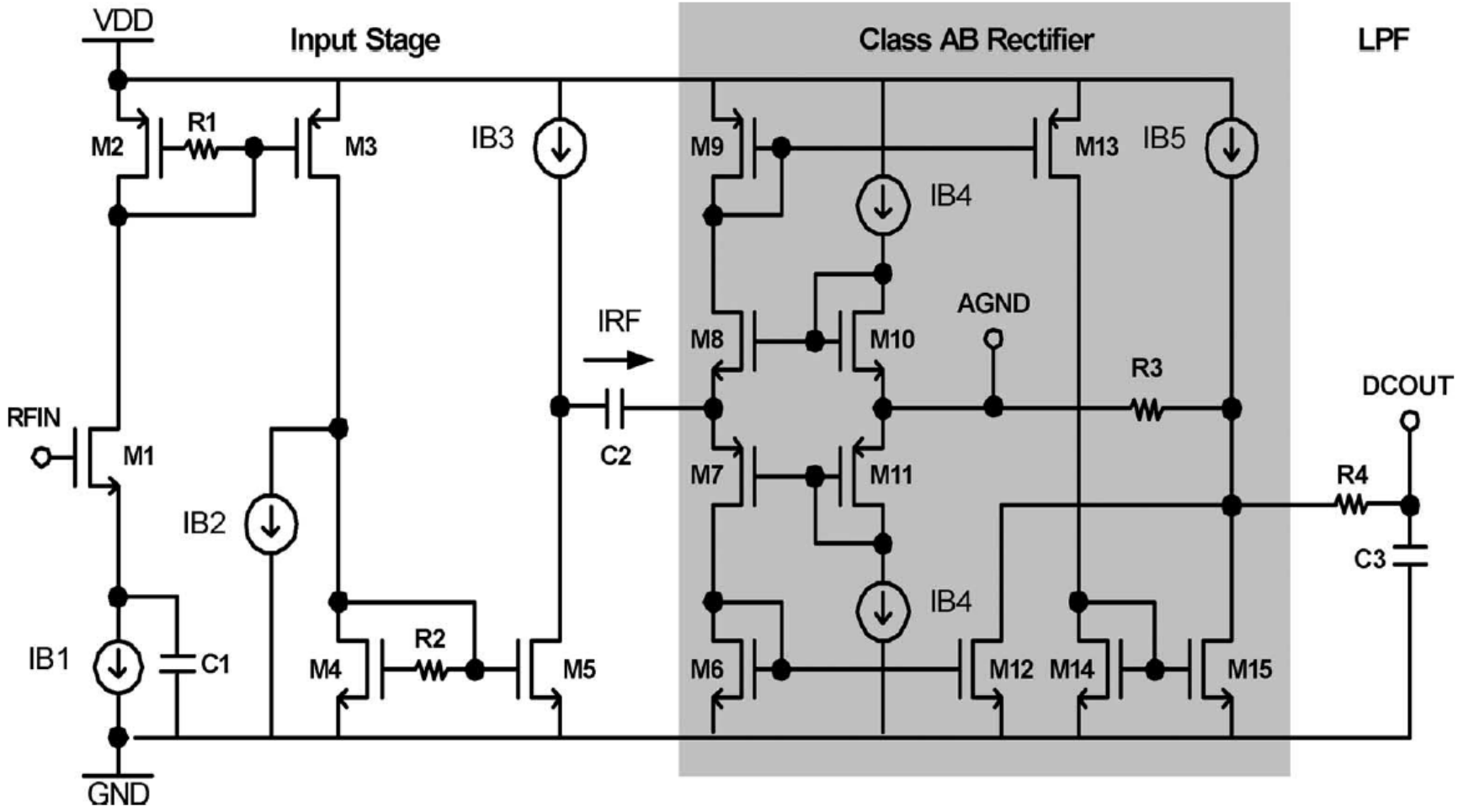
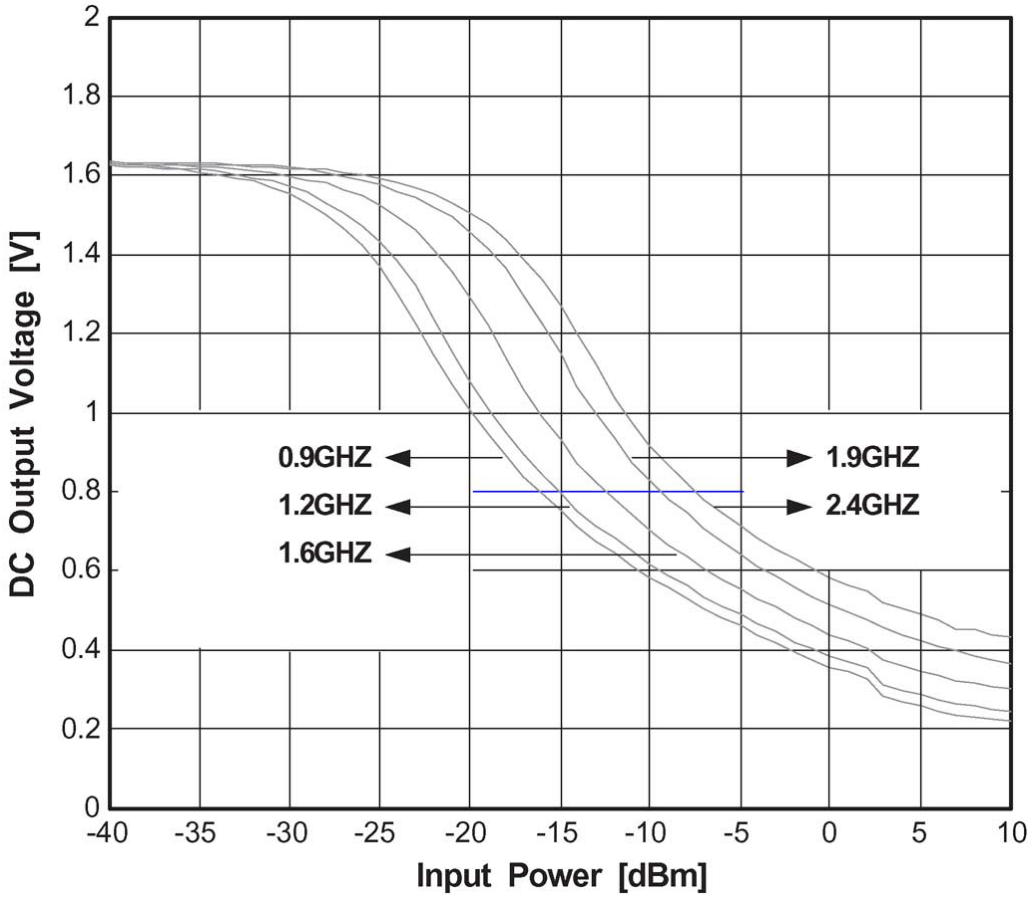


Figure from:
A. Valdes-Garcia, R. Venkatasubramanian, J. Silva-Martinez, and E. Sánchez-Sinencio, “A broadband CMOS amplitude detector for on-chip RF measurements,” *IEEE Trans. Instrum. Meas.*, vol. 57, no. 7, pp. 1470–1477, Jul. 2008.

Example RMS Detector Characteristics



Measured DC output voltage vs. RF input power at several frequencies

- Conversion gain: 50mV/dBm
- Settling time: 40ns
- Dynamic range: 30dB

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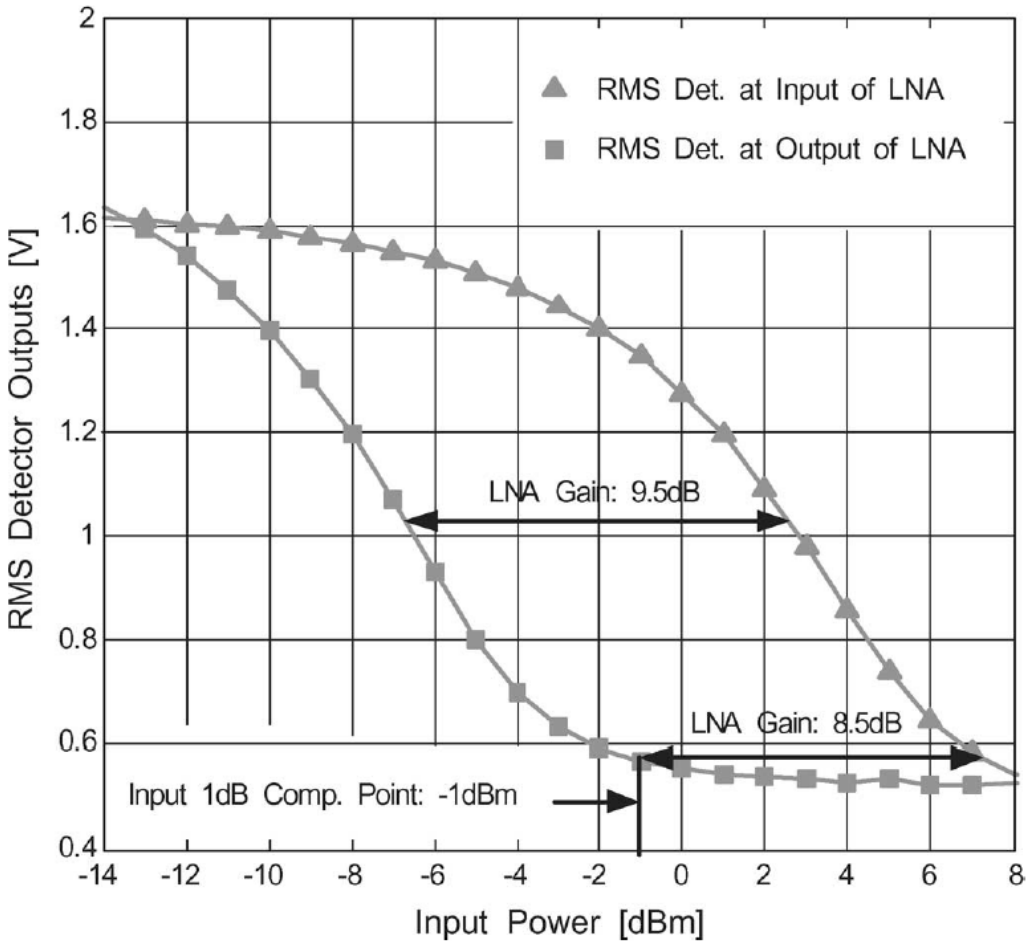
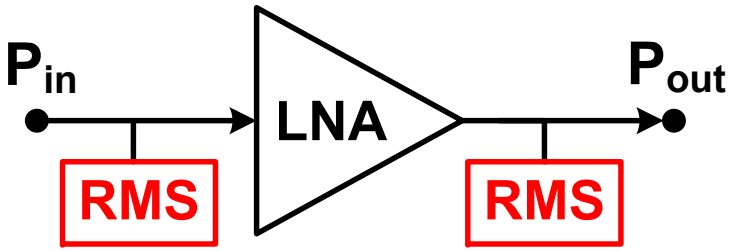
Gain & 1dB-Compression Measurements



Measured response of the RF detectors at the input and output of the LNA



Accuracy: ~1dB

A. Valdes-Garcia, R. Venkatasubramanian, J. Silva-Martinez, and E. Sánchez-Sinencio, “A broadband CMOS amplitude detector for on-chip RF measurements,” *IEEE Trans. Instrum. Meas.*, vol. 57, no. 7, pp. 1470–1477, Jul. 2008.

Detector Performance Examples

Reported Measurement Results:

Reference	[1]	[2]	[3]	[4]
Technology	0.25µm BiCMOS	0.35µm CMOS	0.18µm CMOS	0.18µm CMOS
Area	-	0.031mm^2	0.06mm^2	-
Dynamic Range	40dB	> 30dB	> 25dB	~10dB
Min. Detectable Signal	~ -40dBm	-25dBm	-15dBm	50mV
Operating Frequency	1.3GHz	0.9 – 2.4GHz	5.2GHz	2.5GHz
Power	< 1mW	8.6mW	3.5mW	-

[1] Q.Yin, W. R. Eisenstadt, R. M. Fox, and T. Zhang, "A translinear RMS detector for embedded test of RF ICs," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 5, pp. 1708–1714, Oct. 2005.

[2] A. Valdes-Garcia, R. Venkatasubramanian, J. Silva-Martinez, and E. Sánchez-Sinencio, "A broadband CMOS amplitude detector for on-chip RF measurements," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 7, pp. 1470–1477, July 2008.

[3] H.-H. Hsieh and L.-H. Lu, "Integrated CMOS power sensors for RF BIST applications," in *Proc. IEEE VLSI Test Symp.*, May 2006, pp. 229-233.

[4] F. Jonsson and H. Olson, "RF detector for on-chip amplitude measurements," *Electron. Letters*, vol. 40, no. 20, pp. 1239-1240, June 2004.

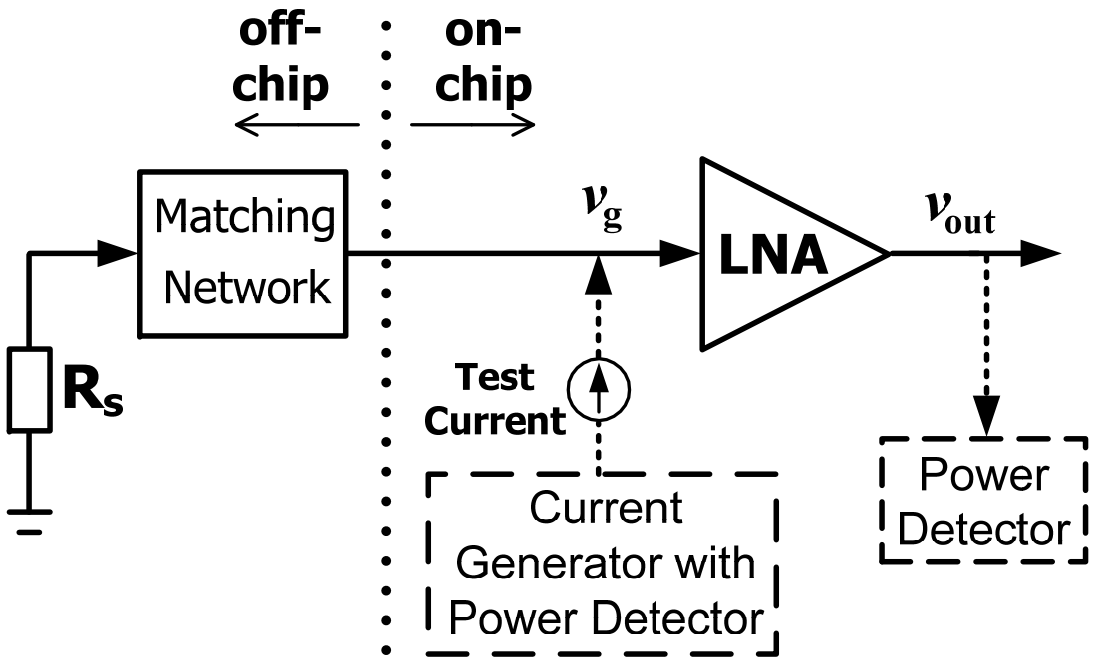
RF Built-In Testing with Current Injection

Team at Texas A&M University:

Xiaohua Fan
Marvin Onabajo
Edgar Sánchez-Sinencio
Jose Silva-Martinez

RF LNA Built-In Testing Example

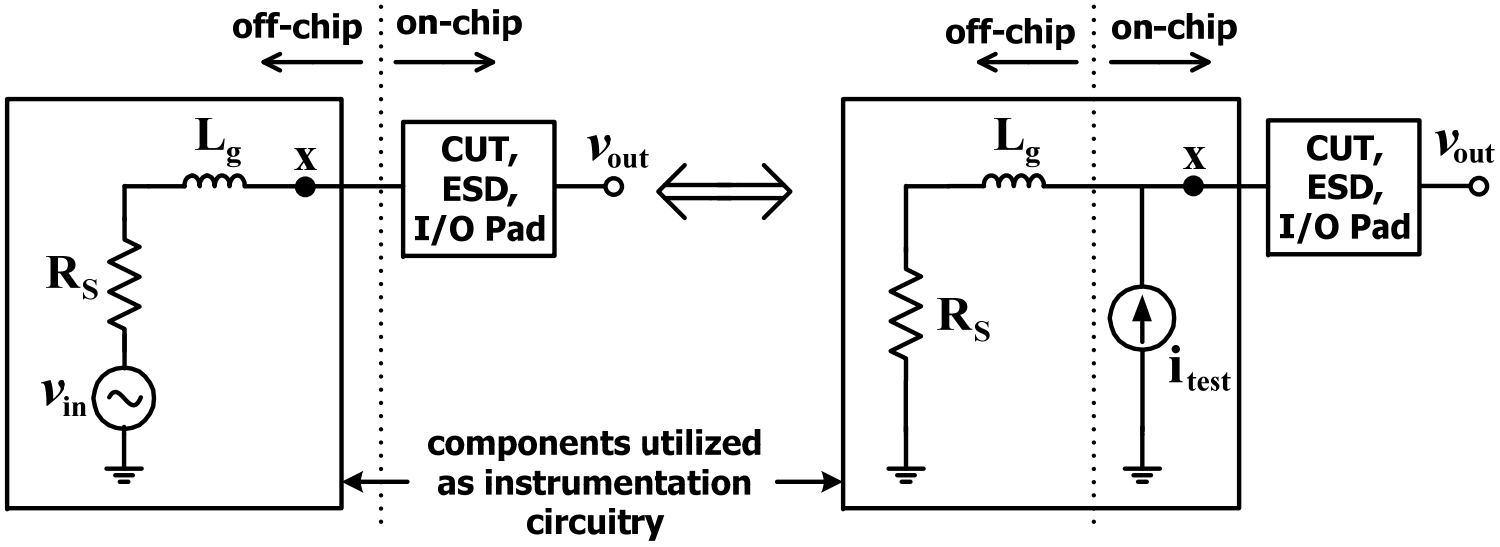
- Input impedance measurements with on-chip power detectors
  - Detection of faults in the off-chip matching network
  - Suitable for final in-package/board-level test stages



X. Fan, M. Onabajo, F. O. Fernández-Rodríguez, J. Silva-Martinez, and E. Sánchez-Sinencio, "A current injection built-in test technique for RF low-noise amplifiers," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 55, no. 7, pp. 1794-1804, Aug. 2008.

Current Injection Testing Theory

Thévenin-Norton transformation:

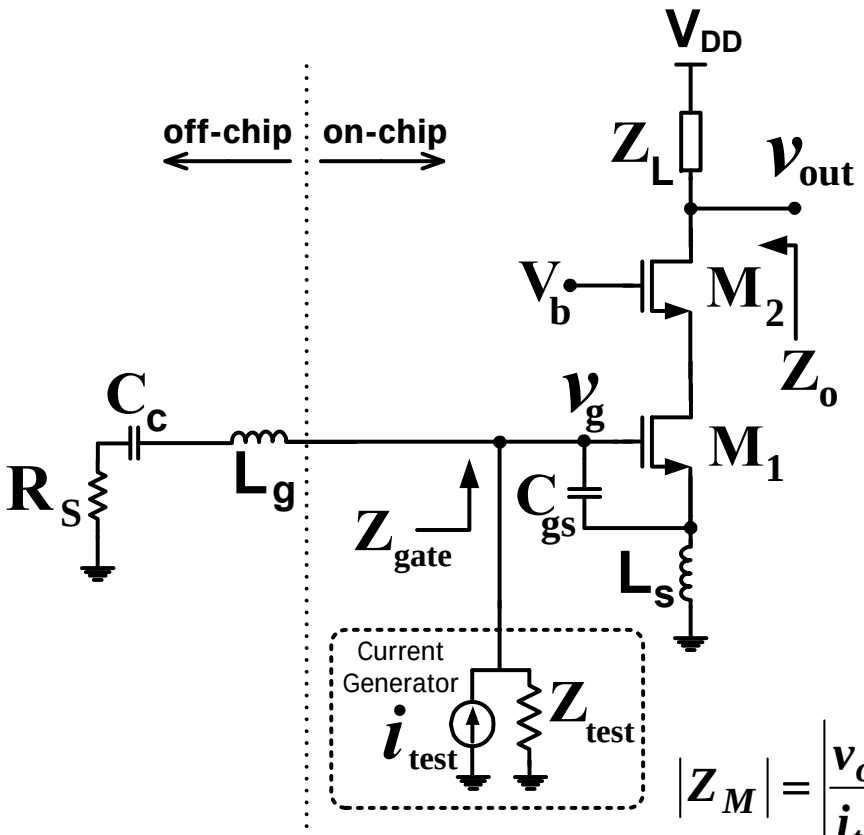


- Voltage gain determination with sensitivity to R_s/L_g
  - part of the test interface hardware
    → well-controlled variation, or:
  - under test (external matching network)
    → sensitivity allows fault detection

$$v_{in} = i_{test} \times (R_s + j\omega L_g)$$

$$G = \frac{v_{out}}{v_{in}} = \left(\frac{1}{R_s + j\omega L_g}\right)\left(\frac{v_{out}}{i_{test}}\right)$$

Current Injection Test Example



- To avoid impact on impedance matching:
  $Z_{test} >> Z_{gate}$
- Measurement with power detectors:
  $|Z_M| = |v_{out}/i_{test}|$

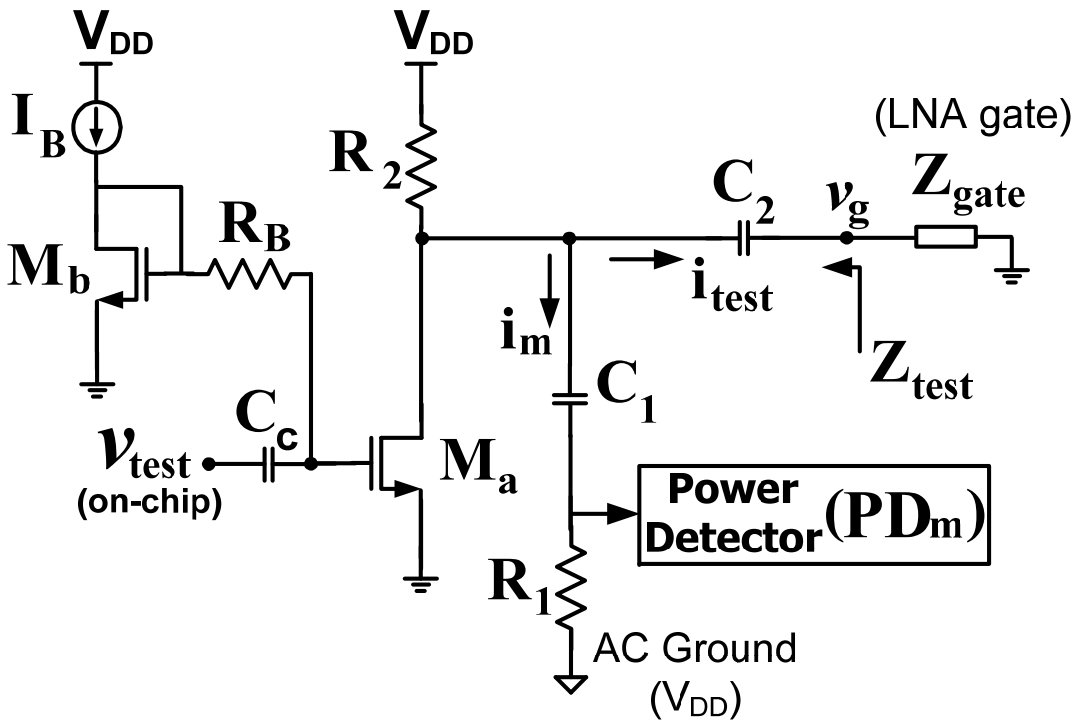
Transimpedance gain:

$$|Z_M| = \left|\frac{v_{out}}{i_{test}}\right| = \frac{\left(\frac{1}{\omega C_{gs}}\right)\left(\sqrt{R_s^2 + (\omega L_g)^2}\right)\left(g_{m1}|Z_o|\right)}{\sqrt{\left(R_s + g_{m1}\frac{L_s}{C_{gs}}\right)^2 + \left(\omega(L_g + L_s) - \frac{1}{\omega C_{gs}}\right)^2}}$$

Voltage gain estimation:

$$|G| = \left|\frac{v_{out}}{v_{in}}\right| = \frac{|Z_M|}{\sqrt{R_s^2 + (\omega L_g)^2}}$$

Current Generator Circuit



- Designed with:
  - $C_1 = m \cdot C_2$
  - $|1/j\omega C_2| >> Z_{gate}$
  - $i_m/i_{test} \approx m$
- Indirect measurement of i_{test} with R_1 and i_m

Layout area (without PD_m): 0.002mm²

$$\frac{i_m}{i_{test}} = \frac{Z_{gate} + \frac{1}{j\omega C_2}}{R_1 + \frac{1}{j\omega C_1}} = m \times \left(\frac{Z_{gate} + \frac{1}{j\omega C_2}}{mR_1 + \frac{1}{j\omega C_2}} \right)$$

- $Z_{test} >> Z_{gate}$ avoids loading (Z_{test}>1.1kΩ for f<2.4GHz)

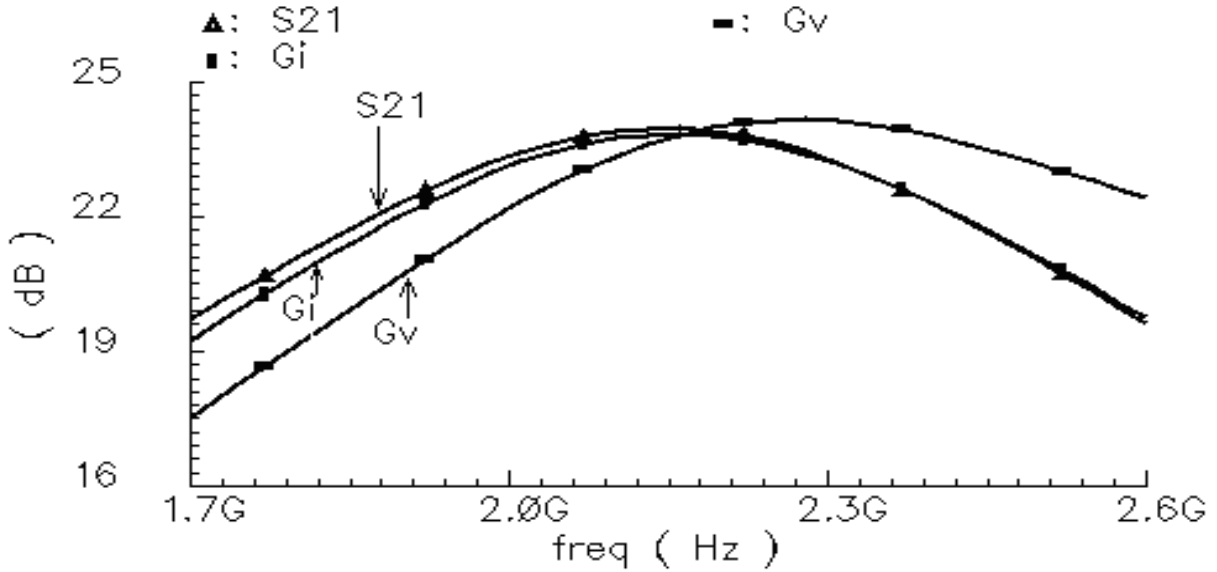
Post-Layout Simulation Results

Voltage-mode gain estimation:

$$G_{V,dB} = 20\log\left(\frac{V_{out\_rms}}{V_{g\_rms}} \times \frac{\sqrt{50^2+(\omega\times 8.1e^{-9})^2}}{2\times 50}\right) + 6$$

Current-mode gain estimation (error < 1dB):

$$G_{I,dB} = 20\log\left(250\frac{V_{out\_rms}}{V_{m\_rms}}\right) - 10\log(50^2+(\omega\times 8.1e^{-9})^2) + 6$$



Simulated comparison of S_{21} with G_v and G_I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Thank You.