Compact Modeling of Thin-Film Transistors

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Goals

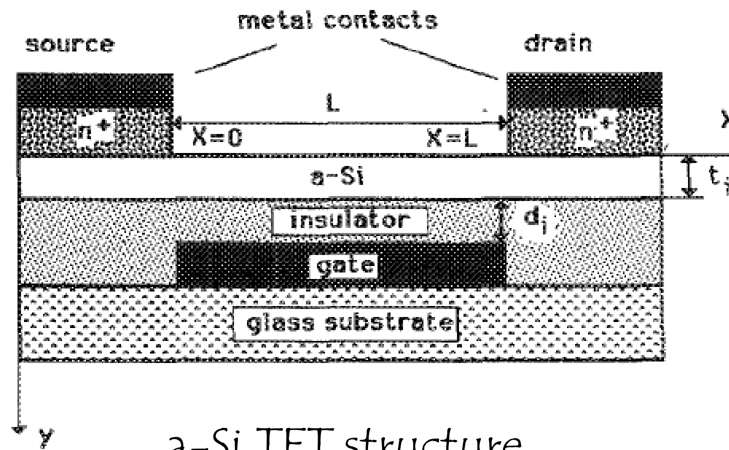
- Review of recent compact models for all kinds of TFTs: a-Si, poly-Si, nc-Si, ZnO, organic, polymer TFT
- Presentation of a universal eight-parameter model for all types of TFTs, which can be used as a first iteration
  - The second iteration consists on a compact model with bias-dependent parameters and adapted to each type of device

- Introduction
- Specific TFT models
  - Amorphous TFT
  - Polycristalline TFT
  - Nanocrystalline TFT
  - Organic TFT
- Universal TFT model
- Conclusion

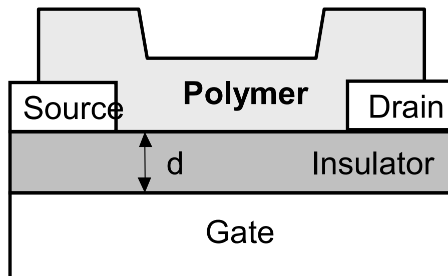
Introduction

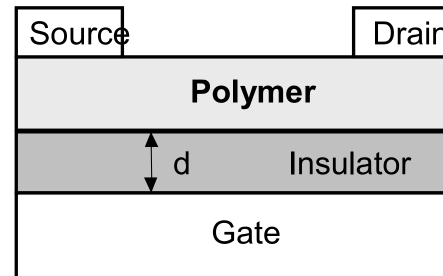
- TFTs are the essential devices in large area low cost circuits (drivers of AMLCDs, transistors for flexible electronics,...)
- **a-Si TFTs** are the most commonly used TFTs
  - **Advantages**: Possibility for deposition over large surfaces at a relatively low temperature.
  - **Disadvantages**: Low mobility, and degradation under illumination and bias stress.
- **Poly-Si TFTs** do not present the disadvantages of a-Si TFTs, and have higher mobility.
  - **Disadvantages**: High temperatures are used for the crystallization of the a-Si:H material.

Introduction



a-Si TFT structure





organic TFT structures

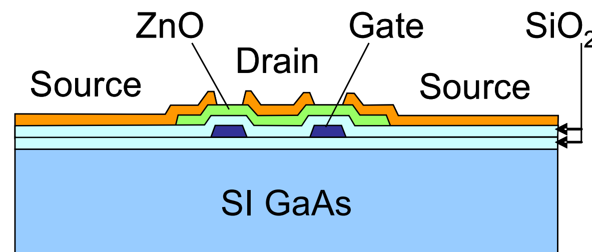
Introduction

- An alternative to both a-Si and poly-Si TFTs are **nanocrystalline Si TFTs** (nc-Si TFTs), obtained by Hot Wire Chemical Vapour Deposition (HWCD) at very low substrate temperatures (down to 120oC) and over large areas
  - nc-Si films consist of small Si crystallites, embedded in amorphous silicon. Therefore, properties of nc-Si TFTs lay between those of a-Si and poly-Si TFTs

- **Organic TFTs** have emerged as potential challengers to a-Si TFTs, because of their low power consumption and cost, and compatibility with flexible substrates
  - They combine the electrical properties of inorganic semiconductors with the simple technological processing of plastics
    - They allow flexible, light and low cost applications in large areas

Introduction

- Another alternative: oxide semiconductor TFTs, such as ZnO TFTs:
  - They can be amorphous, nanocrystalline or polycrystalline
  - They can be deposited over large and flexible substrates at low temperatures
  - They can be applied in transparent electronics



Introduction

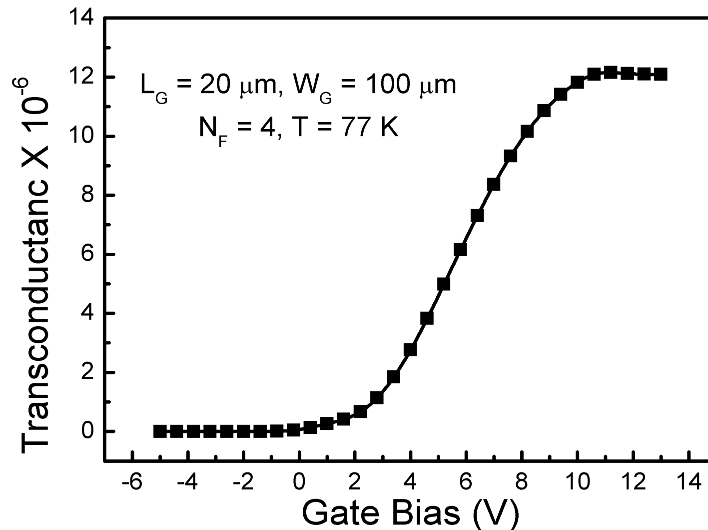
- The huge increase of the applications of Thin-Film Transistors (TFTs) for large-area electronics makes it necessary to have accurate compact models of these devices

- However, accurate TFT modeling is a quite complex task:
  - presence of many special physical phenomena
  - bias and geometry dependence of many parameters

Introduction

- Examples of special effects
  - Voltage drop at the series resistance
  - Nonlinear contact effects
  - Bias-dependences of several key parameters
    - Field-effect mobility
    - Threshold voltage
    - Series resistance

Introduction



Mobility discussion first requires on accurate extraction method.

Difference with SOI: large gap between V_T and g_m peak!

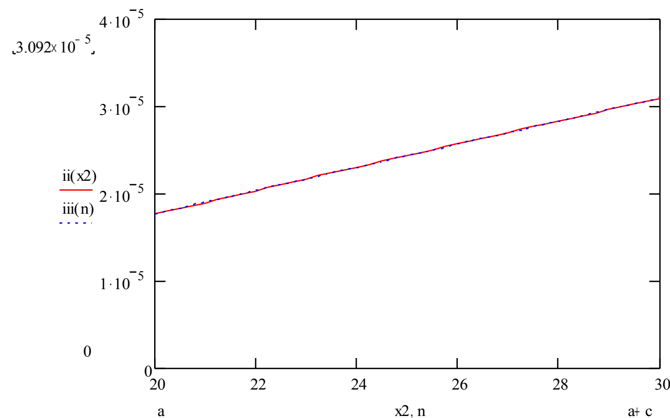
Mobility expression in SOI cannot explain this gap

$$\mu_{eff} = \frac{2\mu_0}{1+\theta(V_G - V_T)}, \qquad Y = \sqrt{\frac{W}{L} C_o x V_D \mu_0} (V_G - V_T)$$

The Y-function, $Y = I_D / \sqrt{g_m}$, cannot be applied as in SOI!

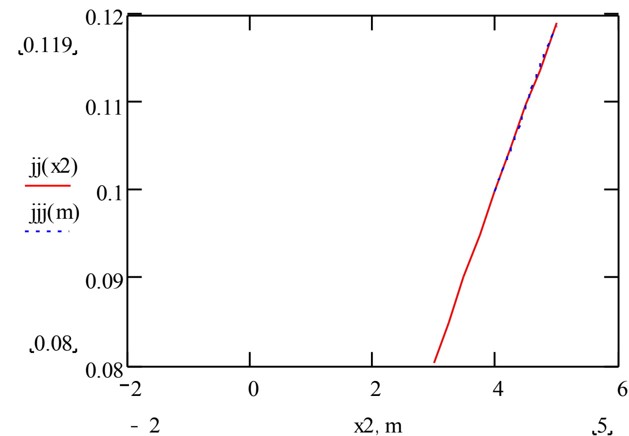
Introduction

- Example: TFT field effect mobility is a power law of V_{gs}-V_T



a-Si TFT above threshold

$$ii(V_{gs}) = I^{1/(\gamma+1)}$$



a-Si TFT below threshold

$$jj(V_{gs}) = I^{1/(\gamma_b+1)}$$

Poly-Si TFT

- Conduction mechanisms in poly-Si TFTs: **drift-diffusion in the grains**, and **thermionic emission in the grain boundaries**
- Effective medium approach: in order to derive a charge control model, in Poisson's equation the non-uniform poly-Si sample is treated as some uniform effective medium with effective material properties
- Poly-Si TFT modeling is developed using a drift-diffusion formulation, in which the effect of the grain boundary potential barrier is included in the expression of the field-effect mobility

Poly-Si TFT

- In the subthreshold regime, diffusion dominates:

$$I_{sub} = \mu_s C_{ox} \frac{W}{L} (\eta V_{th})^2 \exp\left(\frac{V_{gs} - V_T}{\eta V_{th}}\right)\left[1 - \exp\left(\frac{-V_{ds}}{\eta V_{th}}\right)\right]$$

- Above threshold there is a significant number of free carriers and the drain current is given by an expression similar to that used for crystalline MOSFETs.

$$I_a = \mu_{FET} C_{ox} \frac{W}{L}\left(V_{gt} - \frac{V_{dse}}{2\alpha_{sat}}\right) V_{dse}$$

- where μ_{FET} is the gate voltage dependent field-effect mobility that includes the effects of the trap states, α_{sat} is the body effect parameter. It increases with the gate voltage until it saturates.
- The leakage well below threshold is due to thermionic field emission through the grain boundary trap sites and is modeled using an additional term

Poly-Si TFT

$$\frac{1}{\mu_{eff}} = \frac{1}{k(V_G - V_T)^m} + \frac{1}{\mu_0}$$

Two limiting mechanisms: potential barriers + regular transport

The model also accounts for mobility degradation at high field

$$\frac{1}{\mu_{eff}} = \left[\frac{1}{k(V_G - V_T)^m} + \frac{1}{\mu 0}\right]\left[1 + \theta\,(V_G - V_T)\right]$$

$$\frac{1}{I_D} = \frac{1}{\left(\frac{C_{ox} W V_D}{L}\right)\mu_{eff}(V_G - V_T)}$$

k : *low- field mobility* constant
m : *low- field mobility power* law exponent
} : related to grain boundaries barriers

μ_0 : *low- field mobility* (as in SOI)

Θ accounts for high field mobility degradation (surface roughness scattering)

Poly-Si TFT

- We use a unified expresion of the drain current valid from subthreshold to above threshold (***RPI model***):

$$I_d = \frac{g_{ch} V_{ds} \left(1 + \lambda V_{ds}\right)}{\left[1 + \left(g_{ch} V_{ds} / I_{sat}\right)^m\right]^{1/m}}$$

- where

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}\left(R_s + R_d\right)} \qquad g_{chi} = q n_s \mu_{eff} \left(W / L\right)$$

- n_s is a unified expression of the sheet carrier density at the source end of the channel

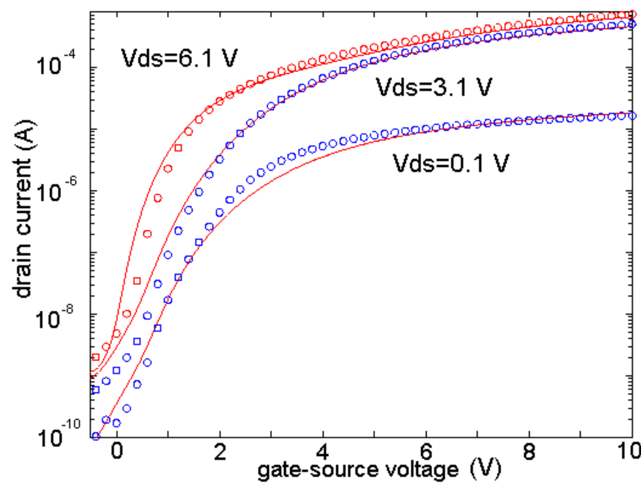
Poly-Si TFT

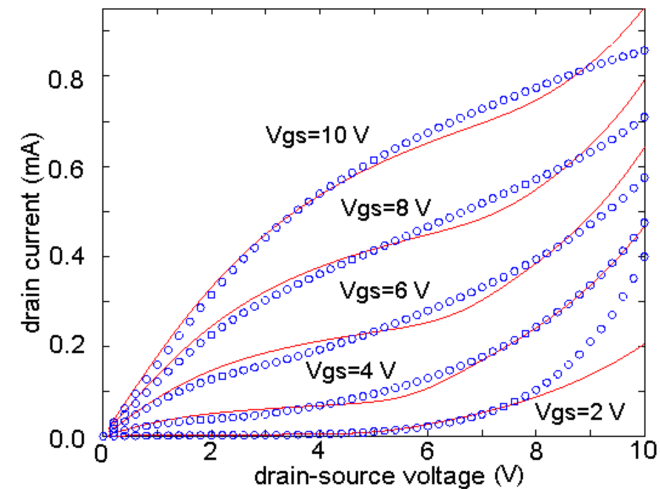
- The expression of the saturation current I_{sat} is derived using an appropriate velocity-field relationship.
- The DIBL effect is included in the threshold voltage expression.
- λ accounts for channel length modulation
- The impact ionization is modeled by an additional term to the drain current:

$$I_D = I_d + \Delta I_{kink} = I_d(1 + M)$$

$$M = \left(\frac{L_{kink}}{L}\right)^{m_{kink}} \left(\frac{V_{ds} - V_{dse}}{V_{kink}}\right) \exp\left(\frac{-V_{kink}}{V_{ds} - V_{dse}}\right)$$

Poly-Si TFT





Comparisons between measured (symbols) and modeled (solid curves) I-V characteristics of an n-channel poly-Si TFT with $W = 10\ \mu m$ and $L = 2\ \mu m$

a-Si TFT

- **Conduction** a-Si TFTs is due to the **drift of the induced free charge**
- As the gate voltage is increased, both trapped and free charge are induced.
- The field-effect mobility is proportional to the fraction of free charge, $n_{free}/(n_{free}+n_{trapped})$, and has the form, above threshold:

$$\mu_{FET} = \mu_n \left(\frac{V_{gs} - V_{T0}}{V_{AA}} \right)^{\gamma}$$

a-Si TFT

- Above threshold, the current is written as:

$$I_a = \mu_{FET} C_{ox} \frac{W}{L}\left(V_{gs} - V_{T0} - \alpha_{SAT} V_{dse}\right) V_{dse}$$

- In short-channel devices, self heating and kink effects become relevant. The final expression is:

$$I_D = \frac{I_{Do}}{1 - \frac{I_{Do} V_{ds}}{R_{total} T_{tot}}} + \Gamma V_{gt}\left(V_{ds} - V_{dse}\right) \exp\left(\frac{-V_K}{V_{ds} - V_{dse}}\right)$$

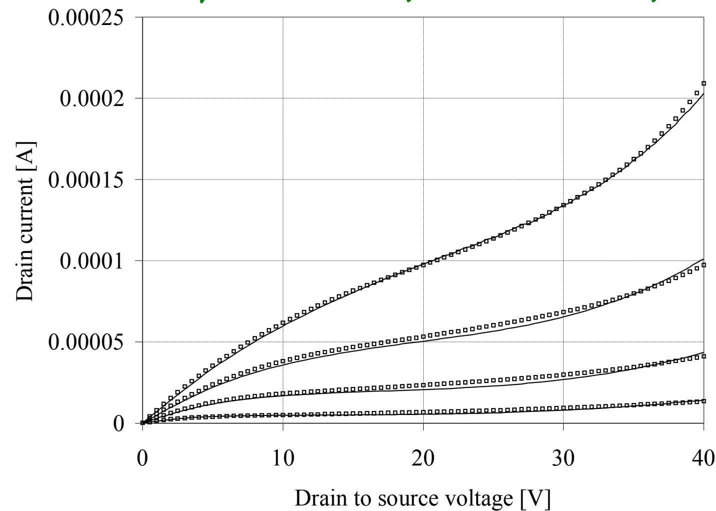
  - where Γ and V_K are adjustable parameters, R_{total} is the thermal resistance, T_{tot} is a function of the bias, and I_{DO} is the long-channel current expression

a-Si TFT

- Below threshold, the current is a power law of V_{gs}-V_{fb} :

$$I_{sub} \propto \left(V_{gs} - V_{fb}\right)^{1+\gamma_b} \qquad \mu_{FET}\left(V_{GS}, V_T\right) = \frac{\mu_{oo}}{V_{aa}^{\gamma_a}} \cdot \left(V_{GS} - V_T\right)^{\gamma_a}$$

- At large negative gate bias, a hole-induced drain leakage current caused by thermionic diffusion at the contacts, is accounted for

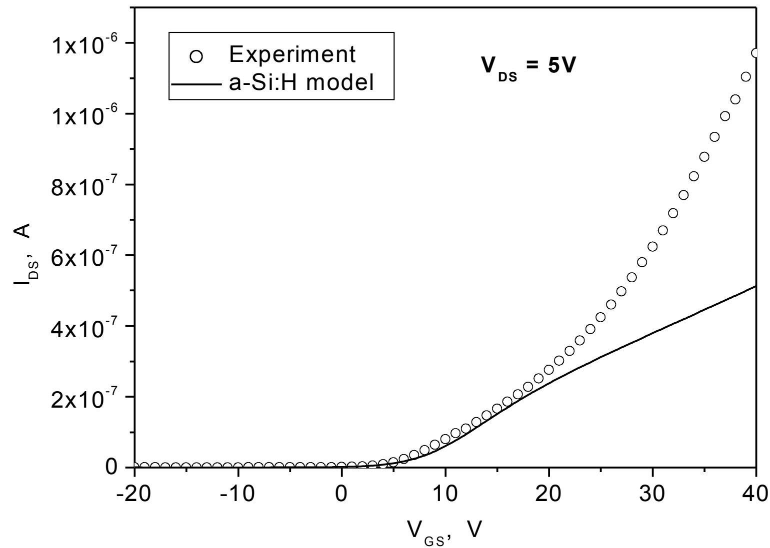


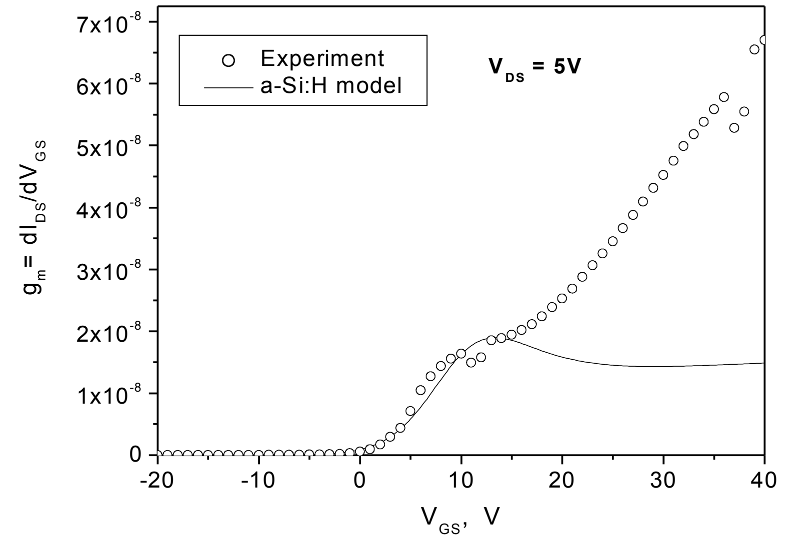
Measured (dots) and modeled (solid lines) output characteristics of an a-Si TFT; L = 4 μm

nc-Si TFT

- The model of nc-Si TFTs is based on the a-Si:H TFT model previously presented and used in the AIM-Spice circuit simulator
- The modeled curve is in good agreement with the experimental curve for $V_{GS}<17$ V.
- For a V_{GS} above that value we observe a dramatic increase on the experimental drain current and transconductance, which are not reproduced by the model

nc-Si TFT





Experimental and modeled transfer and transconductance characteristics using the a-Si:H TFT model

nc-Si TFT

- This high V_{GS} regime is called the transitional (to crystalline behaviour) regime the traps are almost completely filled, $n_{trapped}$ remains constant and n_{free} increases with increasing V_{GS} similarly to crystalline MOSFET
- As a consequence, the field-effect mobility μ_{fet} will increase linearly with increasing V_{GS}
- In nc-Si:H the DOS is lower than in a-Si:H because of the higher internal atomic order, and we can expect that the transition to crystalline-like regime occurs at significantly lower gate voltages than in a-Si TFTs

nc-Si TFT

- We have modified our nc-Si:H TFT model to obtain a suitable model for nc-Si:H TFTs.
- We added an above-threshold drain current term, I_{tr}, to account for the transitional regime.

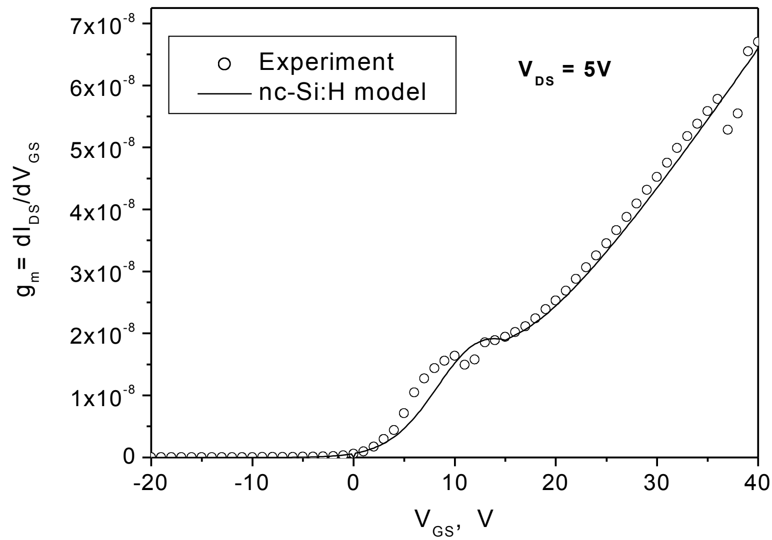
$$V_{Gtre} = V_{th} \cdot \left[1 + \frac{V_{Gtr}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{Gtr}}{2V_{th}} - 1 \right)^2} \right]$$

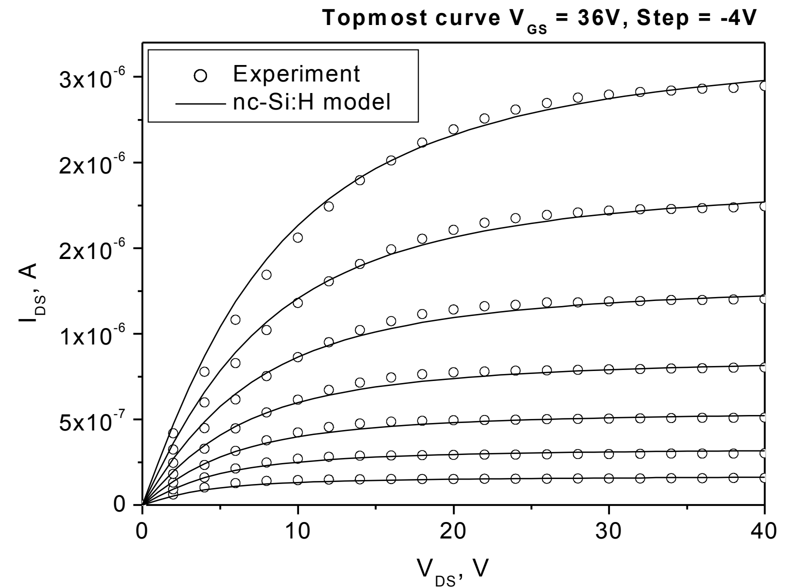
$$I_{tr} = \frac{1}{2} \mu_n C_i \frac{W}{L} V_{DSe} \left(1 + \lambda V_{DS} \right) \cdot M \cdot V_{Gtre}^{2+D}$$

  - where $V_{Gtr}=V_{GS}-V_{tr}$, V_{th} is thermal voltage and δ is a transition width parameter which ensures the good behavior of V_{Gtre}.
- We use the following unified expression of the channel current:

$$I_{DS} = I_{leak} + \left(\frac{1}{I_{sub}} + \frac{1}{I_{abv} + I_{tr}} \right)^{-1}$$

nc-Si TFT





Organic TFT

- In organic TFTs transport is due to **hopping** between localized states
- An analytical solution is possible assuming an exponential DOS and neglecting dopants and free charge
- With these assumptions, well above threshold (linear regime), we obtain:

$$I_{DS} = \frac{W}{L} \cdot C_{diel} \frac{T}{2T_0} \mu_0 \cdot \left[(V_{GS} - V_{FB})^{2T_0/T} - (V_{GS} - V_{DS} - V_{FB})^{2T_0/T} \right]$$

- This expression has the same form as the current in a-Si:H TFT, although the assumed transport mechanism is different.
- It is equivalent to use a crystalline MOSFET model with a field-effect mobility:

$$\mu_{FET} = \mu_0 \left[\frac{(V_{GS} - V_{FB})}{V_{aa}} \right]^{2T_0/T-2} = \mu_{FETo} \cdot (V_{GS} - V_{FB})^{2T_0/T-2}$$

Organic TFT

- Our basic compact model writes the current expression in a more general way:

$$I_{DS} = \frac{W}{L} \cdot C_{diel} \frac{\mu_{FET} \cdot (V_{GS} - V_T)}{\left(1 + R\frac{W}{L} \cdot C_{diel}\mu_{FET} \cdot (V_{GS} - V_T)\right)} \frac{V_{DS}(1 + \lambda \cdot V_{DS})}{\left[1 + \left[\frac{V_{DS}}{V_{DSsat}}\right]^m\right]^{\frac{1}{m}}} + I_O$$

- where $V_{DSsat} = \alpha_S (V_{GS} - V_T)$ R is source plus drain resistance, I_O is the leakage current and m and λ are adjustment parameters related to the sharpness of the knee region and to the channel length modulation respectively, and α_S is the non-ideal saturation parameter

Organic TFT

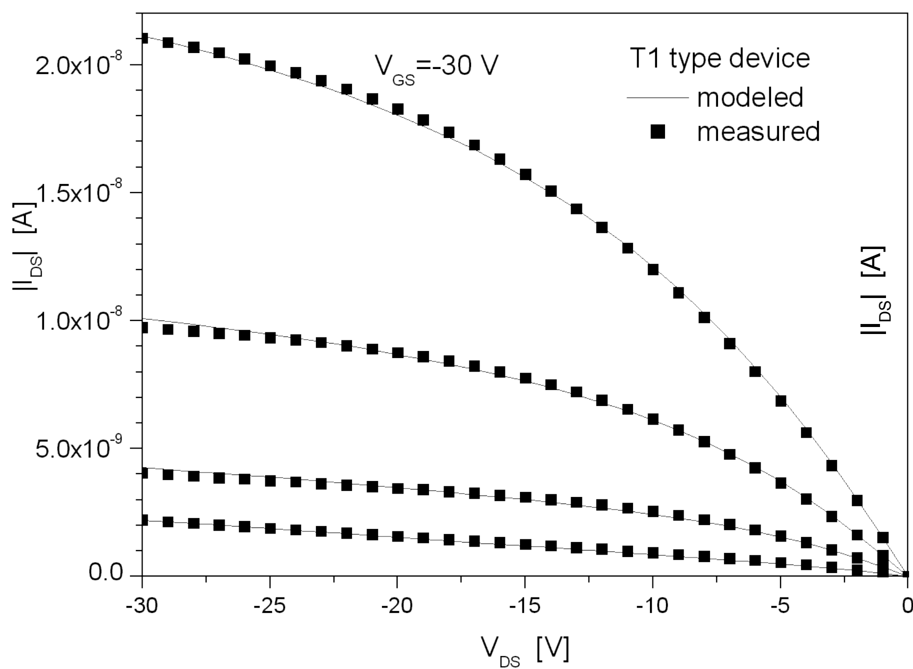
- The expression of the field effect mobility has been derived assuming a transport by hopping between localized states, and using the solution of the Poisson's equation, obtained by assuming that all charge is localized.

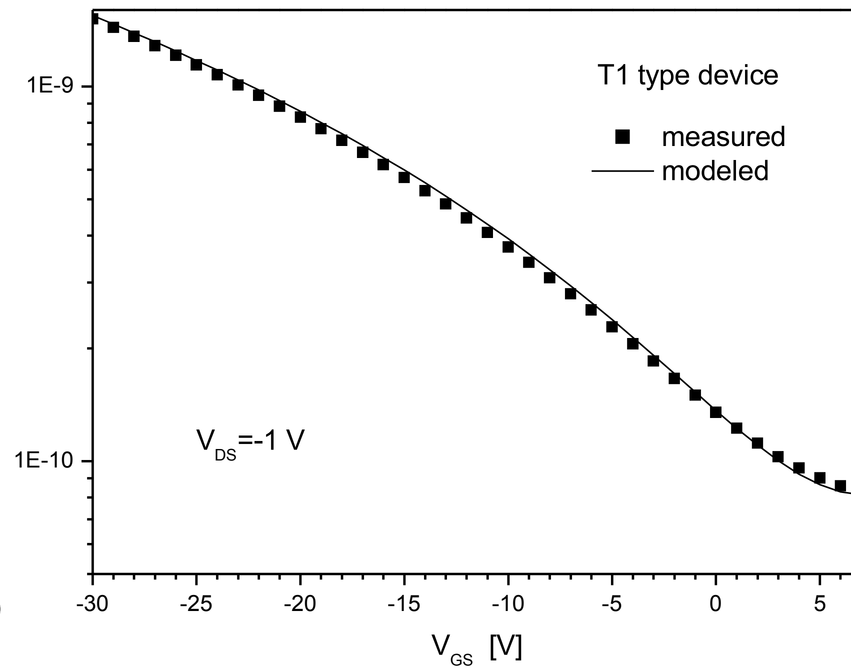
$$\mu_{FET} = P'(T,To)\cdot \frac{C_i^{\left(\frac{2To}{T}-2\right)}}{(\varepsilon_S)^{\left(\frac{To}{T}-1\right)}}(V_{GS}-V_{FB})^{\frac{2To}{T}-2}$$

- where

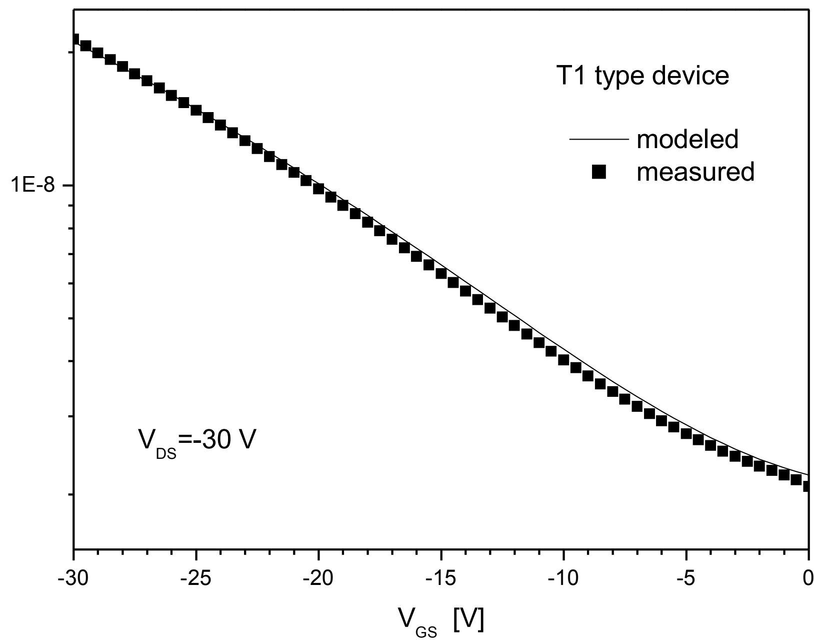
$$P'(T,To) = \frac{q\cdot k_bT\cdot N_V\cdot \exp\left[-\frac{E_{Fo}-E_V}{k_bT}\right]}{\left[\pi q\cdot k_bT\cdot g_{do}\cdot \exp\left(-\frac{E_{Fo}-E_V}{k_bTo}\right)\right]^{\frac{To}{T}}}\cdot\frac{To}{T}\cdot\left[\frac{\sin(\pi T/To)}{2k_bTo}\right]^{\frac{To}{T}}$$

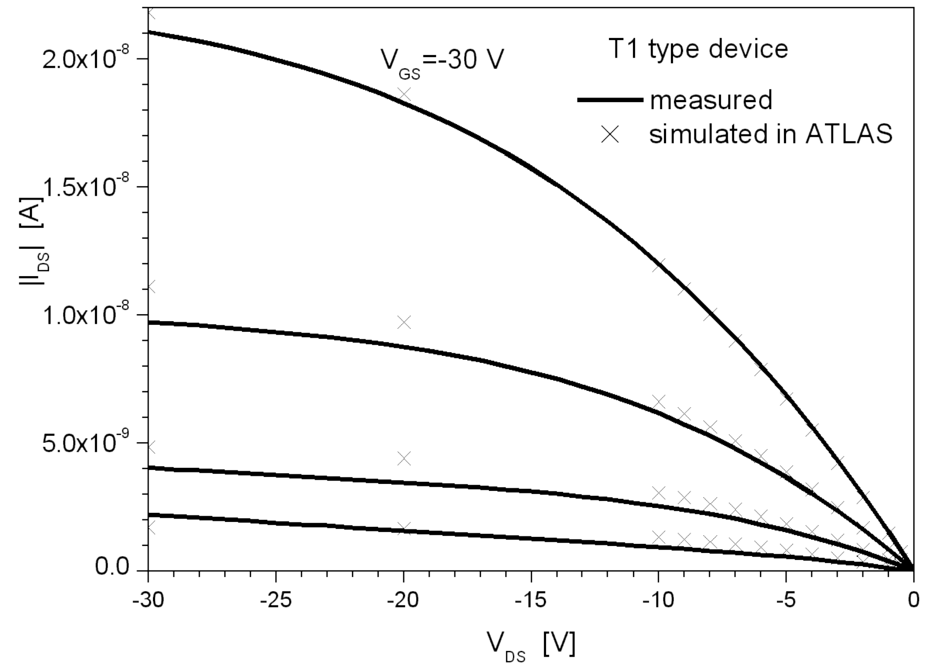
Organic TFT





Organic TFT





Universal TFT Model

- The new approach has been shown to be useful to obtain a relatively simple analytical model allowing simple parameter extraction techniques
- As a first iteration, a universal eight-parameter model is used
  - It can be considered as a first-order estimation valid for all kinds of TFTs
- The model is single-piece and infinitely continuous

Universal TFT model

- First iteration universal drain current model:

$$I = \frac{g_{ch} V_{ds} \left(1 + \lambda V_{ds}\right)}{\left(1 + \left(\frac{g_{ch} V_{ds}}{\left(1 + \lambda V_{ds}\right) I_{sat}}\right)^{m}\right)^{1/m}}$$

$$g_{ch} = \frac{\beta \left(V_{gt} / V_{aa}\right)^{\gamma + 1}}{1 + \beta \left(R_s + R_d\right)\left(V_{gt} / V_{aa}\right)^{\gamma}} \qquad I_{sat} = \frac{\beta V_{gt}^{2}}{1 + \beta R_s V_{gt} + \sqrt{1 + 2\beta R_s V_{gt} + \left(\frac{V_{gt}}{V_L}\right)^{2}}}$$

- This model, valid above threshold, has eight parameters:

$$m, V_T, \gamma, \lambda, \beta / V_{aa}^{\gamma + 1} = \frac{W}{L} C_{ox} \mu / V_{aa}^{\gamma + 1}, V_L = v_s L / \mu, R_s, R_d$$

- After the eight parameters are extracted, we recalculate the intrinsic voltages and extract the specific parameters of the targeted type of device

$$V_{GS} = V_{gs} - I R_s$$

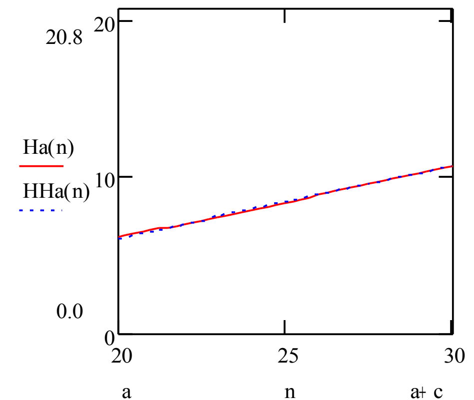
$$V_{DS} = V_{ds} - I\left(R_s + R_d\right)$$

Universal TFT model

- Simple extraction methods are used for the basic model parameters
- The threshold voltage and **γ** are extracted using the integral operator:

$$H\left(V_{gs}\right)=\frac{\int_{V_T}^{V_{gs}} I(V_{gs})dV_{gs}}{I(V_{gs})}=\frac{V_{gs}-V_T}{\gamma+2}$$

- This method is independent of the mobility



Ha(n): $H(V_{gs})$ from a-Si TFT measurements

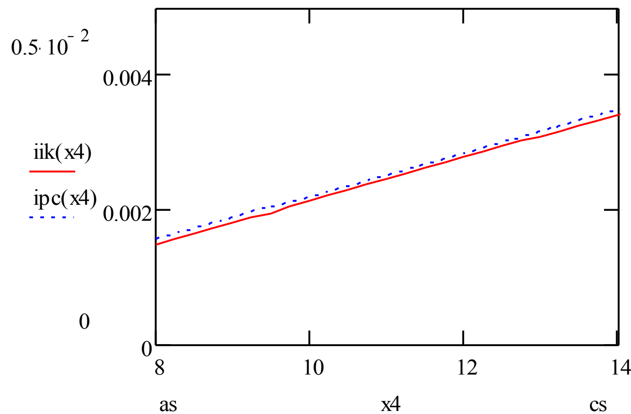
HHa(n): fitted $H(V_{gs})$

Universal TFT model

- The rest of parameters are obtained from specific equations of each type of device
- Subthreshold
  - In a-Si TFT, $I_{sub} \propto (V_{GS} - V_{fb})^{1+\gamma_b}$
    - Using the integral operator we extract V_{fb} and γ_b
  - In poly-Si TFT $I_{sub} \propto e^{V_{gt}/\eta V_{th}}$
    - From a log(I) vs V_{gt} plot we extract η

Universal TFT model

- Saturation threshold voltage (with the DIBL effect)



iik(x4): $H(V_{gs})$ from measurements

ipc(x4): fitted H(Vgs)

$$H(V_{gs}) = \frac{\int_{V_T}^{V_{gs}} I_{sat}(V_{gs})dV_{gs}}{I_{sat}(V_{gs})} = \frac{V_{gs} - V_{Ts}}{\gamma + 3}$$

$$V_T \approx V_{To} + K_{VT} \times V_{ds}$$

- Current dependent resistance:

$$R_{si} = R_{so} + \frac{R_{sio}}{\frac{I}{I_o} + \alpha_{Rs}}$$

- Kink effect (in short-channel poly-Si TFTs)

Universal TFT model

- After extracting all the parameters, we complete the final compact model formulation:

$$I = \frac{g_{ch} V_{ds} (1 + \lambda V_{ds})}{\left(1 + \left(\frac{g_{ch} V_{ds}}{(1 + \lambda V_{ds}) I_{sat}}\right)^m\right)^{1/m}}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(R_s + R_d)} \qquad g_{chi} = \frac{W}{L} \mu q n_s$$

The unified expression of n_s, valid from below to above threshold, depends on the type of device

Poly-Si TFT

$$n_s = 2 n_o \ln\left[1 + \frac{1}{2}\exp\left(\frac{V_{gt}}{\eta V_{th}}\right)\right]$$

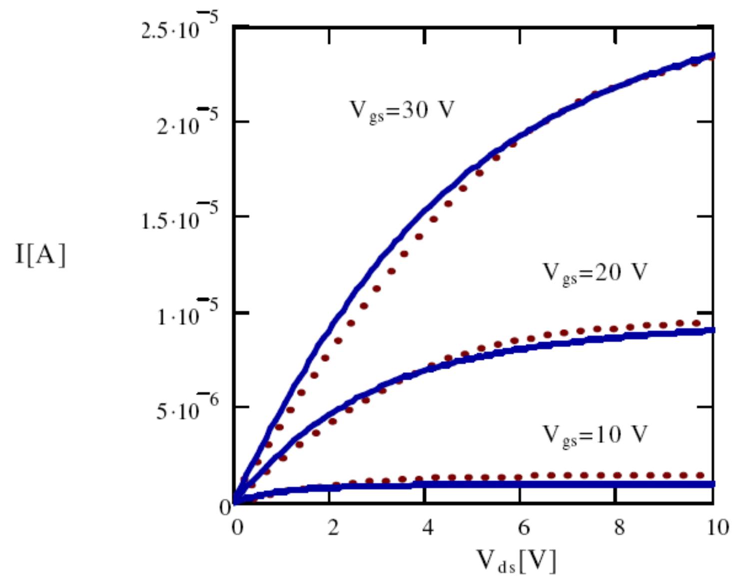
a-Si TFT

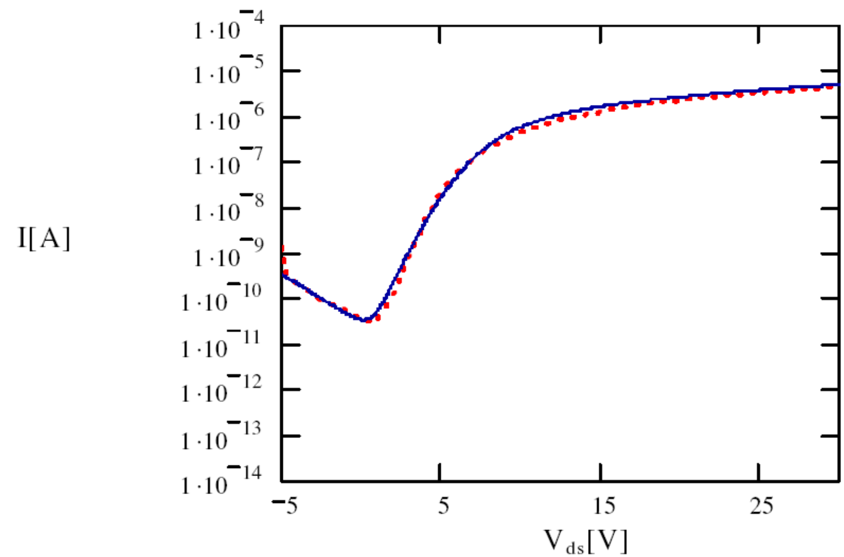
$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

$$n_{sa} = C_{ox} V_{gt}^{\gamma + 1} / V_{aa}^{\gamma}$$

$$n_{sb} = C_{ox} (V_{gs} - V_{fb})^{1 + \gamma_b} / V_{bb}^{\gamma_b}$$

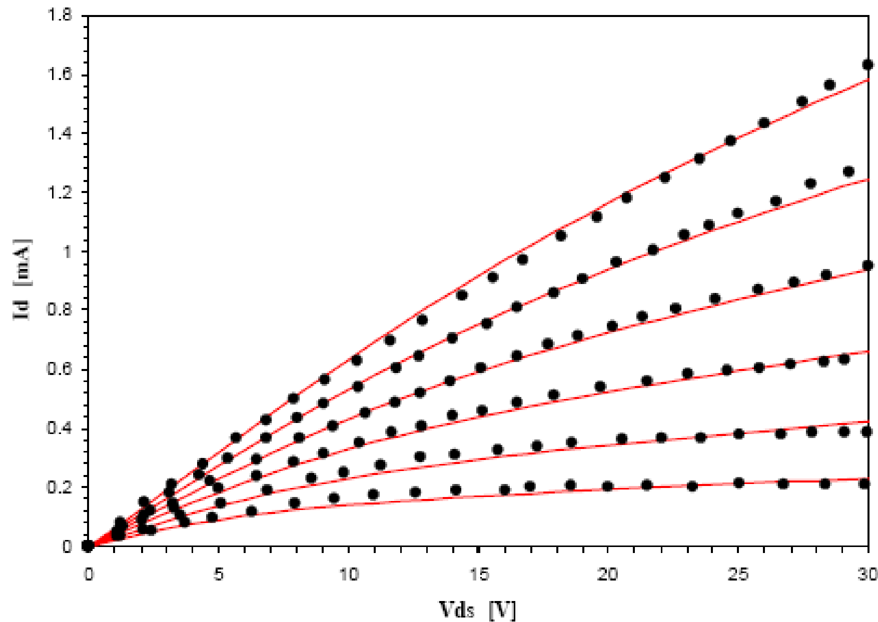
Universal TFT model





Measured (dots) and calculated (solid lines) characteristics of a-Si TFT
TFTs

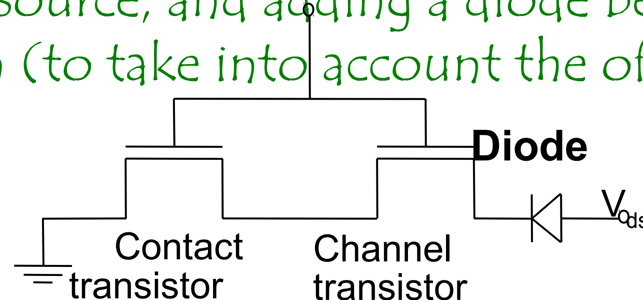
Universal TFT model



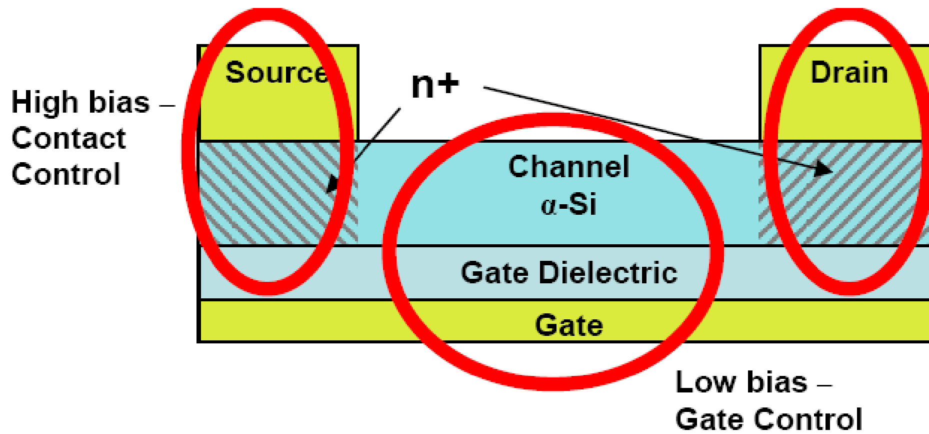
Measured (dots) and calculated (solid lines) output characteristics of polycrystalline ZnO TFTs. Topmost curve, *Vgs* = 30 V, step -5V

Universal TFT model

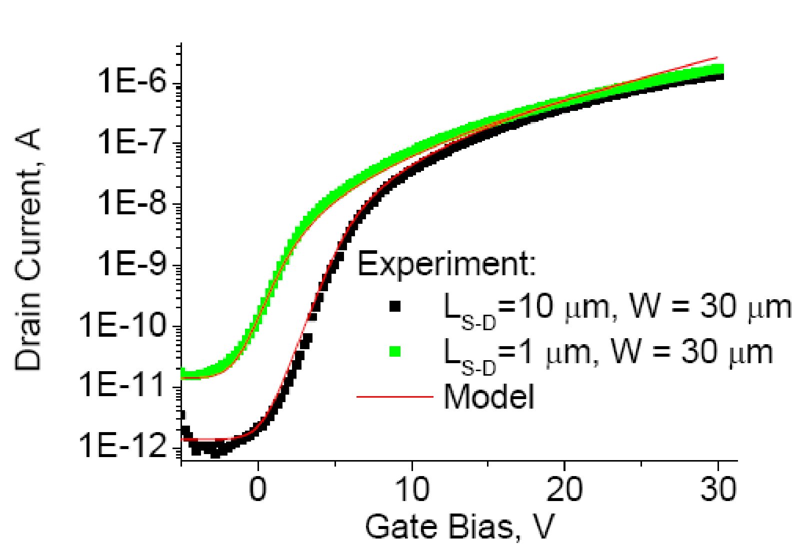
- In short-channel TFTs fabricated by printed, or on flexible substrates, the nonlinear contact effects, due to the injection of carriers through electrode-active layer interface at the source electrode, can be important and even dominate (in the case of organic and polymer TFTs).
- Modeling the contacts with only resistors may be not accurate enough.
- An adequate way to take into account these nonlinear contact effects is to split the device into two transistors: one intrinsic transistor and one contact transistor near the source, and adding a diode between the intrinsic transistor and the drain (to take into account the offset in V_{ds})

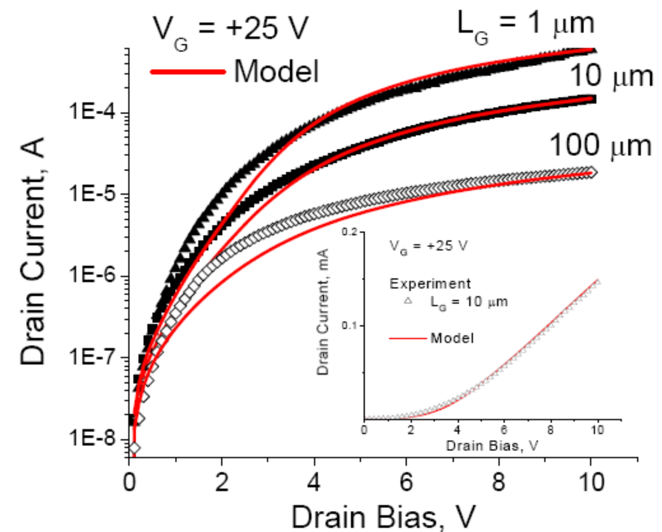


Universal TFT model



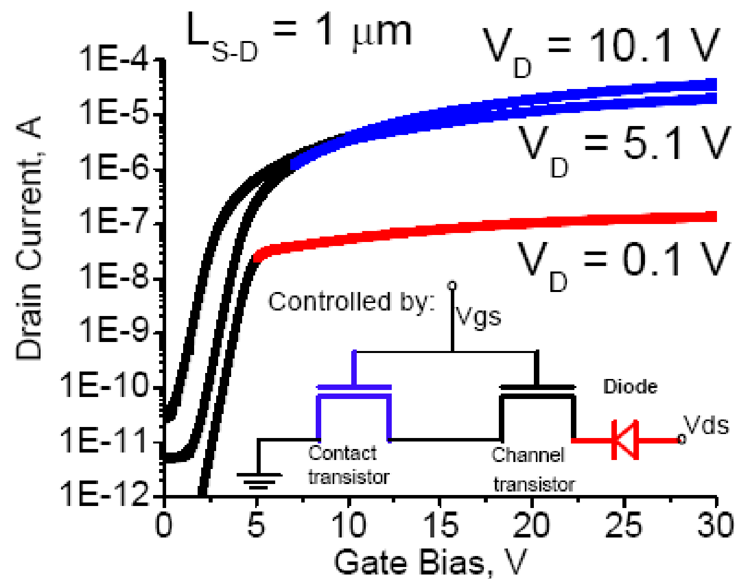
Universal TFT model

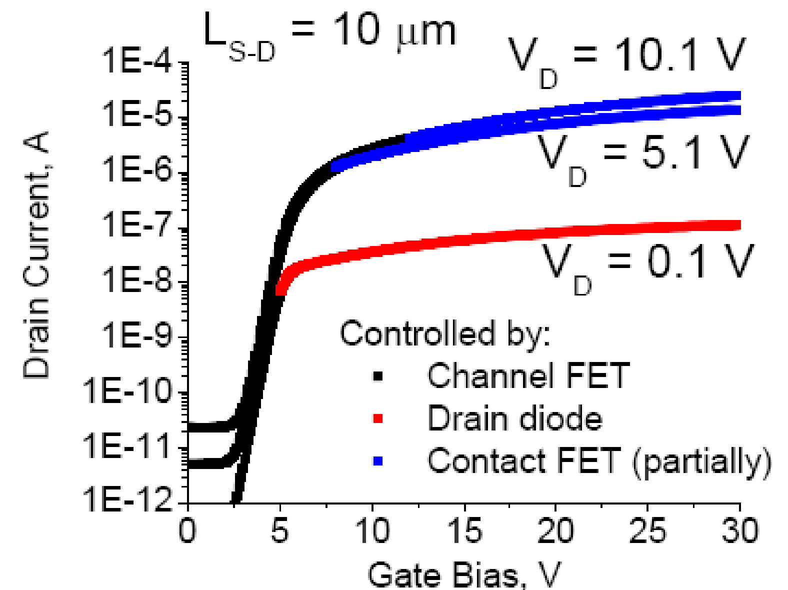




Experimental (symbols) and theoretical (curves)
 transfer characteristics of 1 µm
and 10 µm long printed a-Si TFTs. Vds = 5 V

Universal TFT model





Conclusions

- We have reviewed compact models for the different types of TFTs: amorphous, polycristalline, nanocrystalline, and organic TFTs
- These models are accurate and relatively simple for long-channel devices
- These models become very complex when devices are scaled down, with difficulties to extract model parameters

- We have presented a universal TFT modeling technique
- An eight-parameter basic model is adjusted to the measurements
- Direct extraction techniques are possible
- Using this basic model as a first iteration, we extract the model parameters of the effects which are specific to each type of TFT
- A contact transistor has been added for a better modeling of the nonlinear contact effects in TFTs fabricated by printing or on flexible substrates
- Good agreement with measurements have been found for different types of TFTs