Compact High Frequency MOSFET Modeling

Benjamin Iñiguez

Departament d'Enginyeria Electrònica, Elèctrica i Automàtica ETSE; Universitat Rovira i Virgili

Avinguda dels Països Catalans, 26

43007 Tarragona (Spain)

E-mail: benjamin.iniguez@urv.cat

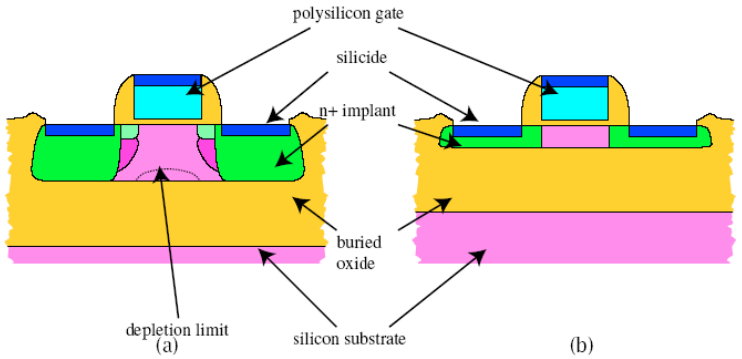
UNIVERSITAT ROVIRA I VIRGILI

Outline

- Introduction
- Development of small-signal models
- High frequency small-signal modeling
- High frequency noise modeling
- Conclusions

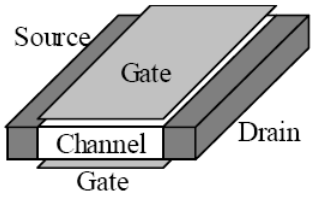
Introduction

- Thin film Fully Depleted SOI MOSFETs offer important advantages over Partially-Depleted SOI MOSFETs:
  - Lower body factor
  - Higher saturation current
  - Better subthreshold slope
  - Smaller mobility degradation
  - Reduced short-channel effects

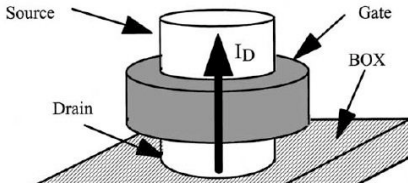


Introduction

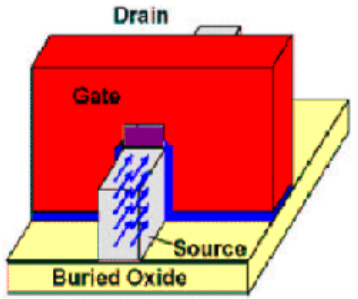
- The non-classical multi-gate devices such as Double-Gate (DG) MOSFETs, FinFETs or Gate-All-Around (GAA) MOSFETs are promising candidates to solve the challenges associated with nanoscale MOSFETs: control of short channel effects, increase of on-currents and threshold voltage control.



DG MOSFET

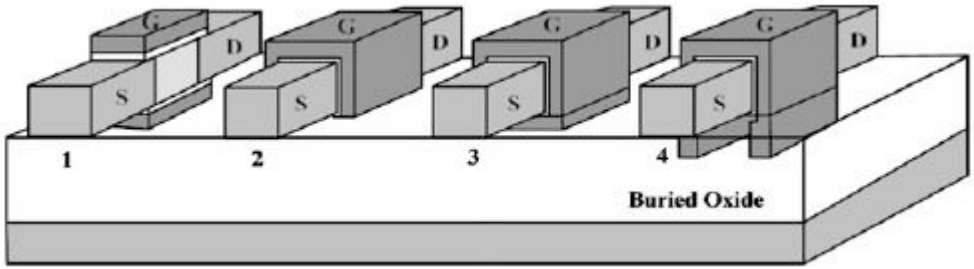


GAA MOSFET



FinFET

Introduction



Schematic device structures of MuGFETs:1) double-gate; 2) triple-gate; 3) quadruple-gate; 4) PI-gate

Introduction

- The availability of accurate compact models of Multiple-Gate MOSFETs in integrated circuits is critical for the future design of circuits using those devices
- Circuit design requires a complete small-signal model, with analytical or semi-analytical expressions of:
  - Current
  - Total charges
  - Transconductance and conductance
  - Transcapacitances

Introduction

- The small-signal equivalent circuit is defined by the transconductance, conductance and capacitances.
- Small-signal gate transconductance, often referred to simply as "transconductance" is defined as:

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{BS},V_{DS}}$$

Small-signal substrate transconductance (4-terminal MOSFET):

$$g_m = \left.\frac{\partial I_D}{\partial V_{BS}}\right|_{V_{GS},V_{DS}}$$

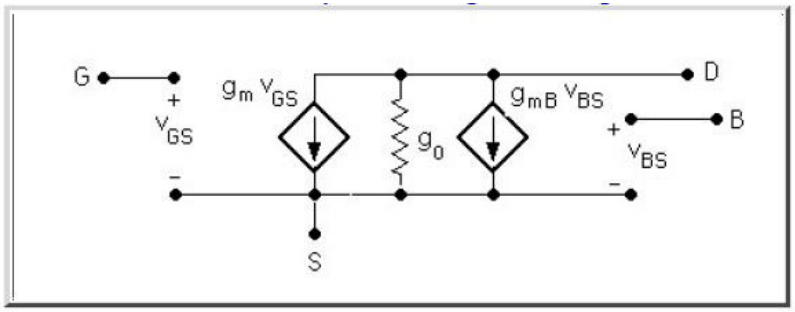
Small-signal drain (or "output") conductance:

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS},V_{BS}}$$

Introduction

- Low frequency small-signal equivalent circuit:

$$\Delta I_D = g_m \Delta V_{GS} + g_{mb} \Delta V_{BS} + g_d \Delta V_{DS}$$



Introduction

- The capacitance model is almost always based on the quasistatic approximation, which assumes that the charges in a device can follow the varying terminal voltages immediately, without any delay.
- The capacitances are computed through mathematical differentiation of the electrode charge with respect to the voltage.

$$C_{ij} = k\frac{dQ_i}{dV_j} \quad \text{where} \quad \begin{cases} 1 \text{ for } i = j \\ -1 \text{ for } i \neq j \end{cases}$$

In addition:

$$\sum_i C_{ij} = \sum_j C_{ji} = 0$$

In a 4-terminal FET (such as a symmetric DG MOSFET), out of the 16 capacitance elements, there are 9 that are independent

In a 3-terminal FET (such as a symmetric DG MOSFET), out of the 9 capacitance elements, there are 4 that are independent

Introduction

- Electrode charges are obtained by integrating the charge densities along the channel

$$Q_G = -W\int_0^L Q_m dx - Q_B$$

$$Q_G + Q_B + Q_S + Q_D = 0$$

Ward-Dutton partitioning:

$$Q_D = W\int_0^L \frac{x}{L} Q_m dx$$

$$Q_S = W\int_0^L \left(1 - \frac{x}{L} Q_m\right) dx$$

Introduction

- However, it has been demonstrated that Ward-Dutton partitioning is not correct when velocity saturation, mobility degradation or lateral asymmetry are considered

[1] A. S. Roy, C. Enz, and J. Sallese, "Charge, current and noise partitioning scheme in presence of mobility degradation," *IEEE Electron Device Lett.*, vol. 27, no. 8, pp. 674–677, Aug. 2006.
[2] A. Aarts, R. van der Hout, J. Paasschens, A. Scholten, M. Willemsen, and D. Klaassen, "New fundamental insights into capacitance modeling of laterally nonuniform MOS devices," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 270–278, Feb. 2006.

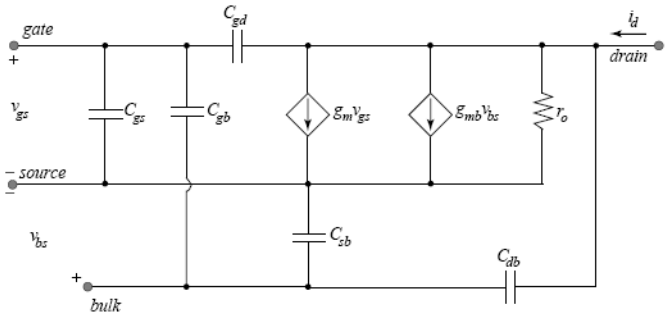
A more general partitioning in:

A. S. Roy, C. Enz, and J. Sallese, **Source–Drain Partitioning in MOSFET**
IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 54 Issue: 6 Pages: 1384-1393

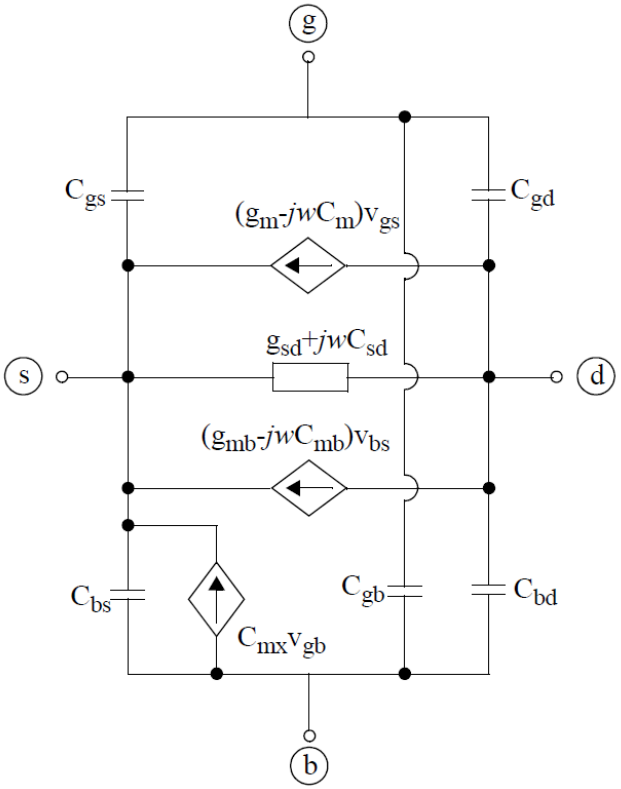
Published: JUN 2007

Introduction

- Simple quasi-static small-signal model and low and medium frequencies:



Introduction



$$C_m = C_{dg} - C_{gd}$$

$$C_{mb} = C_{db} - C_{bd}$$

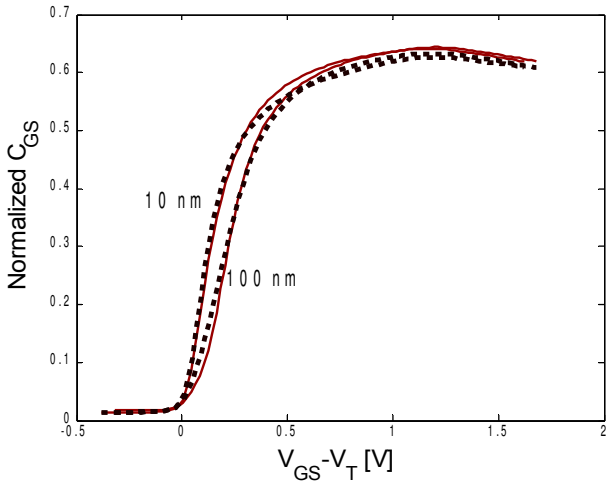
$$C_{mx} = C_{bg} - C_{gb}$$

Introduction

- **Requirements of a suitable compact model:**
  - Analytical or semi-analytical expressions of the channel current and the small- and large-signal parameters
  - Expressions valid in all operating regimes, with continuous transitions between the different regimes
  - Parameters should contain geometry dependences
  - Easy parameter extraction should be possible
  - Accuracy of the expressions and their derivatives, up to the highest possible order

Effect of volume inversion on capacitances in DG MOSFETs

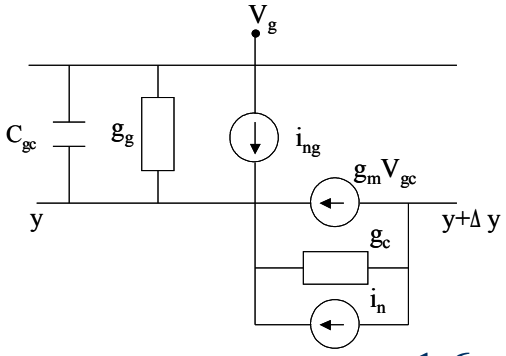
- Volume inversion increases C_{GS}. It might compensate the increase of g_m due to volume inversion and therefore decreasing f_T



Normalized gate-to-source capacitance in saturation regime (V_{DS} = 1 V) with respect to the gate voltage overdrive for T_{Si}= 10 and 100 nm. Symbol line: DESSIS-ISE simulations. Solid line: analytical model.

Small-signal equivalent circuit

- The active line approach, used to extend the model to high frequency operation, is based on splitting the channel into a number of elementary sections
- Our quasi-static small-signal equivalent circuit, to which we add additional microscopic diffusion and gate shot noise sources, is applied to each section
- Our charge control model allows to obtain analytical expressions of the local small-signal parameters in each segment



Small-signal equivalent circuit

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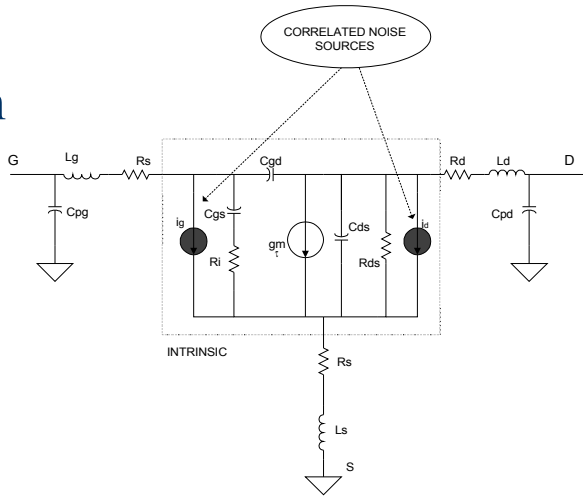
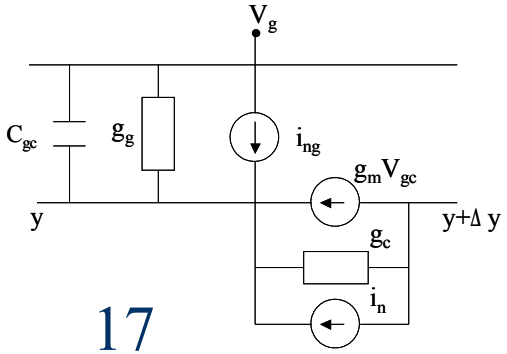
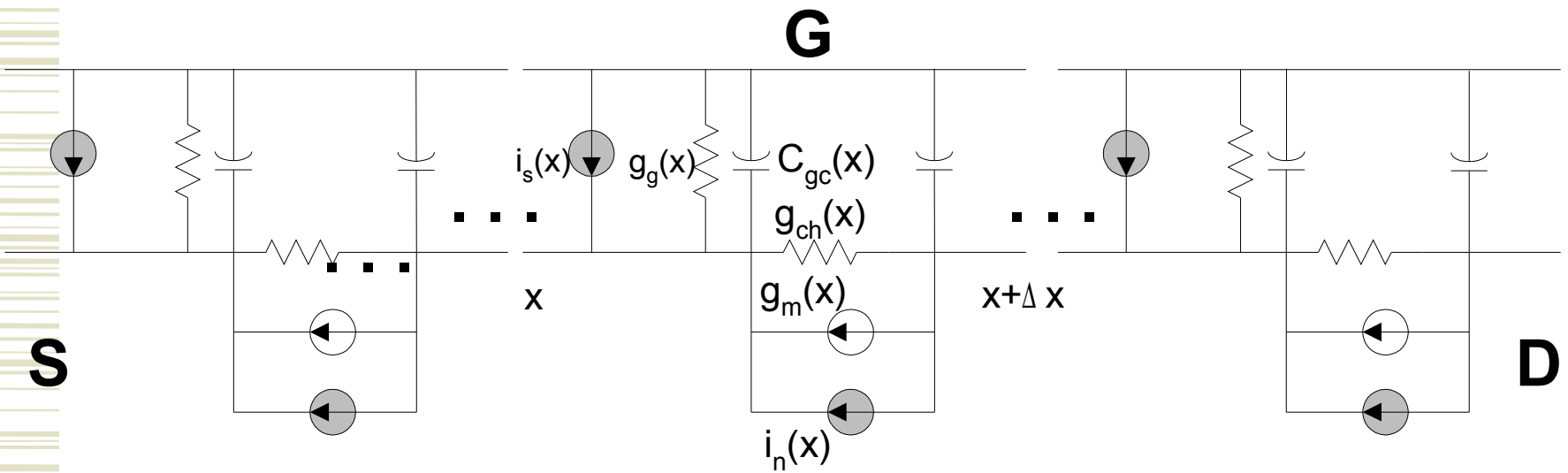




Small-signal equivalent circuit



High frequency noise modelling

- In order to model noise using this technique, several approaches have been considered:
  - The contribution to noise of the length where carriers travel at the saturation velocity must not neglected.
  - A Diffusion Coefficient is used to define the microscopic noise current sources, in order to consider the short channel effect. The expression of the diffusion coefficient is valid from low to high fields
  - Mobility reduction should be considered along the channel.

Small-signal equivalent circuit

- The active transmission line is analysed using the nodal admittance method
- Once the intrinsic admittance matrix, Y_i, and admittance correlation matrix, C_{Yi}, are obtained, extrinsic elements are included
- Thermal noise is considered for access resistances
- Gate tunnelling current, and its associated shot noise source are added

- The model allows to calculate the important P, R and C parameters, which are related to the gate and drain diffusion noise current, and their correlation

- $\langle i_g^2 \rangle = 4kT_a R C_{gsi}^2 \omega^2 \Delta f / g_m \quad \langle i_d^2 \rangle = 4kT_a P g_m \Delta f$

- Using the model, we calculate the S-parameters and the usual noise parameters: F_{min}, R_n (equivalent noise resistance) and G_{opt} (optimum reflection coefficient)

Shot noise modeling

- The effect of the tunneling gate current cannot be neglected for oxide thicknesses smaller than 2 nm.
- Experimental results indicate that in thin-film gate oxides the gate current is due to direct tunneling.
- The expression of the vertical field used in I_G corresponds to the addressed type of multiple-gate MOSFET.
- This gate current adds locally a shot noise source located across the gate conductance.
- Considering the case of local shot noise sources distributed along the channel, it turned out that the tunneling gate current adds two gate and drain shot noise sources.

- Shot noise sources are uncorrelated with diffusion noise sources (different physical origins)

Cut-off and maximum oscillation frequencies

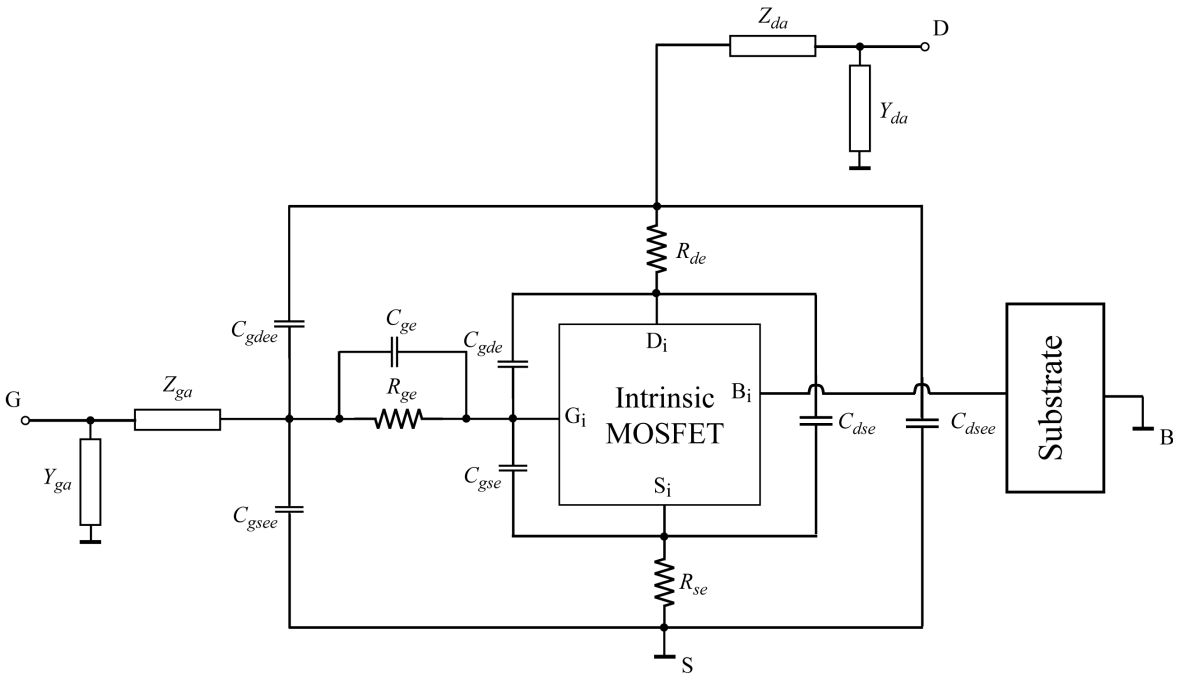
- The cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are the most important RF figure merit parameters

$$f_T = \frac{g_m}{2\pi\, C_{gs}\sqrt{1+\,2C_{gd}\,/\,C_{gs}}} \approx \frac{g_m}{2\pi\,(C_{gs}+\,C_{gd})}$$

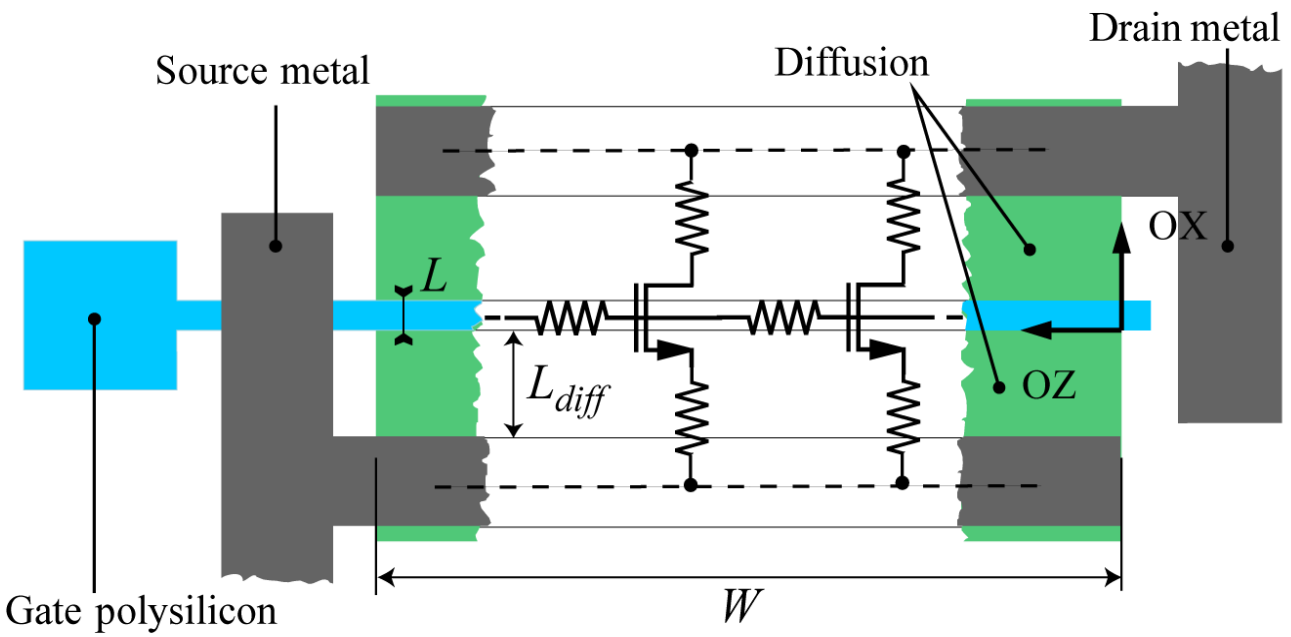
$$f_{\max} \approx \frac{g_m}{2\pi\, C_{gs}\sqrt{4(R_s+\,R_i+\,R_g)\left(\,g_{ds}+\,g_m\,\frac{C_{gd}}{C_{gs}}\right)}}$$

- C_{gs} and C_{gd} are the gate-to-source and gate-to-drain small signal capacitance respectively, including fringing and overlap capacitances
- g_m - gate transconductance
- R_i (in series with C_{gs}) takes into account the distributed nature of the MOSFET
- g_{ds} - drain-to-source conductance

Complete equivalent circuit topology



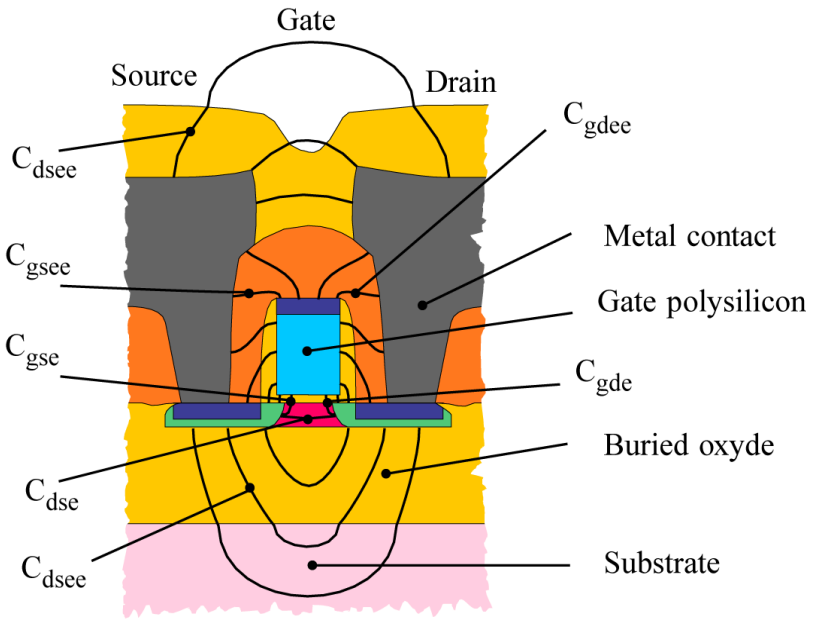
Distributed gate equivalent circuit



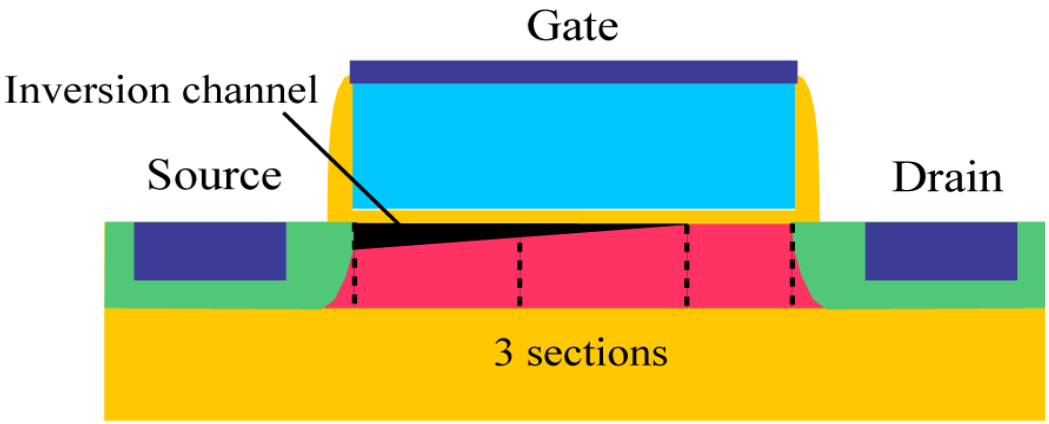
R_{ge} and C_{ge} take into account the propagation effects along the gate width

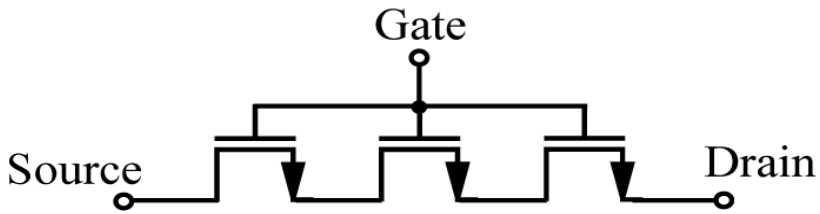
Extrinsic Model

Extrinsic capacitances

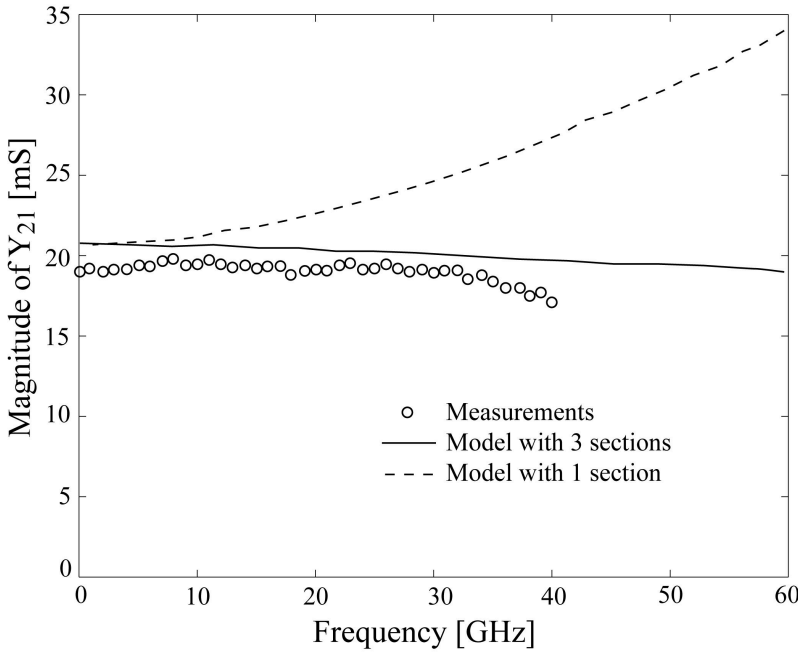


- The device is split into smaller channel sections and a quasi-static (QS) model is applied to each section

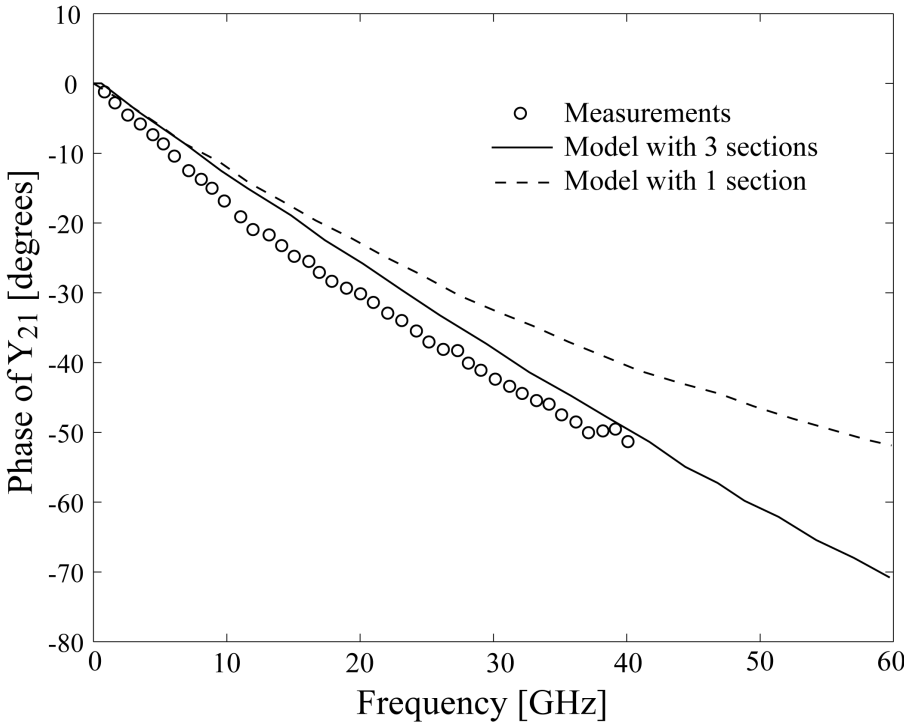




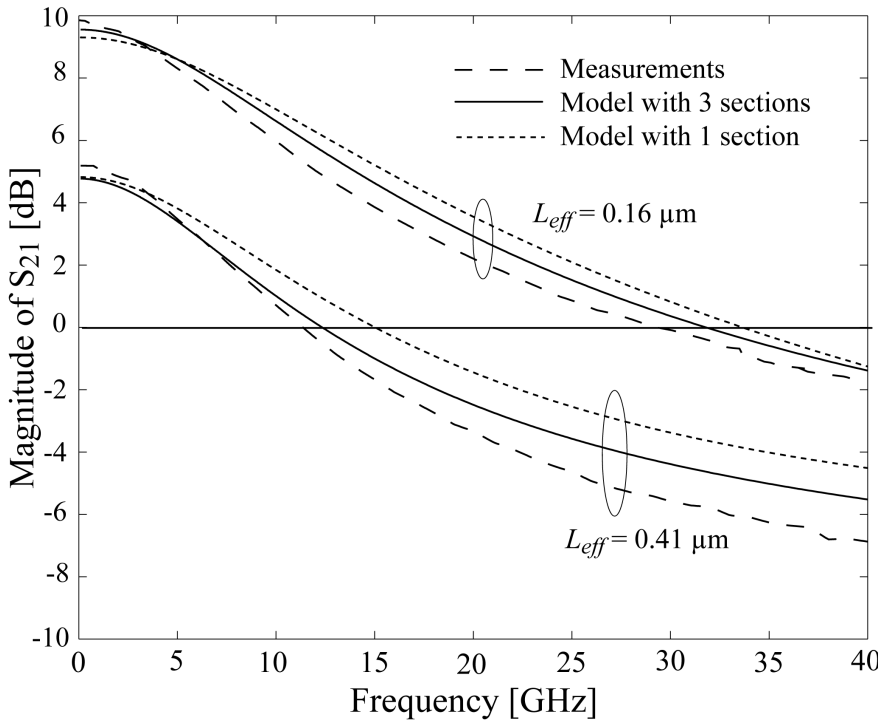
Magnitude of the intrinsic Y_{21}. SOI nMOSFET with $L_{eff} = 0.41$ µm



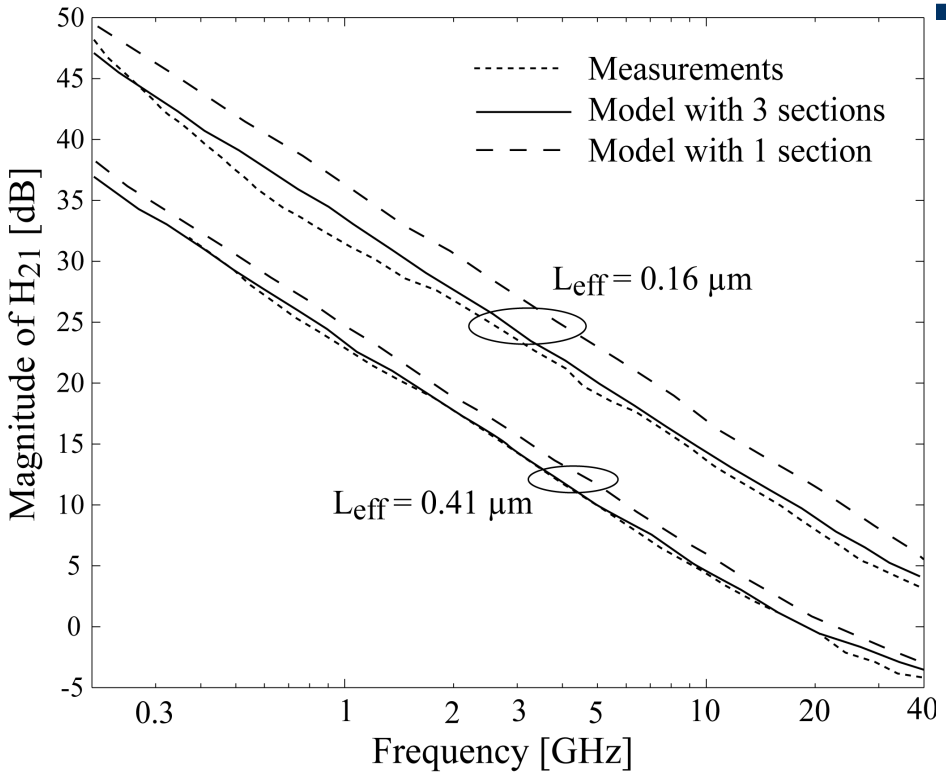
Phase of the intrinsic Y_{21}. SOI nMOSFET with L_{eff}= 0.41 µm



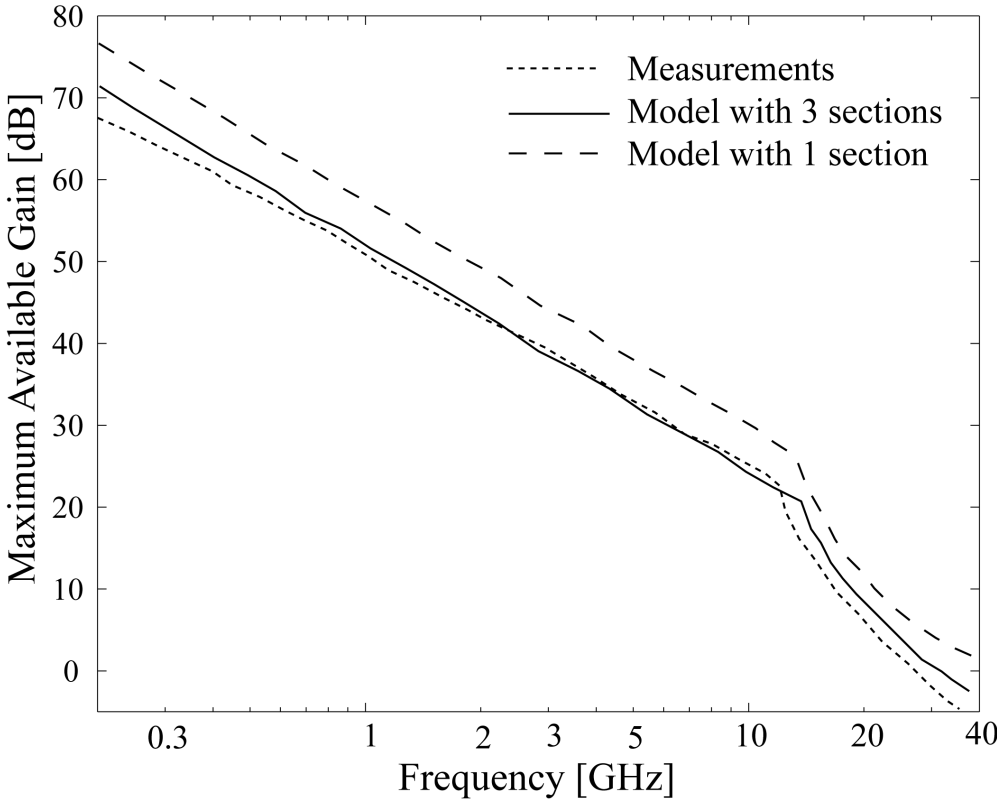
Magnitude of S_{21}



RESULTS H_{21} parameter



MAG parameter for a SOI nMOSFET with L_{eff}=0.16µm



Results

- We have used our model to study the evolution of high frequency characteristics with the downscaling
- For this study, we have considered the scaling of oxide thickness and silicon thickness as the channel length is reduced, t_{Si}=0.4 L for DG MOSFET and t_{Si}=0.2 L for SG MOSFET
- For GAA MOSFET a constant Si radius R=1.25 nm is used
  - The number of parallel fins is selected to have the same total gate width as for SG and DG devices
- The gate oxide thickness is fixed to t_{ox}=1.5 nm
- The scaling of the mobility has also been considered

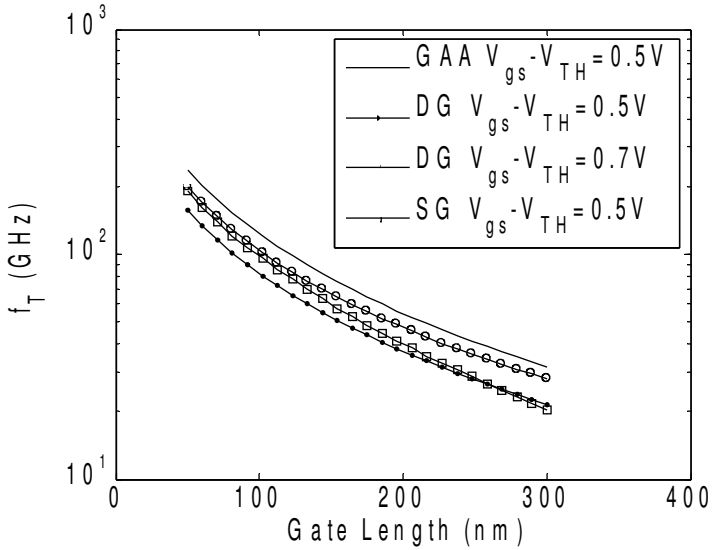
Results: figures of merit

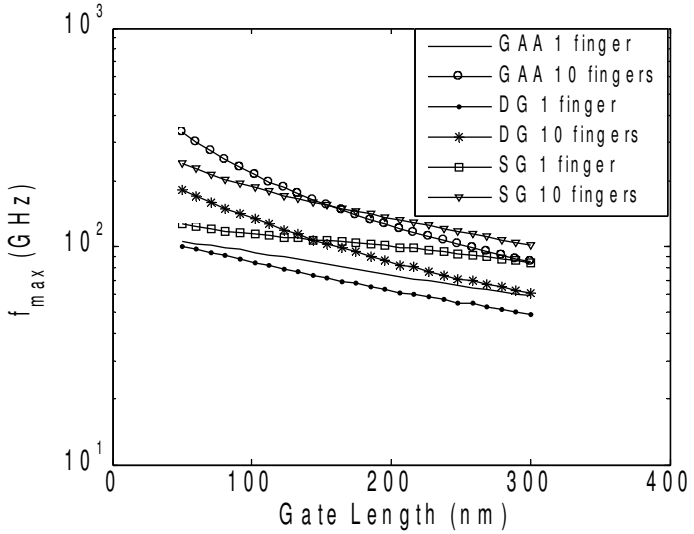
We see a better performance in f_T for GAA than for DG and SG SOI MOSFETs.

This fact is due to the higher transconductance in these devices (due to volume inversion) . For the same bias point ($V_{GS} - V_T = 0.5$ V), the f_T for the long DG is slightly better than for SG devices, but for smaller gate length, the capacitance in DG devices does not decrease as fast as the transconductance increases in comparison with SG devices.

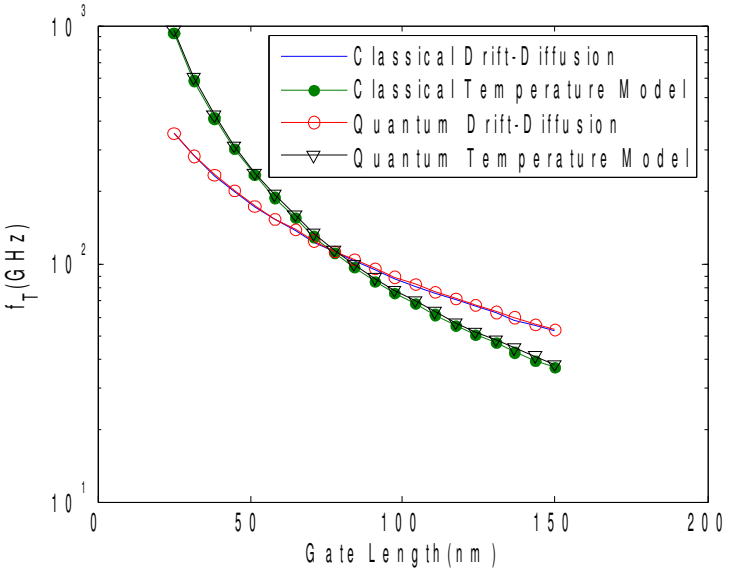
The *fT* for DG devices may be improved with a small increase in the gate voltage. This behaviour is explained because the effective gate voltage at which the peak transconductance in DG devices occurs is slightly higher than in SG SOI MOSFETs. Also, we have to say that the characteristic length is not the same in DG and SG devices due the gate-length scaling rule employed here

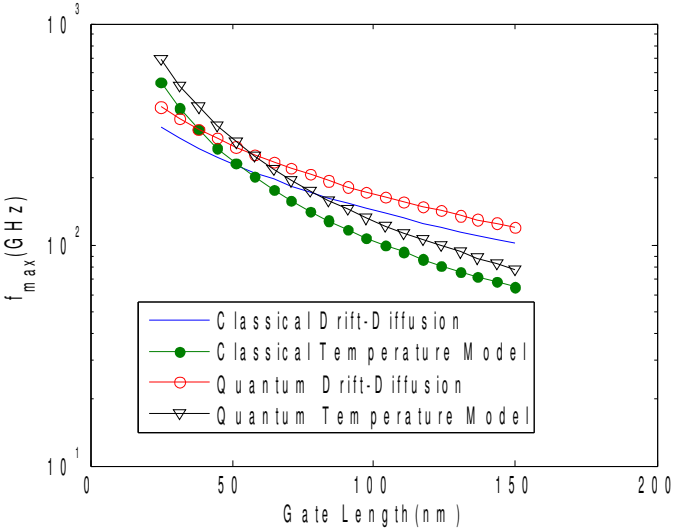
Results: figures of merit





Results: figures of merit

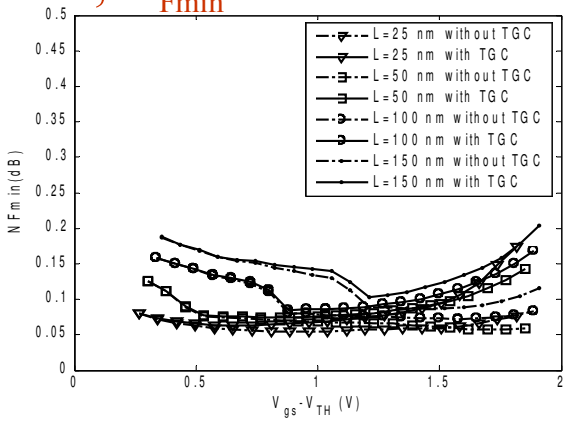




FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, V_{ds}=1 V, V_{gs}-V_{TH}=0.5V).

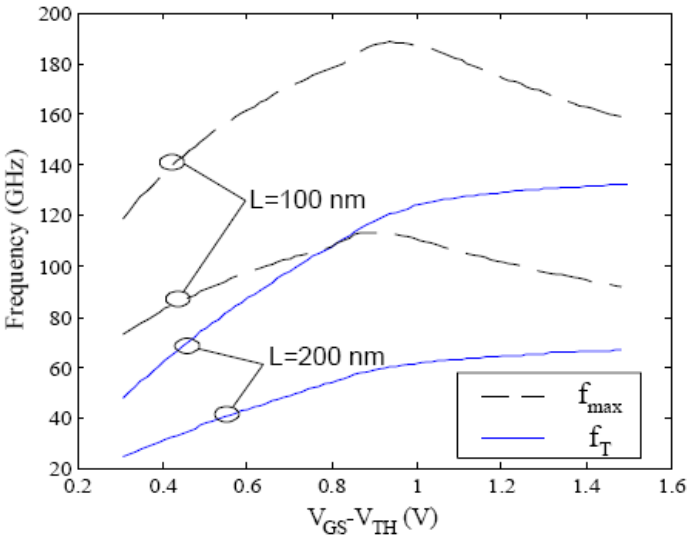
Results: shot noise

- If the gate tunnelling current is neglected, both N_{Fmin} and R_n decrease with channel length
- But as L decreases, the tunnelling current becomes more important (due to the downscaling of t_{ox})
- The tunneling gate current effect dominates for frequencies below the shot gate noise transition frequency (a few GHz)
- When the gate voltage increases, the tunnelling current grows, and as a result, N_{Fmin} increases

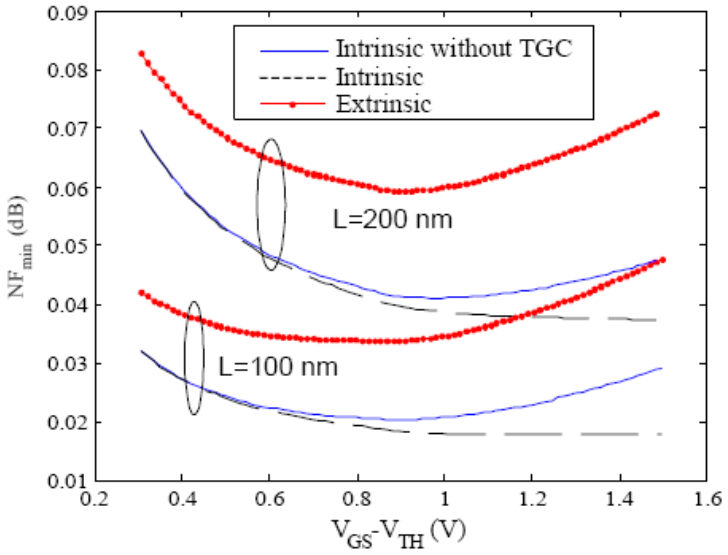


Minimum Noise Figure (NF_{min}) of an undoped DG (t_{ox}=1.5 nm, V_{DS}=1V) as function of gate voltage for several gate lengths at 1GHz

Results: figures of merit

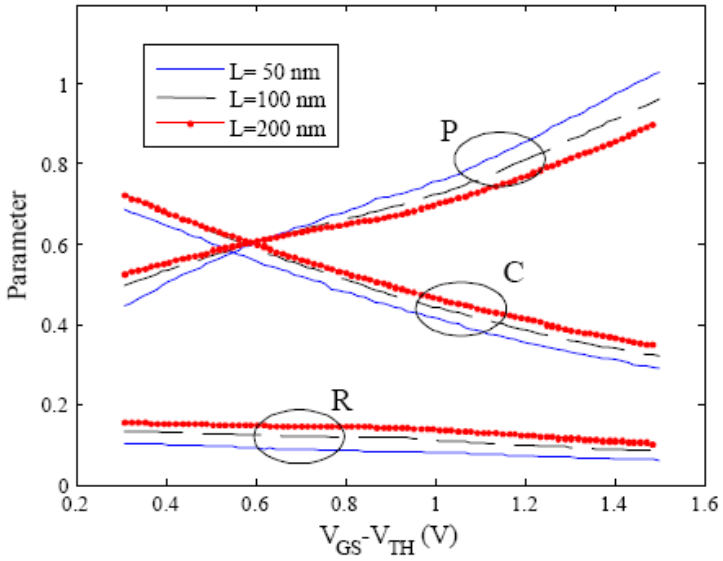


f_T and f_{max} as function of the gate voltage overdrive for GAA MOSFETs (total gate width W=10 µm, V_{ds}=1V)



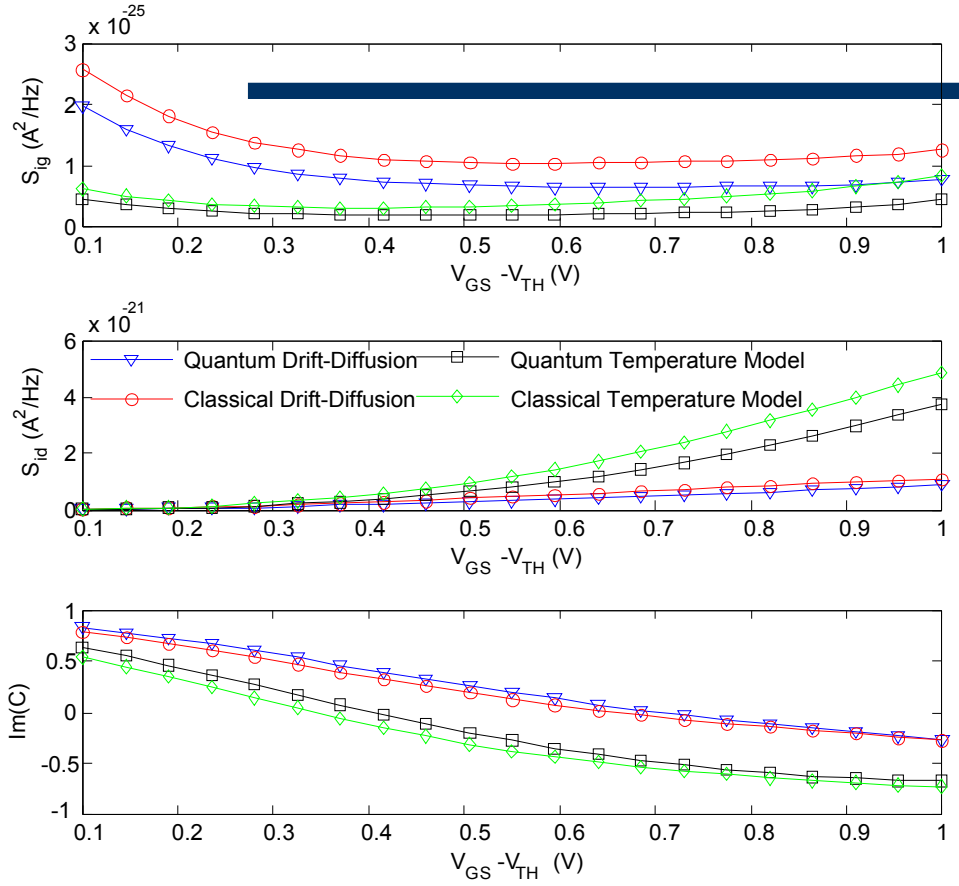
Comparison between intrinsic and extrinsic N_{Fmin} without including tunnel gate effect and including TGC as function of gate voltage, for GAA Intrinsic MOSFETs with 4 fingers (total gate width W=10 µm , V_{ds}=1V).

Results: noise parameters



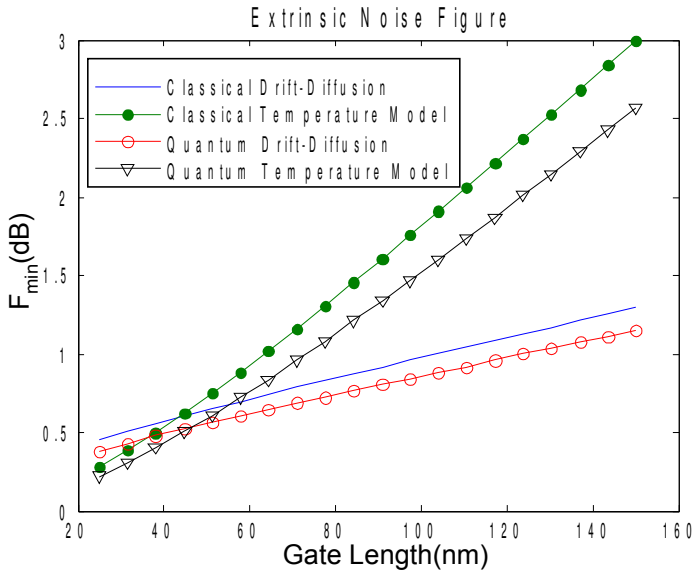
Admittance parameters R,P,C as function of gate voltage for a GAA MOSFETs (total W=10 μm, V_{ds}=1V)

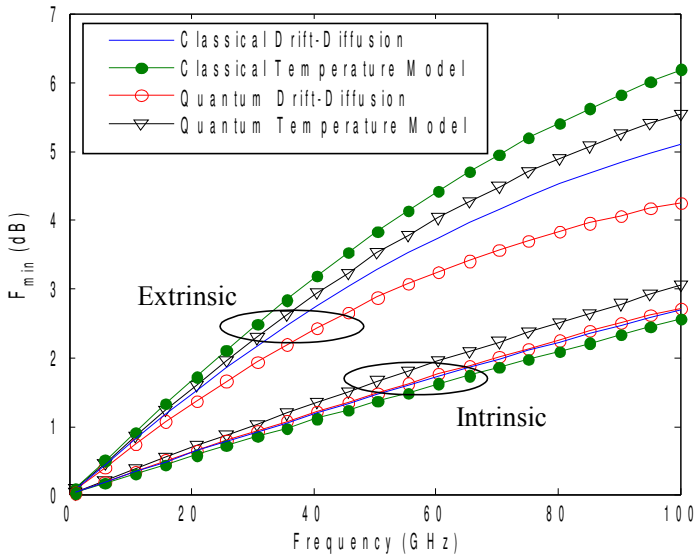
Results: noise parameters



Gate and drain spectral densities and imaginary part of the correlation coefficient as a function of the gate overdrive voltage for a FinFET (Wfin=10 nm, Hfin=30 nm, tox=1.5 nm, tbox=50 nm, L=50 nm, 100 fingers, Vds=1V, f=10 GHz)

Results: noise parameters



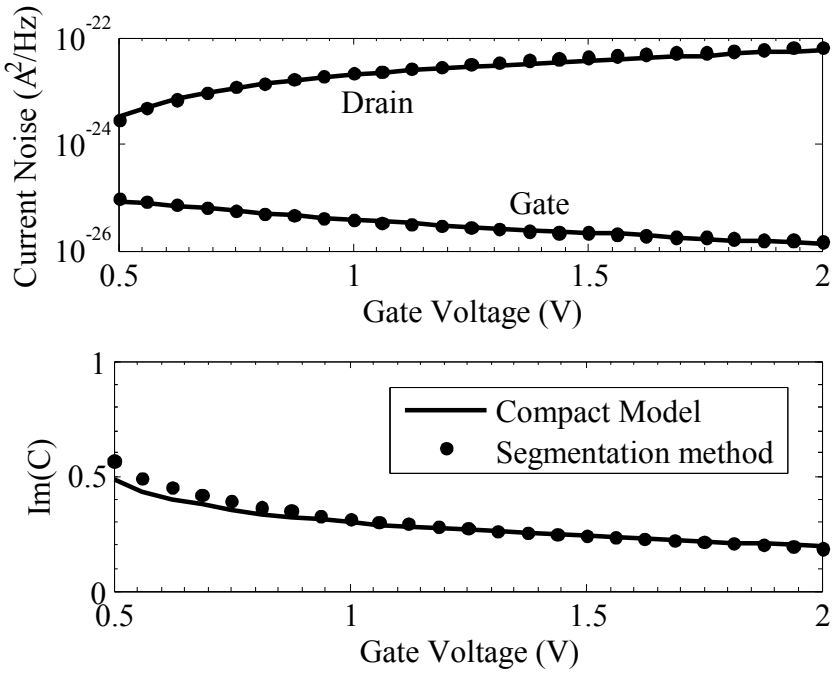


FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, 100 fingers, V_{gs}-V_{TH}=0.5V, V_{ds}=1V)

Results: noise parameters

Singlepiece compact expressions to model the drain, gate current noise spectrum densities and theirs correlation were derived for for DG and GAA MOSFETs.

Comparison of current noise densities and imaginary part of correlation coefficient as function of gate voltage calculated with the segmentation method (●) and the singlepiece model (—) for a DG MOSFET with L=1 μm, t_{ox}=2 nm, t_s=34 nm, V_{DS}=2V, f=1 GHz).



Conclusions

- We have proposed a compact RF modeling scheme for MOSFETs, based on a quasi-static charge control model and the transmission line approach
- The channel current model can be based on an electronic energy transport model which includes the velocity overshoot and hot carrier effects in the noise temperature
- There are important differences in drain current, f_T and f_{max} and noise performances between drift-diffusion and hydrodynamic models for short gate lengths, due to the velocity overshoot increasing the transconductance, thus f_T and f_{max}
- Electronic temperature transport model predicts higher noise temperature in the saturation bias region than the classical relation between carrier temperature and electric field, resulting in a higher noise figure
- For gate lengths shorter than about 50-60 nm, the increase of f_T due to velocity overshoot compensates the channel temperature increment finally resulting in a lower noise figure

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