Simulation and Modeling of Multiple-Gate SOI MOSFETs

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Compact Modeling Network

UNIVERSITAT ROVIRA I VIRGILI

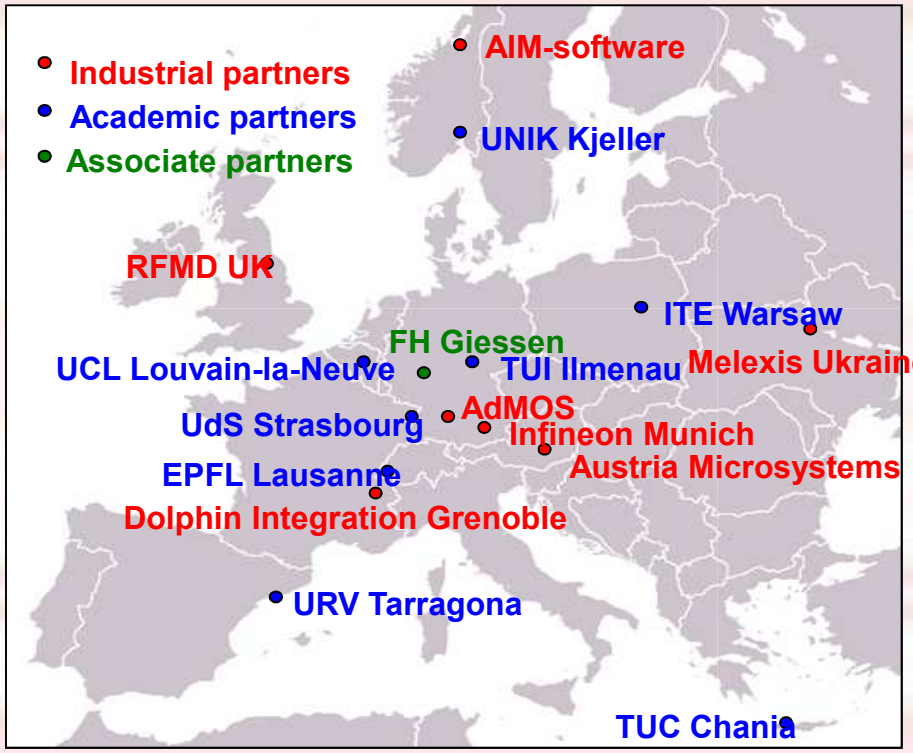
Outline

Presentation of the COMON project
- Who are we?
- Goals

1. Introduction
2. 1D core and Design-Oriented compact models
3. Hyperbolic function based compact models
4. Conformal mapping based compact models
5. Conclusions

EU COMON Project – Who are we?

COMON: COmpact MOdeling Network



✓ "Marie-Curie" Industry-Academia Partneship and Pathways project (IAPP FP7, ref. pro. 218255)

✓ Duration:
4 years, started from December 1 2008.

✓ Coordinator:
Prof. B. Iñiguez
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➢ More information available on our website:
http://www.compactmodelling.eu

Goals of the COMON project

To address the full development chain of Compact Modeling, to develop complete compact models of Multi-Gate MOSFETs (Foundry: Infineon, now Intel), HV MOSFETs (Foundry: Austriamicrosystems) and III-V HEMTs (RFMD (UK)).

Development of complete compact models of these types of advanced semiconductor devices.

Development of suitable parameter extraction techniques for the new compact models.

Implementation of the compact models and parameter extraction algorithms in automatic circuit design tools.

Demonstration of the implemented compact models by means of their utilization in the design of test circuits.

Validation and benchmarking: compact model evaluation for analog, digital and RF circuit design: convergence, CPU time, statistic circuit simulation.

As an IAPP project the ultimate COMON goal is the know-how transfer from the academia to the industry

2nd Training Course on Compact Modeling

- Tarragona, June 28-29 2012
- 12 lectures conducted by top international researchers in fields related to compact modeling
- www.compactmodelling.eu

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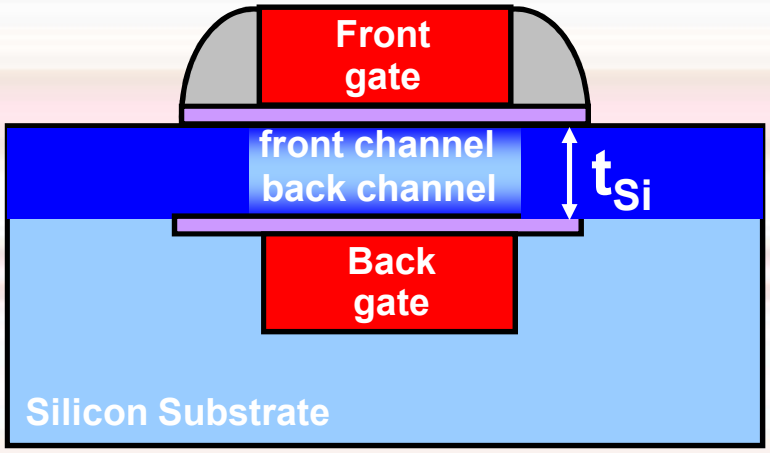
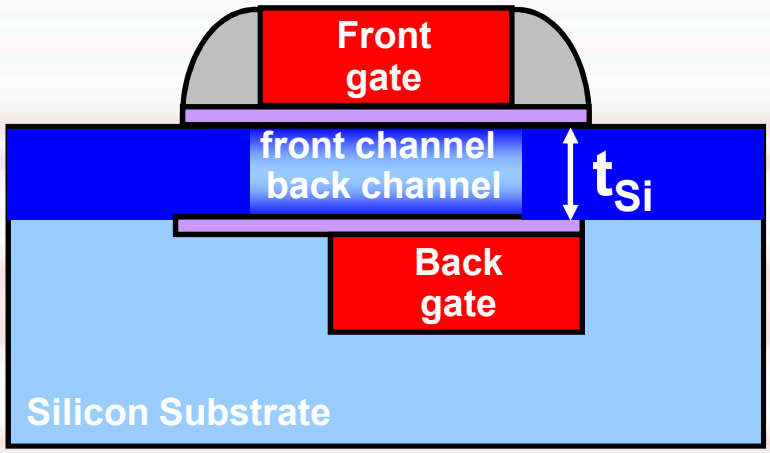
Why several gates?



'Planar double-gate' architecture

- Double-gate transistor
- Two conduction channels
  - → good I_{ON}
- Excellent electrostatic coupling:
  - → ✓ Short Channel Effects (SCEs) reduction
  - ✓ leakage currents reduction

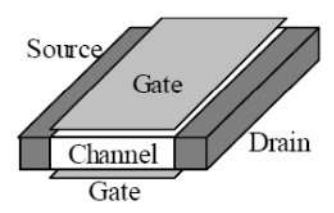
- But self-alignment of the gates required to maintain Double-gate advantages
  - → idea of vertical gates: FinFET type transistors



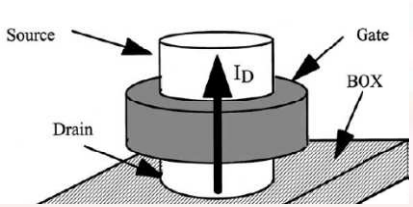
Gate misalignment

Multi-Gate MOSFETs

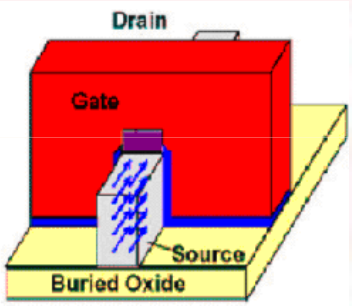
- The non-classical multi-gate devices such as Double-Gate (DG) MOSFETs, FinFETs or Gate-All-Around (GAA) MOSFETs show an even stronger control of short channel effects, and increase of on-currents taking advantage of volume inversion/accumulation.



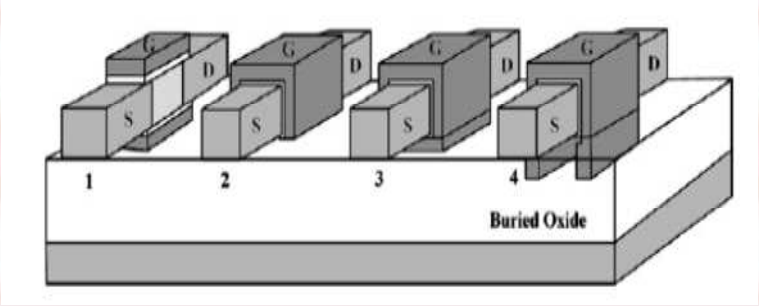
DG MOSFET



GAA MOSFET



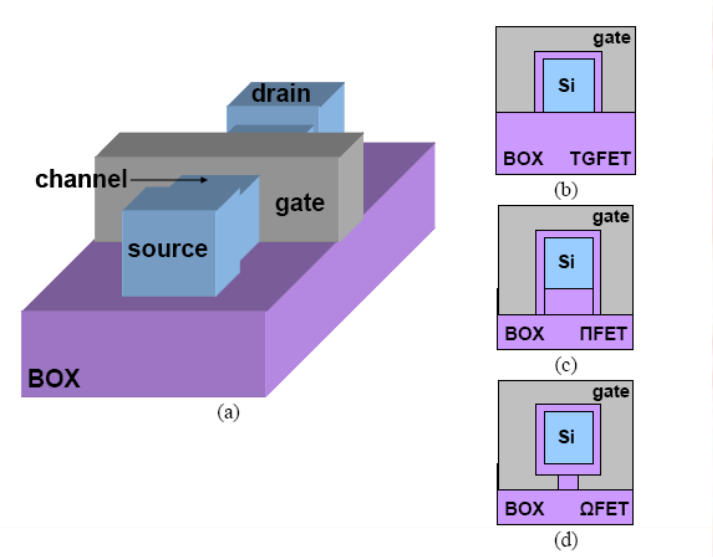
FinFET



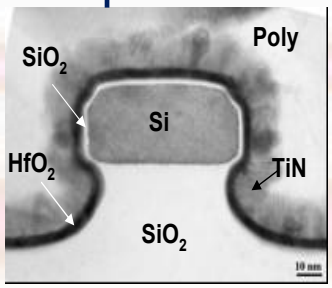
Schematic device structures of MuGFETs:1) double-gate; 2) triple-gate; 3) quadruple-gate; 4) PI-gate

Pi-gate/Omega-gate FETs

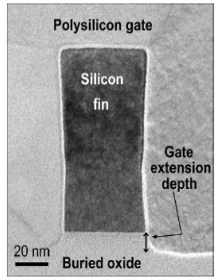
- Pi-gate/Omega-gate FETs: very pragmatic process flow



Tranversal cross-section for Triple-gate (b), Pi-gate FETs (c), and Omega-gateFETs (d).

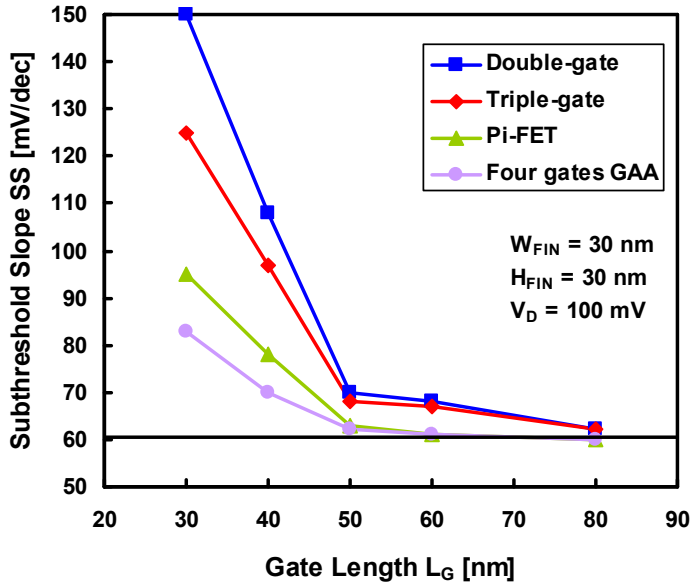


LETI [Jahan'05]



TI / Infineon [Frei'04]

The process-induced gate overetch in the BOX is improving the device scalability



Simulated Subthreshold slope SS vs. gate length L_G for TG and Pi-FETs (from [Park'01])

[Jahan'05] C. Jahan et al., VLSI tech. dig., 2005.
[Frei'04] J. Frei et al., IEEE Electron Device Letters, vol. 25, no. 12, pp. 813-816, 2004.
[Park'01] J.-T. Park, J.-P. Colinge, C.H. Diaz, "Pi-Gate SOI MOSFET", IEEE Electron Device Letters, vol. 22, no. 8, pp. 405-406, 2001.

Compact models

- The availability of accurate compact models of Multiple-Gate MOSFETs in integrated circuits is critical for the future design of circuits using those devices
- Circuit design requires a complete small-signal model, with analytical or semi-analytical expressions of:
  - Current
  - Total charges
  - Transconductance and conductance
  - Transcapacitances

Compact models

- **Requirements of a suitable compact model:**
  - Analytical or semi-analytical expressions of the channel current and the small- and large-signal parameters
  - Expressions valid in all operating regimes, with continuous transitions between the different regimes
  - Parameters should contain geometry dependences
  - Easy parameter extraction should be possible
  - Accuracy of the expressions and their derivatives, up to the highest possible order

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1D Models

The first step to develop a compact model is to consider a well behaved device, with good electrostatic control by the vertical field (from the gate) and where the derivative of the lateral field in the direction of the channel length can be neglected compared to the derivative of the vertical field in the direction perpendicular to the channel.

- This is the gradual channel approximation, and simplifies the electrostatic analysis.
- This leads to neglect the short-channel effects
- In thin-film Multi-Gate MOSFETs, we expect that a long-channel device model can be applied to significantly shorter channels than in standard MOSFETs
- We also have considered an n-channel device, with acceptor doping or with no doping. The hole concentration can be neglected in the normal operation regime.
  - Of course, our analysis can easily be extended to p-channel devices

1D models: DG MOSFETs

By integrating the Poisson's equation between the centre (y=0) and the top surface of the film (y=-t_{si}/2) we get:

$$E_S(x) = \sqrt{\frac{2qN_A}{\varepsilon_{Si}}} \sqrt{(\phi_s - \phi_0) + \frac{kT}{q}\frac{n_i^2}{N_A{}^2} e^{\frac{q}{kT}[\phi_s - V(x)]} \left(1 - e^{-\frac{q}{kT}(\phi_s - \phi_0)}\right)}$$

where $\phi_S = \phi(x, -t_{Si}/2)$ is the surface potential and $\phi_o = \phi(x,0)$ is the potential in the middle of the film.

Unfortunately, the potential at the center is unknown and we cannot analytically integrated for the potential.

An analytical model is possible with an approximate expression of the difference between the two potentials:

an empirical expression that, using adjustable parameters, fits the entire range of operation

Anyway, an analytical solution can be derived for undoped devices. In fact, practical Multi-Gate MOS devices are usually undoped.

Core (1D) undoped DG MOSFET Model

- An analytical solution is possible in the case of undoped DG MOSFET or cylindrical Surrounding-Gate MOSFETs
- For undoped DG MOSFETs, Poisson's equation:

$$\frac{d^2\psi(x)}{dx^2} = \frac{d^2(\psi(x)-V)}{dx^2} = \frac{q}{\varepsilon_{Si}} \cdot n_i \cdot e^{\frac{q(\psi(x)-V)}{kT}}$$

- The resulting charge control model, after a few approximations, can be written as [Sallese'05]:

$$(V_{GS} - V_0 - V) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

Core (1D) Undoped DG MOSFET Model

- The drain current is obtained as:

$$I_{DS} = \frac{W\mu}{L}\int_0^{V_{DS}} Q(V)dV$$

- From the charge control model:

$$dV = -\frac{dQ}{2C_{ox}} - \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+2Q_0}\right)$$

- Where

$$Q_0 = 4\frac{kT}{q}C_{Si}$$

- Finally we get the expression:

$$I_{DS} = \frac{W\mu}{L}\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{4C_{ox}} + 8\left(\frac{kT}{q}\right)^2 C_{Si}\log\left[\frac{Q_d + 2Q_0}{Q_s + 2Q_0}\right]\right]$$

Core (1D) undoped Cylindrical GAA MOSFET Model

- In a well-behaved cylindrical GAA MOSFET, the electrostatic behaviour of the device is described by the 1D Poisson's equation in the radial direction.
- In an undoped cylindrical n-type SGT-MOSFET Poisson's equation takes the following form (in cylindrical coordinates):

$$\frac{d^2\psi}{dr^2}+\frac{1}{r}\frac{d\psi}{dr}=\frac{kT}{q}\delta\cdot e^{\frac{q(\psi-V)}{kT}}$$

- where $\delta = q^2 n_i / kT\varepsilon_{Si}$, ψ(r) the electrostatic potential and V the electron quasi-Fermi potential.
- Boundary conditions: $\frac{d\psi}{dr}(r=0)=0, \qquad \psi(r=R)=\psi_s$

Exact solution:

$$\psi(r)=V+\frac{kT}{q}\log\left(\frac{-8B}{\delta(1+Br^2)^2}\right)$$

B determined from boundary conditions

Core (1D) undoped Cylindrical GAA MOSFET Model

- From Gauss law:

$$C_{ox}(V_{GS} - \Delta\varphi - \psi_s) = Q = \varepsilon_{Si}\left.\frac{d\psi}{dr}\right|_{r=R} \qquad (4)$$

- Using $\left.\frac{d\psi}{dr}\right|_{r=R} = -\frac{kT}{q}\frac{4BR}{1+BR^2}$,the charge control model that is obtained is:

$$(V_{GS} - \Delta\varphi - V) - \frac{kT}{q}\log\left(\frac{8}{\delta R^2}\right) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

- where $Q_0 = \frac{4\varepsilon_{Si}}{R}\frac{kT}{q}$

(no approximations done)

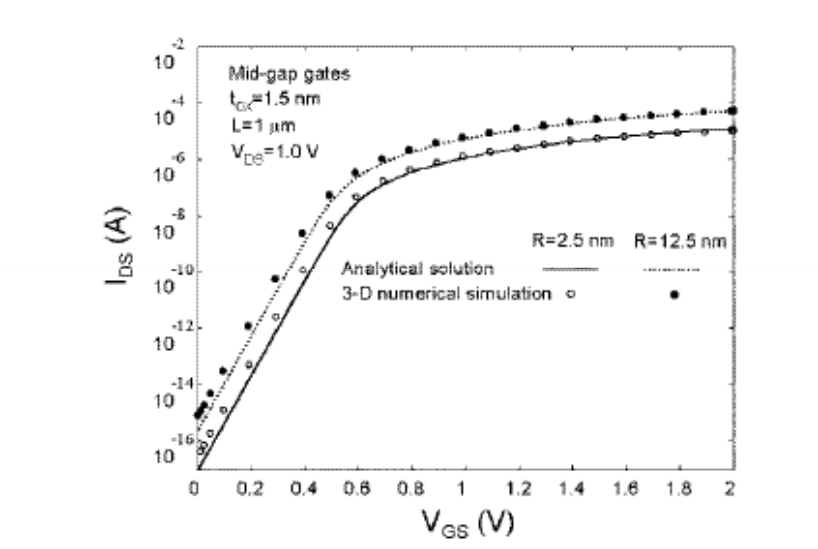
- The drain current is calculated from: $I_{DS} = \mu\frac{2\pi R}{L}\int_0^{V_{DS}} Q(V)dV$

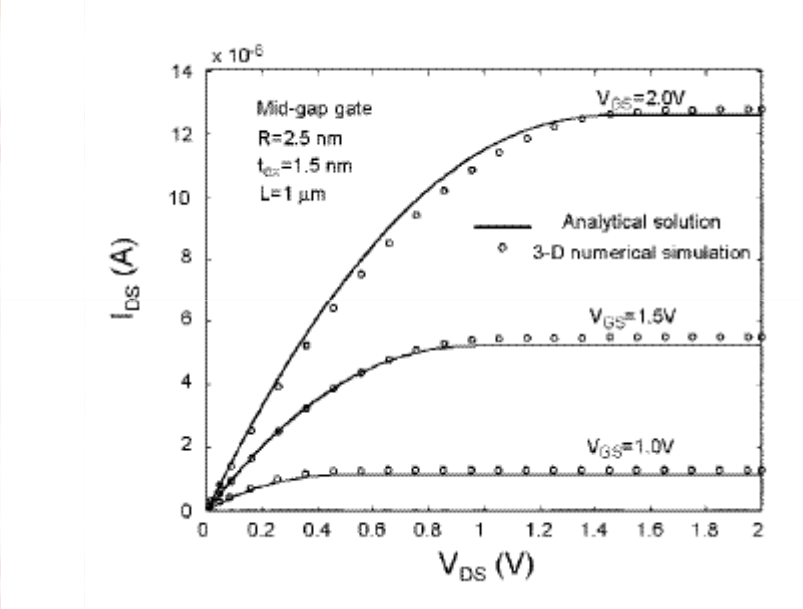
$$dV = -\frac{dQ}{C_{ox}} + \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+Q_0}\right)$$

- Using we obtain:

$$I_{ds} = \frac{2\pi R}{L}\mu\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + \frac{kT}{q}Q_0\log\left[\frac{Q_d + Q_0}{Q_s + Q_0}\right]\right]$$

1D models: Cylindrical GAA MOSFET

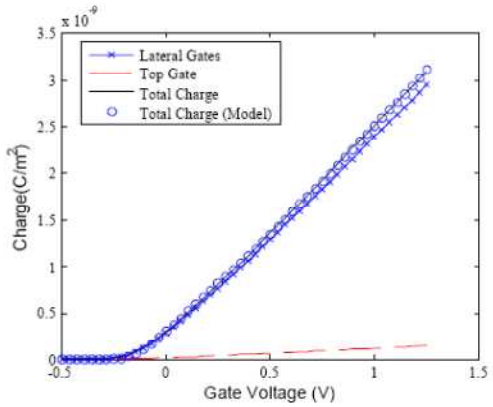




Output and transfer characteristics of cylindrical GAA MOSFETs obtained from the analyticalmodel (solid lines) compared with numerical simulations from DESSIS-ISE® (symbols).

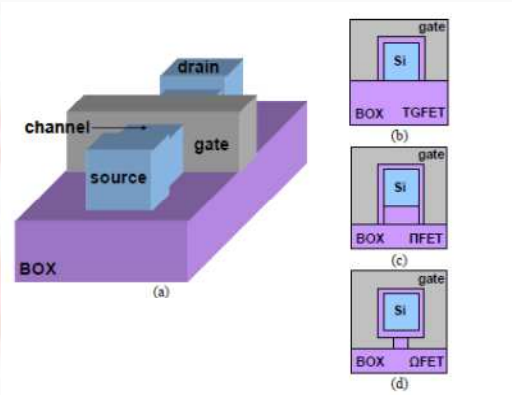
1D models: FinFET and Tri-Gate FET

In general, in symmetric Multi-Gate MOSFETs



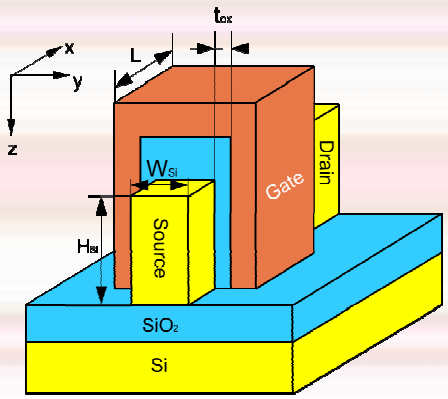
$$(V_{GS} - V_0 - V) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

Charge associated to top, lateral and total charge calculated with ATLAS 3-D simulations and with the unified charge control model (FinFET with W_{fin}=10 nm, H_{fin}=50 nm)



Anyway, a more physical and scalable model is needed, taking also into account the back-bias effects

FinFETs 1D compact modelling



FinFET scheme

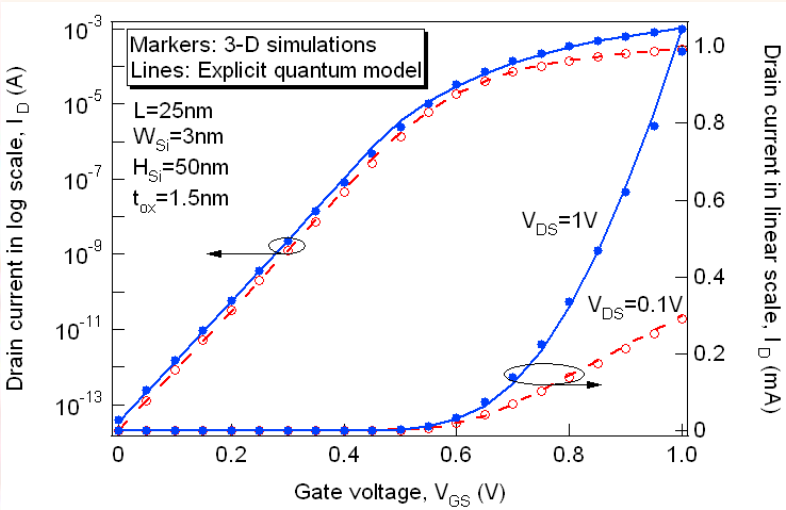
- Relationship between the charge density and the potentials [Sallese'05] [Tang'09] [Prégaldiny'06]:

$$v_g^* - v_{ch} - v_{to} = 4 \cdot q_g + \ln(q_g) + \ln\left[1 + \alpha \cdot q_g\right] \quad \text{with} \quad \alpha = \frac{C_{ox}}{C_{Si}}$$

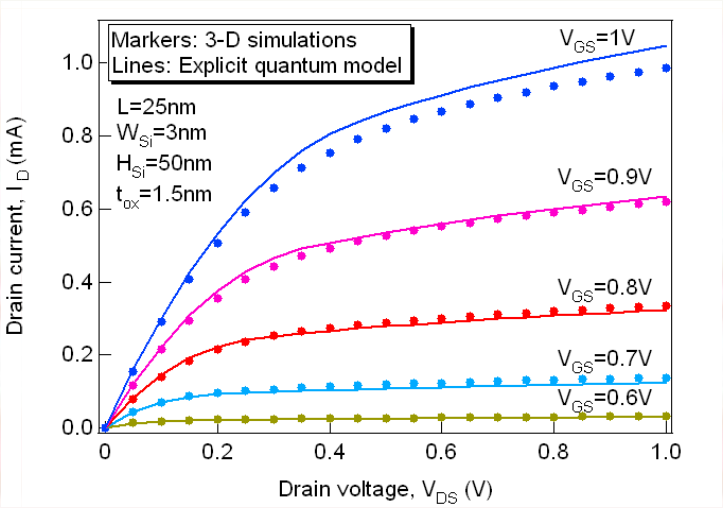
*This equation is solved by an explicit algorithm [Prégaldiny'06].

- Drain current expression:

$$i = -q_m^2 + 2 \cdot q_m + \frac{2}{\alpha} \cdot \ln\left(1 - \alpha \cdot \frac{q_m}{2}\right)\Bigg|_{q_{mS}}^{q_{mD}} \quad \text{with} \quad q_m = f\left(v_g^* - v_{to} - v_{ch}\right)$$



Comparison model/numerical simulations: drain current I_D vs. gate voltage V_G



Comparison model/numerical simulations: drain current I_D vs. drain voltage V_D

[Sallese'05] J. M. Sallese et al., *Solid State Electronics*, vol. 49, no. 3, pp. 485-489, 2005.
[Tang'09] M. Tang, F. Prégaldiny, C. Lallement and J.-M. Sallese, *IEEE TED*, vol. 56, no. 7, pp. 1543-1547, Jul. 2009.
[Prégaldiny'06] F. Prégaldiny et al., Int. J. Numer. Model: Elec. Network Dev. Fields, vol. 19, no. 3, pp. 239–256, May 2006.

Charge modeling

The total channel charge is obtained by integrating the mobile charge density over the channel length.

Capacitances are obtained by differentiating the total charges with respect to the applied voltages.

- In undoped DG MOSFETs: $$Q_{Tot} = -W\int_0^L Q dx = -W^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2 dV$$

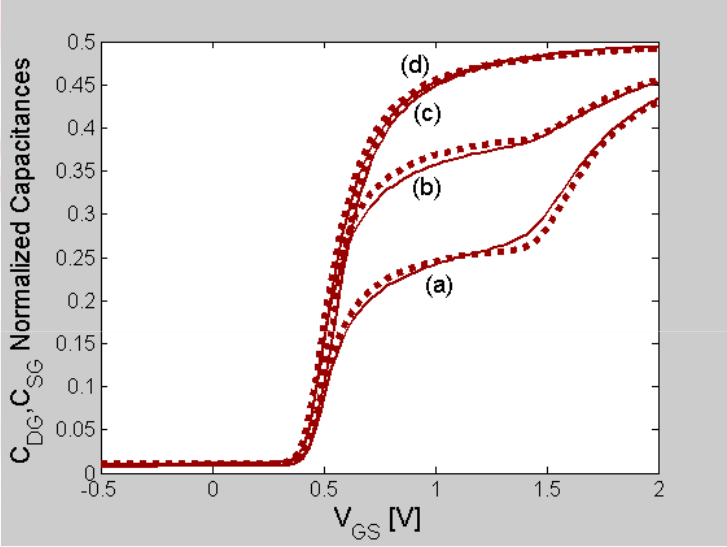
$$Q_{Tot} = -W^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{2C_{ox}} + \frac{kT}{q} Q + \frac{kT}{q} \frac{Q^2}{Q+2Q_0} \right) dQ$$

$$Q_{Tot} = -W^2 \frac{\mu}{I_{DS}} \left(\frac{Q^3}{6C_{ox}} + \frac{kT}{q} \frac{Q^2}{2} + 2\frac{kT}{q} \left(-Q_0 Q + \frac{Q^2}{4} + 2Q_0^2 \log[2Q_0 + Q] \right) \right) \Bigg|_{Q_s}^{Q_d}$$

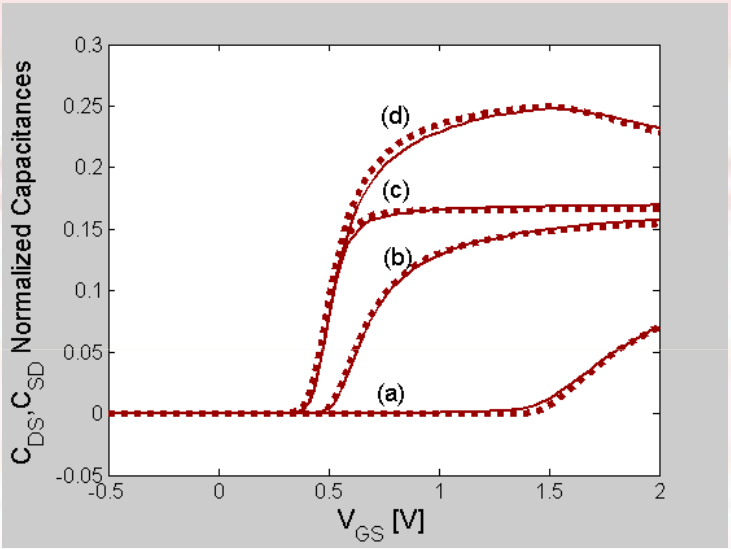
$$Q_D = -W\int_0^L \frac{x}{L} Q dx = -\frac{W^3\mu^2}{L(I_{DS})^2} \int_{Q_s}^{Q_d} Q^2 \left(\left(\frac{Q^2 - {Q_s}^2}{4C_{ox}} \right) + \frac{kT}{q} \left(2(Q - Q_s) - 2Q_0 \log\left[\frac{Q+2Q_0}{Q_s+2Q_0} \right] \right) \right) \cdot$$
$$\cdot \left(\frac{1}{2C_{ox}} + \frac{kT}{q} \left(\frac{1}{Q} + \frac{1}{Q+2Q_0} \right) \right) dQ$$

- The expressions for cylindrical undoped GAA MOSFETs have the same forms

Charge modelling: GAA MOSFETs

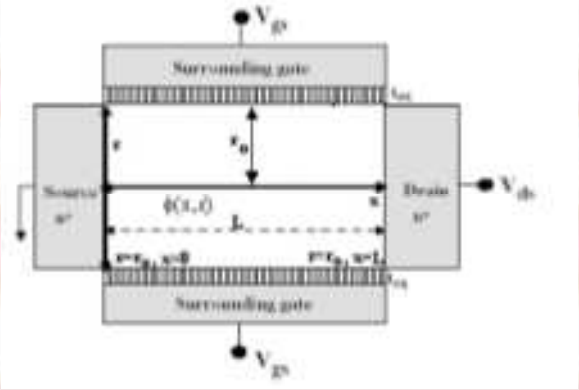


Normalized drain to gate capacitance (a, c) and source to gate capacitance (b, d) with respect to the gate voltage, for V_{DS}=1V (a, b) and V_{DS}=0.1V (c, d). Solid line: DESSIS-ISE simulations; Symbol line: analytical model



Normalized drain to source capacitance (c,d) and source to drain capacitance (a, b) with respect to the gate voltage, for V_{DS}=1V (a, d) and V_{DS}=0.1V (b, c). Solid line: DESSIS-ISE simulations; Symbol line: analytical model

GAA MOSFET, short channel effects



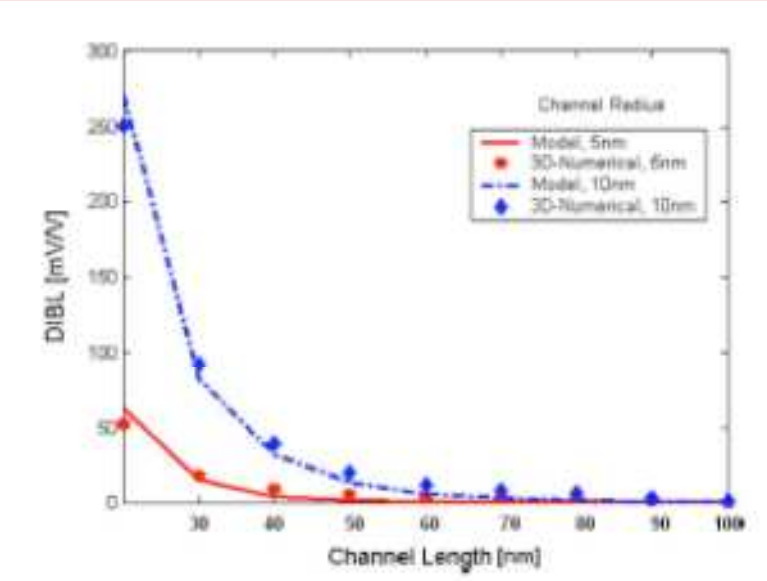
- Inclusion of SCEs [AbdElHamid'07]:

$$\varphi(x,y) = \varphi_1(y) + \varphi_2(x,y)$$

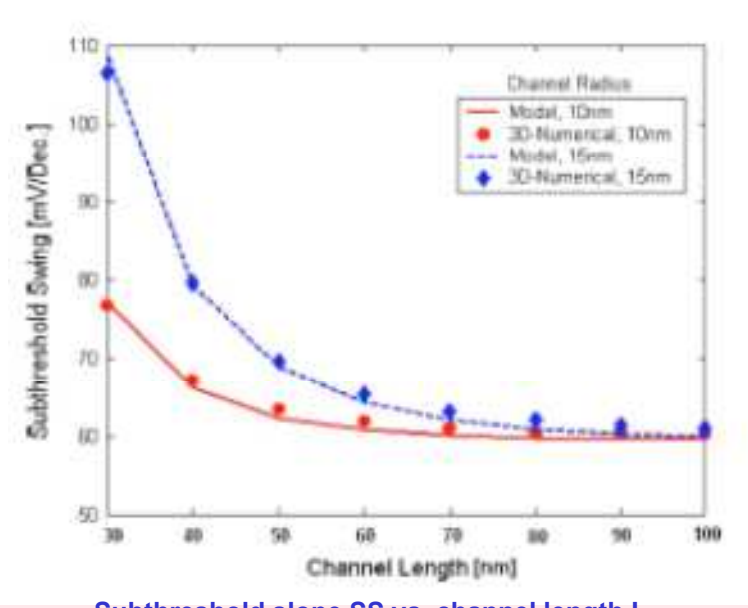
$\varphi_1(y)$ Solution of the 1D Poisson's equation

$\varphi_2(x,y)$ Solution of the remaining 2D equation

- Minimum of potential giving threshold voltage V_{TH} and subthreshold slope SS



DIBL vs. channel length L_G (radius = 5 and 10 nm). Comparison between model (lines) and numerical simulations (circles, diamonds)

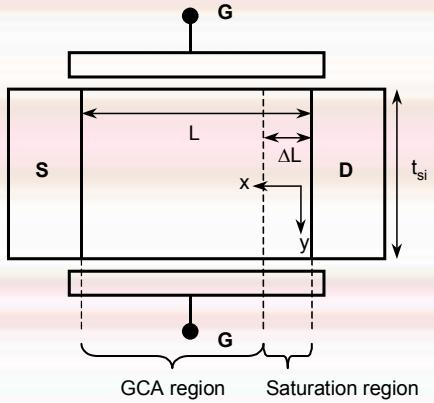


Subthreshold slope SS vs. channel length L_G (radius = 5 and 10 nm). Comparison between model (lines) and numerical simulations (circles, diamonds)

[AbdElHamid'07] H. Abd El Hamid et al., IEEE TED, vol. 54, no. 3, pp. 572-577, 2007.

Channel Length Modulation in Symmetrical Double-gate MOSFETs

- Transistor in saturation [Lime'08]



- Electrostatic potential derived from 2D Poisson's equation:

$$\varphi(x,y) = \varphi_1(y) + \varphi_2(x,y)$$

$\varphi_1(y)$ Solution of the 1D Poisson's equation

$\varphi_2(x,y)$ Solution of the remaining 2D equation

$$\phi(x,y) = a + b(x)y + c(x)y^n$$

$$\frac{\partial^2\varphi}{\partial x^2} - \frac{\varphi}{\lambda^2} = 0 \quad \text{with} \quad \lambda = \sqrt{\frac{\varepsilon_{si} t_{ox} t_{si}}{2\varepsilon_{ox}} + \frac{t_{si}^2}{8}\left(1 - \frac{2}{n(n+1)}\right)} = \frac{t_{si}}{2}\sqrt{\frac{1}{2} + \frac{1}{2r} - \frac{1}{n(n+1)}}$$

$$\varphi(x) = \varphi_{sat}\cosh\left(\frac{\Delta L + x}{\lambda}\right) + \frac{k\, v_{sat}}{\mu}\lambda\sinh\left(\frac{\Delta L + x}{\lambda}\right) \quad \text{with}$$

$$\varphi(x = -\Delta L) = \varphi(\phi_S = V_{deff} + \phi_b) = \varphi_{sat}$$

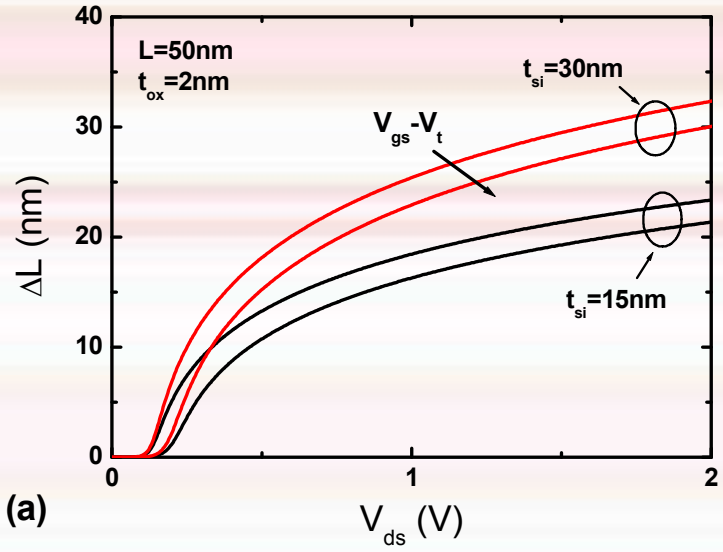
$$\left.\frac{d\varphi}{dx}\right|_{x=-\Delta L} = \frac{k\, v_{sat}}{\mu}$$

NMOS: k=2
PMOS: k=1

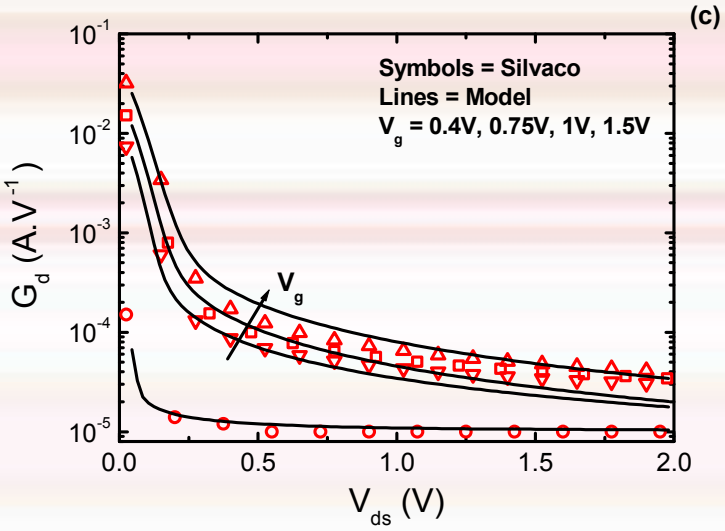
Determination of saturated length ΔL

[Lime'08] F. Lime et al., IEEE TED, vol. 55, no. 6, pp. 1441-1448, 2008.

Channel Length Modulation in Symmetrical Double-gate MOSFETs



Saturation region length ΔL vs. drain current V_{DS} . ($V_{GS} - V_{TH}$ = 0.25 and 0.5V; L = 50nm)



Output conductance G_D vs. drain current V_{DS} . V_{GS} = 0.4, 0.75, 1, and 1.5 V; t_{ox} = 2nm, t_{Si} = 15 nm and L = 50 nm.

Modeling of the saturation for Symmetrical Double-gate FETs

Design-Oriented DG MOSFET model - Calculation of $\phi d=\phi s-\phi o$ in all regions

1) Below threshold region $$\phi d_1 = \phi d_{BT} + 1.19\phi t \left[\frac{e^{\frac{V_G - V_T - V}{1.1\phi t}}}{1 + e^{\frac{V_G - V_T - V}{1.1\phi t}}} \right]$$

2) Above threshold region for $V \le V_M = 2, \quad \phi_M$ can be empirically expressed as:

$$\phi d_M = 0.197 - 0.047\, t_{ox} + 0.0045\, t_{ox}^2 + 0.00418\, t_s - 3\cdot 10^{-5}\, t_s^2;$$

For Na < Na_{max} $$\phi d_{2a} = \left(\frac{\phi d_{BT}}{3} + \phi d_M - 0.042\, V \right) - \left(\frac{\phi d_{BT}}{3} + \phi d_M - 0.042\, V - \phi d_T \right) \left(\frac{1 - \frac{V_G - V_T - V}{V_M - V_T - V}}{1 + 1.357 (V_G - V_T - V)} \right)$$

For Na > Na_{max} $$\phi d_{2b} = \left(\frac{\phi d_{BT}}{2} + \phi d_M - 0.042\, V \right) - \left(\frac{\phi d_{BT}}{2} + \phi d_M - 0.042\, V - \phi d_T \right) \left(\frac{1 - \frac{V_G - V_T - V}{V_M - V_T - V}}{1 + 0.5 (V_G - V_T - V)} \right)$$

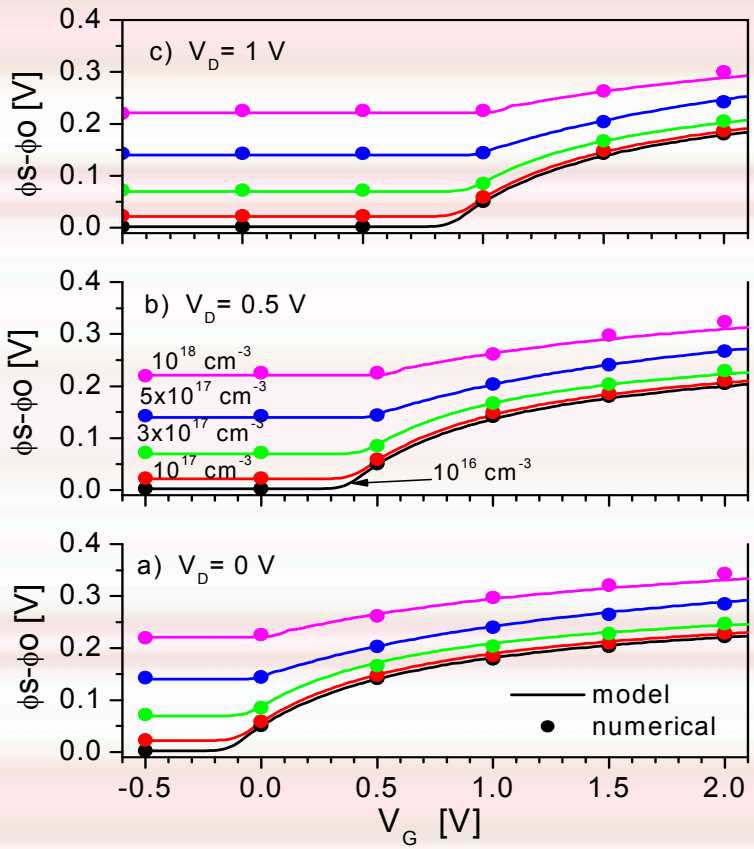
In all regions for above threshold conditions:

$$\phi d_2 = \frac{\phi d_{2a}}{2} \left[1 - \tanh\left[10 \left(\log(Na) - \log(Na_{\max}) - 0.5 \right) \right] \right] + \frac{\phi d_{2b}}{2} \left[1 + \tanh\left[10 \left(\log(Na) - \log(Na_{\max}) - 0.5 \right) \right] \right]$$

General expression for ϕd

$$\phi d = \frac{\phi d_1}{2} \left[1 - \tanh\left[30 (V_G - V_T - V) \right] \right] + \frac{\phi d_2}{2} \left[1 + \tanh\left[30 (V_G - V_T - V) \right] \right]$$

Design-Oriented DG MOSFET model - Calculation of $\phi d=\phi s-\phi o$ in all regions



Design-Oriented DG MOSFET model - Calculation of surface potentials

ϕs_{bt} approximation below threshold

$$\phi s_{bt} = V_G - V_{FB} - \phi t \frac{q_b}{2} - \phi t \cdot LambW\left[\frac{q_b}{4} e^{\frac{V_G - V_{FB} - 2\phi_F - \phi t \frac{q_b}{2}}{\phi t}}\right]$$

ϕs_{at} approximation above threshold

$$\phi s_{at} = V_G - V_{FB} - 2\phi t \cdot LambW\left[\frac{1}{2}\sqrt{\frac{q_b}{2}\frac{1}{\gamma}}\sqrt{1 - e^{-\alpha}}\, e^{\frac{V_G - V_{FB} - 2\phi_F - V}{2\phi t}}\right]$$

Surface potential

$$\phi s = \frac{\phi s_{bt}}{2}\left[1 - \tanh\left[20 \cdot (V_G - V_T)\right]\right] + \frac{\phi s_{at}}{2}\left[1 + \tanh\left[20 \cdot (V_G - V_T)\right]\right]$$

Design-Oriented DG MOSFET Model: Charge Control Model

The general expression for the **Charge Control Model** is obtained:

$$V_G - V_{FB} - 2\phi_F - V - \phi t\,\frac{q_b}{2} + \phi t \ln\left(\frac{1-e^{-\alpha}}{\alpha}\right) = \phi t\, q_n + \phi t \ln\left[\frac{\alpha_{BT}}{\alpha}\left(\frac{4q_n}{q_b}\cdot\left(1+\frac{q_n}{q_b}\right)+1\right)-1\right]$$

$$\frac{\alpha_{BT}}{\alpha}\left(\frac{4q_n}{q_b}\cdot\left(1+\frac{q_n}{q_b}\right)+1\right) >> 1$$

Approximation valid for Na from 10^{14} to $3\text{x}10^{18}$ cm^{-3}

The derivative with respect to *V* is equal to:

$$-1+\frac{d}{dV}\left[\phi t \ln\left(\frac{1-e^{-\alpha}}{\alpha}\right)\right] = \phi t\left[1+\frac{1}{q_n}+\frac{1}{q_n+q_b}\right]\frac{dq_n}{dV} + \phi t\,\frac{d}{dV}\left[\ln\left(4\,\frac{\alpha_{BT}}{\alpha}\right)\right]$$

After neglecting the *ln* terms

$$dV = -\phi t\left[1+\frac{1}{q_n}+\frac{1}{q_n+q_b}\right]\cdot dq_n \qquad dV_G = \phi t\left[1+\frac{1}{q_n}+\frac{1}{q_n+q_b}\right]\cdot dq_n$$

Design-Oriented Doped DG MOSFET ModelCharge Control Model - Drain current

Total drain current considering both surfaces

$$I_{DS} = 2\frac{W}{L}\mu C_{ox}\phi t\int_{V_S}^{V_D} q_n(V)\,dV$$

Long channel and μ = const

Using the relation between V and q_n the following expression for total current is obtained:

$$I_{DS} = I_0\left[\frac{q_{ns}^2 - q_{nd}^2}{2} + 2(q_{ns} - q_{nd}) - q_b \ln\left(\frac{q_{ns} + q_b}{q_{nd} + q_b}\right)\right]$$

Where I_0 is equal to:

$$I_0 = 2\frac{W}{L}\mu_0\, C_{ox}\phi t^2$$

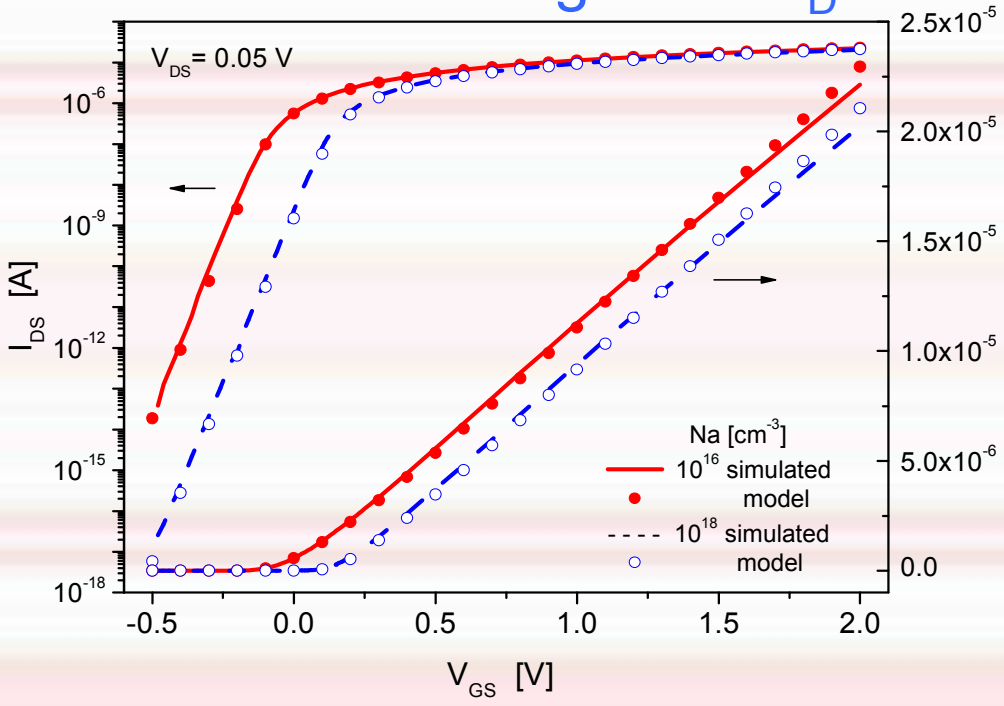
Current model validation

L= 5 μm

μ= 400 cm^2/Vs

Comparison of modeled and simulated transfer characteristics

Lineal region at V_D= 50 mV



Design-Oriented Doped DG MOSFET Model with variable mobility and short channel effects

INTRODUCTION OF SHORT-CHANNEL EFFETS (SCE) IN THE CORE MODEL

- Variable mobility considering transversal and longitudinal electric fields
- Short channel effects (SCE) taken into acount:
  - V_T variation with channel length reduction and DIBL;
  - Velocity saturation effects;
  - Series resistance;
  - Channel shortening;
  - Subthreshold slope degradation

Doped DG MOSFET Model: Short Channel Effects – Drain current

Effect of series resistance *R* as function of the external voltages.

$$I_D \propto \frac{1}{1+\left[2\frac{W}{L}C_{ox}\mu_{eff}\cdot R\cdot\left|V_{GT}-\beta\cdot V_{Def}\right|\right]\cdot\frac{1}{2}\left[1+\tanh\left(60\cdot V_{GT}\right)\right]}$$

$$I_D = \frac{\left(2\frac{W}{L}C_{ox}\phi t^2\mu_{eff}\right)}{\left(1-\frac{\Delta L}{L}\right)}\frac{\left[\frac{1}{2}\left(q_{ns}^2-q_{nd}^2\right)+\left[2\left(q_{ns}-q_{nd}\right)-q_b\ln\left(\frac{q_{ns}+q_b}{q_{nd}+q_b}\right)\right]^n\right]}{1+\left[2\frac{W}{L}C_{ox}\mu_{eff}\cdot R\cdot\left|V_{GT}-\beta\cdot V_{Def}\right|\right]\cdot\frac{1}{2}\left[1+\tanh\left(60\cdot V_{GT}\right)\right]}$$

$$q_{ns} = q_n(V_G+\Delta V_T, V=0) \qquad q_{nd} = q_n(V_G+\Delta V_T, V=V_{efs})$$

Doped DG MOSFET Model: Short Channel Effects – Drain current

Effect of series resistance *R* as function of the external voltages.

$$I_D \propto \frac{1}{1+\left[2\frac{W}{L}C_{ox}\mu_{eff}\cdot R\cdot\left|V_{GT}-\beta\cdot V_{Def}\right|\right]\cdot\frac{1}{2}\left[1+\tanh\left(60\cdot V_{GT}\right)\right]}$$

$$I_D = \frac{\left(2\frac{W}{L}C_{ox}\phi t^2\mu_{eff}\right)}{\left(1-\frac{\Delta L}{L}\right)}\frac{\left[\frac{1}{2}\left(q_{ns}^2-q_{nd}^2\right)+\left[2\left(q_{ns}-q_{nd}\right)-q_b\ln\left(\frac{q_{ns}+q_b}{q_{nd}+q_b}\right)\right]^n\right]}{1+\left[2\frac{W}{L}C_{ox}\mu_{eff}\cdot R\cdot\left|V_{GT}-\beta\cdot V_{Def}\right|\right]\cdot\frac{1}{2}\left[1+\tanh\left(60\cdot V_{GT}\right)\right]}$$

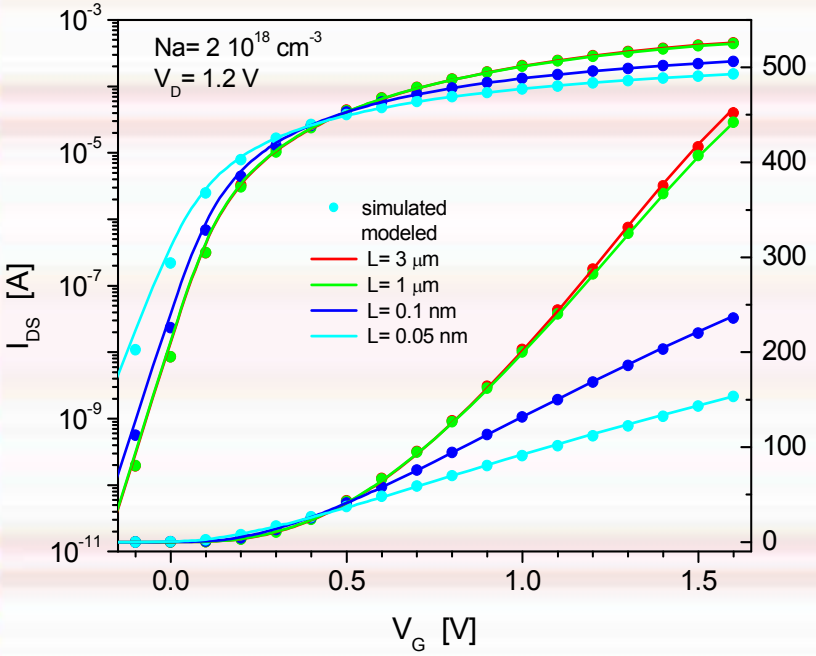
$$q_{ns} = q_n(V_G+\Delta V_T, V=0) \qquad q_{nd} = q_n(V_G+\Delta V_T, V=V_{efs})$$

ΔV_T includes threshold voltage roll-off and DIBL

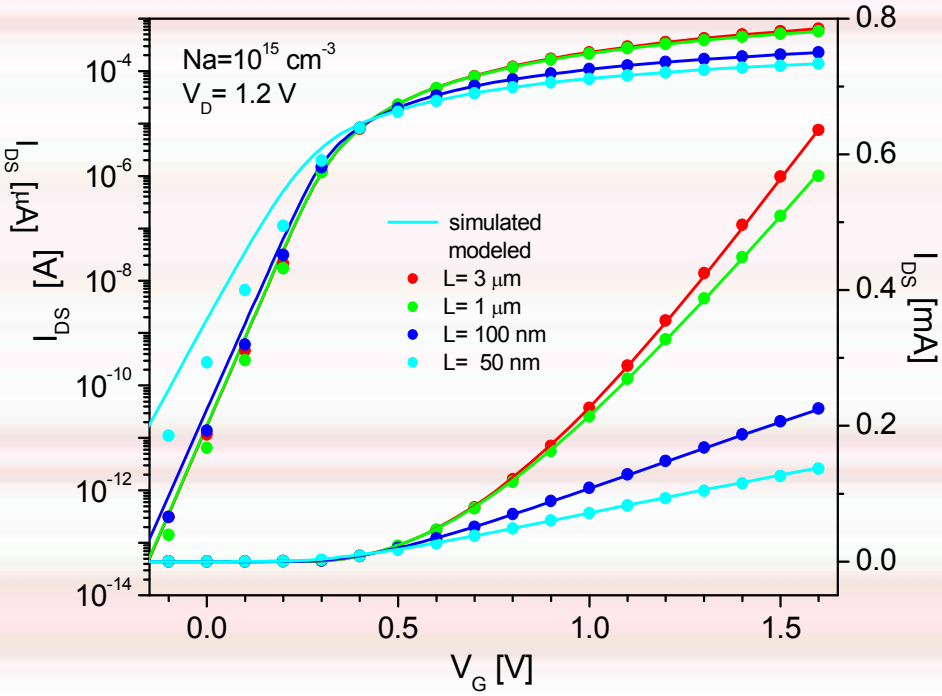
Doped DG MOSFET Model: Short channel model validation:

Simulated and modeled transfer characteristics at V_D= 1.2 V

HD



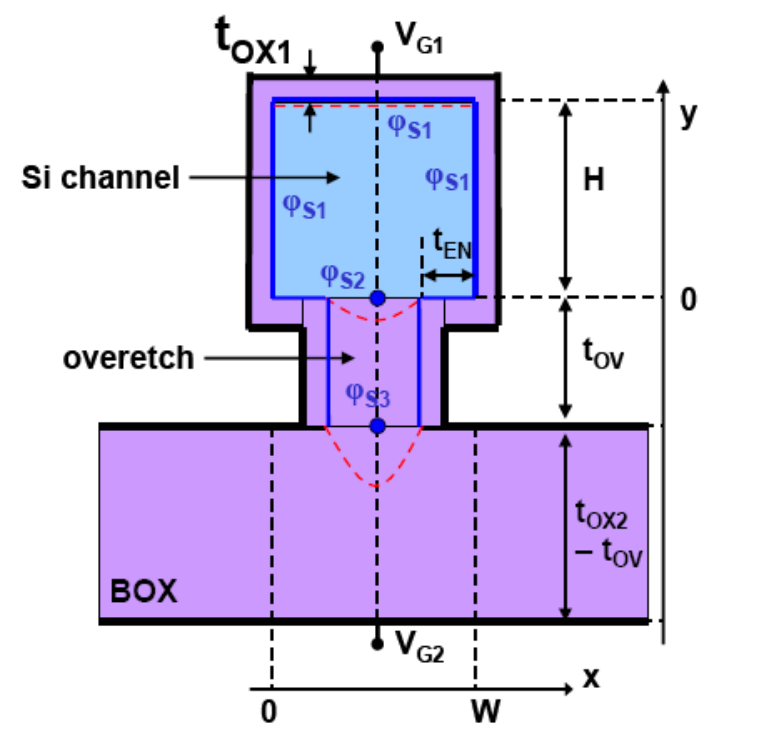
LD



Outline

1. Introduction
2. 1D core and Design-Oriented compact models
3. Hyperbolic function series based compact models
4. Conformal mapping based compact models
5. Conclusions

Tri-Gate MOSFET Modeling Assumptions



Transversal cross-section of an ΩFET transistor, with the notations used in this work.

- Undoped channels (mandatory for TG/Pi/Omega-gate FETs due to process considerations)
- 'Well-behaved' devices
- No corner effects (undoped channels)
- Constant surface potential (φ_{S1})
- Parabolic approximation at the body/overetched BOX boundary and at the overetched BOX/BOX boundary
- No quantum effects (W and H > 10 nm)
- Negligible carrier's concentrations up to threshold

✓ Simplified boundary conditions
✓ Electrostatics described by the Laplace equation ($\Delta\varphi \approx 0$)

Obtaining the potential (1)…

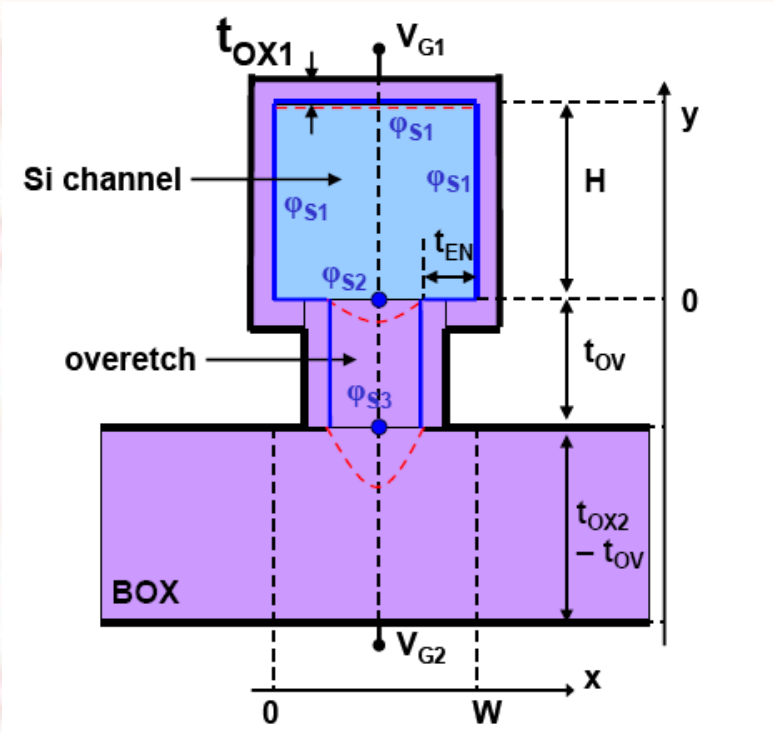
Solution: development in Fourier's series with the coefficient calculated with respect to the boundary conditions (here, surface potentials $\varphi_{S1,2,3}$):

✓ In the channel:

$$\psi_{Si}(x,y) = \varphi_{S1} + (\varphi_{S2} - \varphi_{S1}) \sum_{n=1}^{+\infty} \frac{F_n}{W} \frac{sh(\frac{n\pi(H-y)}{W})}{sh(\frac{n\pi H}{W})} \sin(\frac{n\pi x}{W})$$

✓ In the overetched region:

$$\psi_{OV}(x,y) = \varphi_{S1} + \left[P_n \sin(\frac{n\pi x}{W_2}) \sum_{n=1}^{+\infty} \frac{(\varphi_{S2} - \varphi_{S1}) sh(\frac{n\pi y}{W_2}) + (\varphi_{S3} - \varphi_{S1}) sh(\frac{n\pi(t_{OV} - y)}{W_2})}{sh(\frac{n\pi t_{OV}}{W_2})} \right]$$



Transversal cross-section of a ΩFET transistor, with the notations used in this work.

with: $W_2 = W - 2t_{EN}$ the overetched region width.

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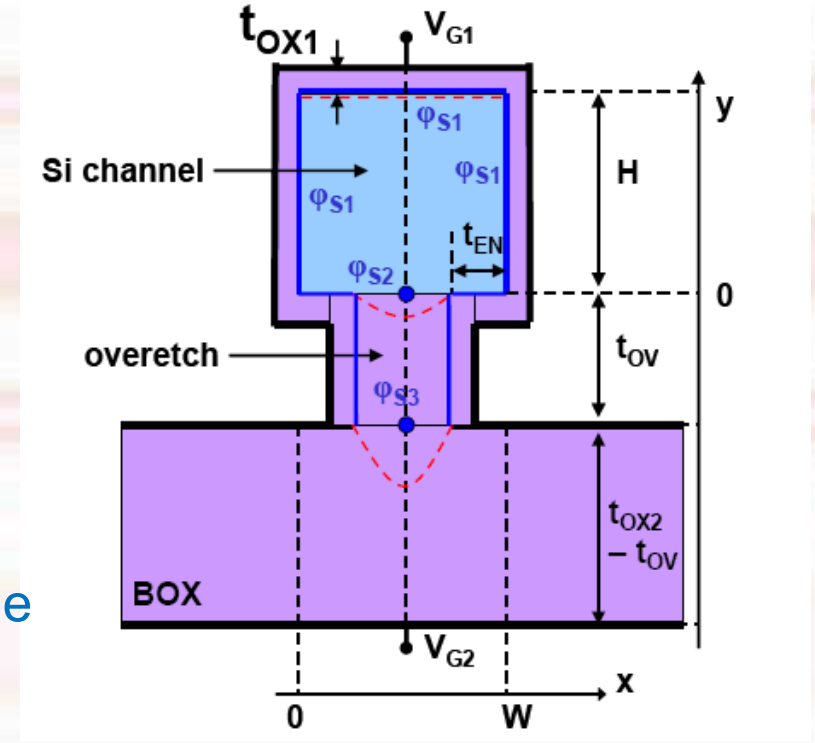
Obtaining the potential (2)…

with: $$P_n = \frac{2(1-\cos(n\pi)) - n\pi\sin(n\pi)}{(\frac{n\pi}{2})^3}$$

Coefficients coming from the **parabolic** approximation

Coefficients coming from the **Ω-shape** approximation

and:



Transversal cross-section of a ΩFET transistor, with the notations used in this work.

$$F_n = \frac{W\left[\begin{array}{l}(2t_{EN}n\pi\sin(n\pi) - n\pi W\sin(n\pi) - 2W\cos(n\pi) + 2W)\cos(\frac{n\pi t_{EN}}{W}) + \\ (-2t_{EN}n\pi\cos(n\pi) + n\pi W\cos(n\pi) + 2t_{EN}n\pi - n\pi W))\sin(\frac{n\pi t_{EN}}{W})\end{array}\right]}{(\frac{n\pi}{2})^3(W - 2t_{EN})}$$

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Obtaining the potential (3) …

➢ link between the surface potential $\varphi_{S1,2,3}$ and the front/back-gate biases $V_{G1,2}$: Gauss' theorem at mid-channel and at the interfaces:

- $V_{G1} = V_{FB1} + \varphi_{S1} + \Delta V$

$$V_{G1} = V_{FB1} + \varphi_{S1} + \frac{\varepsilon_{Si}}{C_{OX1}} E\left(\frac{W}{2}, H\right)$$

$$V_{G1} = V_{FB1} + \varphi_{S1}(1 + B) - \varphi_{S2} B$$

$$B(W,H) = \frac{C_{LAT}}{C_{OX1}} \sum_{n=1}^{+\infty} \frac{n\pi F_n}{sh\left(\frac{n\pi H}{W}\right)} \sin\left(\frac{n\pi}{2}\right) \qquad \text{with:} \quad C_{LAT} = \frac{\varepsilon_{Si}}{W}$$

- $V_{G2} = V_{FB2} + \varphi_{S3} + C(\varphi_{S2} - \varphi_{S1}) + D(\varphi_{S1} - \varphi_{S3})$

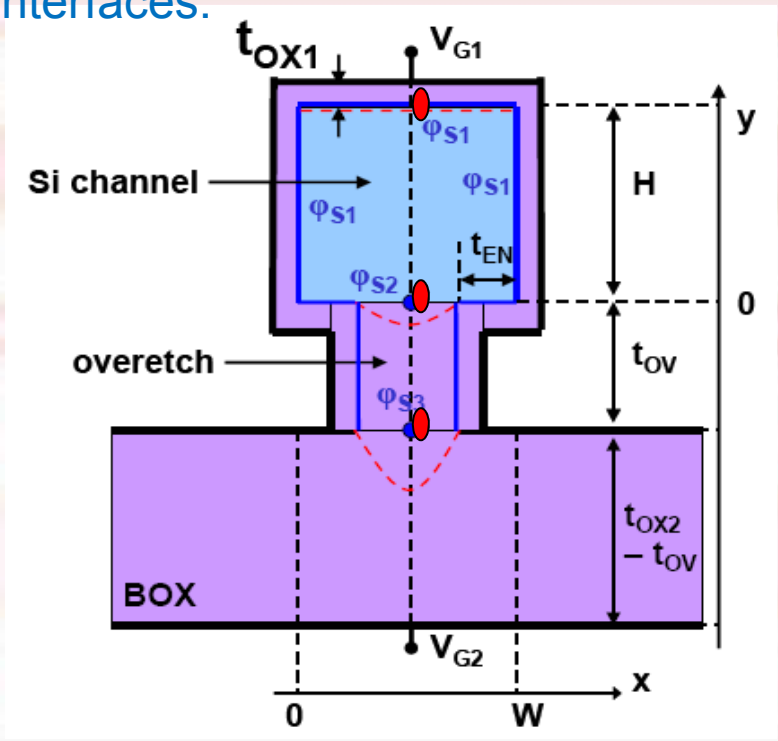
$$C(W,H) = \frac{C_{LAT}^{BOX}}{C'_{OX2}} \sum_{n=1}^{+\infty} \frac{n\pi P_n}{sh\left(\frac{n\pi t_{OV}}{W_2}\right)} \sin\left(\frac{n\pi}{2}\right) \quad D(W,H) = \frac{C_{LAT}^{BOX}}{C'_{OX2}} \sum_{n=1}^{+\infty} \frac{n\pi P_n}{th\left(\frac{n\pi t_{OV}}{W_2}\right)} \sin\left(\frac{n\pi}{2}\right)$$

with: $C_{LAT}^{BOX} = \frac{\varepsilon_{OX2}}{W_2}$ and: $C'_{OX2} = \frac{\varepsilon_{OX2}}{t_{OX2} - t_{OV}}$

- $E.(\varphi_{S2} - \varphi_{S1}) = G.(\varphi_{S1} - \varphi_{S2}) + F.(\varphi_{S3} - \varphi_{S1})$

$$E(W,H) = C_{LAT} \sum_{n=1}^{+\infty} \frac{n\pi F_n}{sh\left(\frac{n\pi H}{W}\right)} \sin\left(\frac{n\pi}{2}\right)$$

$$F(W,H) = C_{LAT}^{BOX} \sum_{n=1}^{+\infty} \frac{n\pi P_n}{sh\left(\frac{n\pi t_{OV}}{W_2}\right)} \sin\left(\frac{n\pi}{2}\right) \quad G(W,H) = C_{LAT}^{BOX} \sum_{n=1}^{+\infty} \frac{n\pi P_n}{th\left(\frac{n\pi t_{OV}}{W_2}\right)} \sin\left(\frac{n\pi}{2}\right)$$



Transversal cross-section of a ΩFET transistor, with the notations used in this work.

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Obtaining the front-gate threshold voltage

- Finally, obtention of the two master equations:

$$\begin{cases} V_{G1} = V_{FB1} + \varphi_{S1}(1+B) - \varphi_{S2}B \\ V_{G2} = V_{FB2} + \varphi_{S1}(C - D - (\frac{1+D}{F})(E+G-F)) + \varphi_{S2}((\frac{1+D}{F})(E+G) - C) \end{cases}$$

- Spliting the back-interface regimes (accumulation, depletion, and inversion)

[Lim'83][Akarvardar'07]:

$$a)\,back-gate\,accumulated\,(V_{G2} < V_{G2,ACC2} = V_{FB2} + (C - D - (\frac{1+D}{F})(E+G-F)\varphi_{ST}))$$

$$V_{TH1,ACC2} = V_{FB1} + (1+B)\varphi_{ST}$$

$$b)\,back-gate\,inverted\,(V_{G2} > V_{G2,INV2} = V_{FB2} + \varphi_{ST}):$$

$$V_{TH1,INV2} = V_{FB1} + \varphi_{ST}$$

$$c)\,back-gate\,depleted\,(V_{G2,ACC2} < V_{G2} < V_{G2,INV2}):$$

$$V_{TH1,DEP2} = V_{FB1} - (\frac{B}{1+\frac{1+D}{F}(E+G-F)-C+D})(V_{G2} - V_{FB2}) + (1+\frac{B}{1+\frac{1+D}{F}(E+G-F)-C+D})\varphi_{ST}$$

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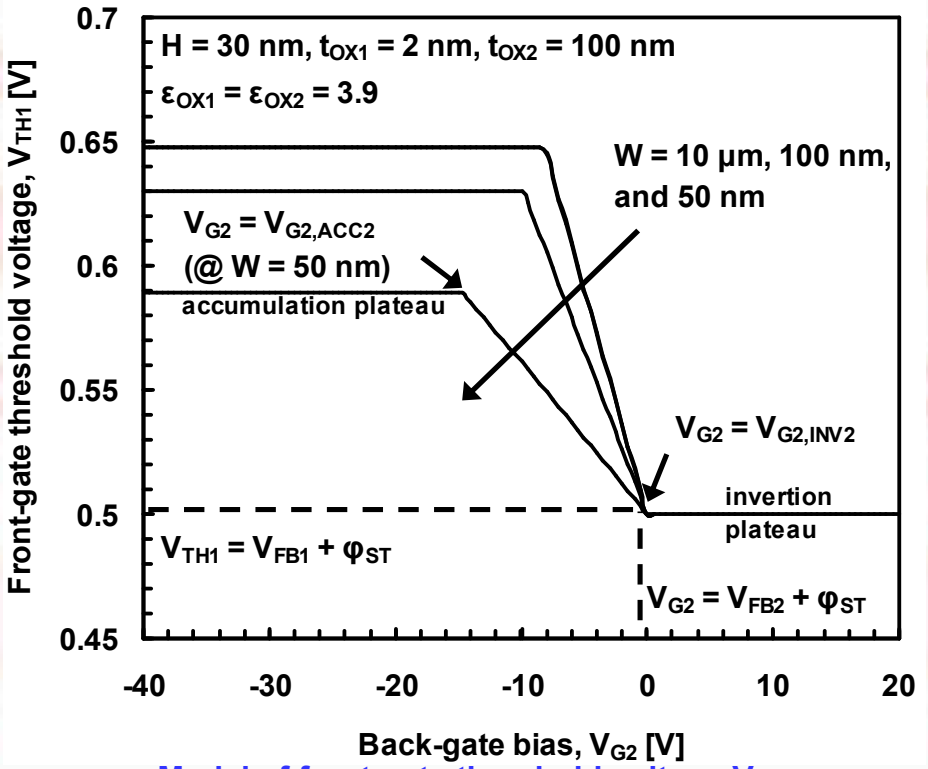
Front-gate threshold voltage…



Model of front-gate threshold voltage V_{TH1} vs. back-gate bias V_{G2} for Triple-gate FETs

- Plateaus when the back-interface is accumulated/inverted, linear decrease when the back-interface is depleted.
- Narrow devices: larger 'depleted back-interface' region and smaller amplitude of threshold voltage.

Obtaining the back-gate threshold voltage

- With the two master equations:

$$\begin{cases} V_{G1} = V_{FB1} + \varphi_{S1}(1+B) - \varphi_{S2}B \\ V_{G2} = V_{FB2} + \varphi_{S1}(C - D - (\frac{1+D}{F})(E+G-F)) + \varphi_{S2}((\frac{1+D}{F})(E+G) - C) \end{cases}$$

- Similarly, it yields:

a) front – gate accumulated $(V_{G1} < V_{G1,ACC1} = V_{FB1} - B\varphi_{ST})$

$$V_{TH2,ACC1} = V_{FB2} + ((1+D)(\frac{E+G}{F}) - C)\varphi_{ST}$$

b) front – gate inverted $(V_{G1} > V_{G1,INV1} = V_{FB1} + \varphi_{ST})$:

$$V_{TH2,INV1} = V_{FB2} + \varphi_{ST}$$

c) front – gate depleted $(V_{G1,ACC1} < V_{G1} < V_{G1,INV1})$:

$$V_{TH2,DEP1} = V_{FB1} - (\frac{(1+D)(\frac{E+G}{F}) - C - 1}{1+B})(V_{G1} - V_{FB1}) + (1 + \frac{(1+D)(\frac{E+G}{F} - C - 1)}{1+B})\varphi_{ST}$$

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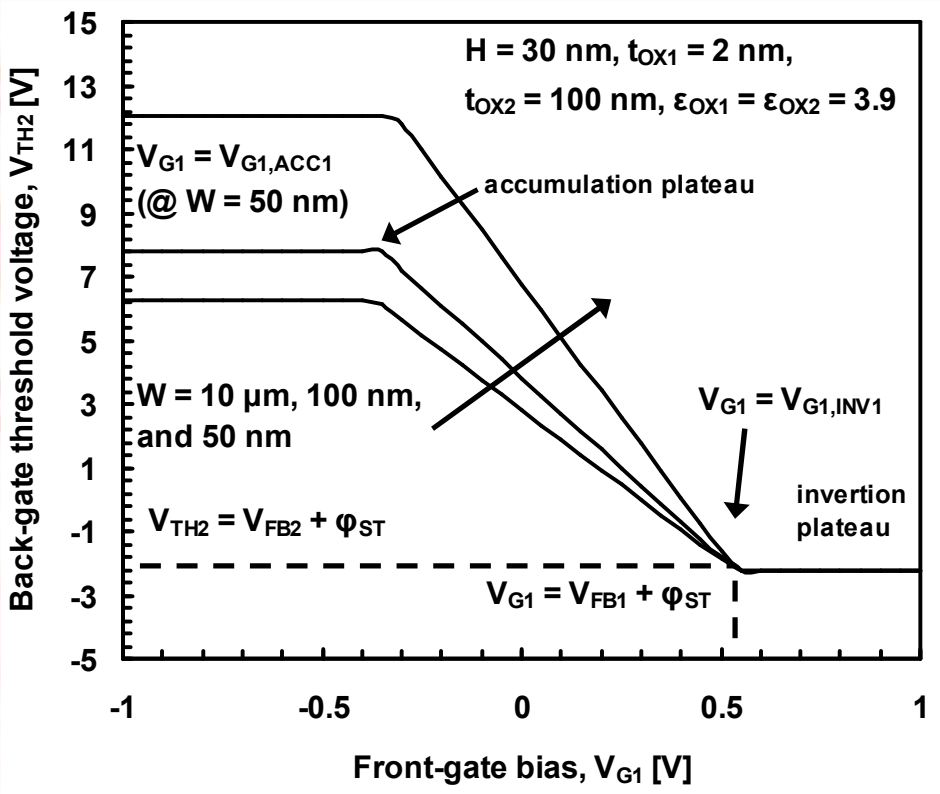
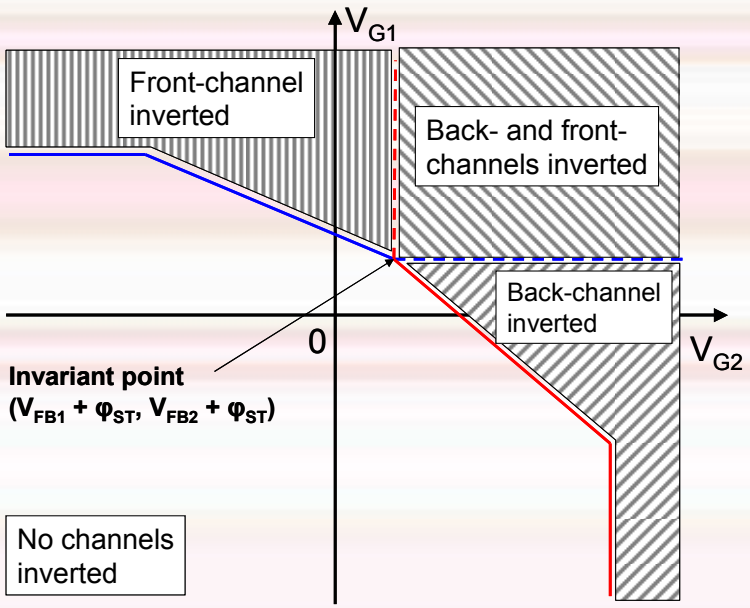
Back-gate threshold voltage…



Model of back-gate threshold voltage V_{TH2} vs. front-gate bias V_{G1} for Triple-gate FETs

- Plateaus when the back-interface is accumulated/inverted, linear decrease when the back-interface in depleted.
- Narrow devices: SMALLER ‘depleted back-interface’ region and LARGER amplitude of threshold voltage.

Total threshold voltage…



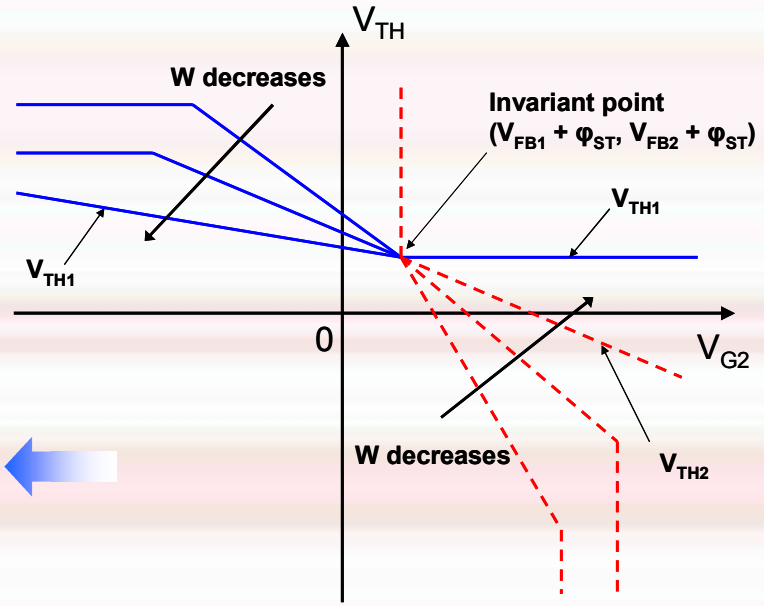
Activation of the front- and back- channels vs. front and back-gate biases (V_{G1}, V_{G2}).

➢ In the situation of a fixed back-gate bias V_{G2} and of a front-gate bias V_{G1} sweep.

Calculation of the total threshold voltage 'as seen during normal operation'.

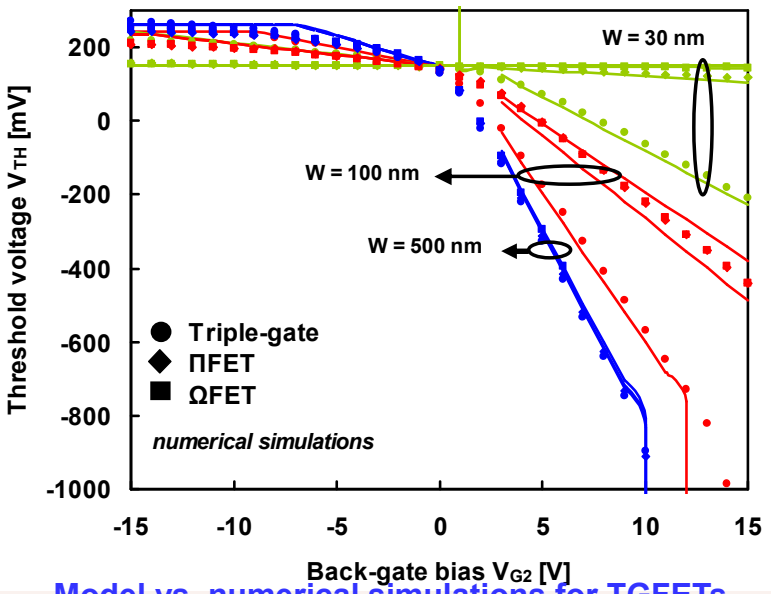
➢ Using the previously calculated front- and back-channel threshold voltage:

Calculation of the 4 zones corresponding to the channels respective activations.



Total threshold voltage V_{TH} (front-gate V_{TH1}, back-gate V_{TH2}) vs. back-gate bias V_{G2}.

Validation – Numerical Simulations

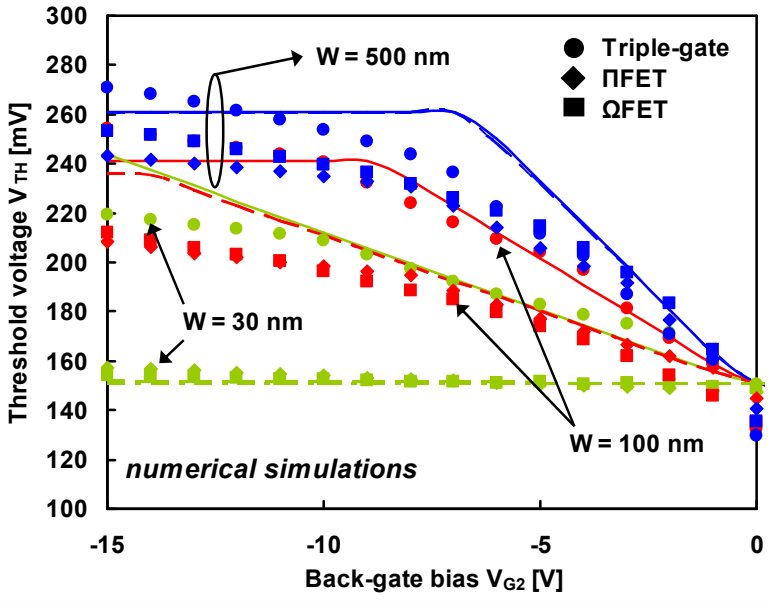


Model vs. numerical simulations for TGFETs, Pi-gateFETs, ΩFETs, and for channel width W=30, 100, and 500 nm.

- Good agreement model/simulations for TGFETs, Pi-gate FETs, and ΩFETs.
- Pi-gate FET threshold voltage less sensitive to back-gate bias than TGFET.
- ΩFET threshold voltage less sensitive to back-gate bias than Pi-gate FETs.
- Narrow devices threshold voltage less sensitive to back-gate bias than wide devices.

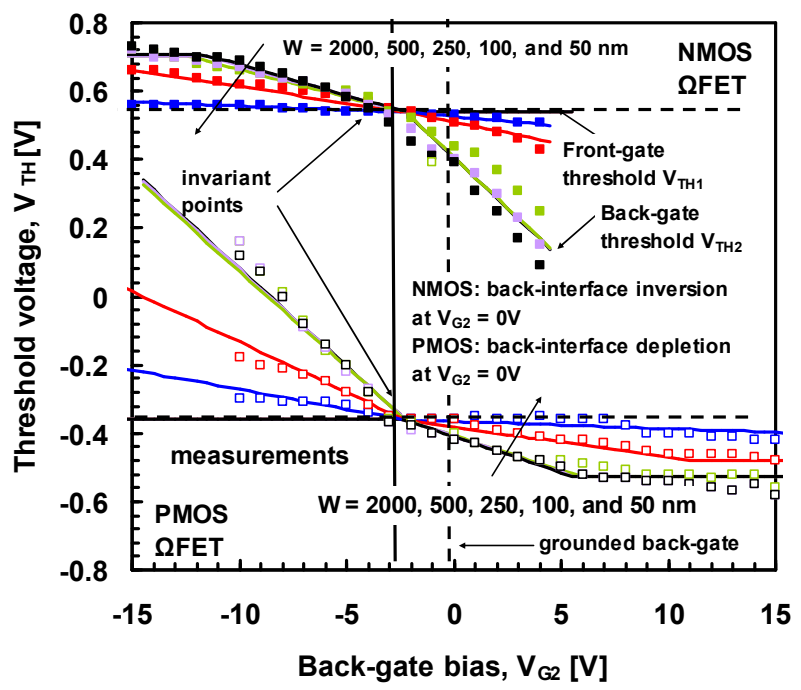
- Zoom of the previous figure in the back-interface accumulation/depletion zones:

Acceptable agreement and correct modelling of the 'front- to back-interfaces coupling' coefficients



Model vs. numerical simulations for TGFETs, Pi-gateFETs, ΩFETs, and for channel width W=30, 100, and 500 nm.

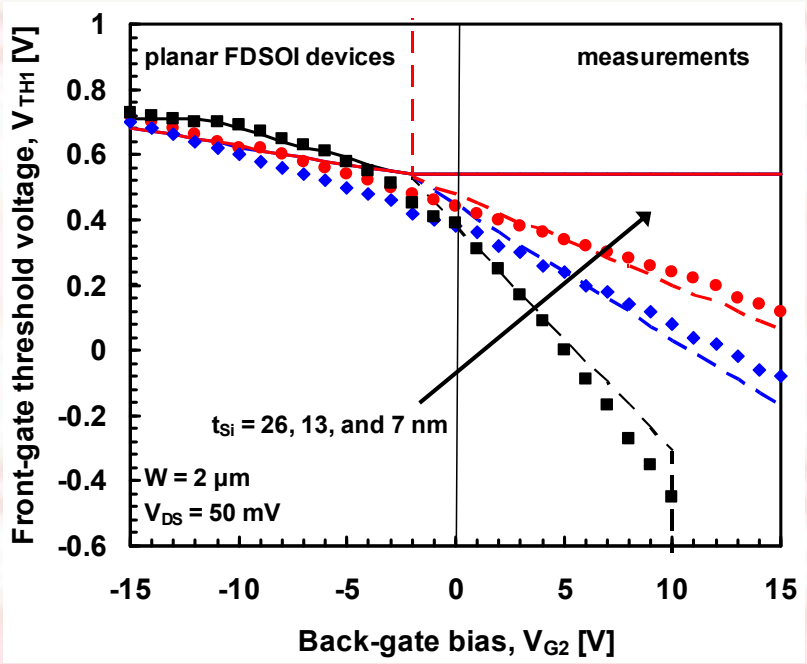
Validation – Experimental meas.



Model vs. measurements for ΩFETs, and for channel width W from 2 µm down to 50 nm.

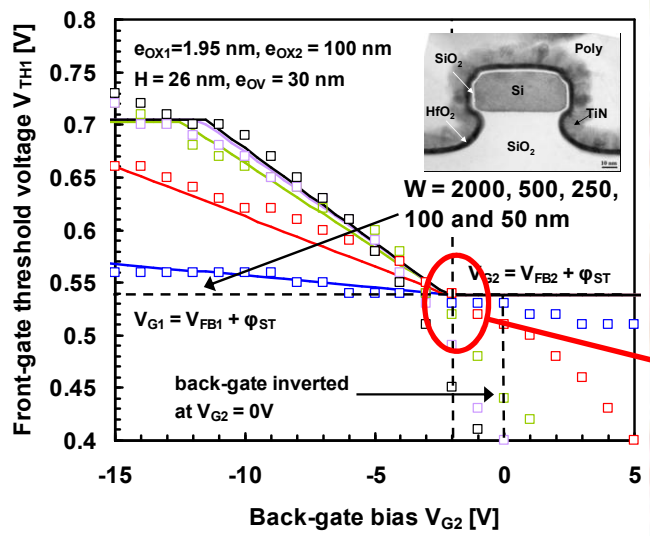
- Good agreement model/measurements for experimental wide devices (ΩFETs in the planar FDSOI configuration) for different channel thicknesses (26, 13, and 7 nm).

- Good agreement model/measurements for experimental ΩFETs (H = 26 nm, W from 2 µm down to 50 nm).
- Good modelling for both NMOS and PMOS devices.



Model vs. measurements for wide ΩFETs (W = 2 µm), and for channel thicknesses (t_{Si} or H) of 26, 13, and 7 nm.

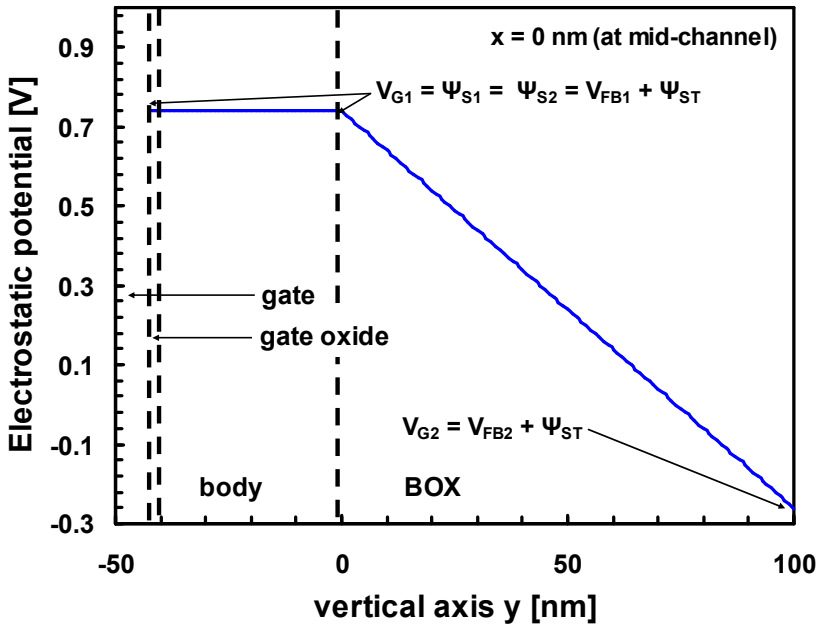
Invariant point



➢ Invariant point predicted by the model experimentally observed

➢ Invariant point occuring for $V_{G1} = V_{FB1} + \varphi_{ST}$ and $V_{G2} = V_{FB2} + \varphi_{ST}$

Invariant point



Model of the potential at mid-channel (x=W/2) for $V_{G2} = V_{FB2} + \varphi_{ST}$ and $V_{G1}=V_{TH1}=V_{FB1}+\varphi_{ST}$

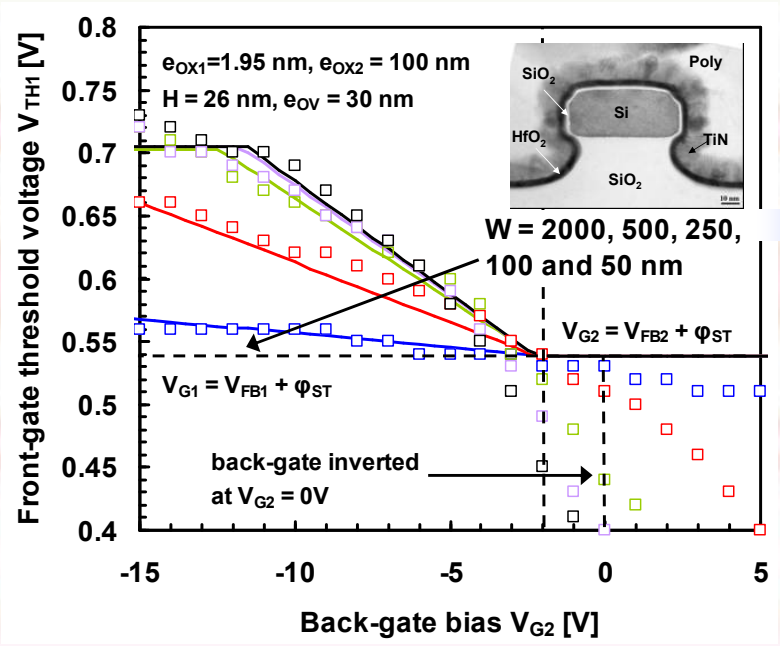
➢ Compensation of the back-gate induced potential drop

➢ Flat potential in the channel

➢ Potential insensitive to channel width and height W and H

Interesting solution to alleviate the threshold voltage variations due to the process variability of W and H.

Why is that so important to take into account the back-gate?



Comparison front-gate threshold voltage V_{TH1} vs. back-gate bias V_{G2} with model (lines) and experimental measurements (squares)

➢ Under 'normal' condition, with a grounded back-gate (V_{G2} ≈ 0 V):

- Direction and amplitude of the $V_{TH}(W)$ curves driven by the position of the invariant point
- No amplitude at the invariant point. Not true elsewhere.
- Back-interface in accumulation, in depletion or in inversion?

➢ Experimental determination of the invariant point position with the $V_{TH1}(V_{G2})$ curves for several Fin widths W:

→ Determination of the back-gate regime at V_{G2} = 0 V

→ Determination of the correct $V_{TH1}(W)$ evolution

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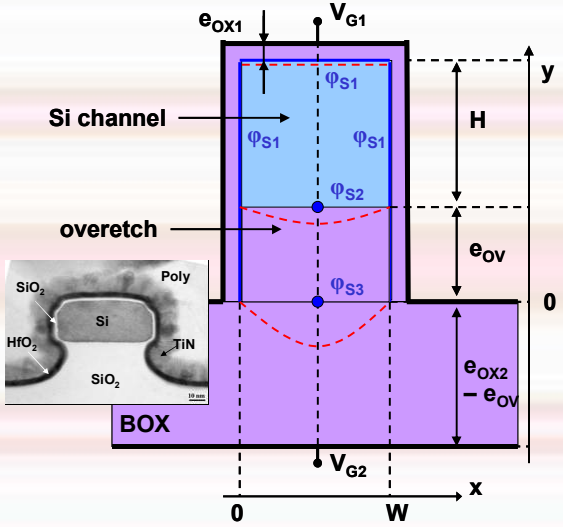
3D potential, TG and PiFETs

- 3D Laplace's equation to solve:

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2}+\frac{\partial^2\psi(x,y,z)}{\partial y^2}+\frac{\partial^2\psi(x,y,z)}{\partial z^2}\approx 0$$

- Boundary conditions
  - ✓ Influence of the 6 terminals (3 sides of the top-gate, back-gate, source and drain) considered separately.
  - ✓ Dirichlet (with constant or parabolic boundary conditions) or Neumann.



Transversal cross-section TGFET/PiFET, with notations.

- 3D potential

$$\psi(x,y,z)=\psi_{Top-gate\,(TG)}(x,y,z)+\psi_{Back-gate\,(BG)}(x,y,z)+\psi_{Lateral-gates\,(LG)}(x,y,z)+\psi_{Source\,/\,Drain\,(SD)}(x,y,z)$$

$$\psi_{TG}(x,y,z)=(V_{G1}-V_{FB1})\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_P(m)F_P(n)\sin\left(\frac{m\pi x}{W}\right)\sin\left(\frac{n\pi z}{L_G}\right)\left[\cosh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi y\right)\Big/\cosh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi(H+e_{OV})\right)\right]$$

$$\psi_{LG}(x,y,z)=(V_{G1}-V_{FB1})\sum_{m=1}^{+\infty}\sum_{n=0}^{+\infty}F_P(m)F_n(n)\sin\left(\frac{m\pi z}{L_G}\right)\sin\left(\frac{(2n+1)\pi(H+e_{OV}-y)}{2(H+e_{OV})}\right)\left[\frac{\sinh\left(\sqrt{\left(\frac{m}{L_G}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\,\pi(W-x)\right)+\sinh\left(\sqrt{\left(\frac{m}{L_G}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\,\pi x\right)}{\sinh\left(\sqrt{\left(\frac{m}{L_G}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\,\pi W\right)}\right]$$

$$\psi_{SD}(x,y,z)=\sum_{m=1}^{+\infty}\sum_{n=0}^{+\infty}F_P(m)F_n(n)\sin\left(\frac{m\pi x}{W}\right)\sin\left(\frac{(2n+1)\pi(H+e_{OV}-y)}{2(H+e_{OV})}\right)\left[\frac{V_S\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\,\pi(L_G-z)\right)+V_D\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\,\pi z\right)}{\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\,\pi L_G\right)}\right]$$

$$\psi_{BG}(x,y,z)=\varphi_{S3}\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_P(m)F_P(n)\sin\left(\frac{m\pi x}{W}\right)\sin\left(\frac{n\pi z}{L_G}\right)\left[\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi(H+e_{OV}-y)\right)\Big/\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi(H+e_{OV})\right)\right]$$

with:

$$\varphi_{S3}=(V_{G2}-V_{FB2})\Big/\left(1+\frac{\varepsilon_{Si}}{\varepsilon_{BOX}/(e_{OX2}-e_{OV})}\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_P(m)F_P(n)\sin\left(\frac{m\pi}{2}\right)\sin\left(\frac{n\pi}{2}\right)\left[\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi\Big/\tanh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\,\pi(H+e_{OV})\right)\right]\right)$$

W being the fin width, H the fin height, L_G the gate length, e_{OV} the overetch depth, ε_{BOX} the BOX permittivity, ε_{Si} the silicon permittivity, V_{FB1} (resp. V_{FB2}) the front-gate (resp. back-gate) flat band voltage. The series coefficient F_p, F_n, and F_c are defined in the Appendix.

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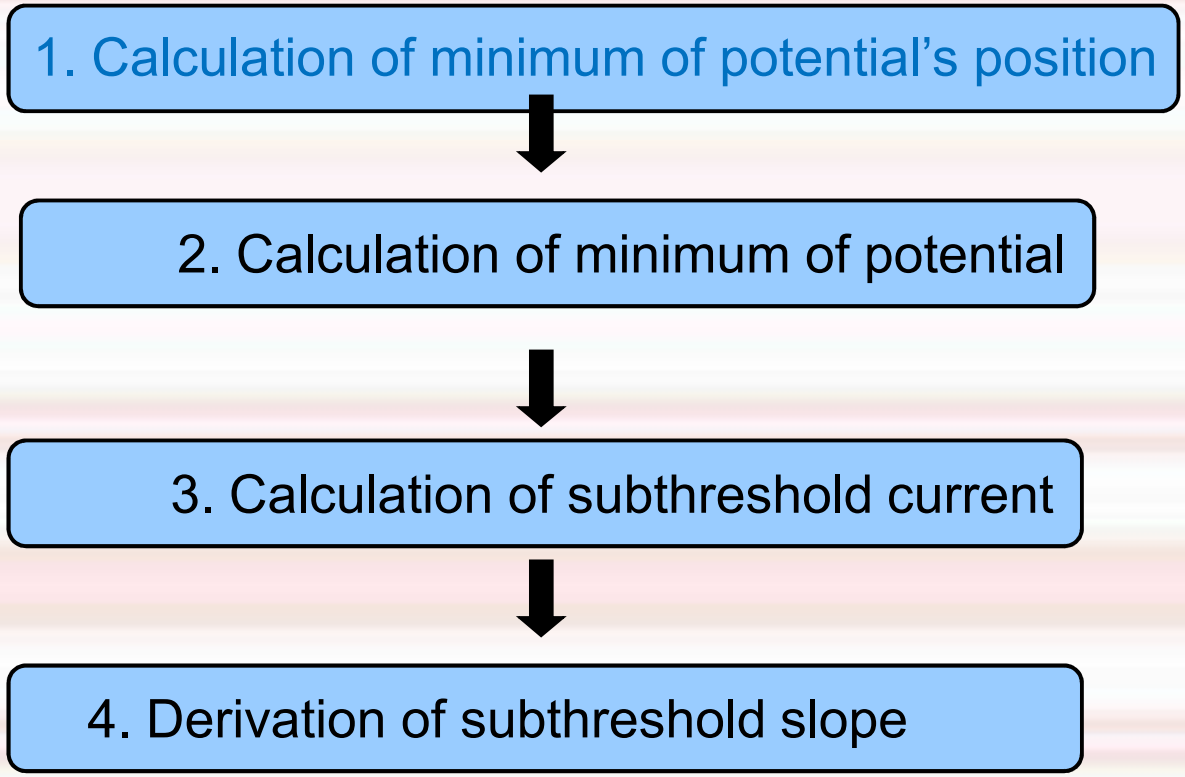
Model Flow Chart

- ✓ For undoped channels and deep subthreshold operation, the position of the most leaky path is determined mostly by the the device geometry (and gate biases boundary conditions)
- ✓ Most leaky path: approximation saying that the current flowing where the gate control is the weakest gives a good reproduction of the global device's behavior.



Calculation of the minimum potential

- ✓ Position of the 'most leaky path':
  - ✓ At mid-channel (y=W/2) for obvious symmetry considerations
  - ✓ At the body/BOX interface (x = t_{OV}): generally true, not necessarily for L<(W,H) but is a correct approximation
  - ✓ Along the Source/Drain axis:
    - ✓ Low V_{DS}: $Z_C = L_G/2$
    - ✓ High V_{DS}: minimum of potential moving closer to the source

- ✓ Formula from [Pei´02]:

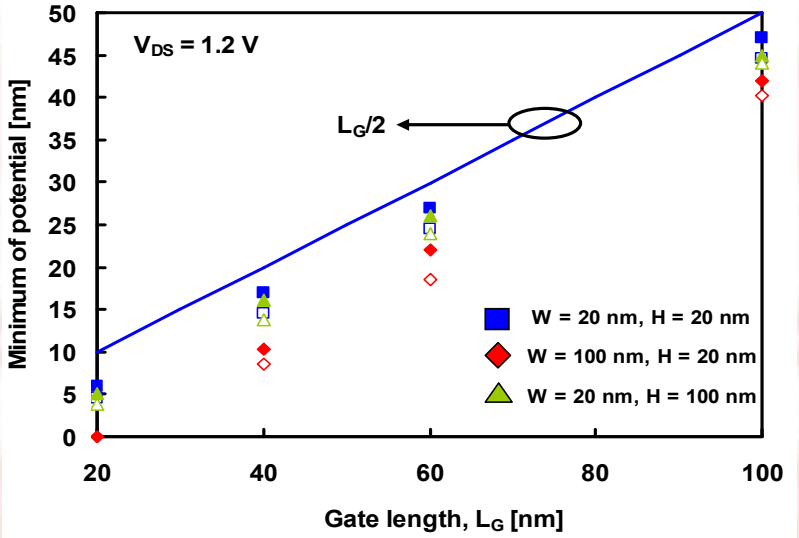
$$Z_C = \frac{L_G}{2} + \frac{L_D}{2\pi} \ln\left(\frac{-\varphi_{MS}}{-\varphi_{MS} + V_{DS}}\right)$$

with:

$$L_D = \left(\frac{1}{W^2} + \frac{0.5}{H^2}\right)^{-1/2}$$

➡ Simpler and acceptable approximation

- ✓ Finally: $\varphi_{MIN} = \varphi(t_{OV}, W/2, Z_C)$



Position of the minimum of potential along the S/D axis – comparison between the results given by the numerical simulations (closed symbols) and the analytical formula (open symbols)

[Pei'02] G. Pei et al., IEEE TED, 2002.

Calculation of the subthreshold current

- ✓ Assuming Drift-Diffusion transport, drain current written as:

$$I_{DS} = q\mu n_i \frac{\int_0^{V_{DS}} e^{-\varphi_F/V_T} d\varphi_F}{\int_0^{L_G} \frac{dz}{\int_{t_{OV}}^{t_{OV}+H} \int_{-W/2}^{W/2} e^{\varphi(x,y,z)/V_T} dxdy}}$$

- ✓ Using the most leaky path approach, current expressed as:

$$I_{DS} = \frac{\mu q n_i V_t}{L_G}(1 - e^{-V_{DS}/V_t}) \int_{t_{OV}}^{t_{OV}+H} \int_{-W/2}^{W/2} e^{\varphi_{MIN}(x,y,Z_C)/V_T} dxdy$$

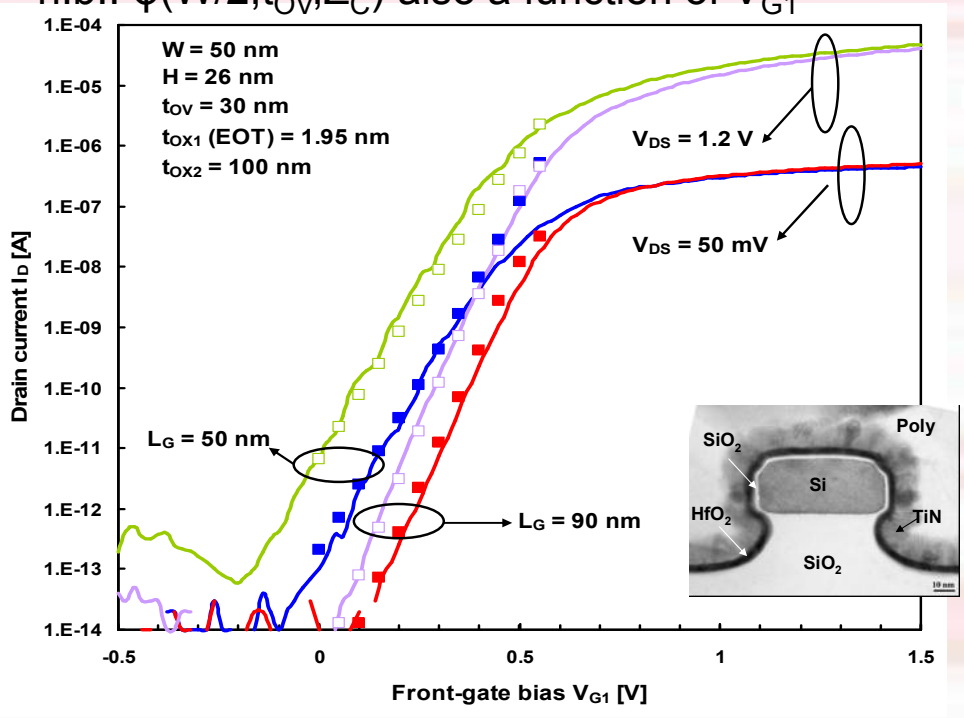
  - ✓ This work: approximation that the exponential of the potential can be described by a parabola in the width direction and is constant in the height direction.
  - ✓ Approximation amounting to say that a majority of carriers are located close to φ_{MIN}, i.e. in the vicinity of ($x=W/2$, $y=t_{OV}$)

Calculation of the subthreshold current

✓ Finally, after integration:

$$I_{DS} = \frac{\mu q n_i V_T}{L_G}(1 - e^{V_{DS}/V_t}) WH \frac{2e^{\varphi(W/2, t_{OV}, Z_C)/V_t} + e^{V_{G1}/V_t}}{3}$$

n.b.: $\varphi(W/2, t_{OV}, Z_C)$ also a function of V_{G1}

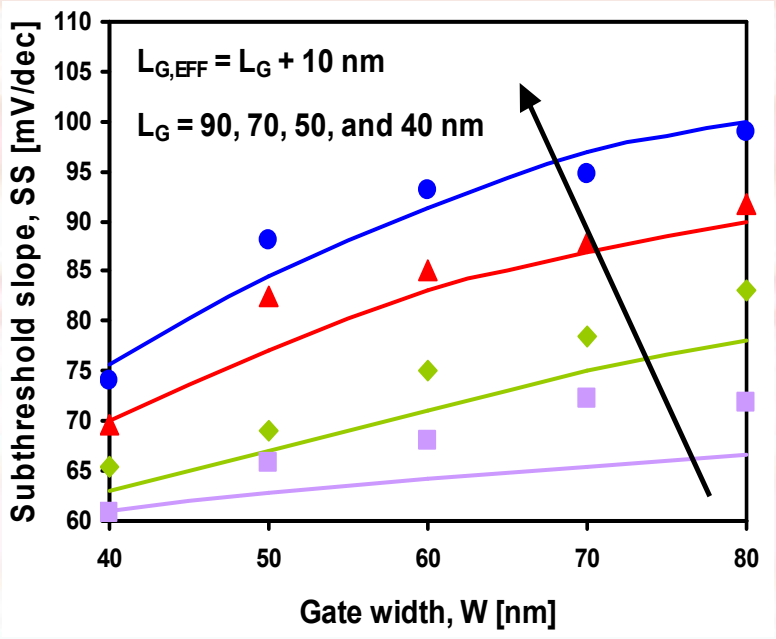


Subthreshold analytical (symbols) and experimental (solid lines) drain currents I_D vs. front-gate bias V_{G1} for gate lengths L_G of 90 nm (squares) and 50 nm (diamonds). Gate width W = 50 nm, H = 26 nm.

Good precision obtained compared to experimental measurements [Jahan'05]

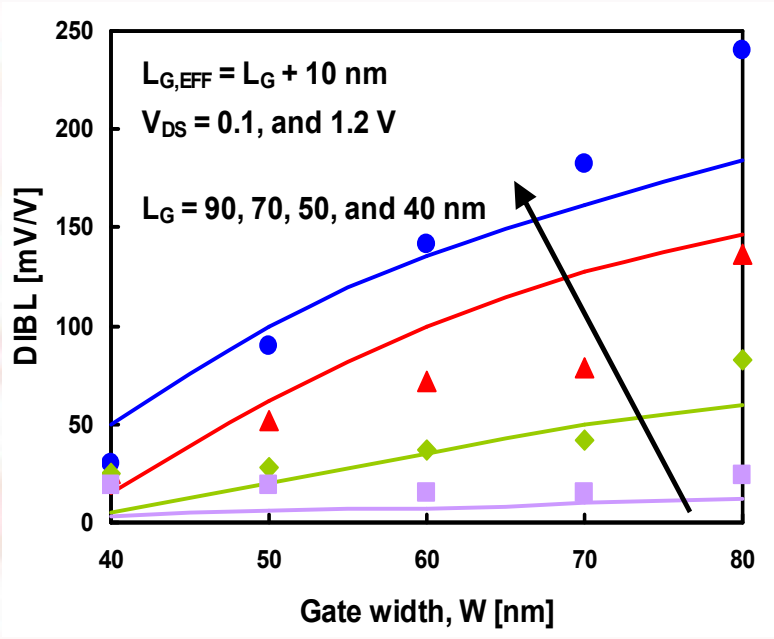
Formula allowing to take into account the drain and short channels effect in the subthreshold regime

Subthreshold slope, DIBL



SS vs. gate width W and gate length L_G. Model (lines) and experimental measurements (symbols)

- Calculation of the potential minimum and derivation of the subthreshold slope and DIBL.



DIBL vs. gate width W and gate length L_G. Model (lines) and experimental measurements (symbols)

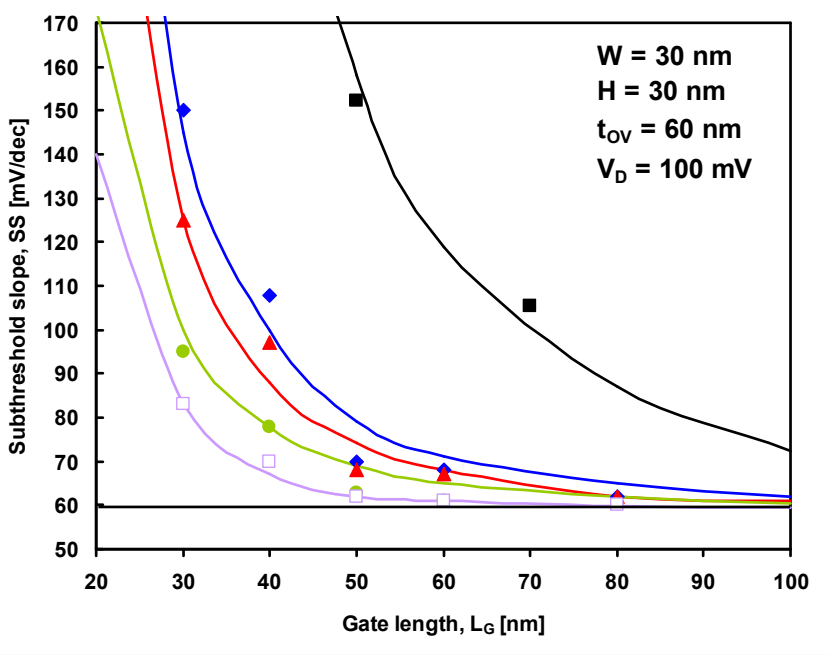
- Correct agreement model/experimental.
- Subthreshold characteristics improved with narrower devices

Device Scaling

- PiFET structure adaptable to TGFETs, DGFETs, planar FDSOI devices, and GAA transistors.
- Expressions extendible to a large number of MuGFETs.

Structure	Features
Pi-gateFET (core structure)	$t_{OV} \neq 0$
TGFET	$t_{OV} \approx 0$
Planar FDSOI	$t_{OV} \approx 0$, W>>H
DGFET/FinFET	$t_{OV} \approx 0$, W<<H
Gate All Around	$t_{OV} \approx 0$, $\varphi_{S3} = V_{G1} - V_{FB1}$

Variations of the core structure



SS vs. gate gate length L_G for GAA (open squares), PIFET (circles), TGFETs (triangles), DGFET (diamonds) and planar FDSOI (squares). Model (lines) and simulations (symbols)

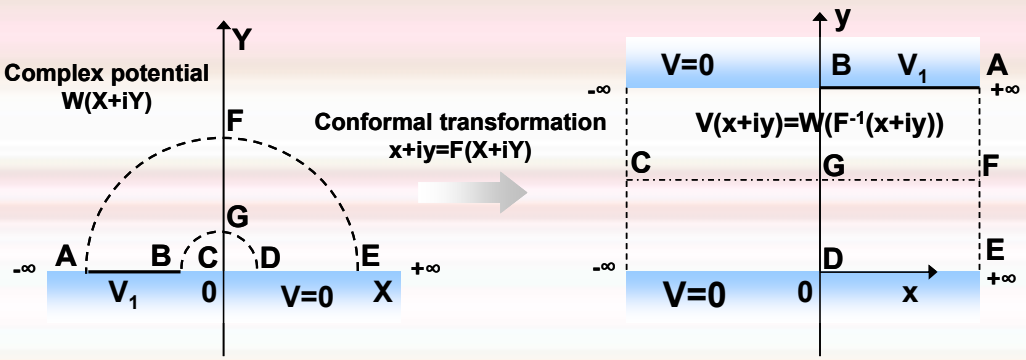
[Park'01] J.-T. Park, J.-P. Colinge, C.H. Diaz, "Pi-Gate SOI MOSFET", IEEE Electron Device Letters, vol. 22, no. 8, pp. 405-406, 2001.

Outline

1. Introduction
2. 1D core and Design-Oriented compact models
3. Hyperbolic function based compact models
4. Conformal mapping based compact models
5. Conclusions

What is conformal mapping?

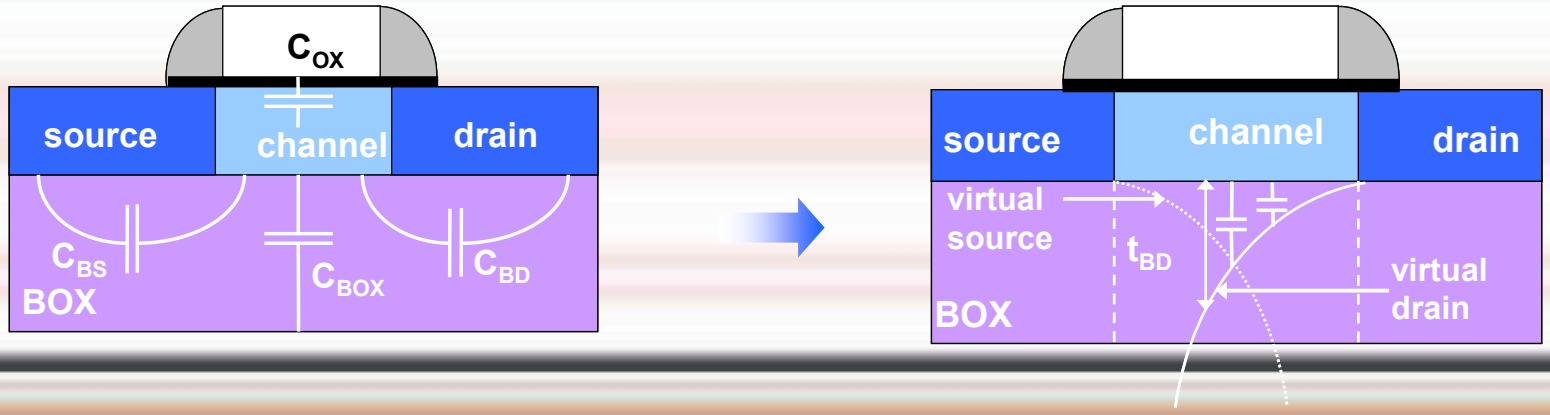
➢ Conformal transformation: transformation of an analytical function in a complex space:



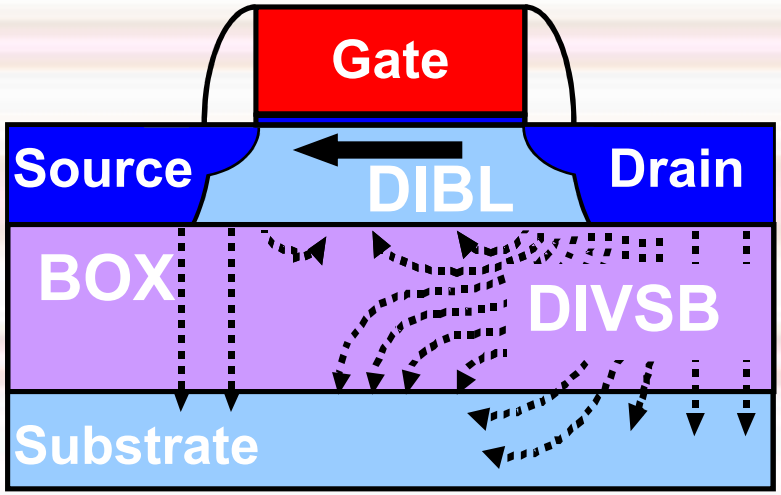
➢ Conservation of the Laplace's equation in the two spaces

→ Simplification of the geometry possible

➢ Application to FDSOI structures



FDSOI: effect of the Drain through the BOX



✓ Penetration of the electric field from the drain into the BOX and the substrate

→ electrostatic potential at the body-BOX interface modified

→ because of coupling between back and front channels (Lim & Fossum model), front channel properties degraded

'*Drain Induced Virtual Substrate Biasing*' (DIVSB) effect [Ernst'99]

[Ernst'99] T. Ernst, S. Cristoloveanu, IEEE Int. SOI conf. 1999, pp. 38-39.

Conformal Mapping Based Multi-Gate MOSFET Modeling

Objectives:

- Establish unified analytical models for nanoscale MugFETs (multigate MOSFETs) including FinFET and GAA devices

Procedure :

- Decompose Poisson's equation into a Laplace equation and a residual Poisson's equation (superposition principle)

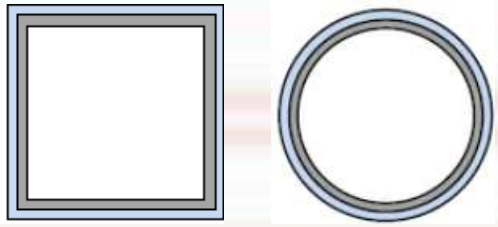
Capacitive inter-electrode effects

- From 2D/3D Laplace equation determine potential distribution associated with capacitive inter-electrode coupling.
- Use this to calculate *subthreshold* electrostatics, drain current and capacitances

Near and above threshold

- Apply residual Poisson's equation, boundary conditions, and modeling expressions to determine *self-consistent* device properties

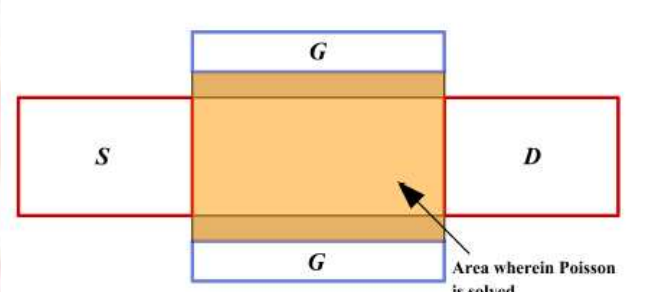
Schematic representation of 2D cut-plane of DG FinFET and trigate FinFET respectively



Schematic representation of 2D cut-plane of quad- and cylindrical GAA devices respectively

Application to Symmetrical Double-Gate MOSFETs

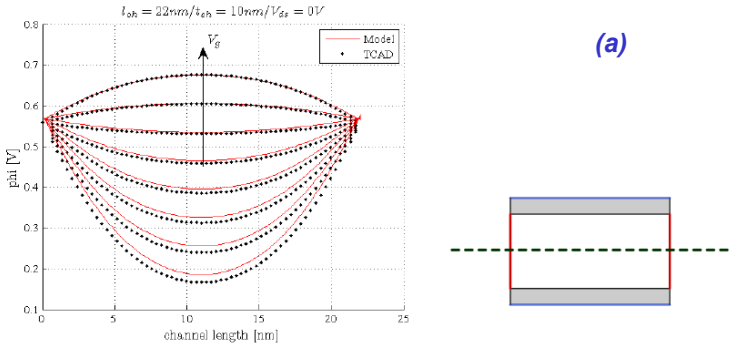
➢ In the subthreshold regime (resolution of 2D Laplace's equation) for Double-gate FETs [Børli'08] and Schottky Barriers DGFETs [Schwarz'09]:

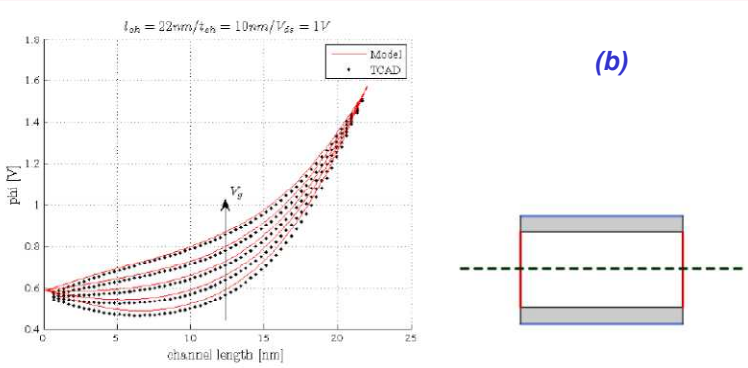


$$\varphi(u,v) = \frac{1}{\pi}\int_{-\infty}^{+\infty} \frac{v}{(u-\overline{u})^2+v^2}\varphi(\overline{u})d\overline{u}$$

Scheme and core formula ('Poisson's integral')

- ✓ 2D closed form
- ✓ No fitting parameters
- ✓ Intrinsically compact expression
- ✓ Excellent agreement with numerical simulations





Potential in the channel obtained for a step of gate bias V_G with model (solid lines) and numerical simulations (points). Drain voltage V_D = 0 V (a) and 1 V (b). L_G = 22 nm, t_{Si} = 10 nm.

[Børli'08] H. Børli et al., IEEE TED, vol. 55, no. 10, oct. 2008.
[Schwarz'09] M. Schwarz et al., to appear in ISDRS'09 proceedings, Dec.. 2009

Conformal Mapping + Isomorphic Functions for Multi-Gate MOSFET Modeling

The final model is based on the use of *isomorphic modeling* expressions for the potential distribution in (*x,y*) cross sections perpendicular to the source-drain *z* axis.

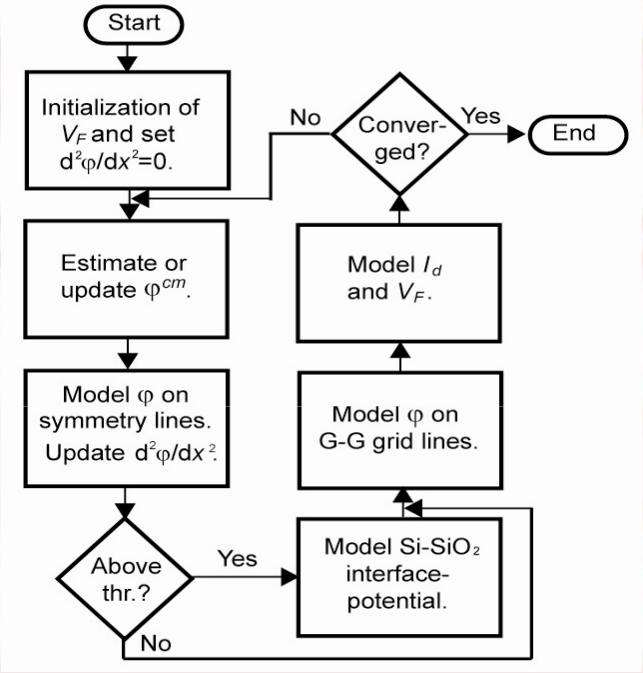
In subthreshold, this allows the complete potential distribution in the device body to be obtained based on the Laplace equation.

Short-channel effects are included by introducing auxiliary boundary conditions, such as the device center potential and the electrical field at the source center, derived analytically from the conformal mapping analysis.

A similar procedure, again using isomorphic modeling expressions, can also be applied to strong inversion by invoking Poisson's equation.

Starting from a rectangular gate structure, the present modeling can be generalized to include FinFETs, trigate, square gate, DG, and even circular gate devices, laying the groundwork for a unified, compact modeling framework for a wide range of multigate MOSFETs.

Near-threshold and Strong Inversion Modeling



The iterations are computationally efficient!

In strong-inversion, the device attains long channel behavior, and can be modeled as a long-channel device

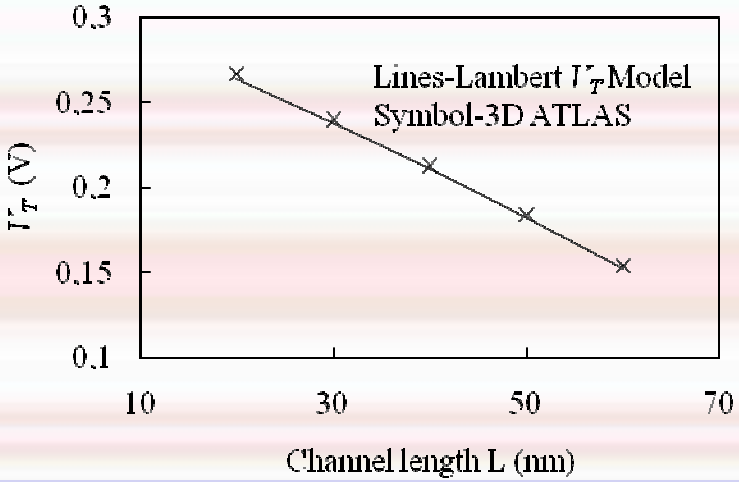
Transition (threshold) voltage (V_{DS} = 0V)**:**

Defined as the gate voltage for which center G-G potential becomes flat– pseudo flatband condition

Unified equation for transition voltage:

$$\frac{V_{bi}-V_T+V_{FB}}{V_{th}}\exp\left(\frac{V_{bi}-V_T+V_{FB}}{V_{th}}\right)=\beta\left(\frac{V_{bi}}{V_{th}}\right)$$

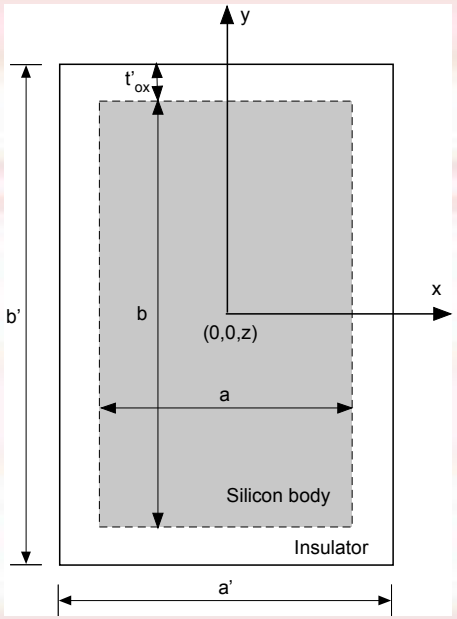
β **is a physical parameter dependent on device dimensions**



Potential expression in the channel cross section using isomorphic functions

We first consider a MugFET with a rectangular (x,y) cross-section of silicon widths a and b, for which we write the potential distribution as a 'power expansion' of the following isomorphic form,

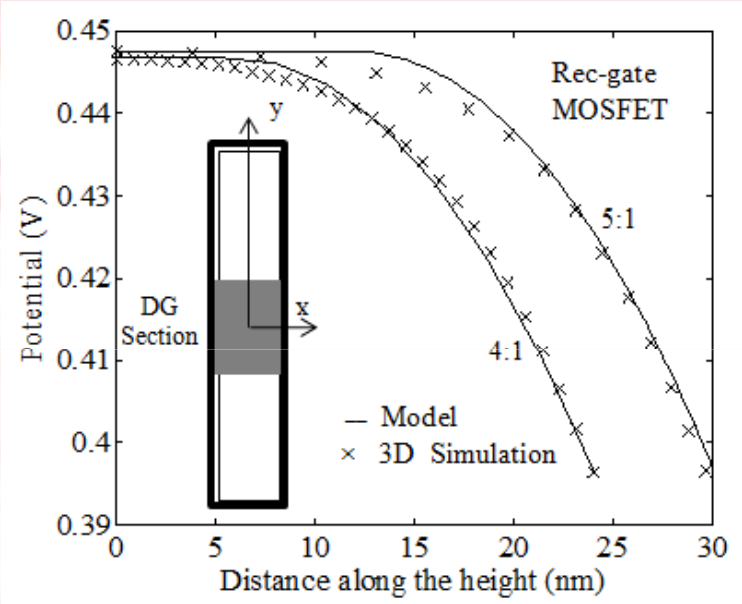
$$\hat{\phi}(x,y,z) = \hat{\phi}(0,0,z)\sum_{i=1}^{n}\alpha_i\left[1-\left(\frac{2x}{a'}\right)^{2i}\right]\left[1-\left(\frac{2y}{b'}\right)^{2i}\right]$$



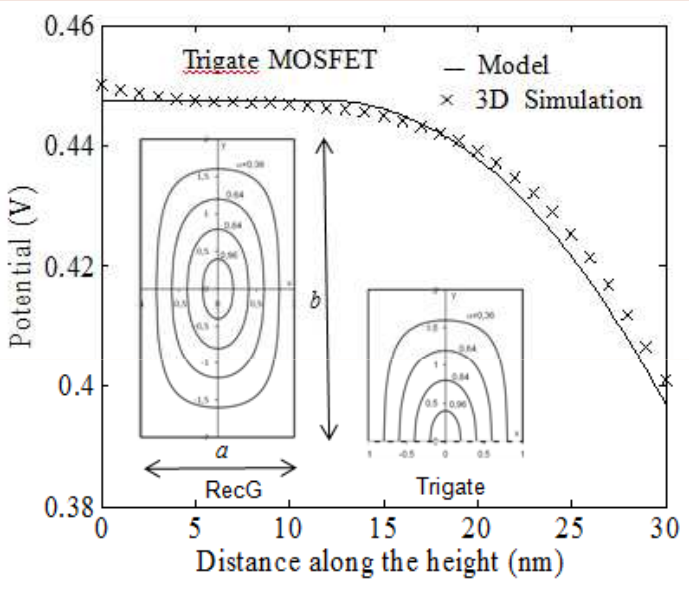
Here $a' = a + 2t'_{ox}$, $b' = b + 2t'_{ox}$ and $t'_{ox} = t_{ox}\varepsilon_{si}/\varepsilon_{ox}$ is an equivalent silicon layer that represents the electrostatic effect of the true gate insulator

$\hat{\varphi}(x,y,z)$ is the body potential relative to the gate interface.

Results for Tri-Gate MOSFETs

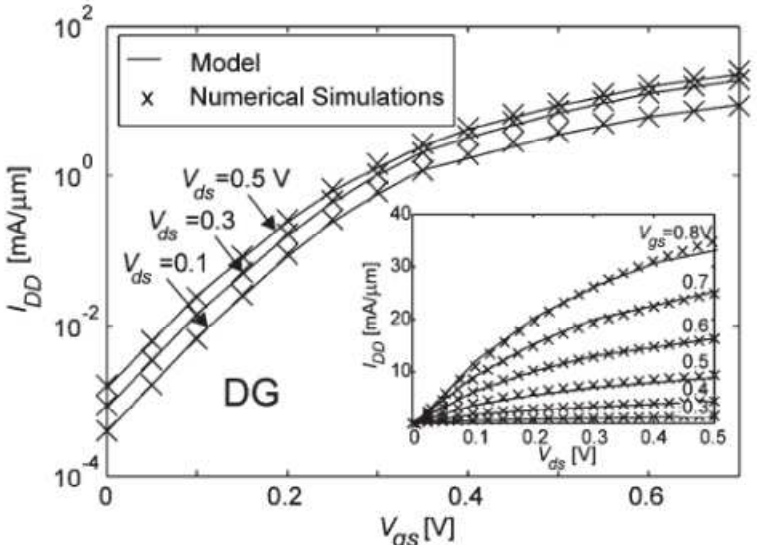


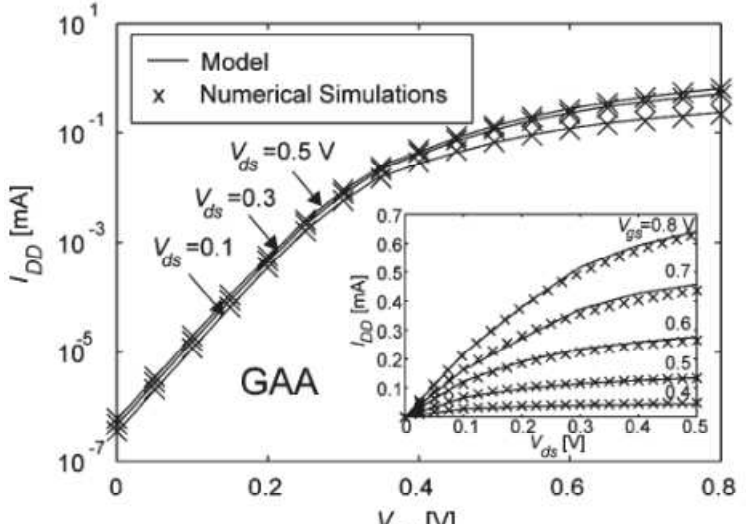
Modeled potential compared to numerical simulations along the height (y) direction for rec-gate devices with $\kappa = 4$ and 5, $V_{ds} = 0$ V, $V_{gs} = -0.1$V.

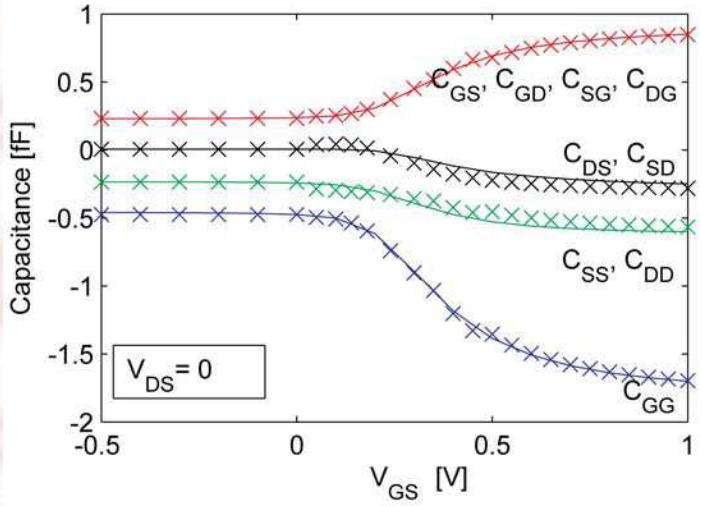


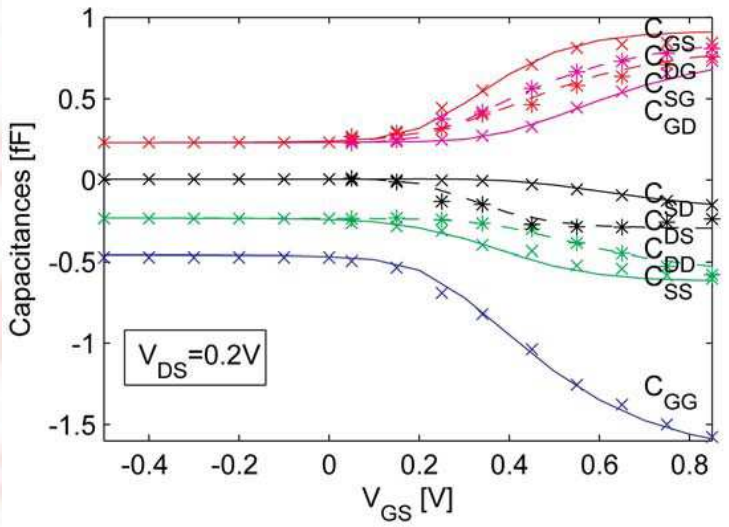
Modeled potential compared to numerical simulations along the height direction for a trigate device. Aspect ratio of original rec-gate device: 5:1. $V_{ds} = 0$ V, $V_{gs} = -0.1$V

Drain current and capacitance results









Outline

1. Introduction
2. 1D core and Design-Oriented compact models
3. Hyperbolic function based compact models
4. Conformal mapping based compact models
5. Conclusions

Conclusions

- Recent developments in compact/analytical Multi_Gate MOSFET modeling presented:

  - ✓ **Compact charge based models in Multiple-Gate MOSFETs (DG MOSFETs, GAA MOSFETs, FinFETs):**
    - A core model, developed from a unified charge control model obtained from the 1D Poisson's equation (using some approximations in the case of DG MOSFETs).
    - A design-oriented model, developed from a 1D electrostatic model with the incorporation of short-channel effects.
    - 2D or 3D scalable models of the short-channel effects (threshold voltage roll-off, DIBL, subthreshold swing degradation and channel length modulation), developed by solving the 2D or 3D Poisson's equation using appropriate techniques.

  - ✓ **Hyperbolic series´s development used to develop compact threshold voltage models for 2D interface coupling in Triple-gate and Pi-FETs architectures**

  - ✓ **Conformal mapping technique presented, so far applied to the case of Multi-Gate MOSFETs (DG, GAA, Tri-Gate MOSFETs, DG Schottky Barriers DG MOSFETs) , and fringing fields in FDSOI MOSFETs**

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Thank you for your attention!