SHORT COURSE:

VARIATION-TOLERANT DESIGN OF ANALOG CMOS CIRCUITS

by Marvin Onabajo

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COURSE DESCRIPTION:

Contemporary single-chip mixed-signal systems manufactured with complementary metal-oxide-semiconductor (CMOS) technology become increasingly susceptible to process-voltage-temperature variations, which create diverse design, testing, and reliability concerns. In this short course, several design techniques are described to address variation-related challenges for analog blocks in mixed-signal systems-on-a-chip. The presented methods are results from research works involving receiver front-end circuits, baseband filter linearization, and data conversion. The circuit-level techniques are described with their relationships to system-level calibration approaches that are emerging in the industry to tune the performances of analog circuits with digital assistance or control. Furthermore, the course will cover a strategy to utilize on-chip temperature sensors for the measurement of signal power and linearity characteristics of analog/RF circuits, allowing these sensors to be employed as variation monitors.

In the first lecture, process variations as well as associated technical and cost impacts will be introduced, followed by a discussion of transceiver design approaches to alleviate these problems. The main emphasis will be on transceivers with digitally-assisted calibrations of analog blocks. Opportunities for high-volume manufacturing test cost reduction will be exemplified with an implementation case study of the loopback testing method. Next, built-in test circuitry for analog circuits will be presented with an emphasis on on-chip power detection for characterization of RF parameters such as gain, linearity, and impedance matching. Various

analog circuits will be introduced that contain digitally-controllable elements to enable performance tuning in support of system-level calibration schemes.

In the second lecture, the use of digitally controllable elements to compensate for variations will be illustrated with two examples: i) a distortion cancellation method for baseband operational transconductance amplifiers and filters that enables a third-order intermodulation (IM3) improvement of up to 22dB; ii) a 3-bit two-step quantizer with adjustable reference levels, which was designed and fabricated in 0.18µm CMOS technology as part of a continuous-time ΣΔ analog-to-digital converter system. Next, an alternative strategy will be outlined for built-in testing of analog circuits with on-chip temperature sensors used as electrical power detectors. Comparisons of an amplifier's measurement results at 1GHz with the measured DC voltage output of an on-chip temperature sensor show that the amplifier's power dissipation can be monitored and its 1-dB compression point can be estimated with less than 1dB error.

Finally, an analog calibration technique will be explained, which lessens the mismatches between transistors in the differential high-frequency signal paths of analog CMOS circuits. The methodology involves auxiliary transistors that sense the existing mismatch as part of a feedback loop for error minimization. It was assessed by performing statistical Monte Carlo simulations of a differential amplifier and a double-balanced mixer designed in CMOS technologies

PROGRAM:

DAY1: Tuesday 5th June, 2012, 9:30 – 13:00h, Aula de Postgrau, 116, Edifici C5, Campus Nord UPC, Barcelona (http://maps.upc.edu/)

- CMOS process variation challenges
- System-level calibration trends (transceiver systems-on-a-chip examples)
- Production test simplification and cost reduction (example: loopback testing)
- Built-in testing of analog circuits
- Digitally-assisted analog circuit design and performance tuning

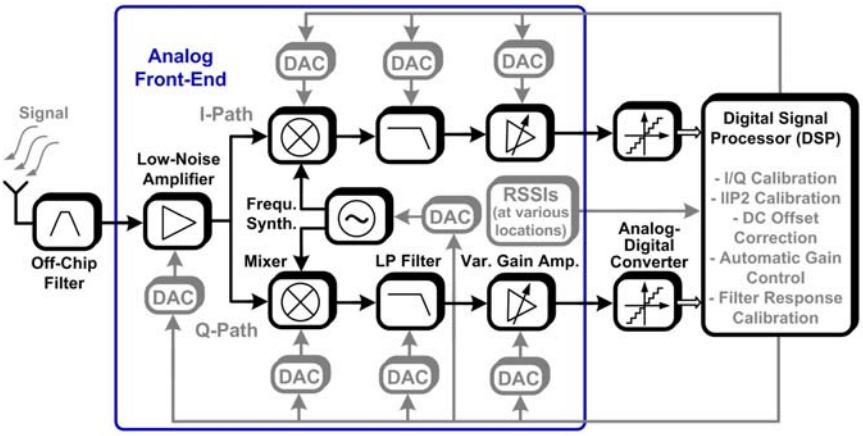
DAY2: Wednesday 6th June, 2012, 9:30 – 13:00h, Aula de Postgrau, 116, Edifici C5, Campus Nord UPC, Barcelona (http://maps.upc.edu/)

- Case study: digitally-assisted linearization of operational transconductance amplifiers
- Case study: variation-aware continuous-time ΔΣ analog-to-digital converter design
- On-chip DC and RF power measurements with differential temperature sensors

- Case study: differential temperature sensor design

<u>DAY3</u>: Thursday 7th June, 2012, 9:30 – 12:30h, Aula de Postgrau, 116, Edifici C5, Campus Nord UPC, Barcelona (http://maps.upc.edu/)

- Temperature sensors as variation monitors
- - Mismatch reduction for transistors in high-frequency differential analog signal paths
- - Example: mixer design with analog tuning for transistors biased in weak inversion



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