Field Programmable Arrays for Neuromorphic Computation

Alister Hamilton

14th & 15th June 2010
UPC, Barcelona

Talks Schedule

14th June 2010: Neuromorphic Systems in Analogue VLSI: developments at the University of Edinburgh

15th June 2010: Programmable Analogue VLSI Architectures: two novel approaches

Neuromorphic Systems in Analogue VLSI: development at the University of Edinburgh

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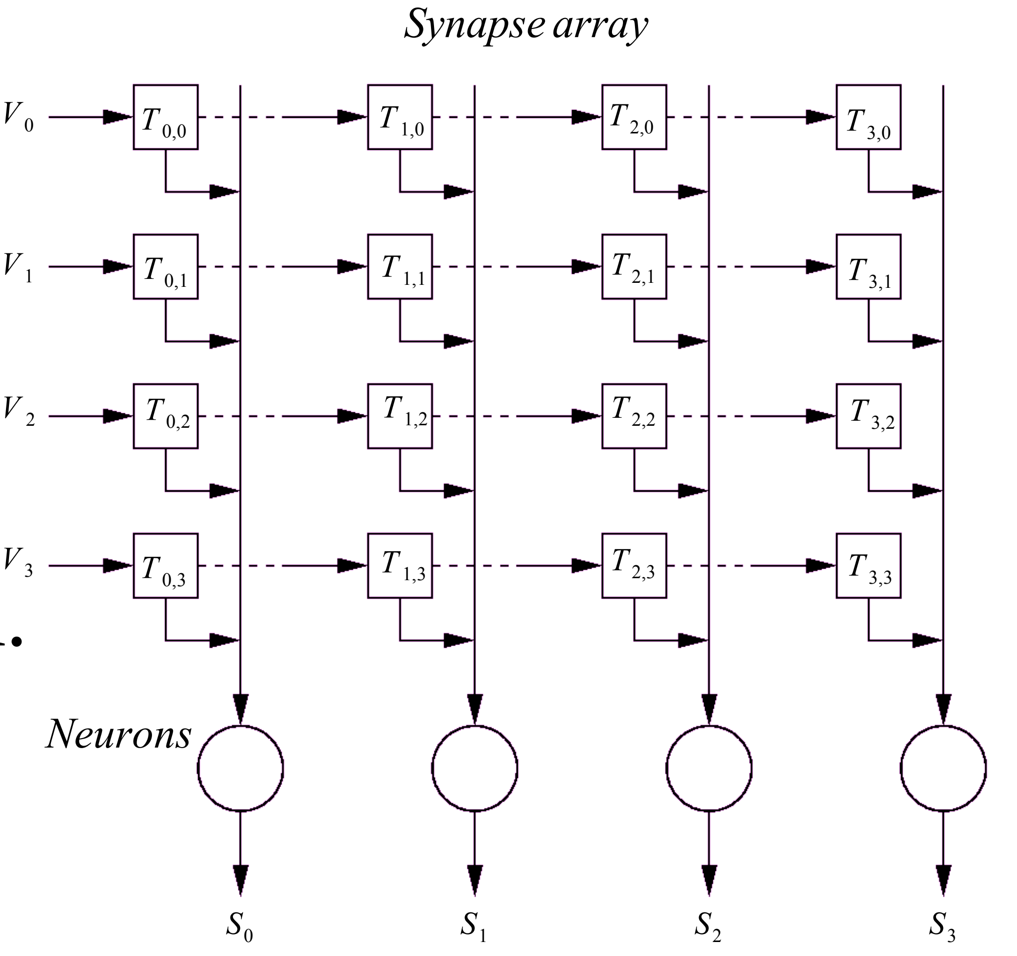
Agenda

- Neural Network implementations
  - Pulse stream and pulse width schemes
  - Epsilon chip and applications
- Neuromorphic Systems
  - Integrate and Fire neurons in auditory system
  - Adaptive Neuromorphic Olfaction Chip
  - Cricket hair sensor
  - MEMS/CMOS microphone

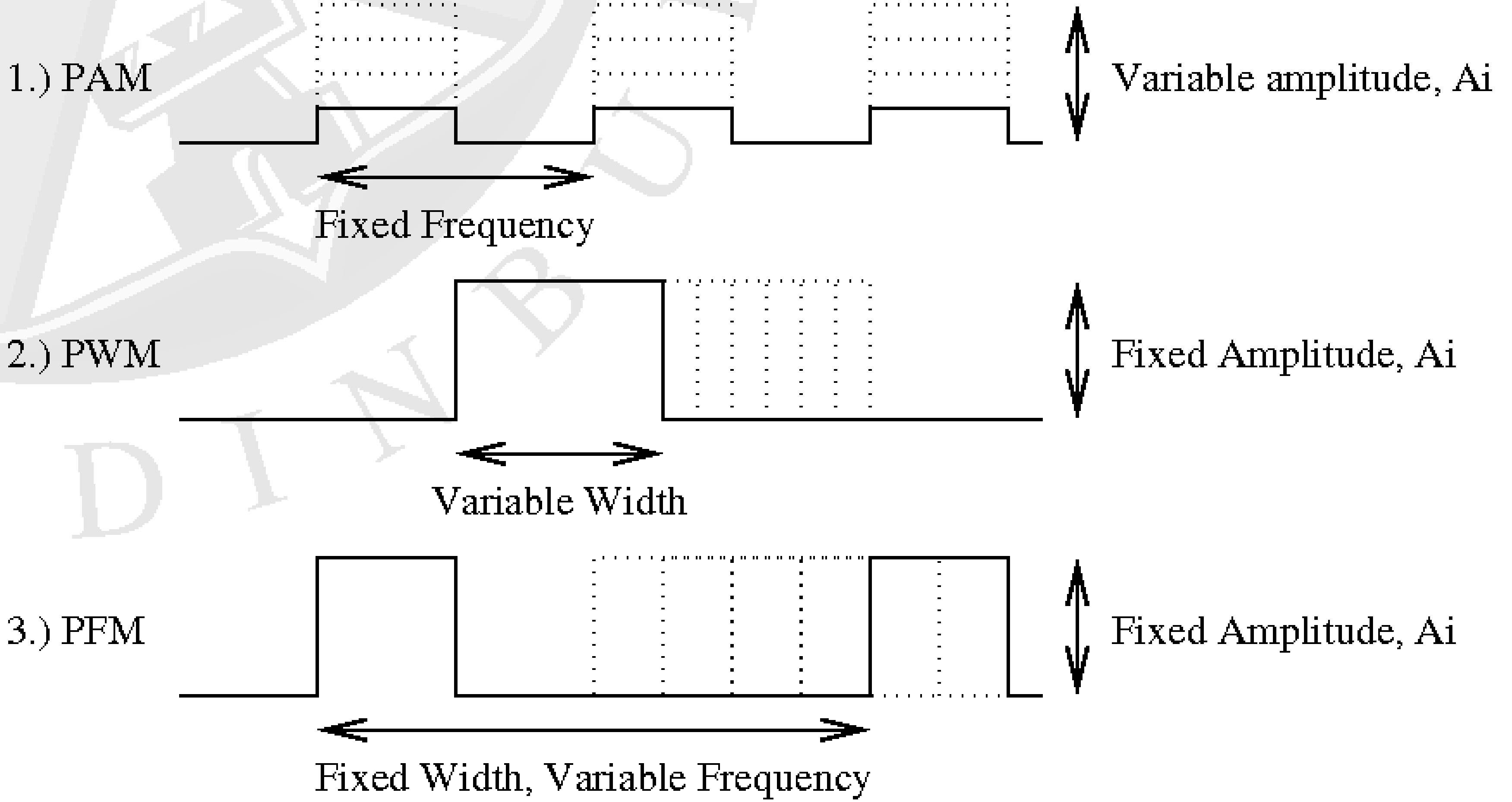
Neural network implementations

- ***Synapse*** multiplies incoming ***pre-synaptic neural state*** (V_j) by a ***synaptic weight*** (T_{ij}).
- ***Synapse*** outputs are ***summed*** in each column.
- ***Non-linear neuron*** generates ***post-synaptic neural state*** (S_i).



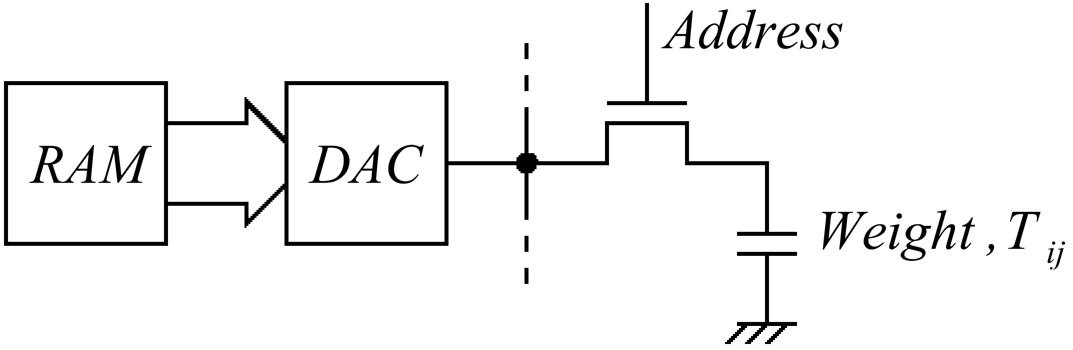
Information encoded in time (#1)

- Non-exhaustive set of time coding examples



Implementation strategy

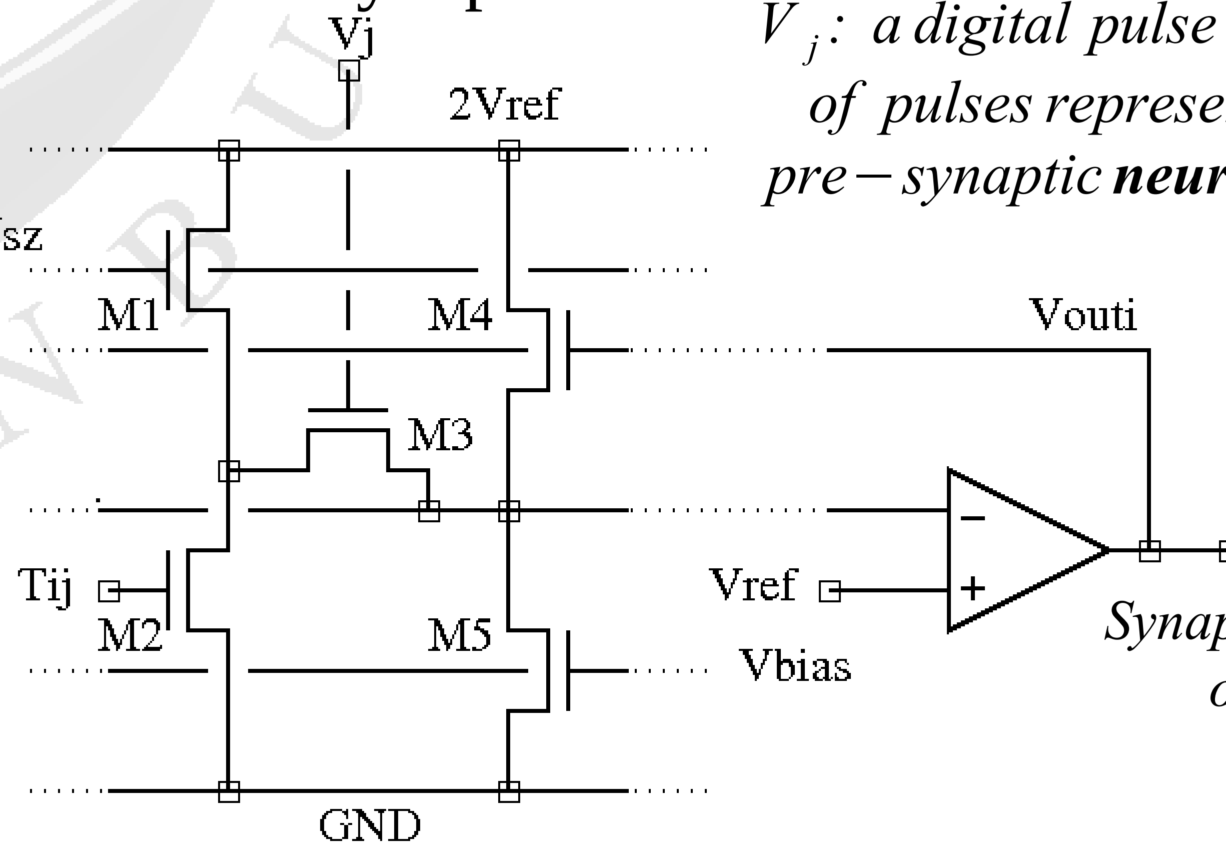
- Encode neural states as PWM or PFM signals
  - leads to a new range of circuit implementations
- Encode synaptic weights as analogue voltages
  - Stored on capacitors locally at each synapse
  - Refreshed from off-chip RAM
  - Refresh mechanism updates each synaptic weights



Implementation in analogue VLSI

- Novel implementations inspired by biology
  - Example column of synapses

V_j: *a digital pulse* or *series of pulses represents the pre−synaptic* ***neural state***.

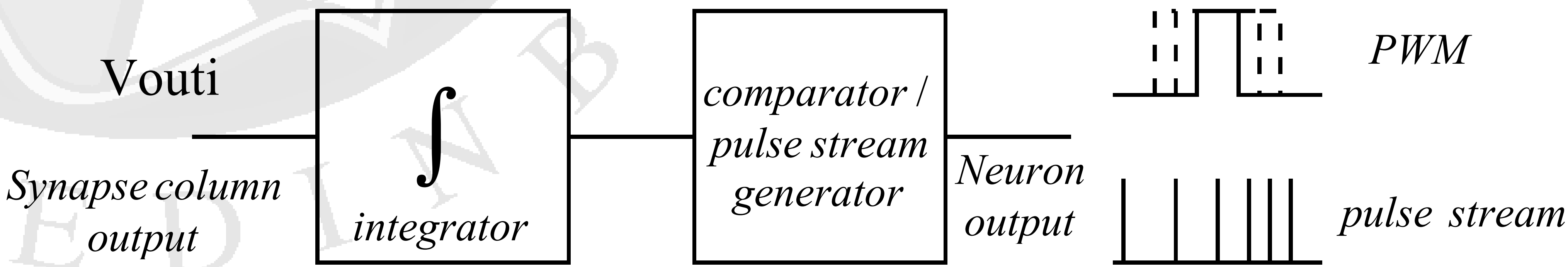


T_{ij}: *analogue voltage represents* ***synaptic weight***

Synapse column output

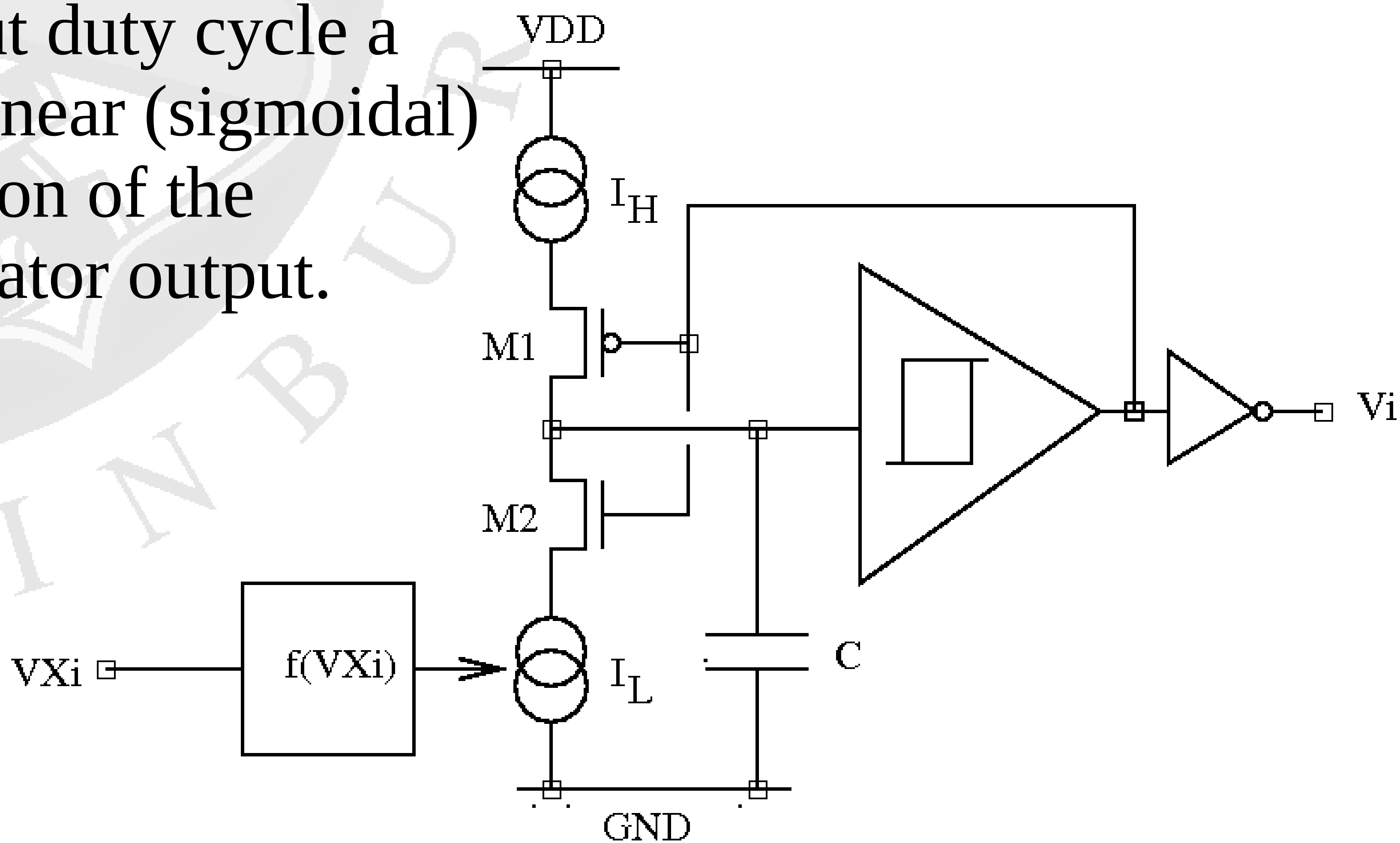
Neuron implementation

- Neuron output represented by a digital ***width modulated pulse***, or a ***stream of digital pulses***.



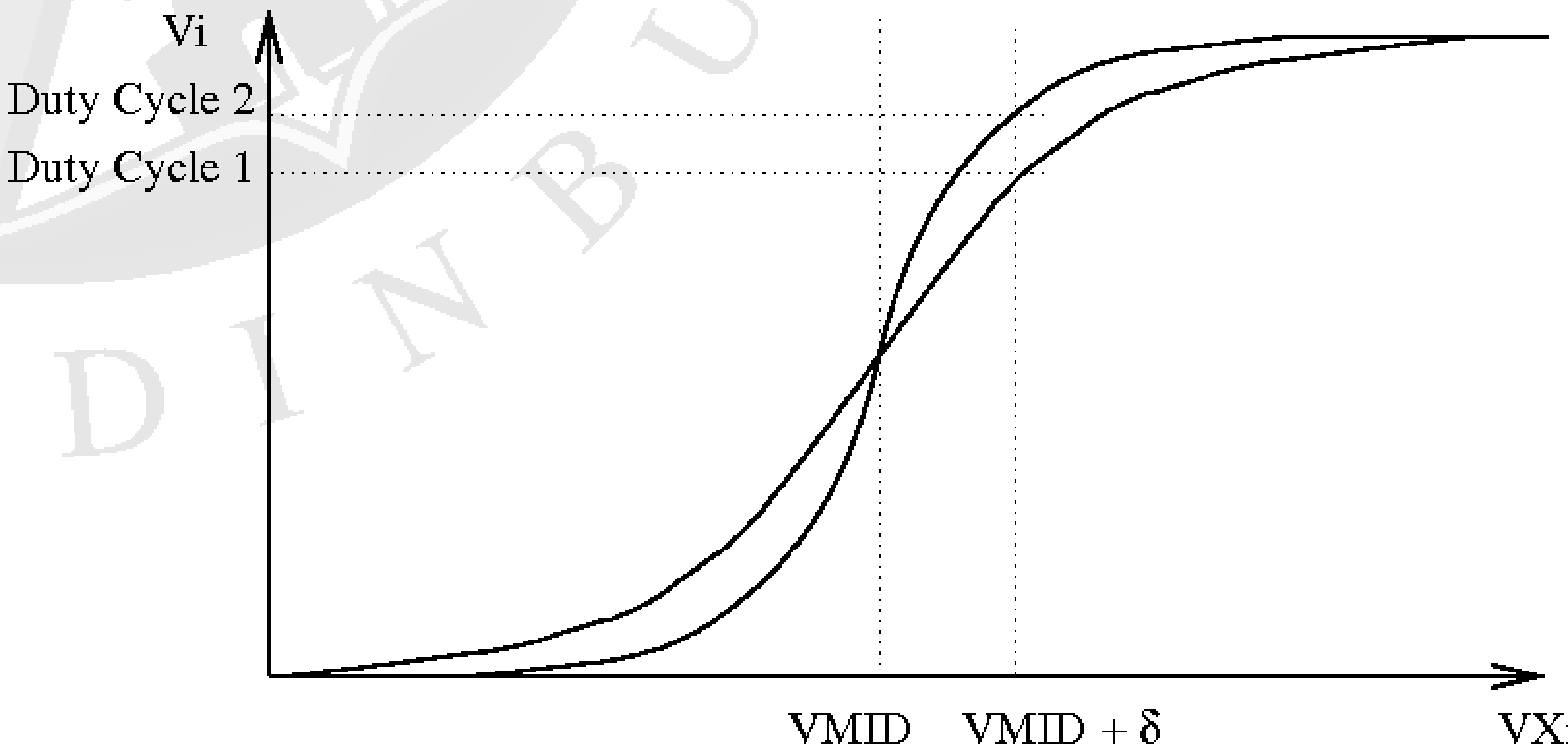
Pulse stream neuron

- Output duty cycle a non-linear (sigmoidal) function of the integrator output.



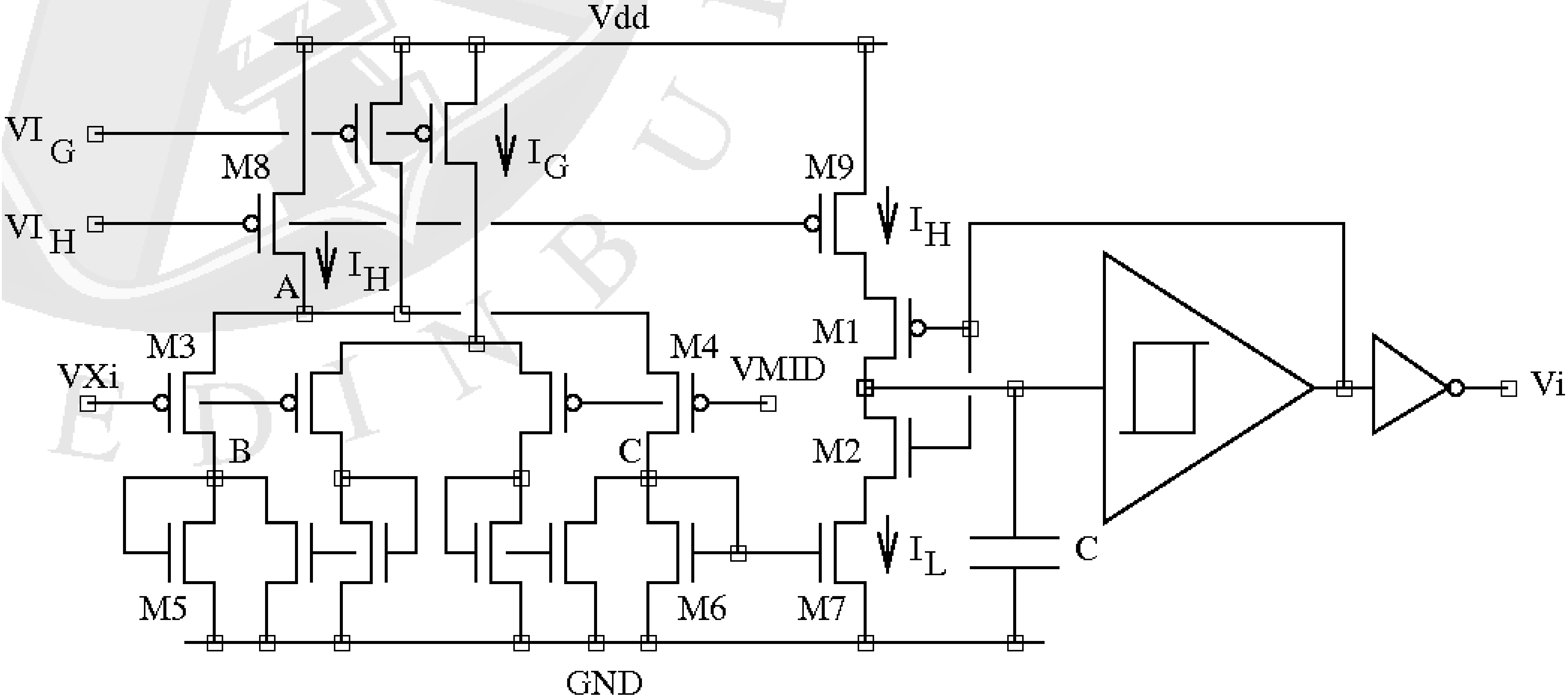
Pulse stream neuron gain change

- Modify the slope of the transfer characteristic
  - realised using phase lock loop mechanisms



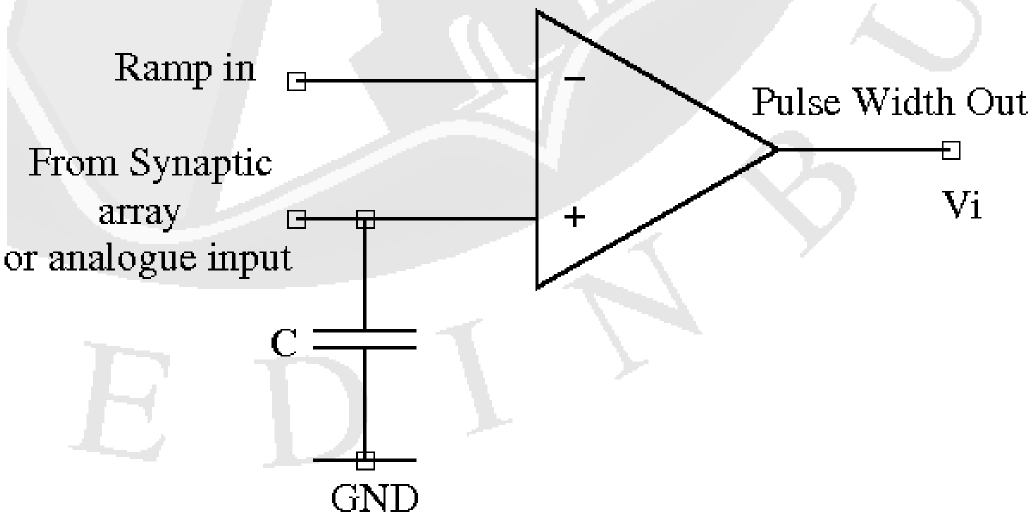
Variable gain neuron circuit

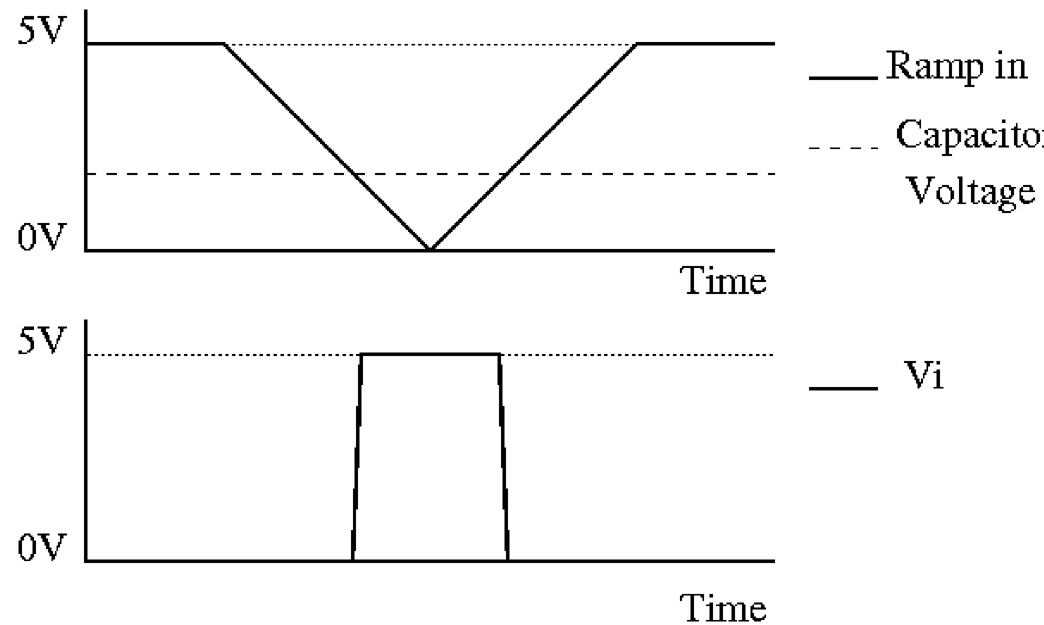
- Two diff stages provide sigmoid & gain control



Pulse width neuron

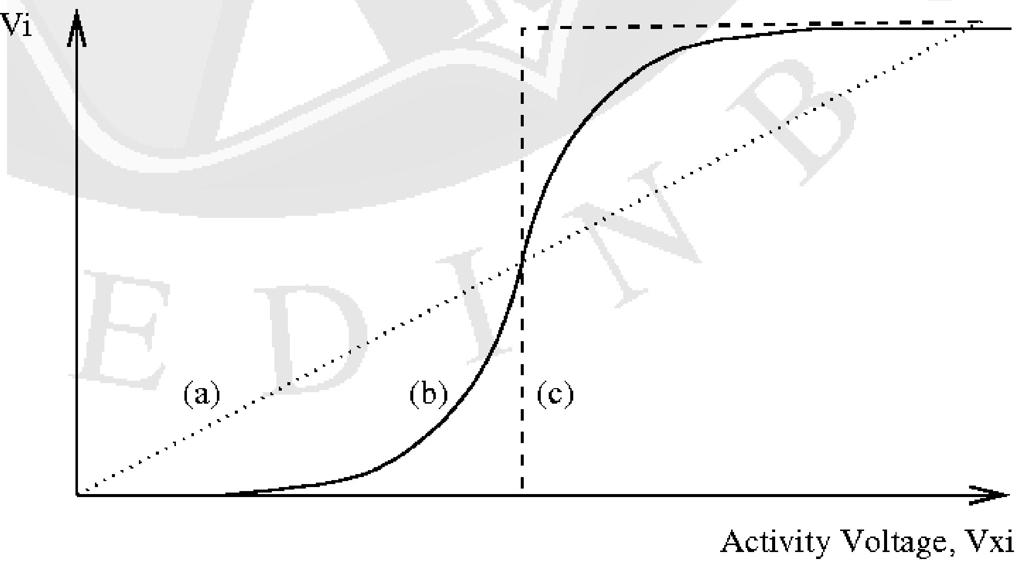
- Simple comparator fed with a (linear) ramp.

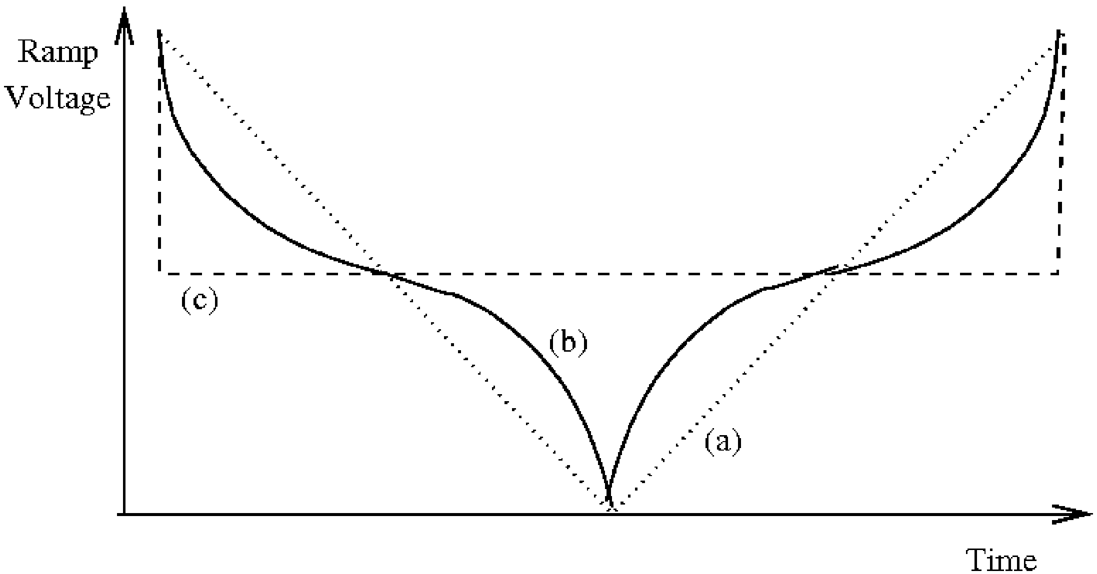




Pulse width neuron ramp control

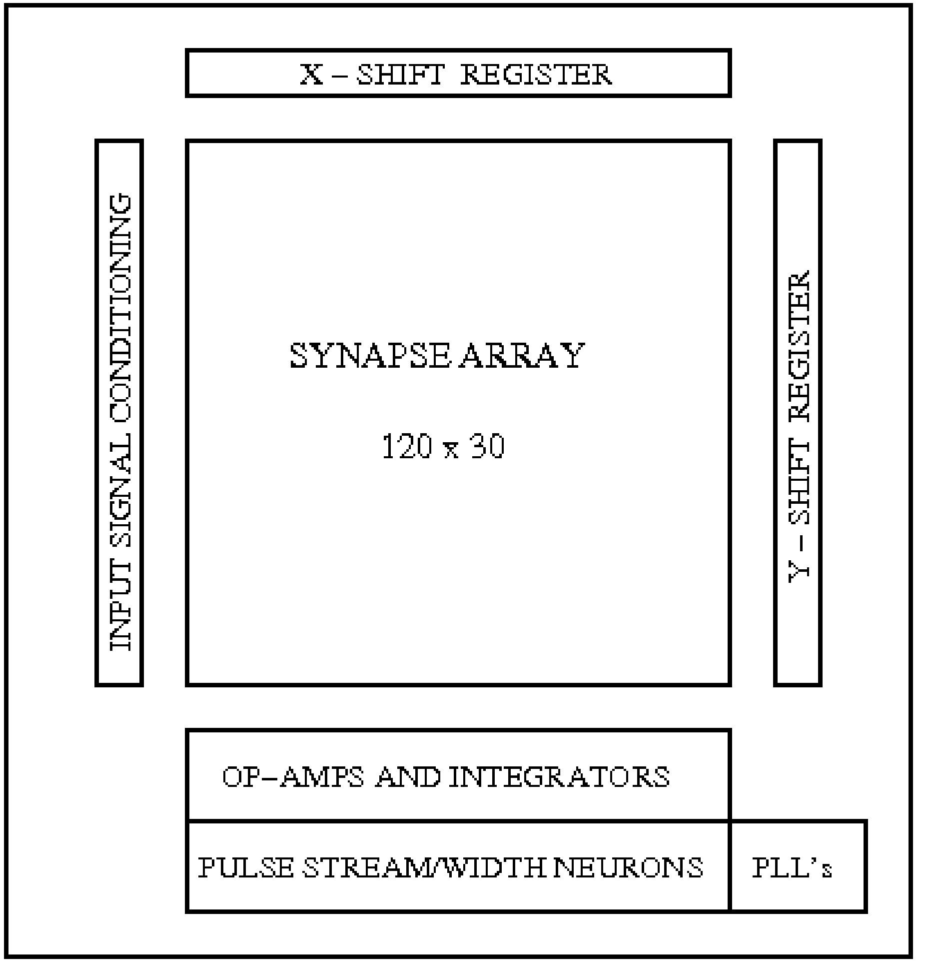
- Simple comparator fed with a non-linear ramp.
  - non-linear ramp generated off-chip (RAM and DAC)



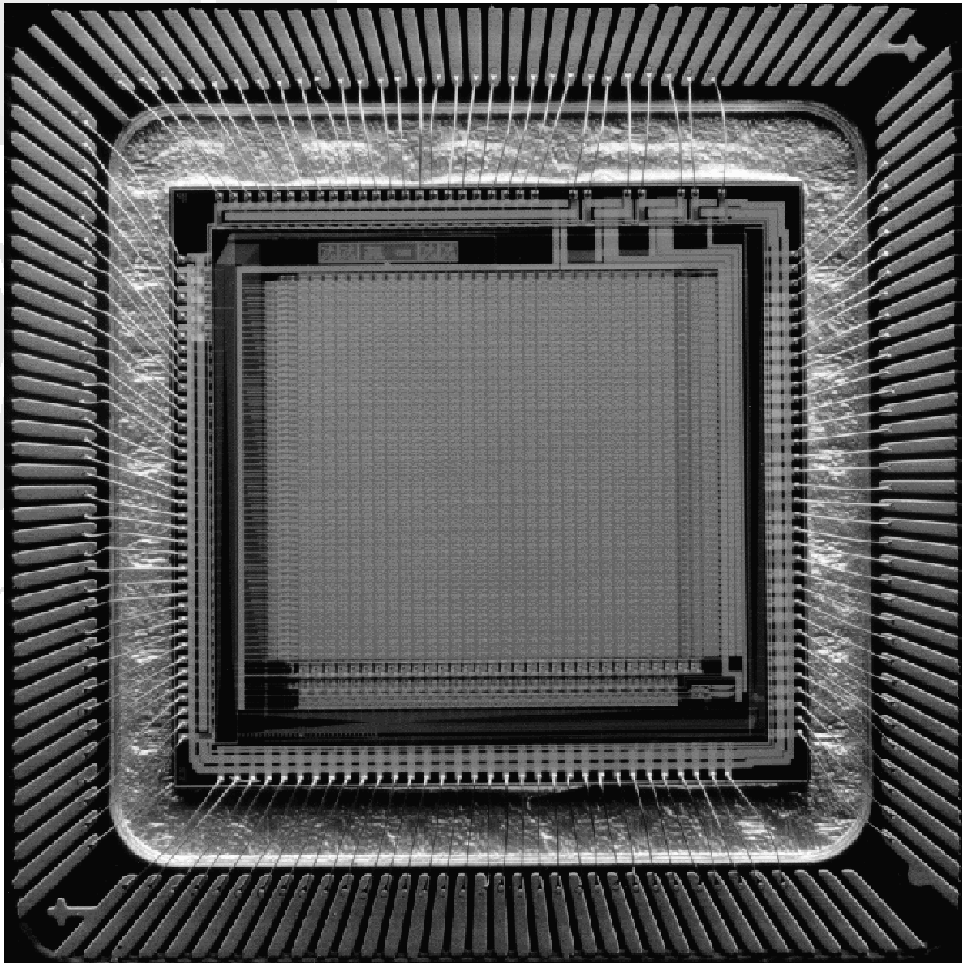


EPSILON Outline

- **E**dinburgh **P**ulse **S**tream **I**mplementation of a **L**earning **O**riented **N**etwork
  - 120 inputs, 30 outputs
  - 3600 synapses
  - 18Mcps - 360Mcps
  - 9.5mm x 10.1mm in 1.5µm CMOS

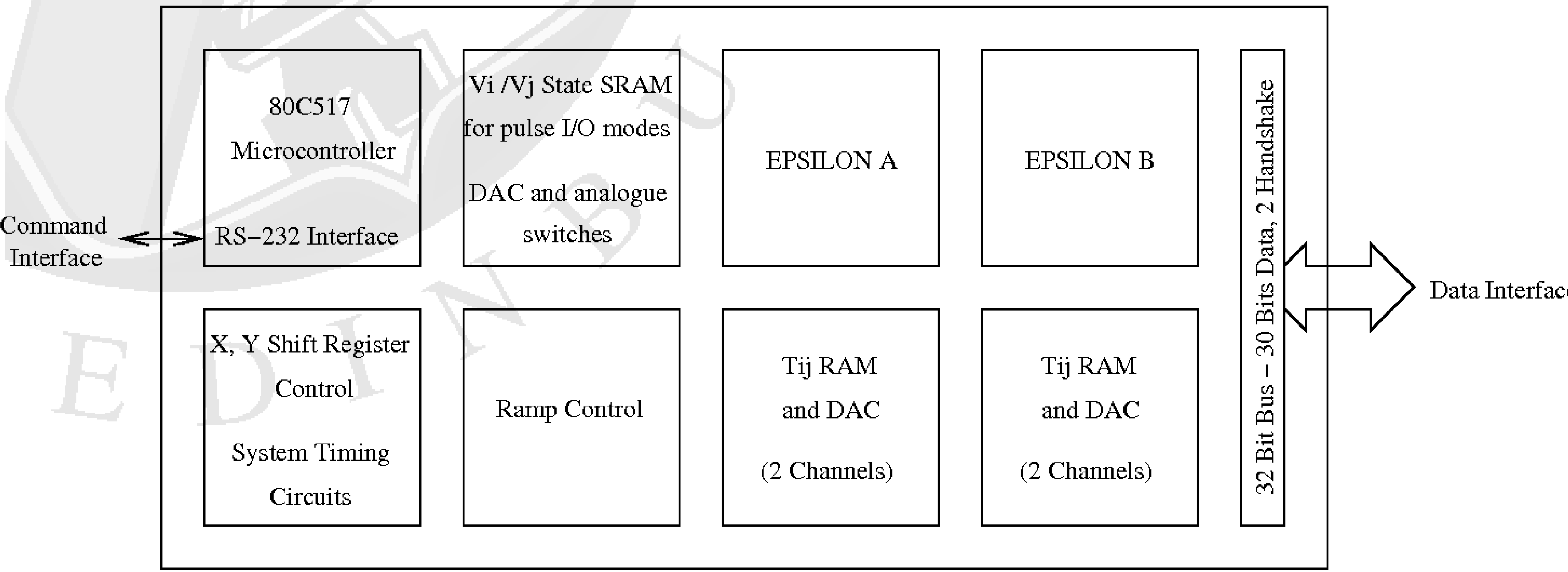


EPSILON: chip photo



System integration

- EPSILON chips and support circuitry on a PCB

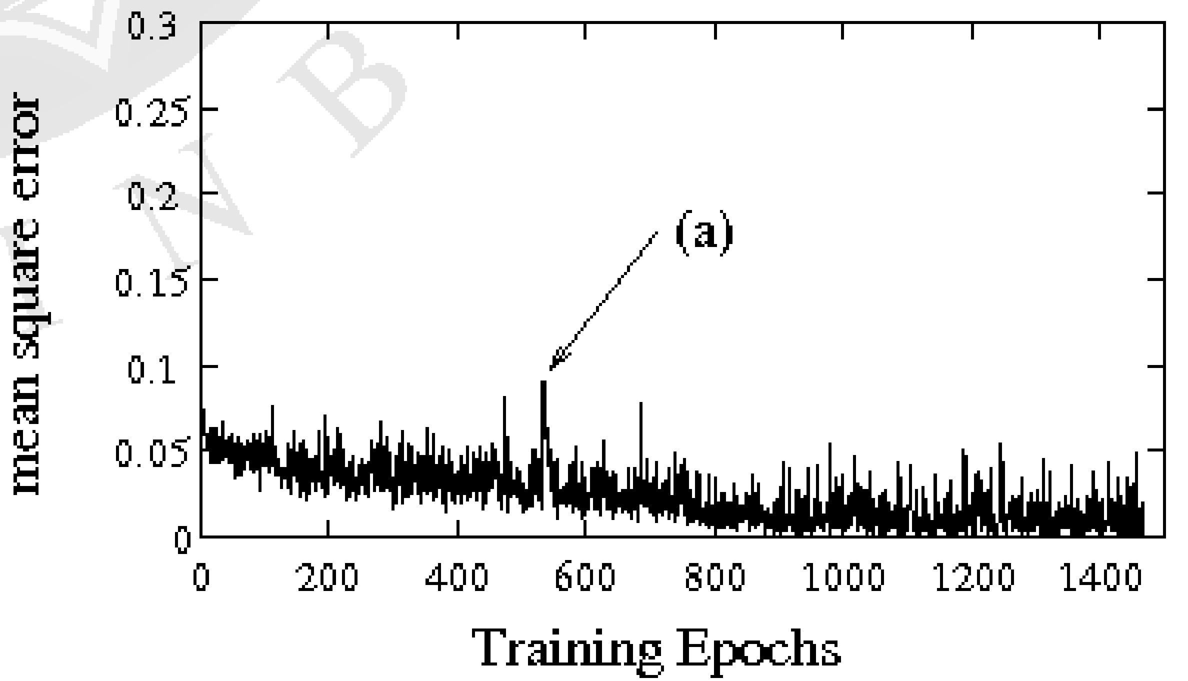


Oxford/Alvey vowel database

- Vowel sounds from 18 female and 15 male speakers
  - Analogue outputs from a bank of 54 band-pass filters
  - Feedforward network of 54 input neurons, 27 hidden layer neurons and 11 output neurons
  - Network trained with 2 female speakers using a virtual target training algorithm (similar to back propagation)
  - Network then presented with remaining 16 female speakers to test generalisation performance.

Mean square error results

- Mean square error reduced as training progresses
  - Initial weight set developed on workstation
  - Chip-in-loop training follows. (a) system reset.

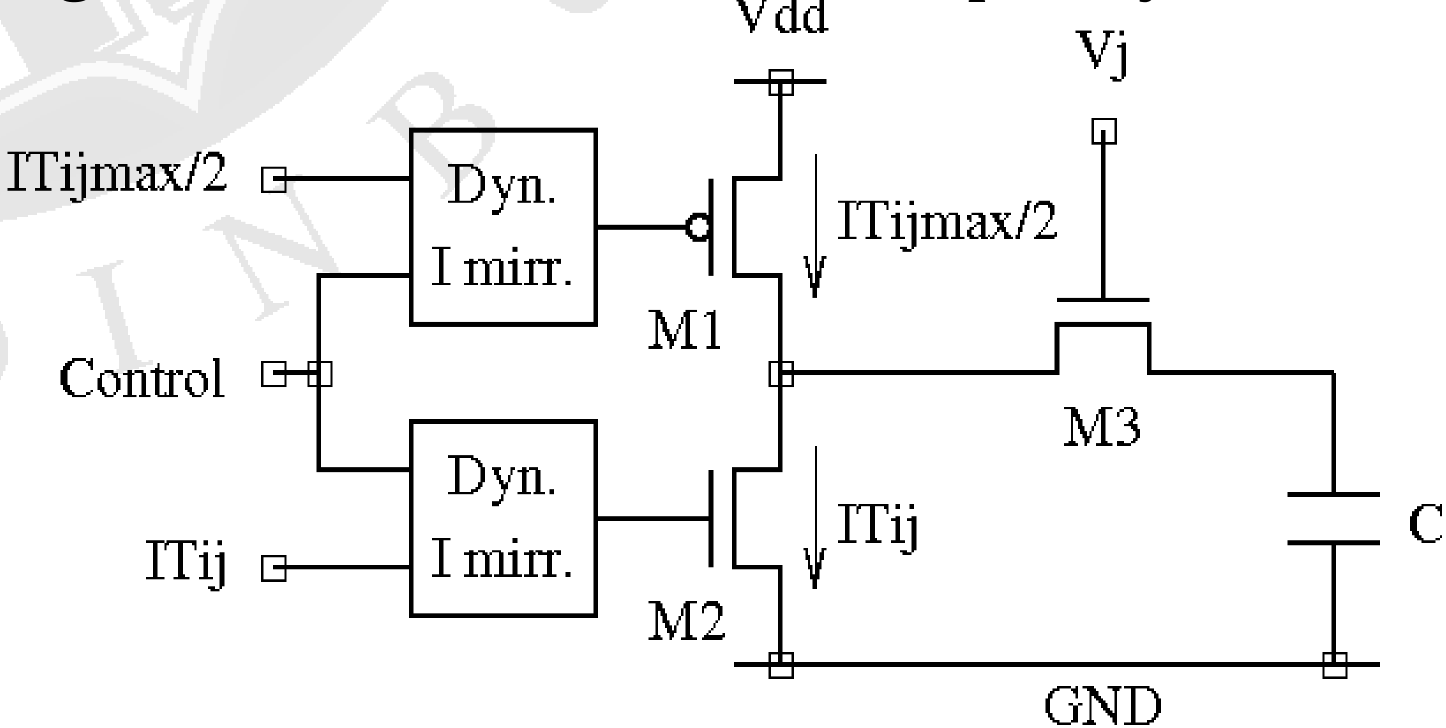


Generalisation performance

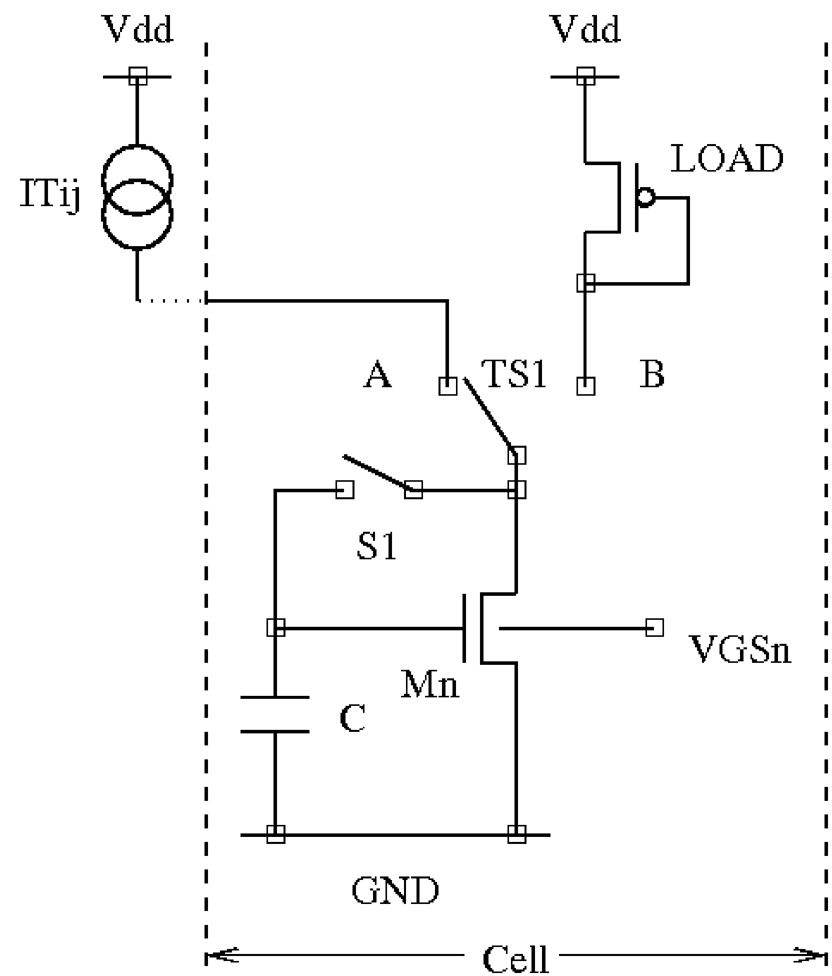
- EPSILON chip
  - 65%
- Workstation trained on the same data and seeded with 20 random weight sets achieved
  - Minimum 48%
  - Maximum 68%
  - Mean 58%
- EPSILON comparable with workstation performance on this simple test

Variations on a theme

- Simpler more "***portable***" synapse
  - easier to port between projects and processes
  - larger circuit, but ***much*** less complexity



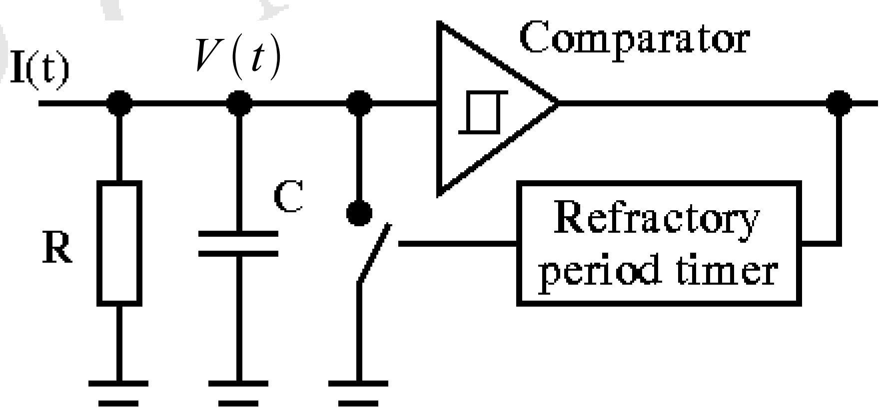
The dynamic current mirror

- Allows currents to be matched across large synaptic arrays.
- Synaptic weights represented by currents derived from simple on-chip current digital to analogue converter.
- 

Integrate & Fire Neurons in Auditory Systems

Information encoded in time (#2)

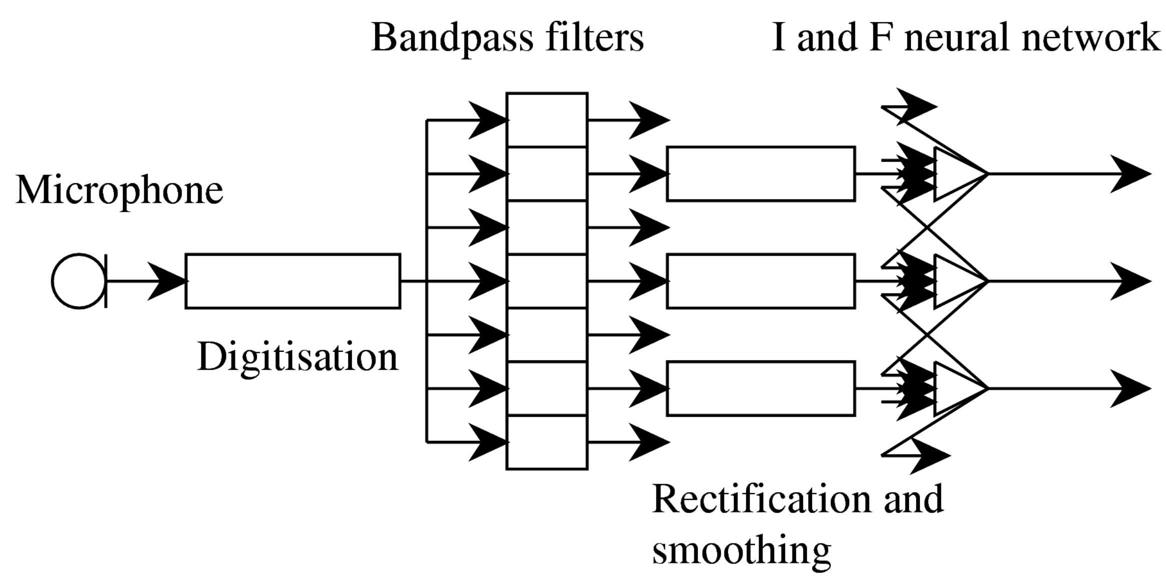
- EPSILON neuron model makes use of time but neuron model is simplistic
- Integrate and Fire neuron model is a step nearer the biological neuron
  - Leaky integration of input current, neuron spikes once threshold reached



$$\frac{dV(t)}{dt} = \frac{V(t)}{RC} + \frac{I(t)}{C}$$

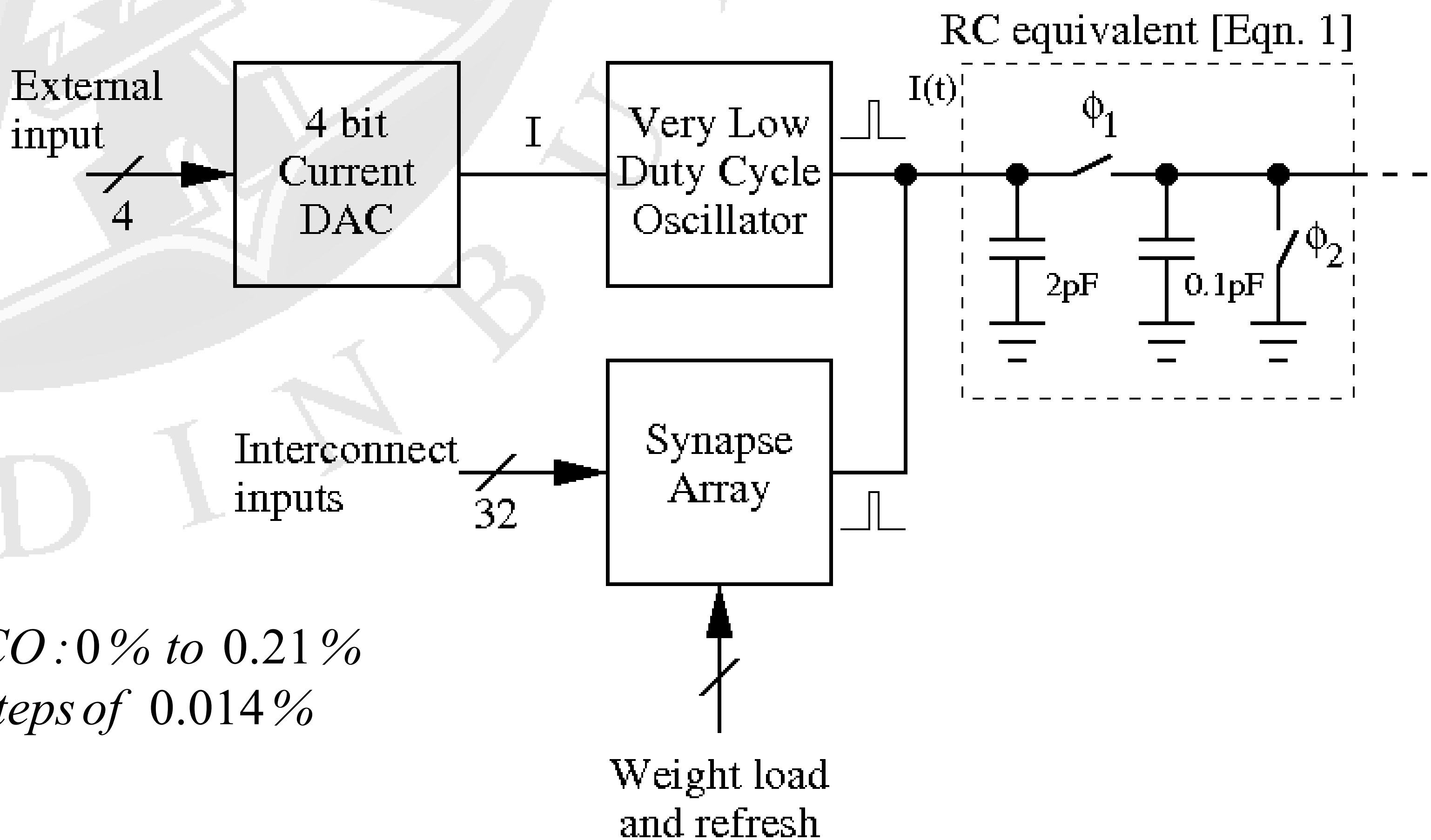
Sound Segmentation

- Integrate and Fire neurons useful for processing signals that vary with time
- Analogue VLSI of an integrate and fire system to detect onsets and offsets in speech
- Sound segments
  - 20-200 mS range
  - slow c.f. aVLSI
- Lateral inteconnect



Slowing down the I&F neuron

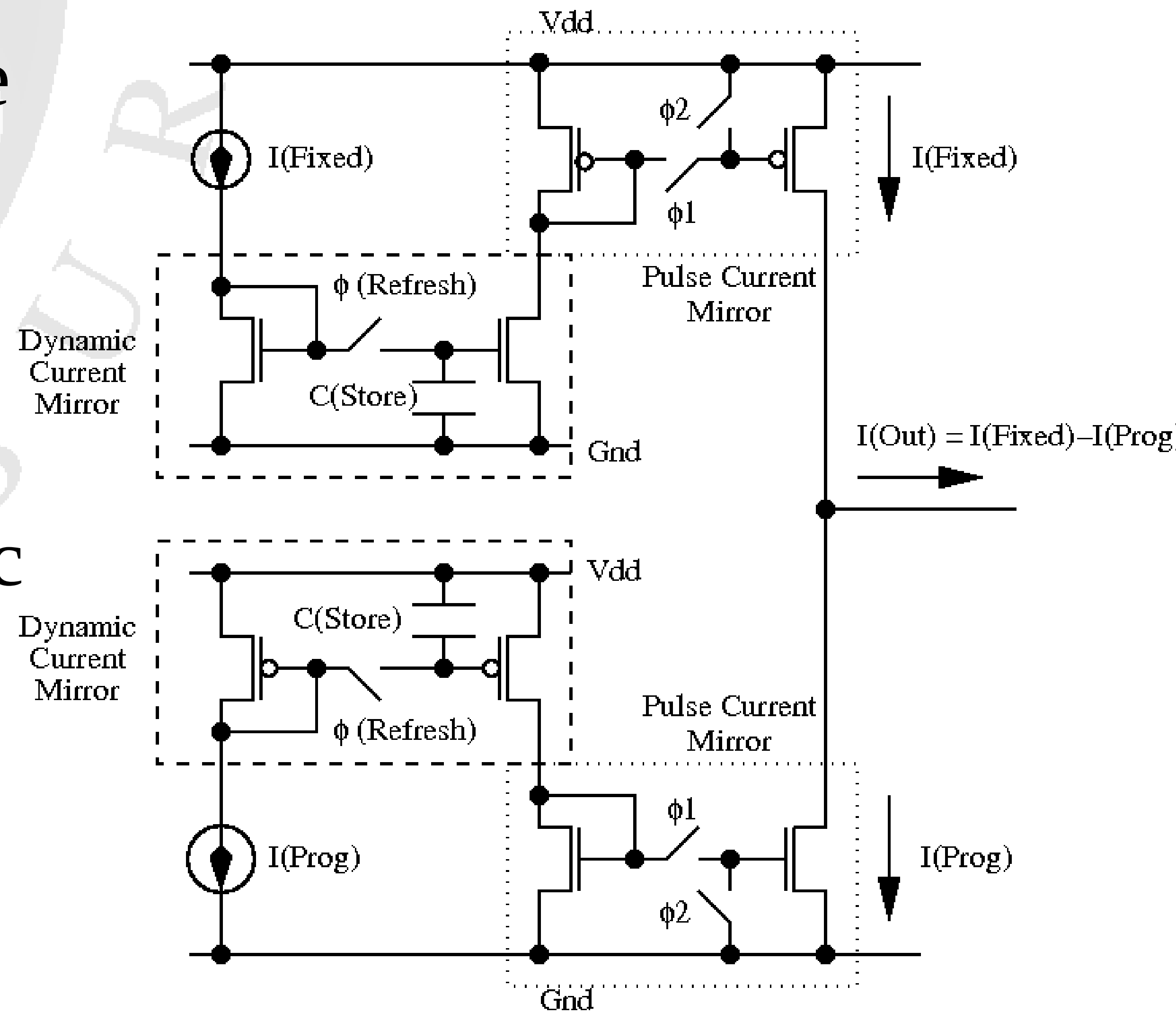
- I&F neuron input stage



$$VLDCO: 0\% \ to \ 0.21\%$$
$$in\ steps\ of\ \ 0.014\%$$

Synapse implementation

- Presynaptic spike
  - Closes ϕ_1
  - Opens ϕ_2
- On-chip DAC refreshes synaptic weight



Envelope of hand claps sound

Software onset volleys

Hardware onset volleys

High freq.
32 neurons
Low freq.

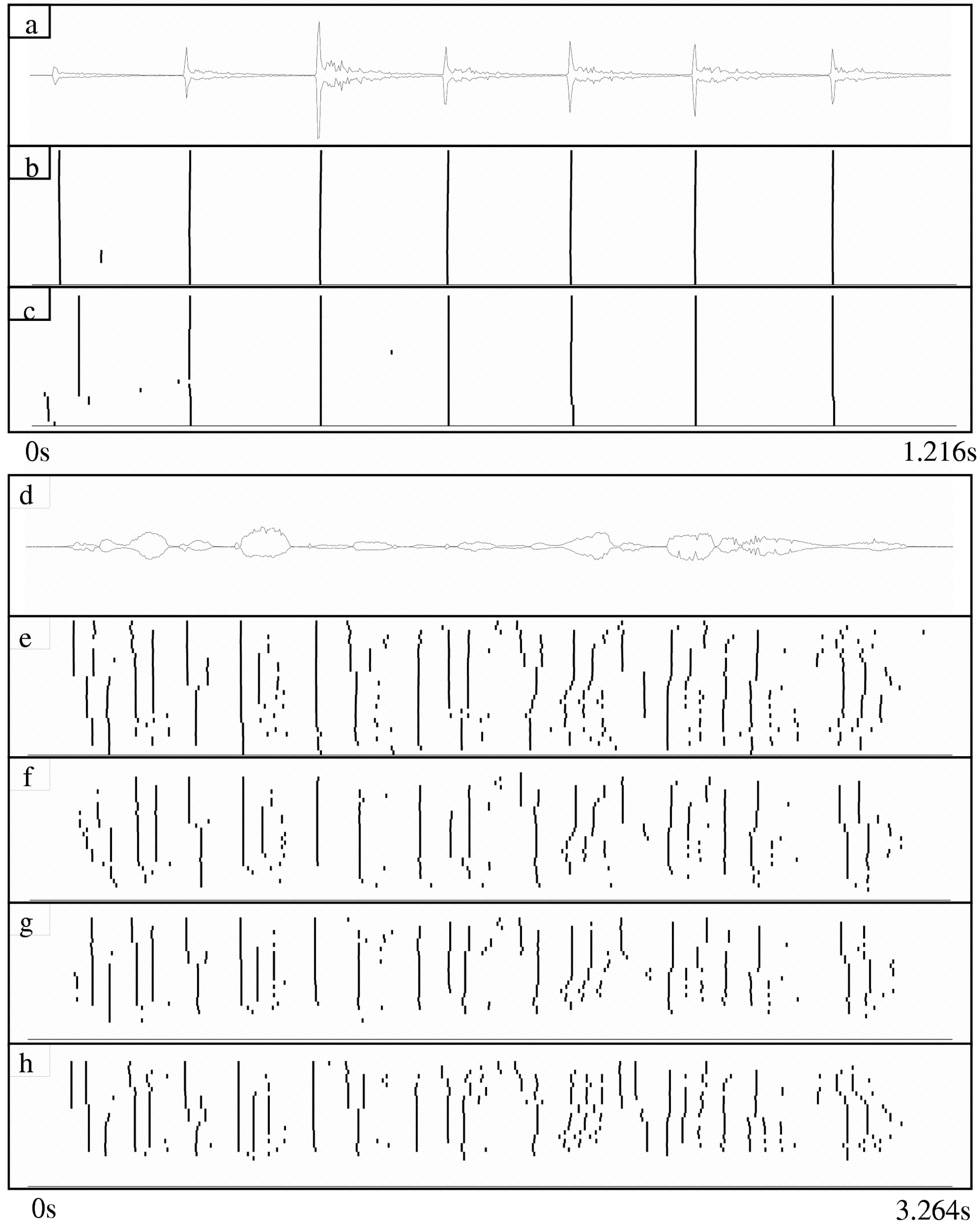
Envelope of TIMIT vowel utterance

Software onset volleys — *dissipation 50*

Hardware onset volleys — *dissipation 15, i/p 0.25*

Hardware onset volleys — *dissipation 50, i/p 0.5*

Hardware onset volleys — *dissipation 150, i/p 1.0*



Clap sounds: zooming in

- 50 mS of results from the I&F network in aVLSI
  - A: i/p = 0.25 FS, dissipation = 10; B: i/p = 0.5 FS, dissipation = 20; C: i/p = 1.0 FS, dissipation = 40

Adaptive Neuromorphic Olfaction Chip

Information encoded in time (#3)

- Integrate and Fire neuron model is a step nearer the biological neuron
  - Leaky integration of input current, neuron spikes once threshold reached
- But synapse model used so far takes no account of the time of occurrence of pre- or post-synaptic neural firing
  - several models exist of time dependent synapses

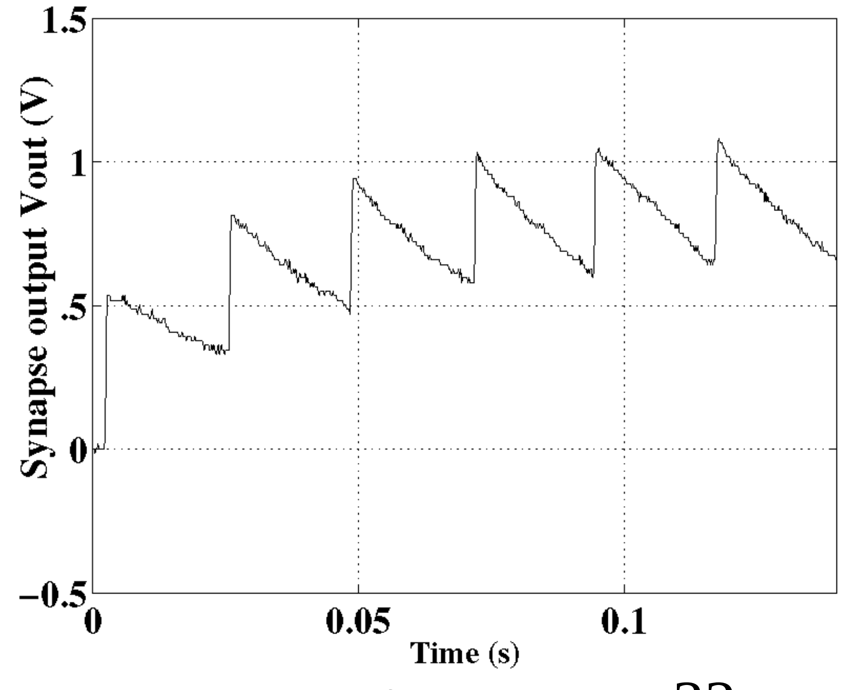
Time dependent synapse function

- The ***exponential summing*** synapse

$$i_{BA}(t) = \Theta(t)\,\omega_{BA}\,e^{\frac{-t}{\tau_d}}$$

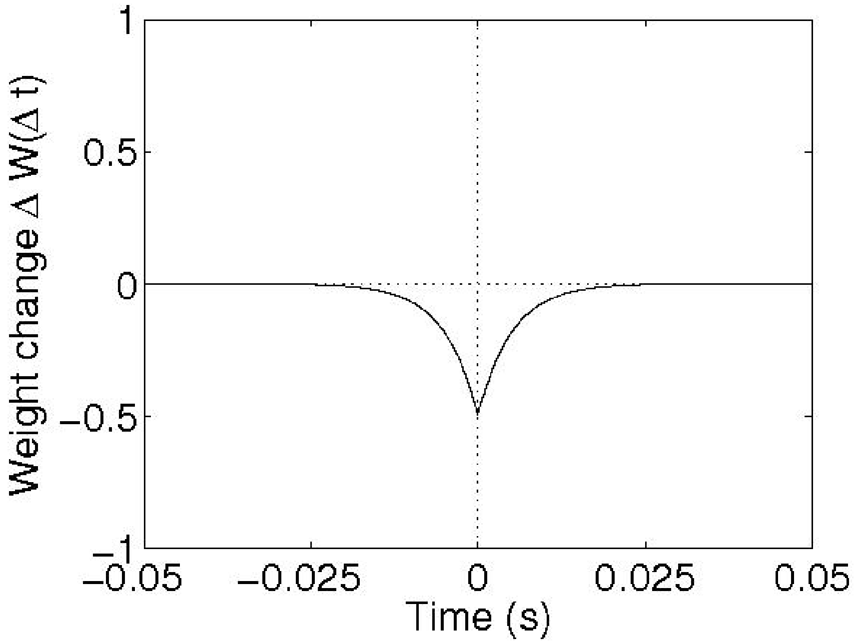
$$I_{BA}(t) = \sum_n i_{BA}(t - t_n)$$

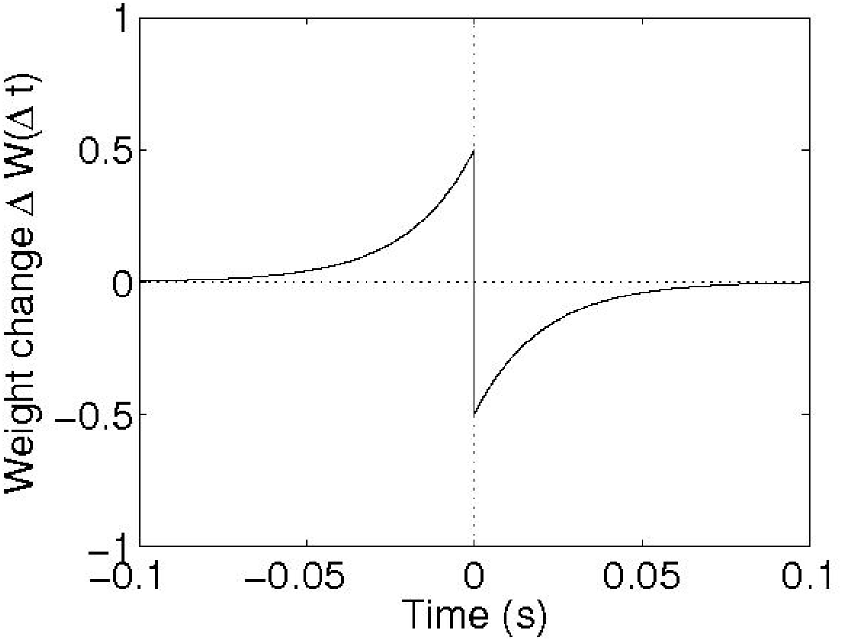
- Synapse output
  - Pre-synaptic spike event period = 23mS, V_{wt} = 500mV.



Spike time dependent weight adaption

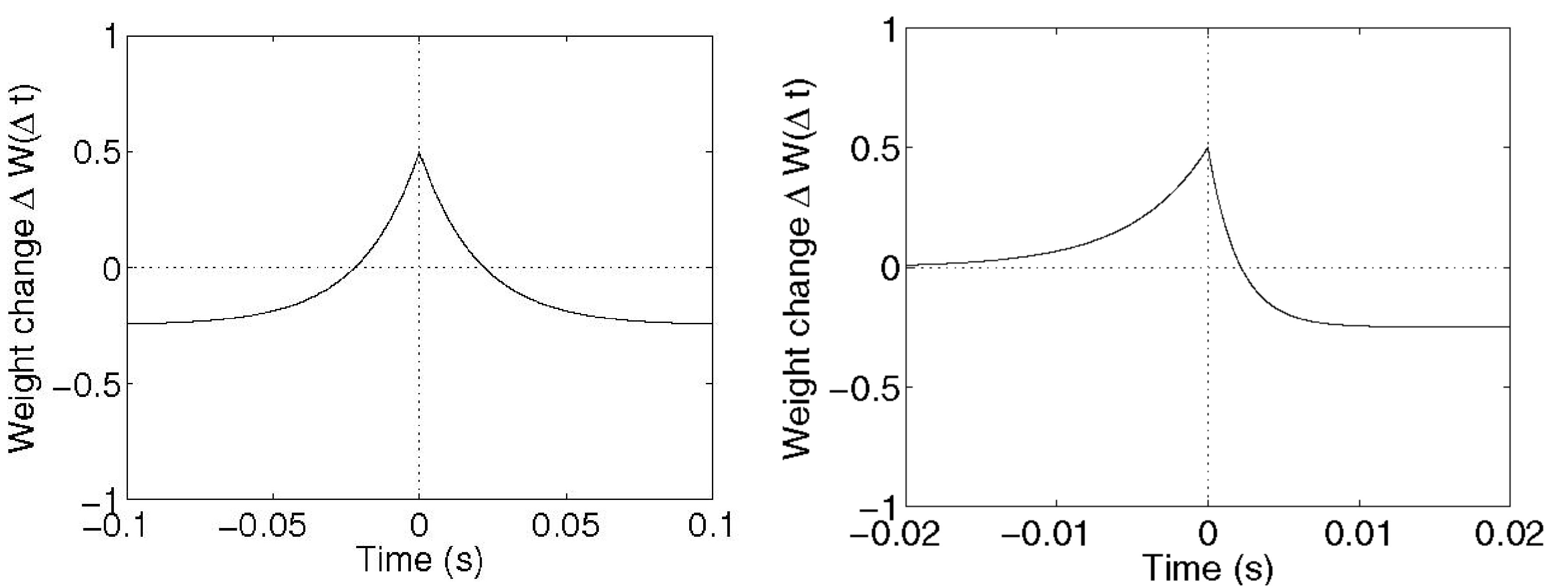
- Egger et al. 1999
- Song et al. 2000
  - Synaptic weight change based on ***pre*** and ***post*** synaptic ***spike time correlation***





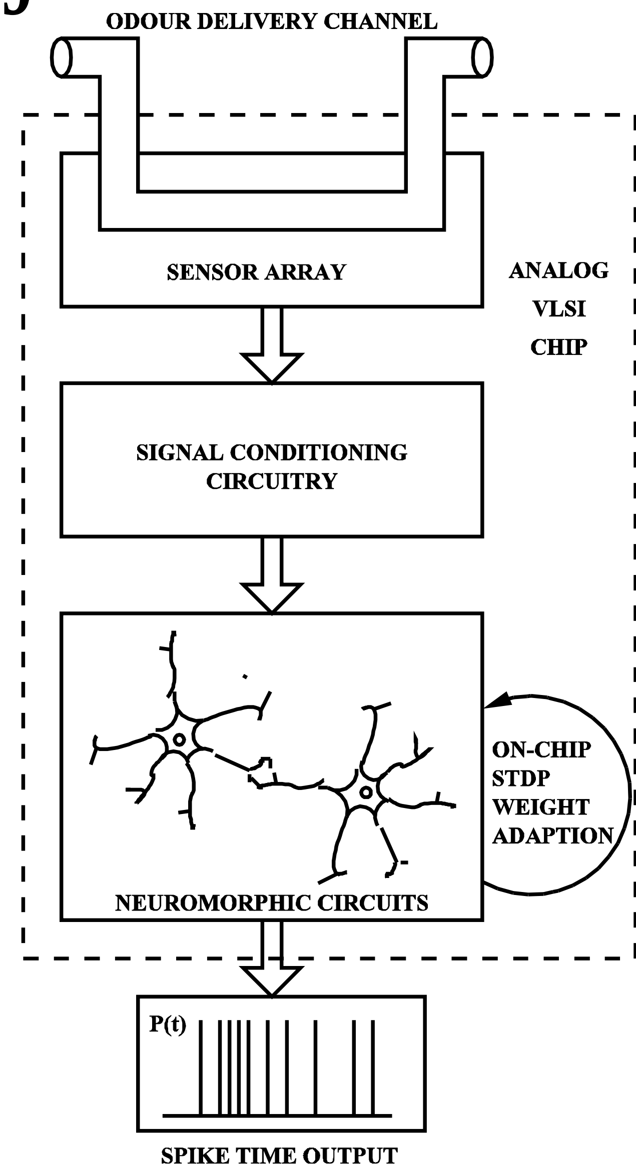
Spike time dependent weight adaption

- Dan et al. 1992
- Gerstner et al. 1996
  - Synaptic weight change based on ***pre*** and ***post*** synaptic ***spike time correlation***



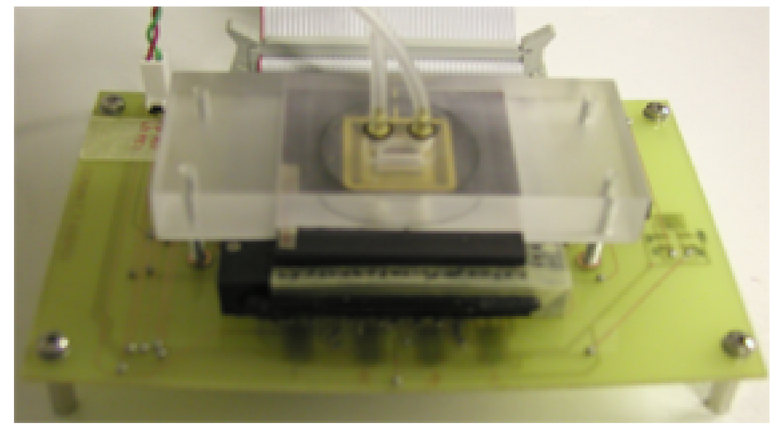
Electronic nose project

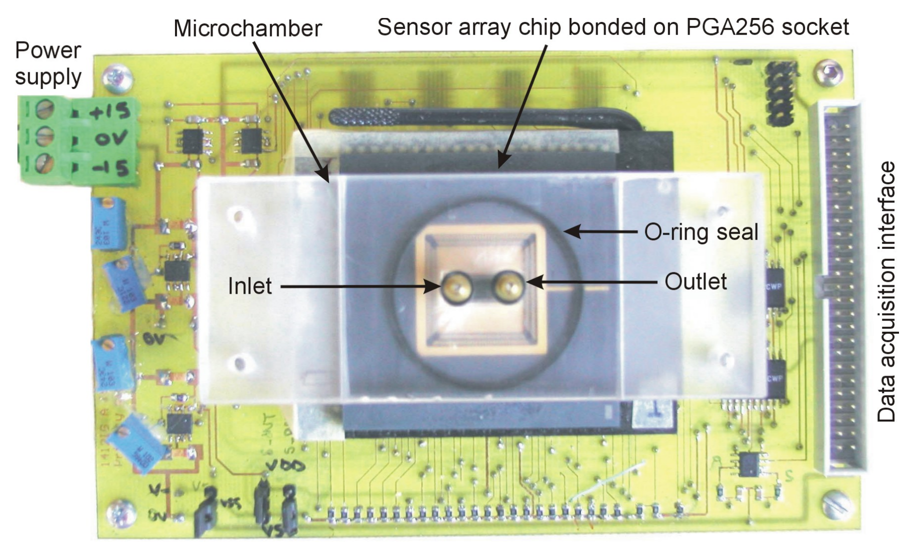
- Integration of
  - odour delivery mechanism
  - chemical sensor array + adaptive analogue interface
  - neuromorphic analogue VLSI
- Neuromorphic analogue VLSI
  - integrate and fire neurons
  - exponential summing synapses with weight adaption



Odour delivery & adaptive interface

- Odour delivered via a ***micro-channel*** on top of chip.
- Micro-channel delivers odour to sensor array.
- Programmable current sources bias sensors.
- Set-up phase cancels sensor DC offsets.

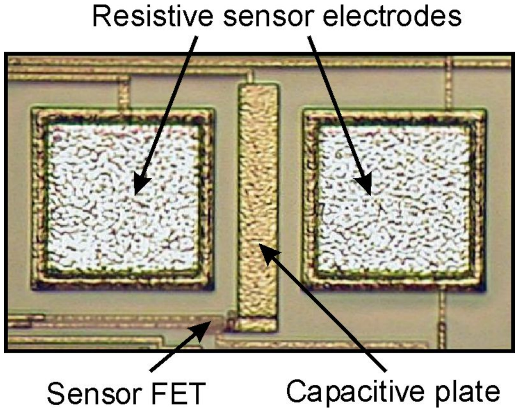


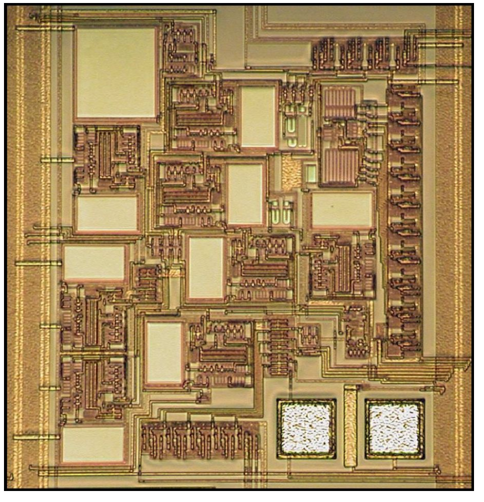


Sensor array interface PCB

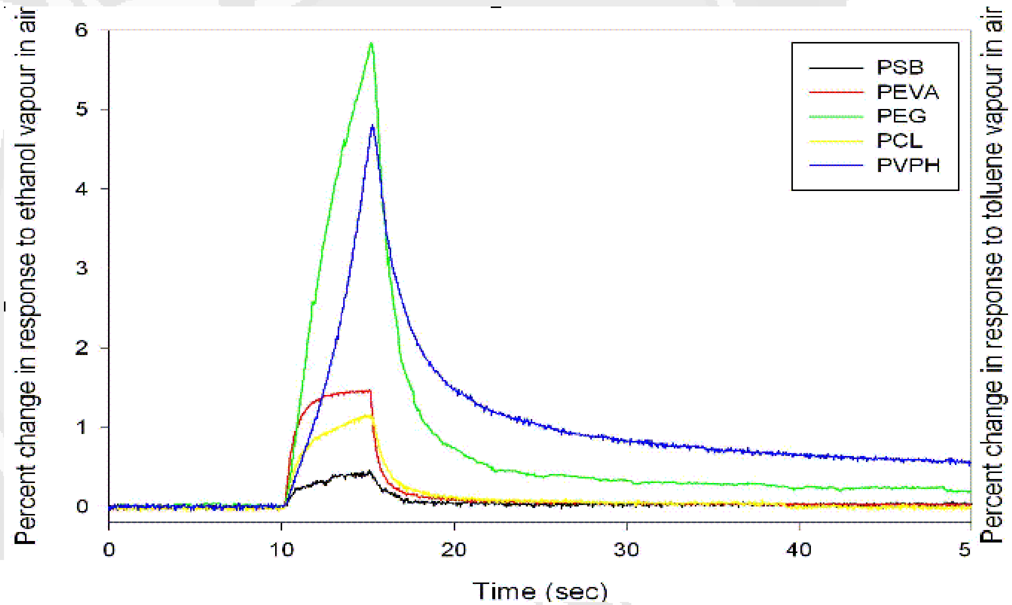
Odour sensors on chip

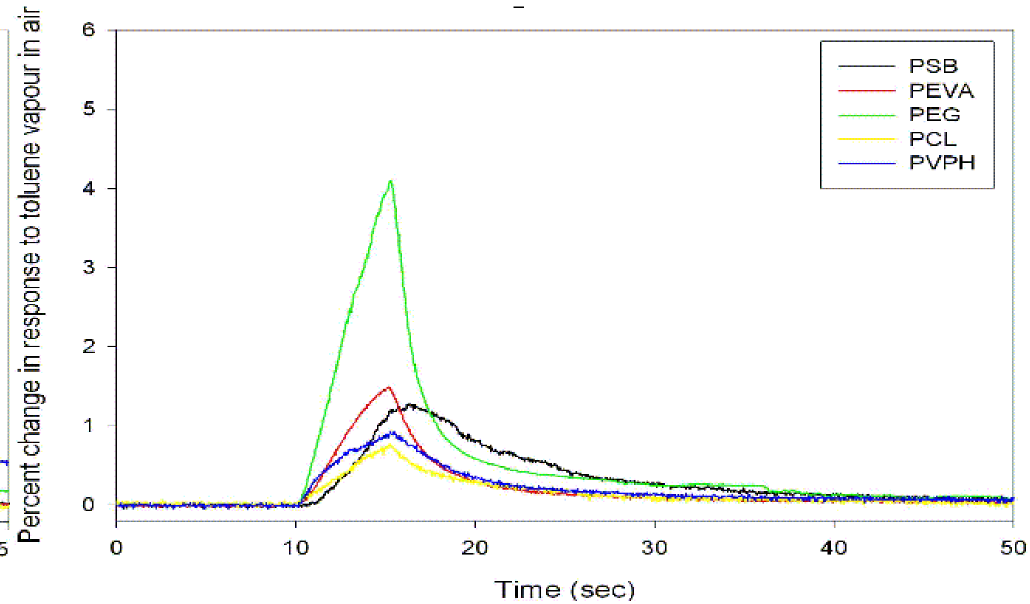
- ***Carbon black polymer materials*** deposited between two sensor electrodes.
- Exposure to gas causes sensor material to ***swell*** increasing resistance.
- Sensor embedded with adaptive analogue interface.





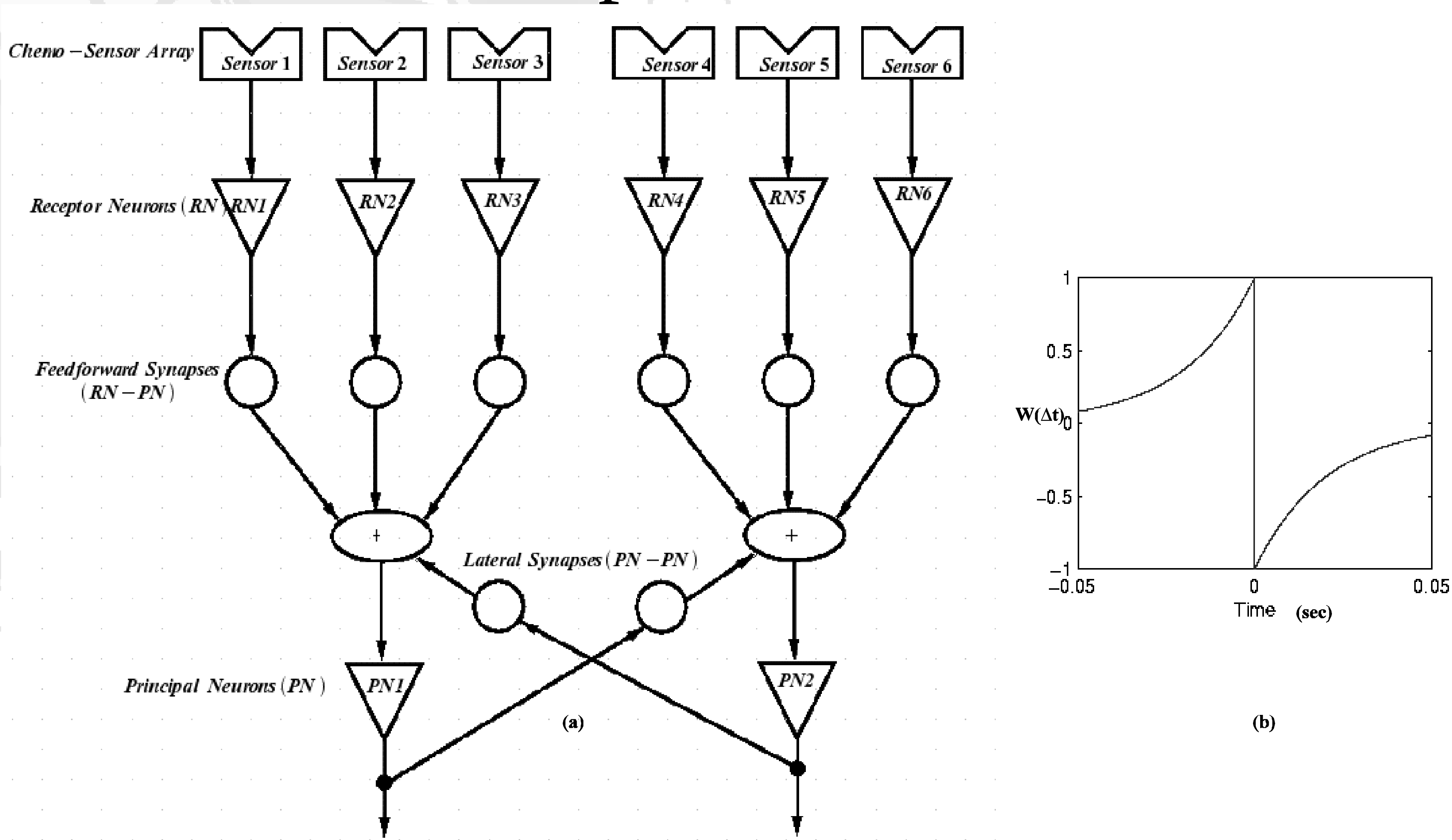
Odour sensor responses



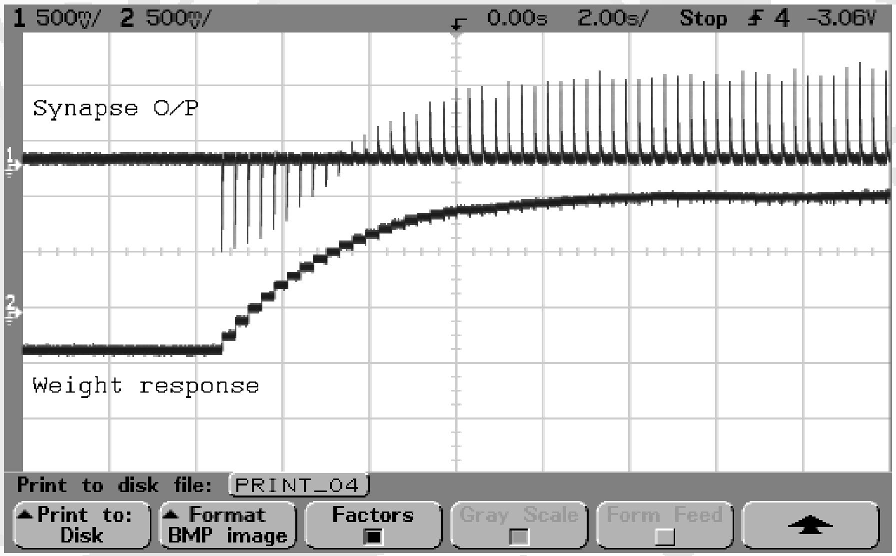


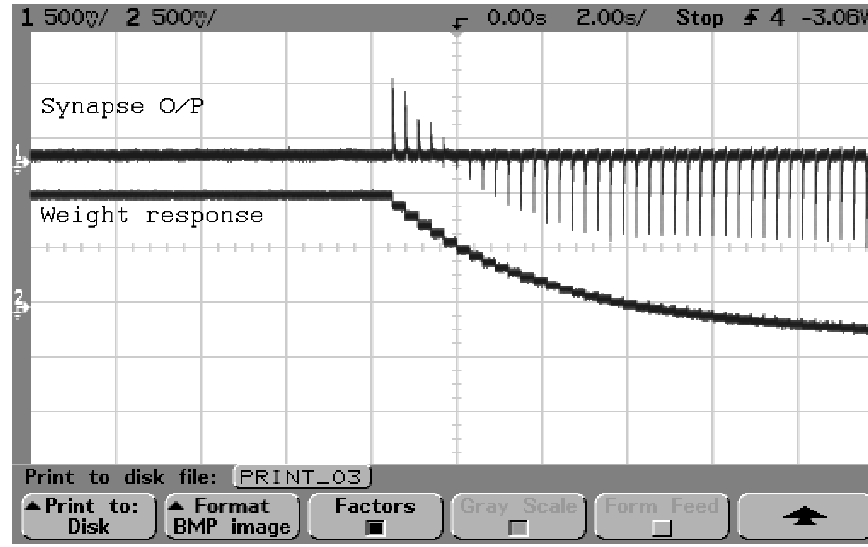
- Responses to ***ethanol*** and ***toluene*** vapour in air
- Sensor responses ***distinct*** to each analyte
- Neuromorphic circuits extract ***spatio-temporal*** information from odour sensor array

Neuromorphic architecture



On chip weight adaption

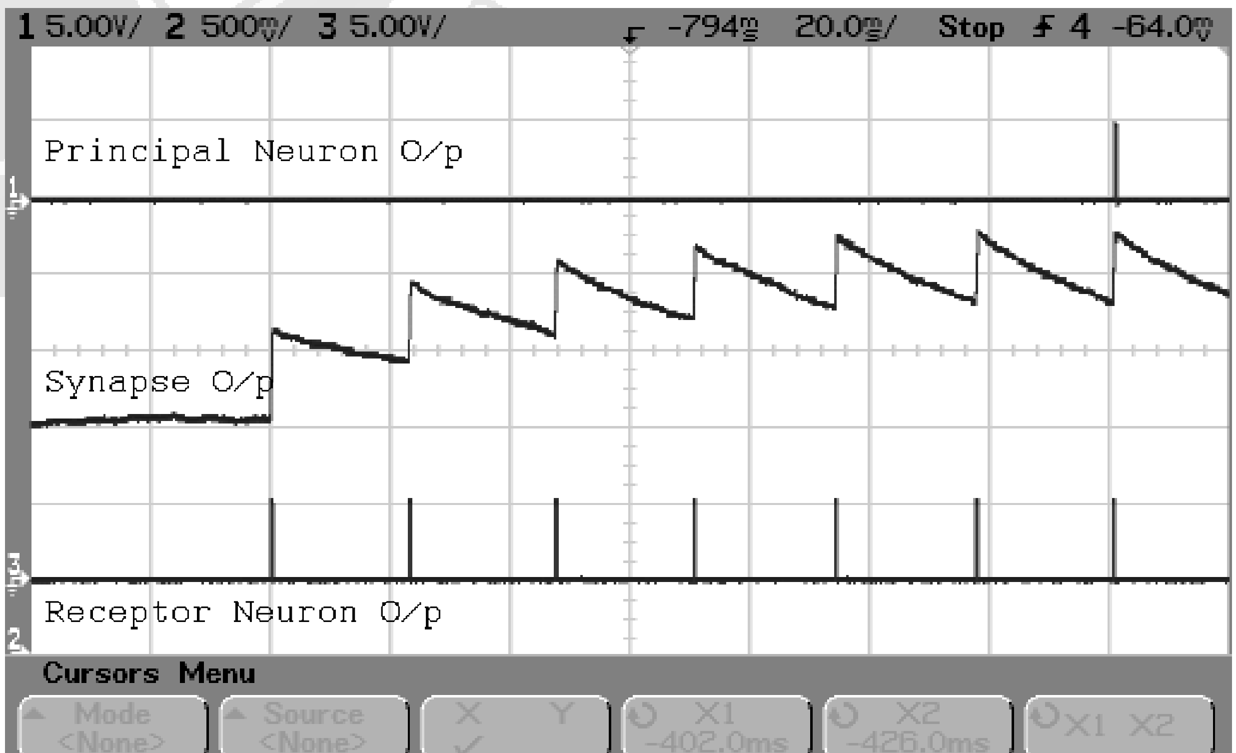




- Weight adaption due to pre-synaptic spikes ***preceeding*** post-synaptic spikes (***left*** traces)
- Weight adaption due to pre-synaptic spikes ***following*** post-synaptic spikes (***right*** traces)

Neuromorphic network response

- Principal neuron fires as a result of synchronous excitation by the receptor neurons.



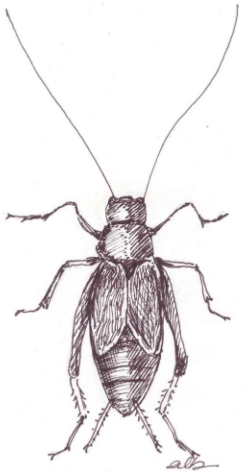
Neuromorphic Olfaction Chips

- Chip #1: Sensor array
  - 70 resistive sensors and offset cancellation interface
- Chip #2: Neuromorphic circuits
  - 3 receptor neurons, 27 synapses and 1 principal neuron; learning off-chip
- Chip #3: Adaptive neuromophic olfaction chip
  - On-chip chemosensor array, on-chip sensor interface and neuromorphic olfactory circuits with on-chip STDP learning.

Adaptive Neuromorphic Olfaction Chip: Performance Summary

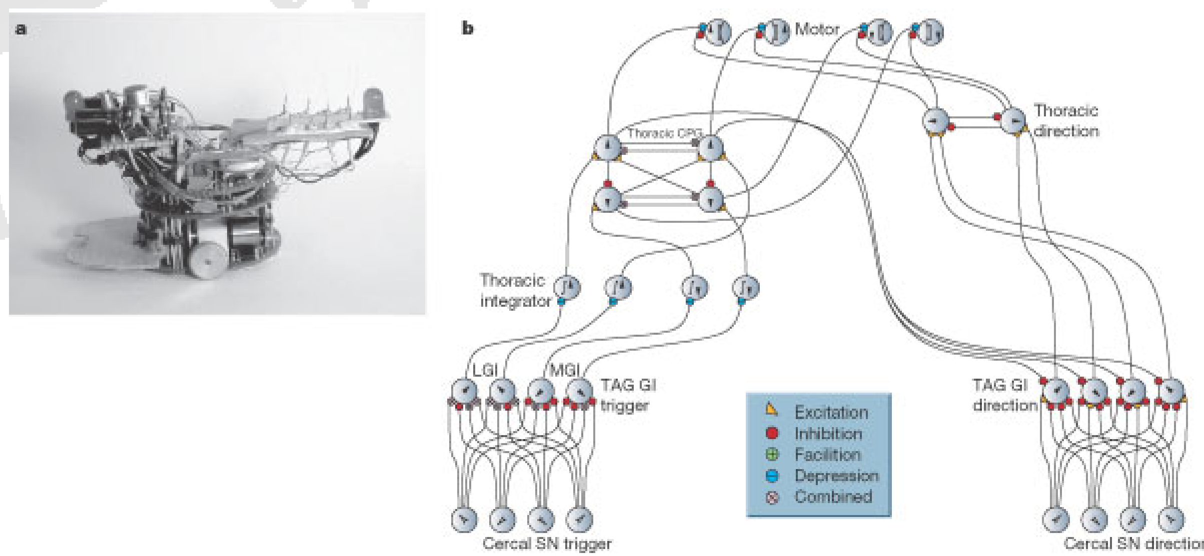
Parameter	**Values**
Supply Voltage	5V
Area	6.5mm^2
Sensor Resistance	10 kΩ – 200 KΩ
Sensor driving current	1 µA, 10 µA, 100 µA
Sensor bandwidth	< 1 Hz
Sensor DC baseline variation	± 1 V
Input referred DC offset	< ±5 mV
Prog. Amplifier gains	10, 10, 1000
Synaptic time constant	10 ms – 300 ms
Weight range	± 1 V
Neuron time constant	10 ms – 300 ms
Neuron spike width	10 µs – 1 ms
Neuron refractory time period	10 ms – 300 ms

Cricket Hair Wind Sensor

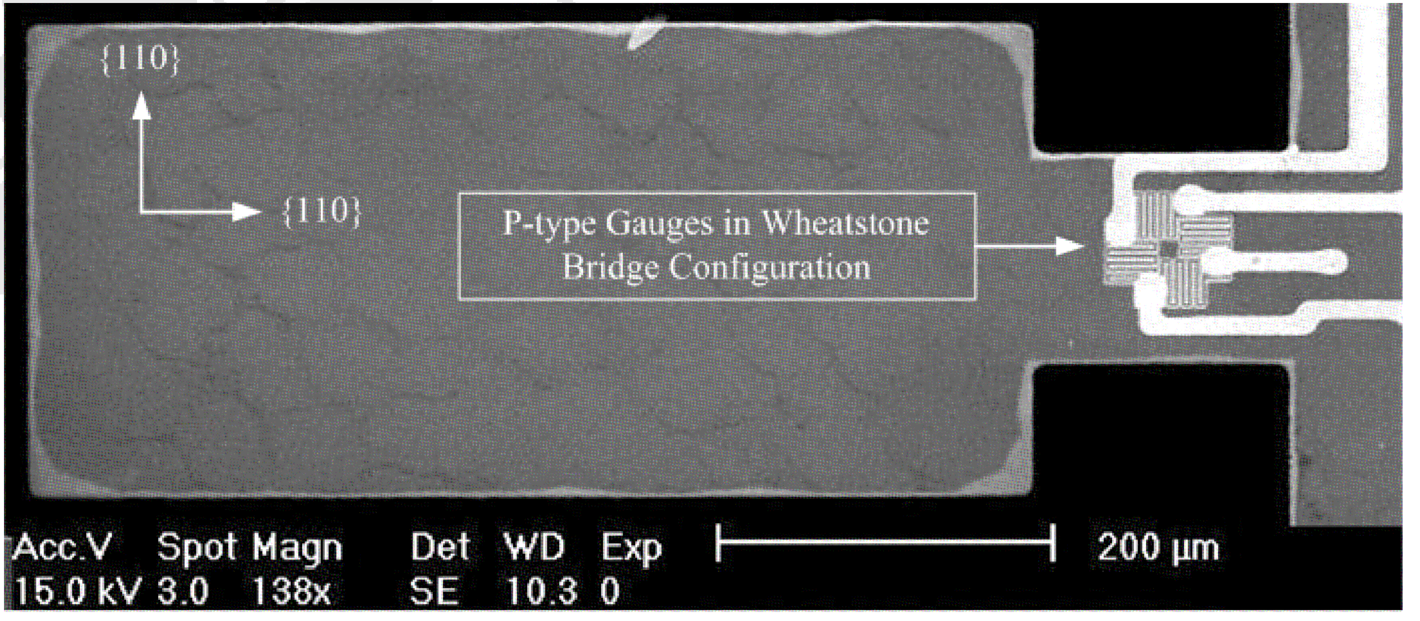


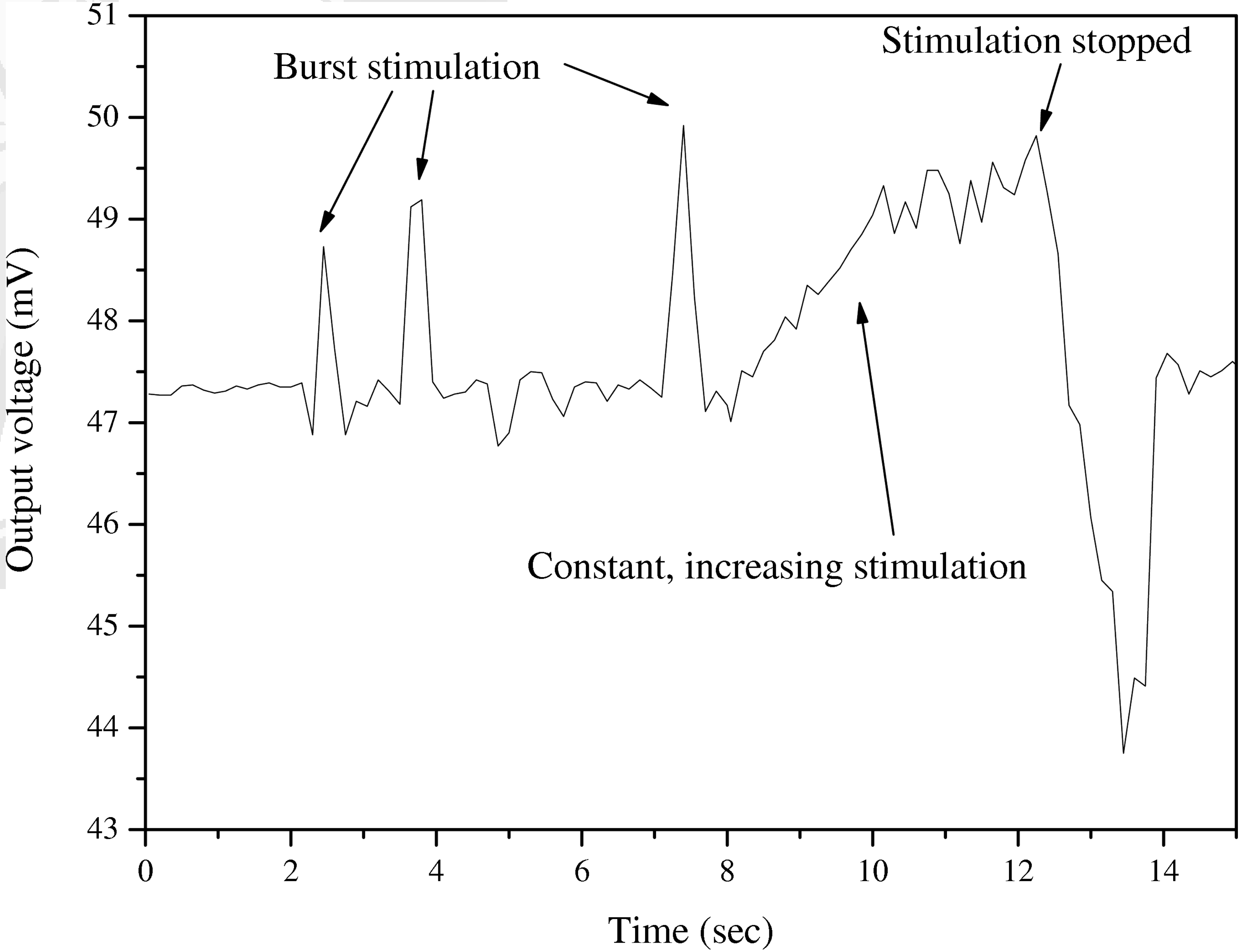
Robot Crickets

- Robot modeling of a cricket's escape response
  - Robot with artificial cercal wind sensors and neural model for escape response
  - Can we use MEMS to make wind sensors?



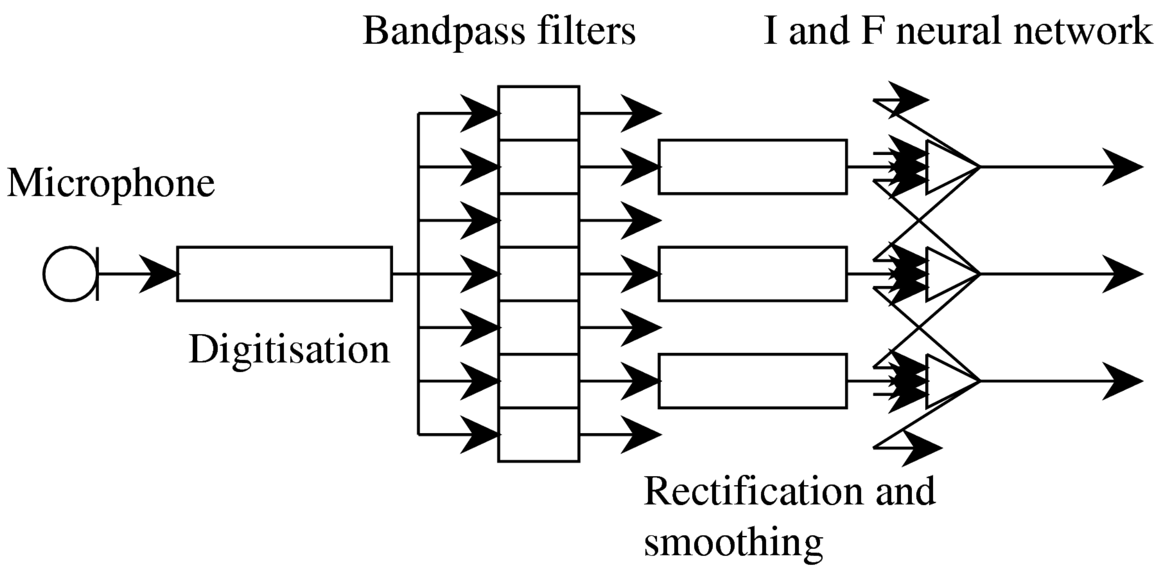
MEMS wind sensor

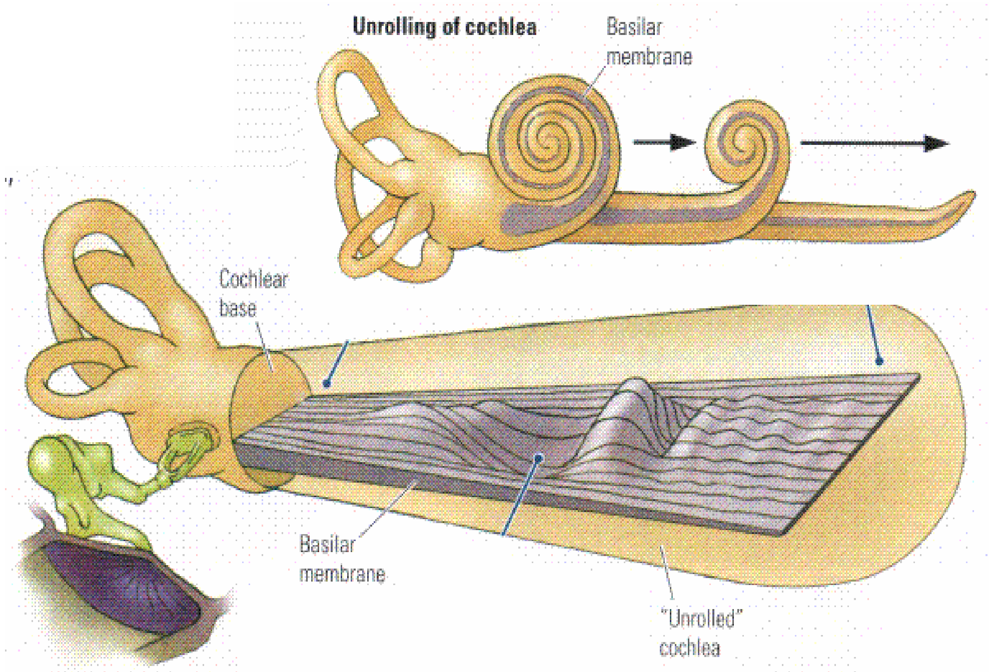



Burst stimulation
Stimulation stopped
Constant, increasing stimulation
Output voltage (mV)
Time (sec)
51
50
49
48
47
46
45
44
43
0
2
4
6
8
10
12
14

MEMS/CMOS microphone

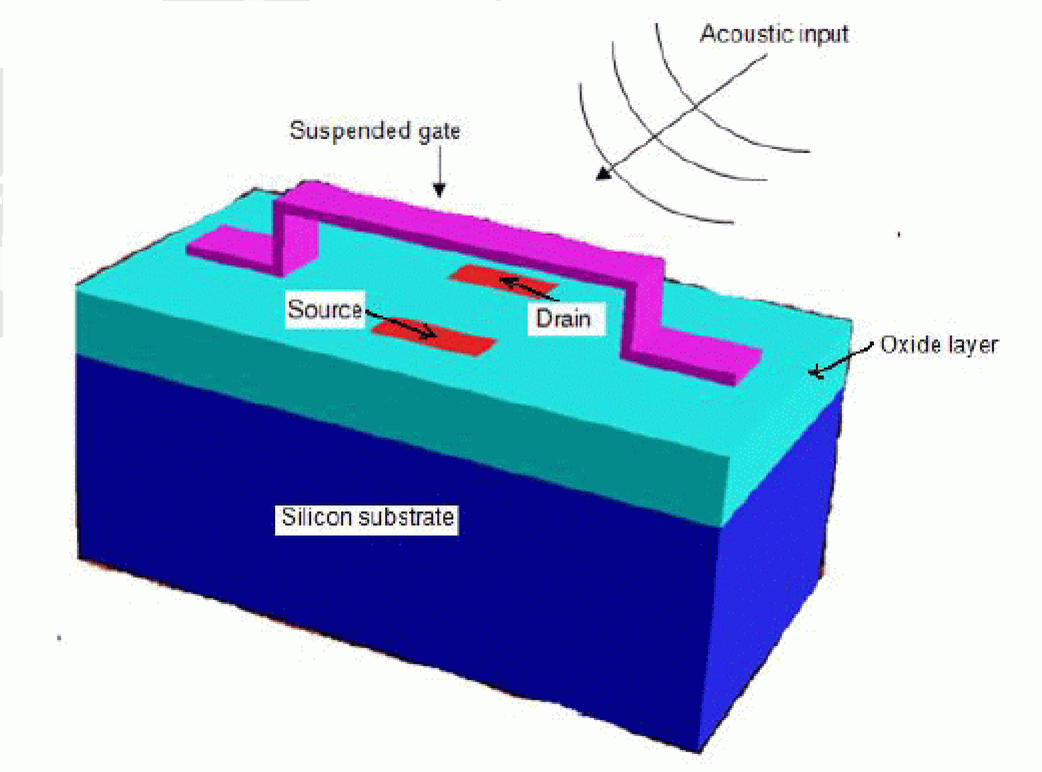
Implement bandpass filters in MEMS





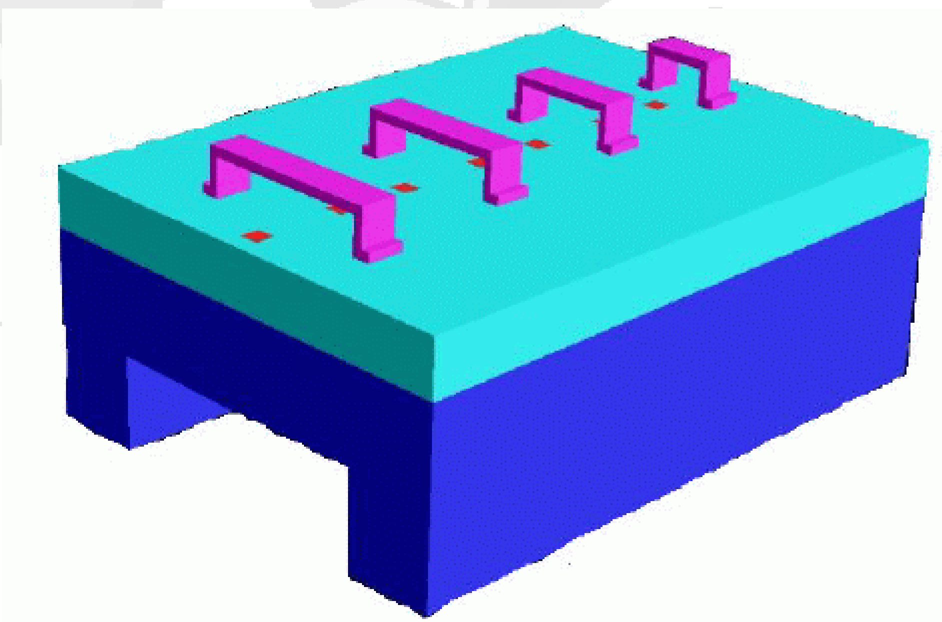
Resonant Gate Transistor (RGT)

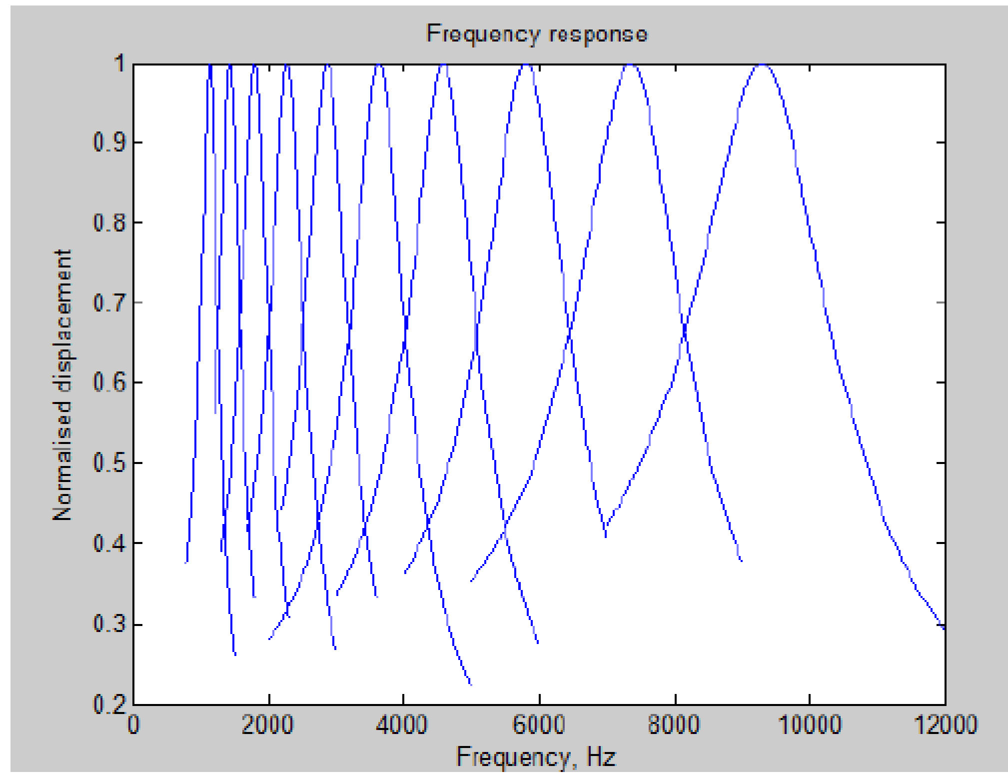
- Acts as a transducer for incoming acoustic signal



Array of RGTs

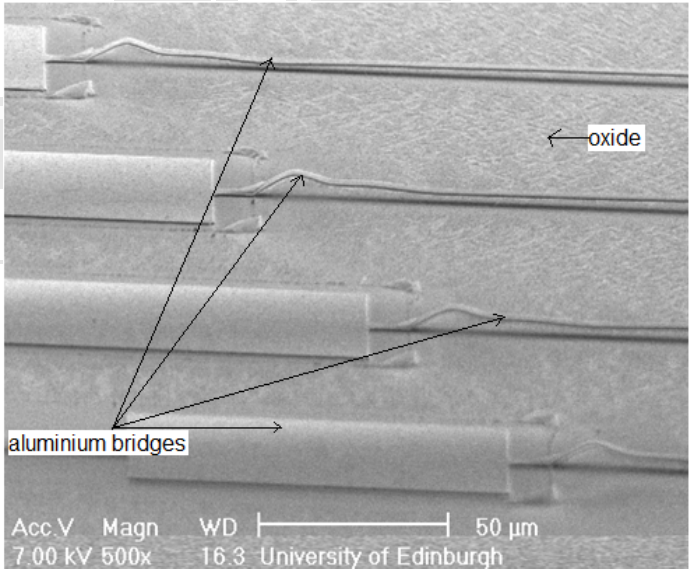
- Array of RGTs implement audio bandpass filters
  - Adaptive gain can be implemented by controlling gate bias voltage



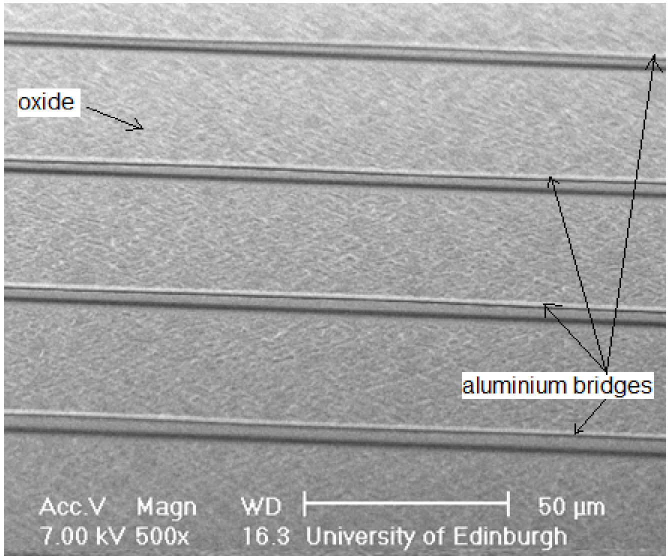


Manufactured MEMS bridges

- View at anchor of the bridge



- View at the middle of the bridge



Conclusion

- Neural and neuromorphic circuits presented process analogue signals in time.
  - Initially simply a convenience but increasingly
  - static neuron and synapse models give way to time dependent models
- Research focused on early neuromorphic signal processing
  - Olfaction, wind sensing and audition

Key references

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