Variability in Microprocessor Logic Design: Trends, Sources, Consequences, & Solutions

Keith A. Bowman
Circuit Research Lab, Intel

keith.a.bowman@intel.com

Acknowledgements:
Jim Tschanz, Vivek De, Tanay Karnik, and Steve Duvall

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UPC Seminar

Problem Statement:

- Variability is one of the primary challenges in the semiconductor industry
- Adversely impacts performance, power, yield, reliability, & time-to-market

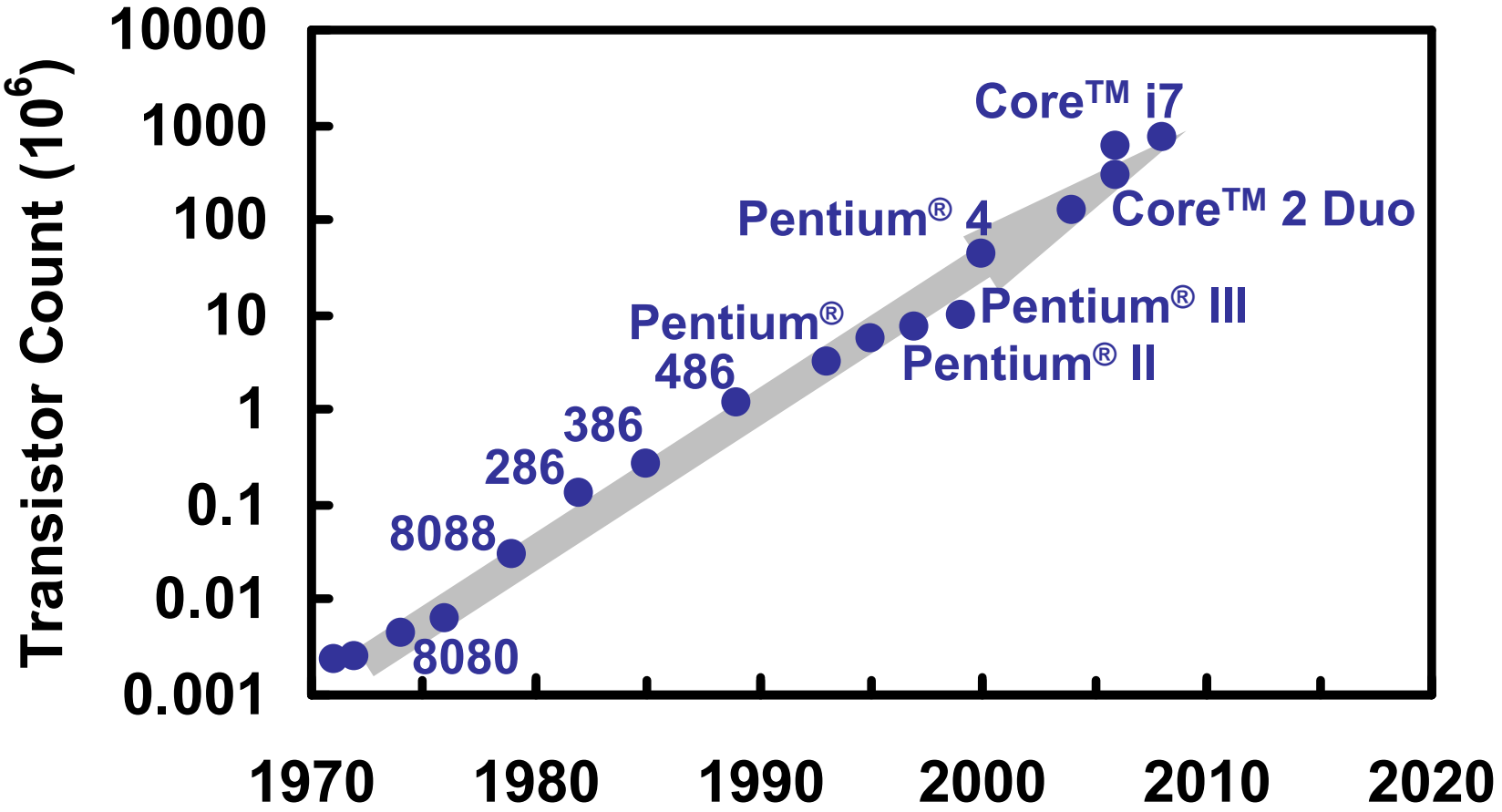
Focus Areas:

1) Impact of variations on logic design
2) Variation-tolerant circuits
3) Tomorrow: Resilient microprocessor design for dynamic variation tolerance

Outline

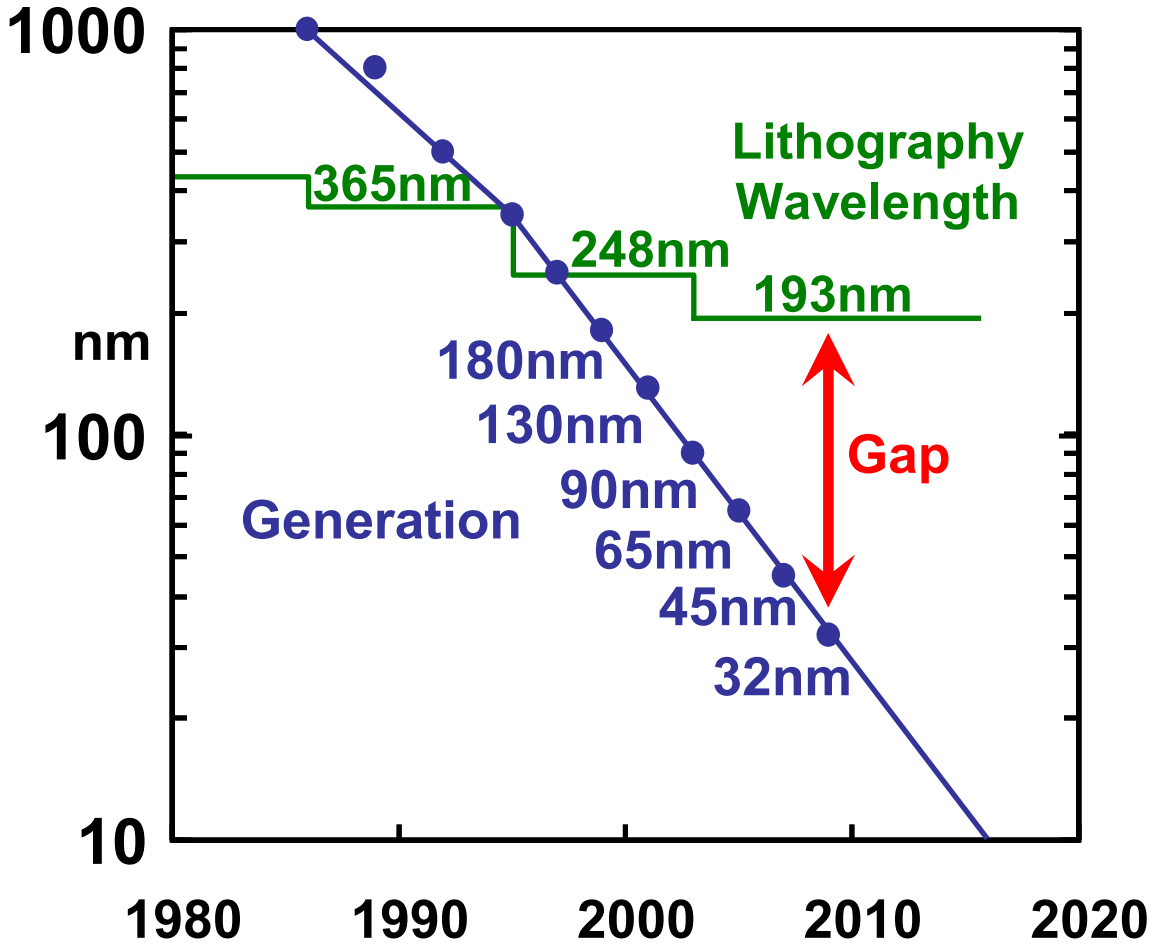
- Motivation & Technology Trends
- Sources of Variability
- Static Variations:
  - Impact on Logic Design
  - Variation-Tolerant Circuits
- Dynamic Variations:
  - Impact on Logic Design
  - Variation-Tolerant Circuits
- Summary

Moore's Law Continues…



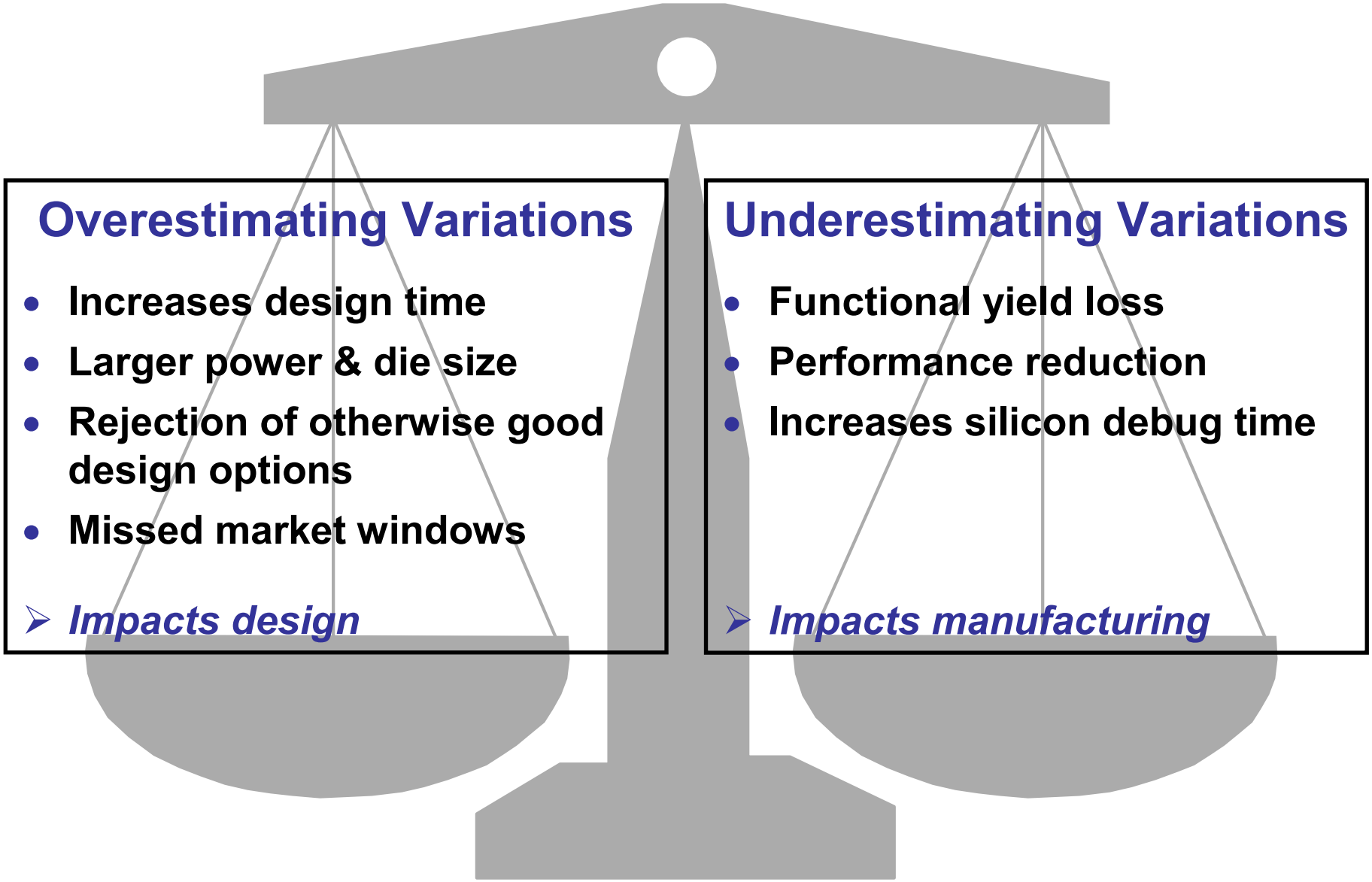
- ✓ Microprocessors with multi-billion transistors…
- ✓ Trillion instructions per second performance…
- ✓ Constant power envelope…
- ✓ Lower costs…

Challenge: Variations



- Gate length control is one of the "grand challenges" in the semiconductor industry – *ITRS, 2009*

Cost of Variations



Overestimating Variations

- Increases design time
- Larger power & die size
- Rejection of otherwise good design options
- Missed market windows

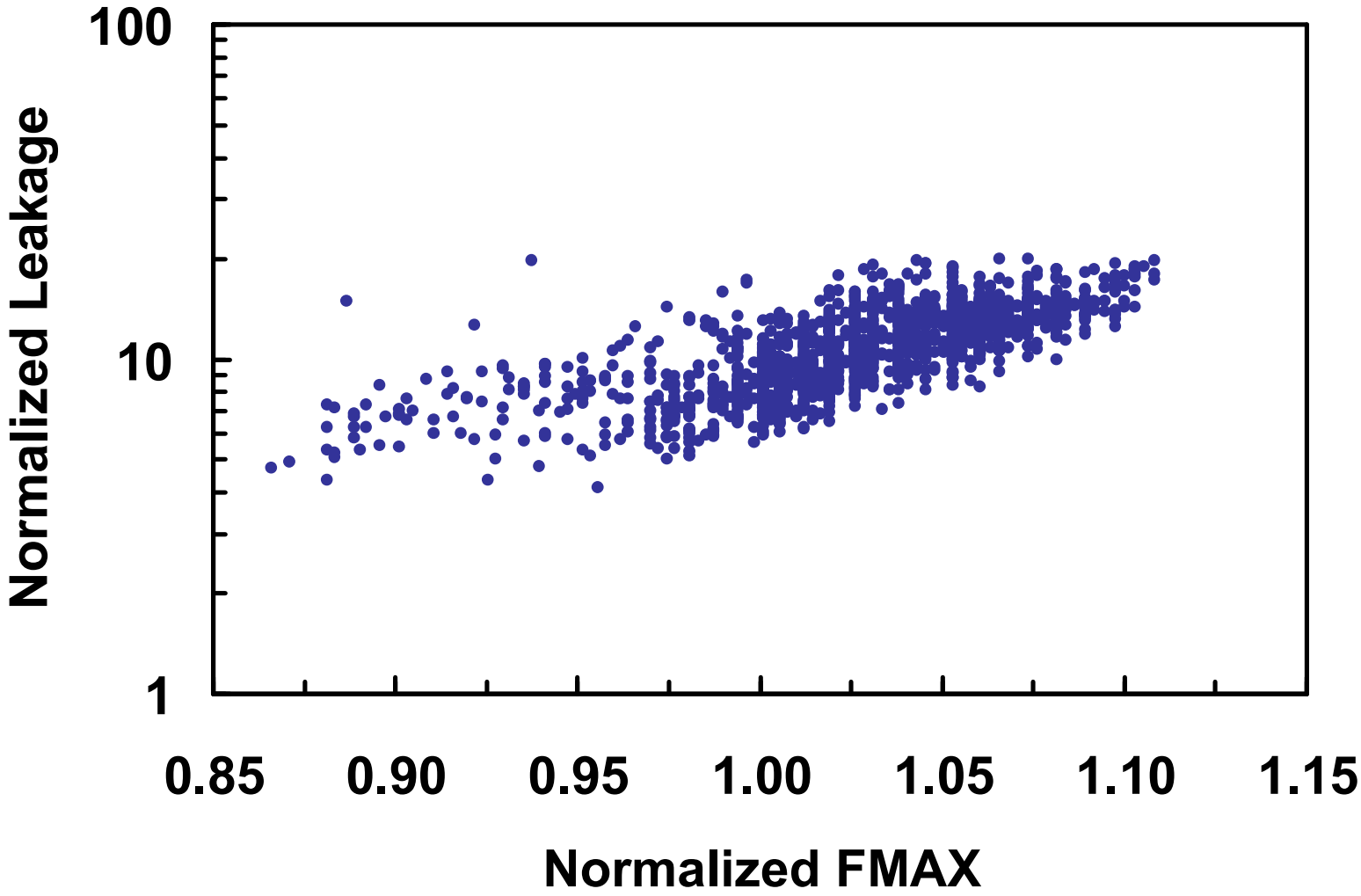
➢ *Impacts design*

Underestimating Variations

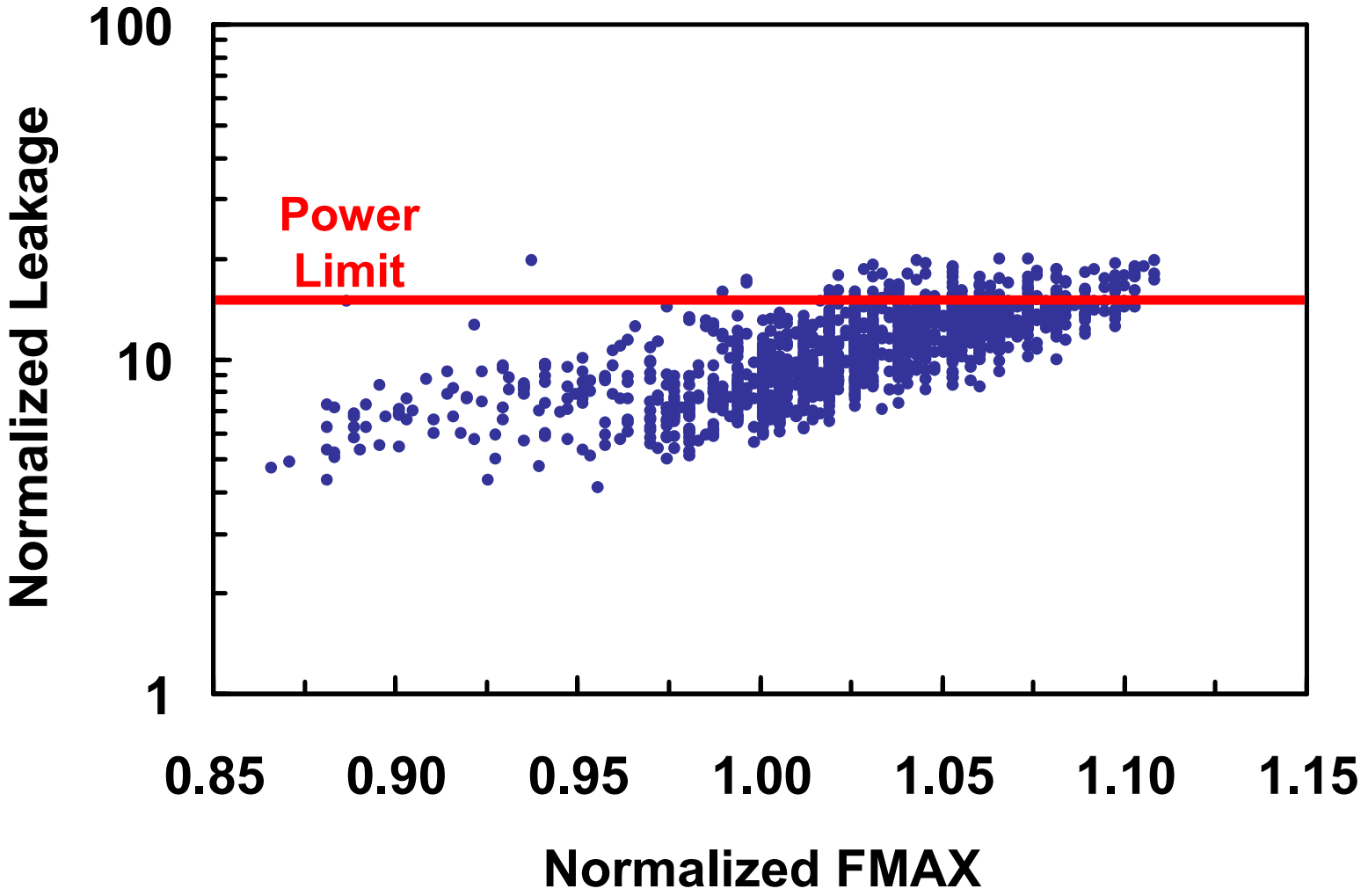
- Functional yield loss
- Performance reduction
- Increases silicon debug time

➢ *Impacts manufacturing*

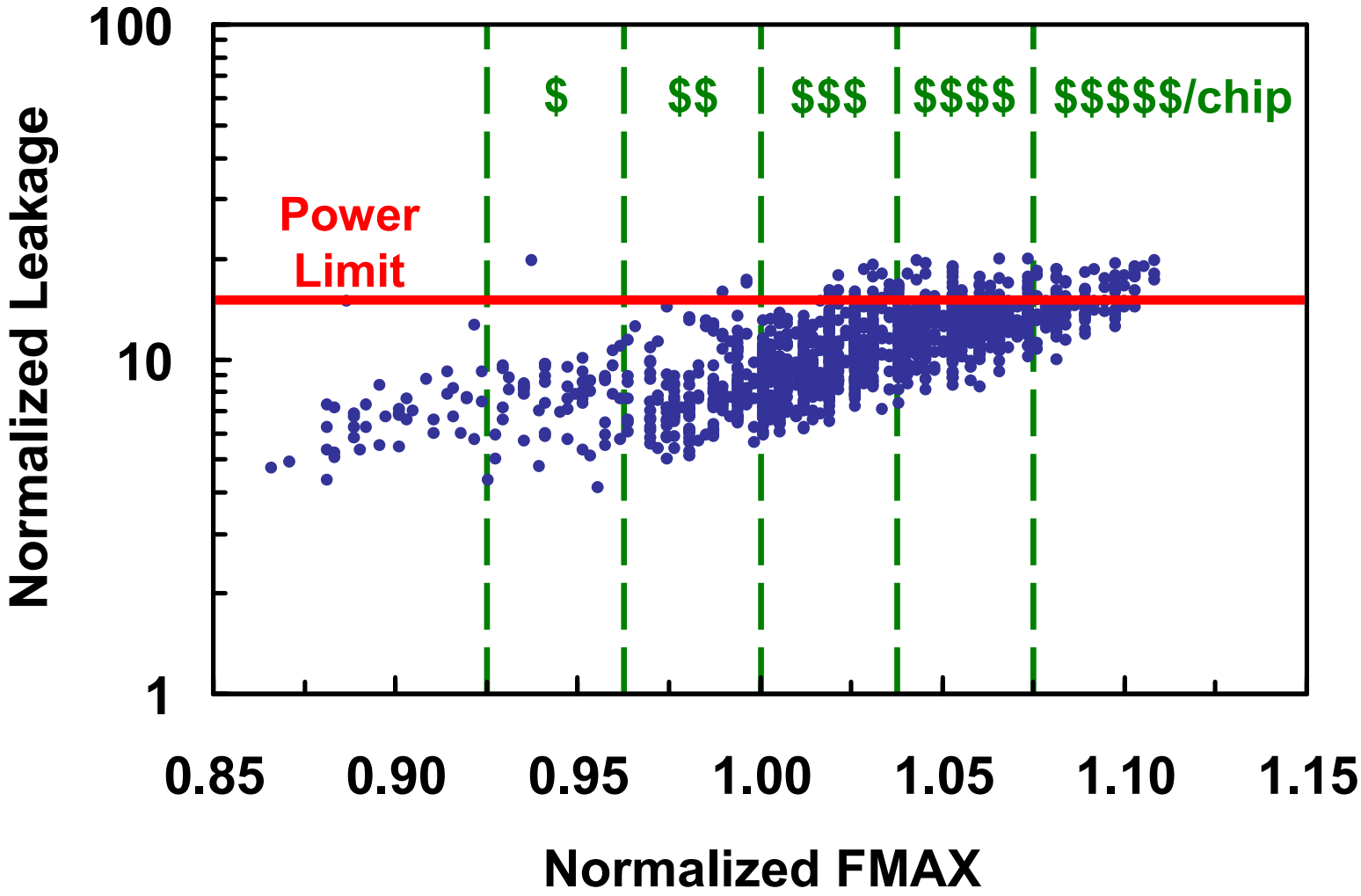
Impact of Variations on Revenue



Impact of Variations on Revenue



Impact of Variations on Revenue



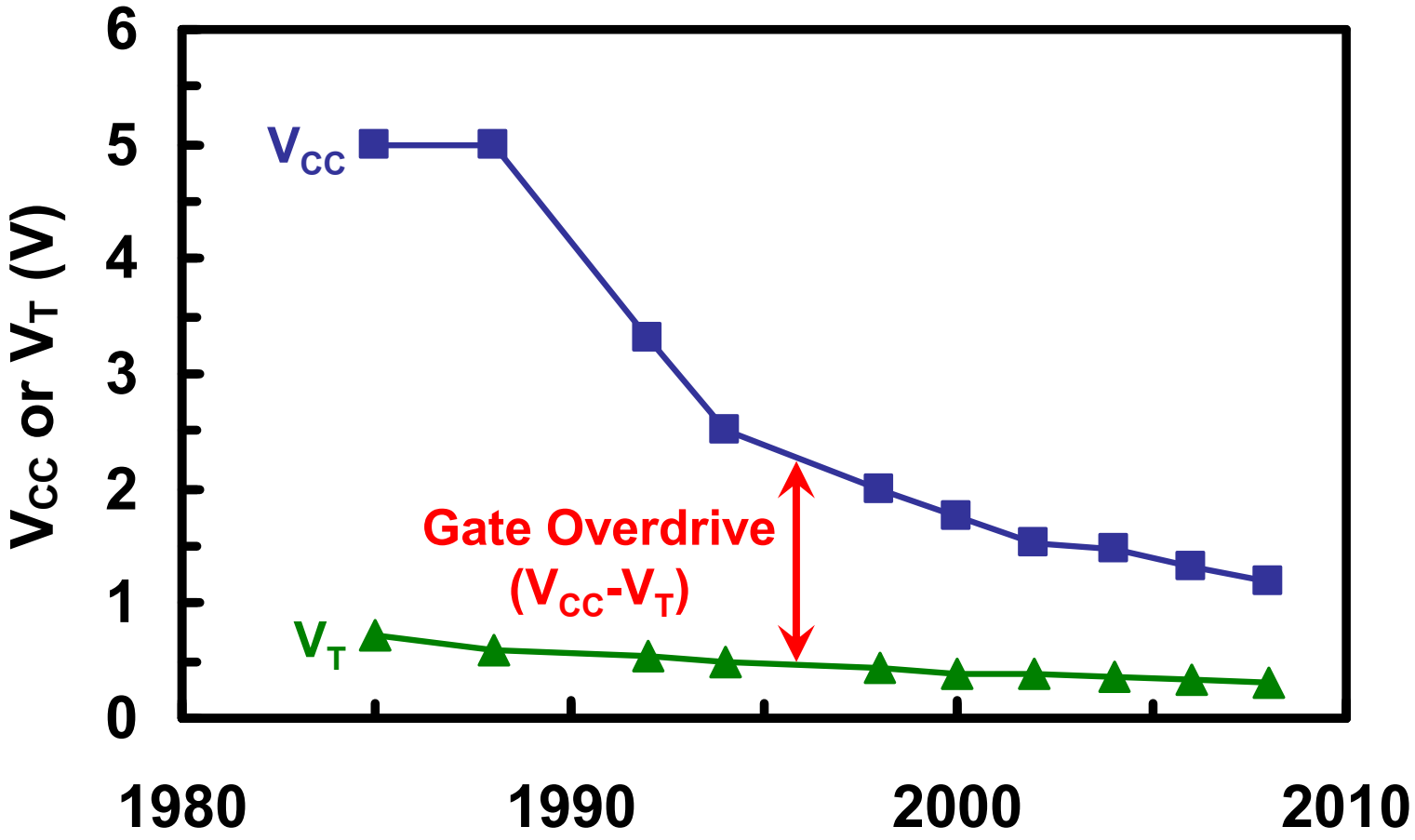
- Revenue exponentially increases across FMAX bins

Technology Outlook

Year	2008	2010	2012	2014	2016	2018
Technology Node (nm)	45	32	22	16	11	8
Bulk Planar CMOS	High Probability					Low Probability
Alternative Device (3G)	Low Probability					High Probability
Variability	Medium			High		Very High

Source: Shekhar Borkar, Intel

Gate Overdrive Degradation



- Gate overdrive reduction amplifies impact of V_{CC}, V_T, & L variations on drive current

Strategic Research Objective

Design Reliable Systems with Unreliable Components

Outline

- Motivation & Technology Trends
- Sources of Variability
- Static Variations:
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Sources of Variability

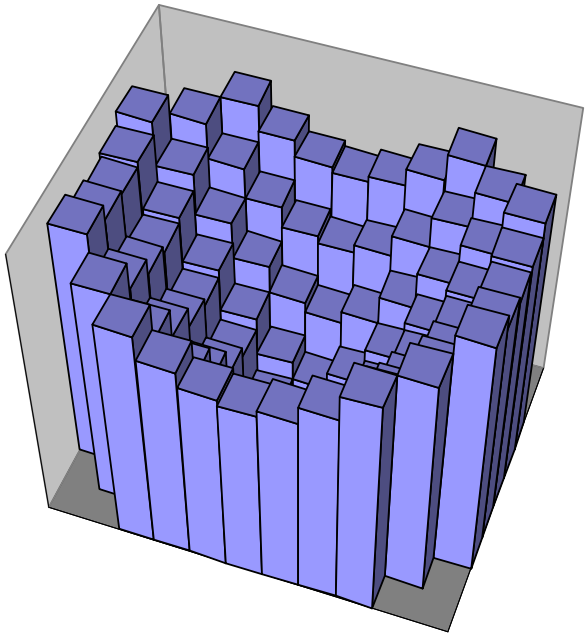
1) Static Process Variations

2) Dynamic Operational Variations

3) Simulation Tool Uncertainty

Scale of Variations

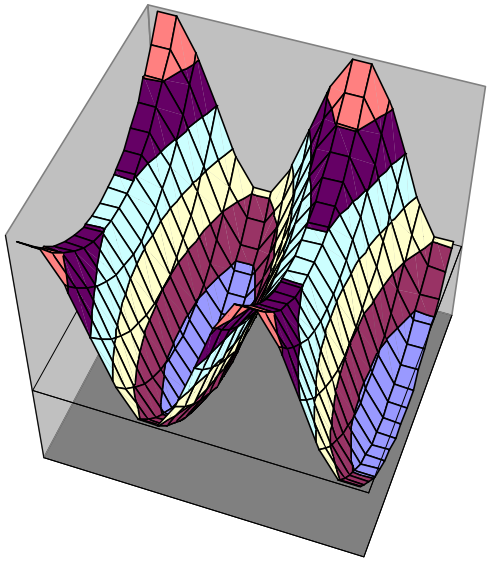
Die-to-Die (D2D) Variations



Wafer Scale

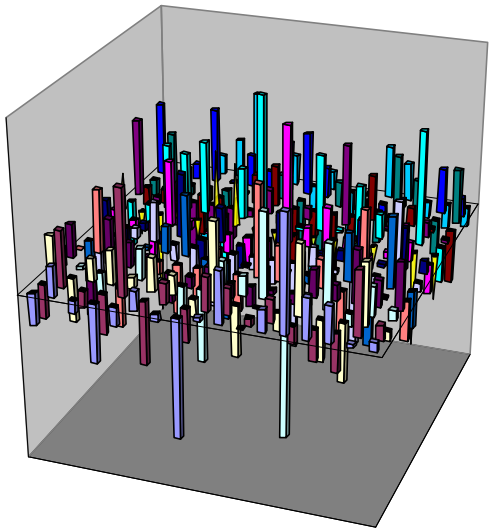
Within-Die (WID) Variations

Systematic



Die Scale

Random



Feature Scale

Static Variations

Gate Length Variation

Die-to-Die Variation

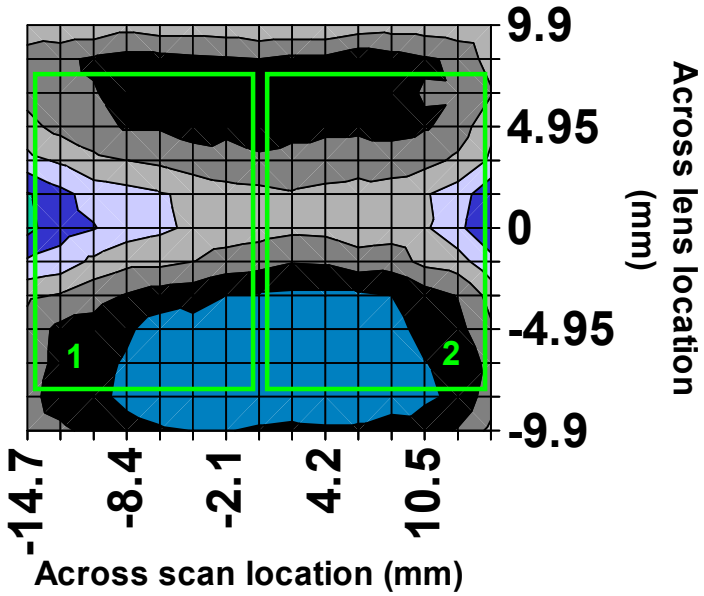
- **Examples: Processing temperatures, equipment properties, polishing, die placement, resist thickness**

Systematic Within-Die Variation

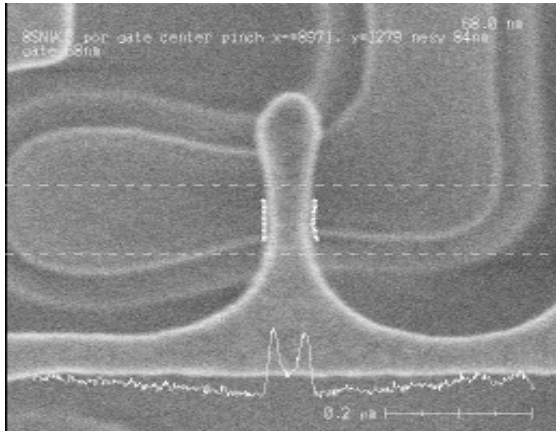
- **Examples: Lens aberrations, mid-range flare, stepper non-uniformities, scanner overlay control, multiple dies per reticle, wafer topography**

Random Within-Die Variation

- **Examples: Patterning limitations, short-range flare, line edge roughness**

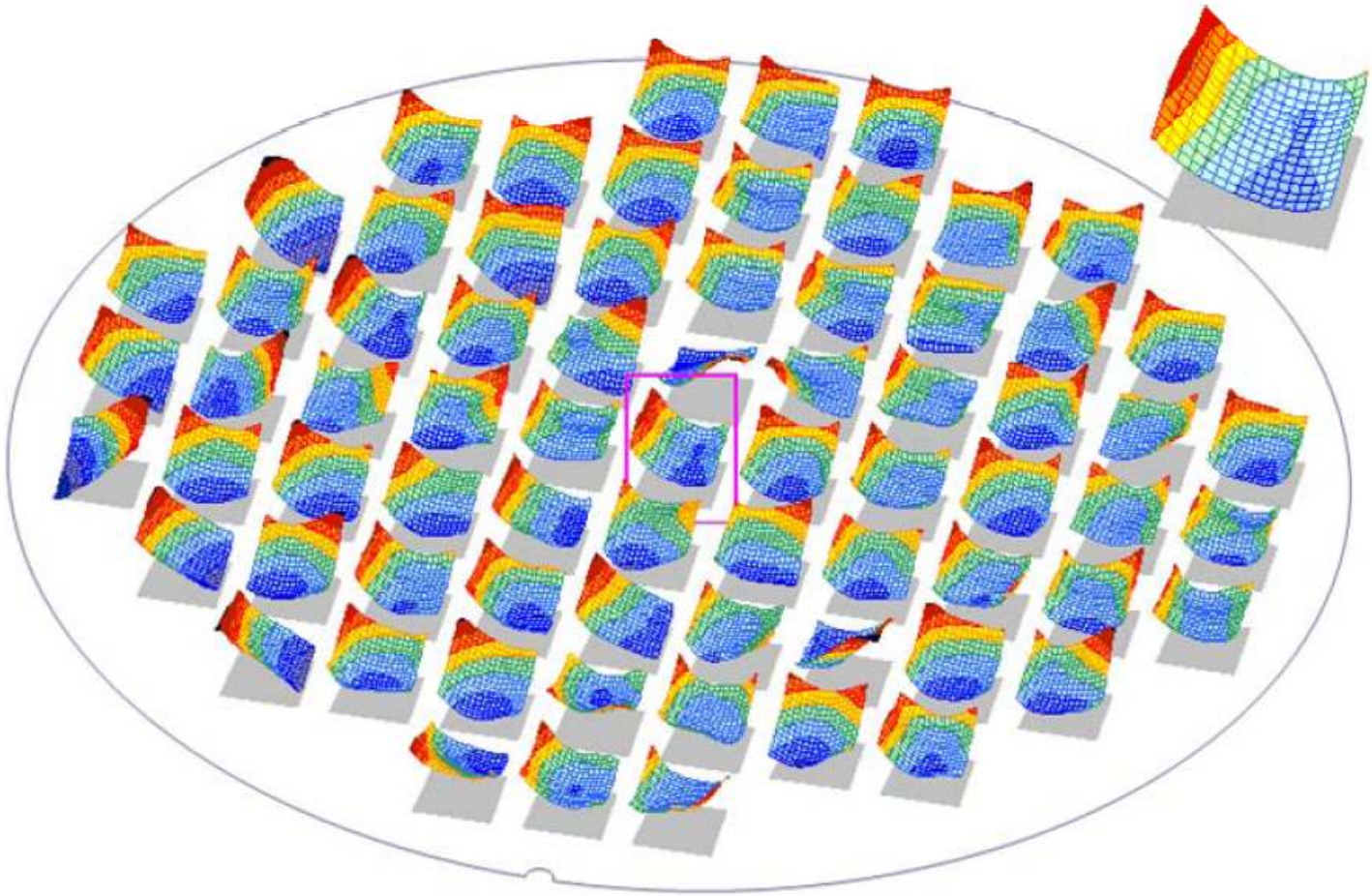


Source: Steve Duvall



Source: Nagib Hakim

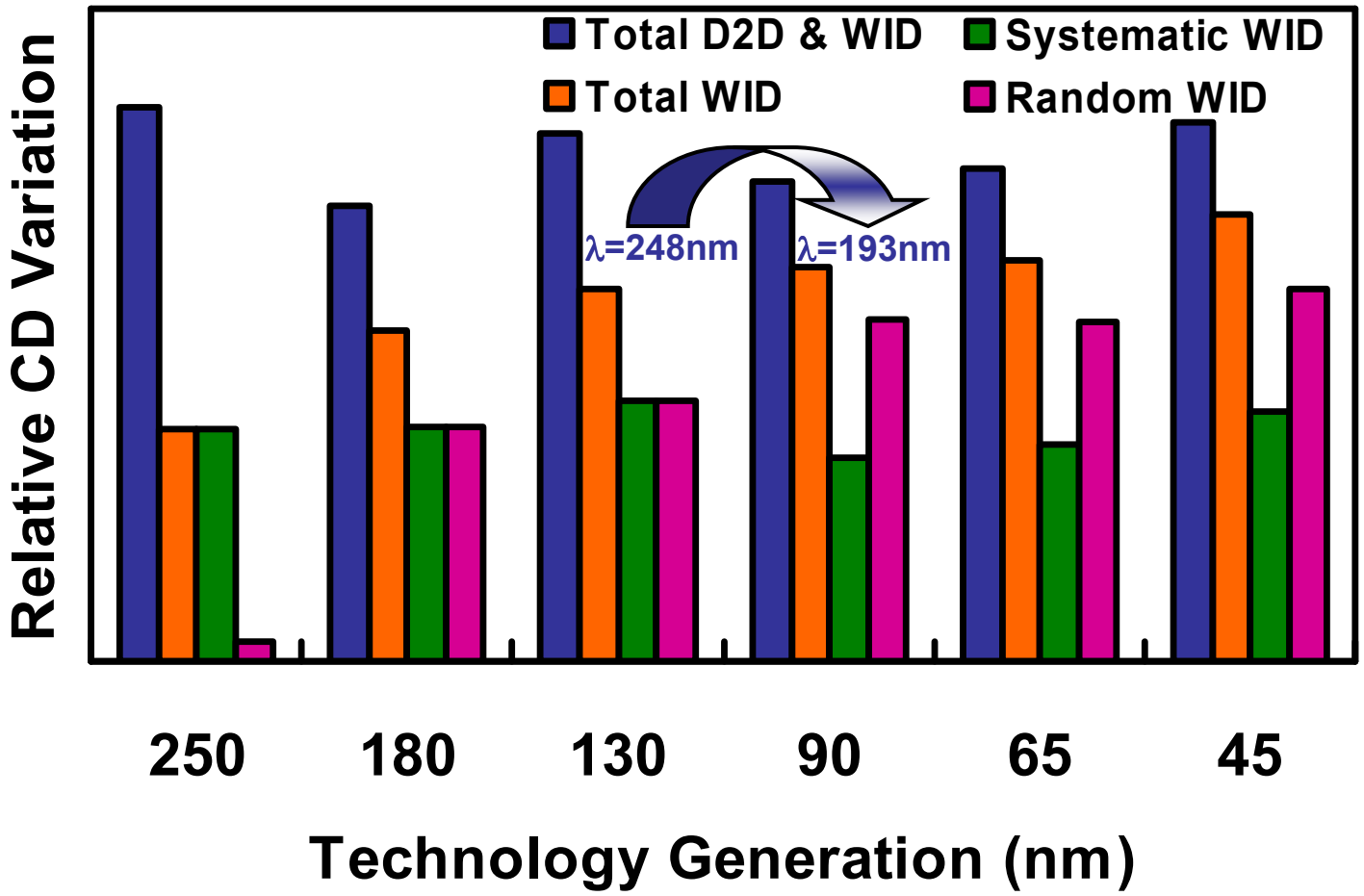
Systematic-WID Variation



Source: H. Masuda, et al., *CICC*, 2005.

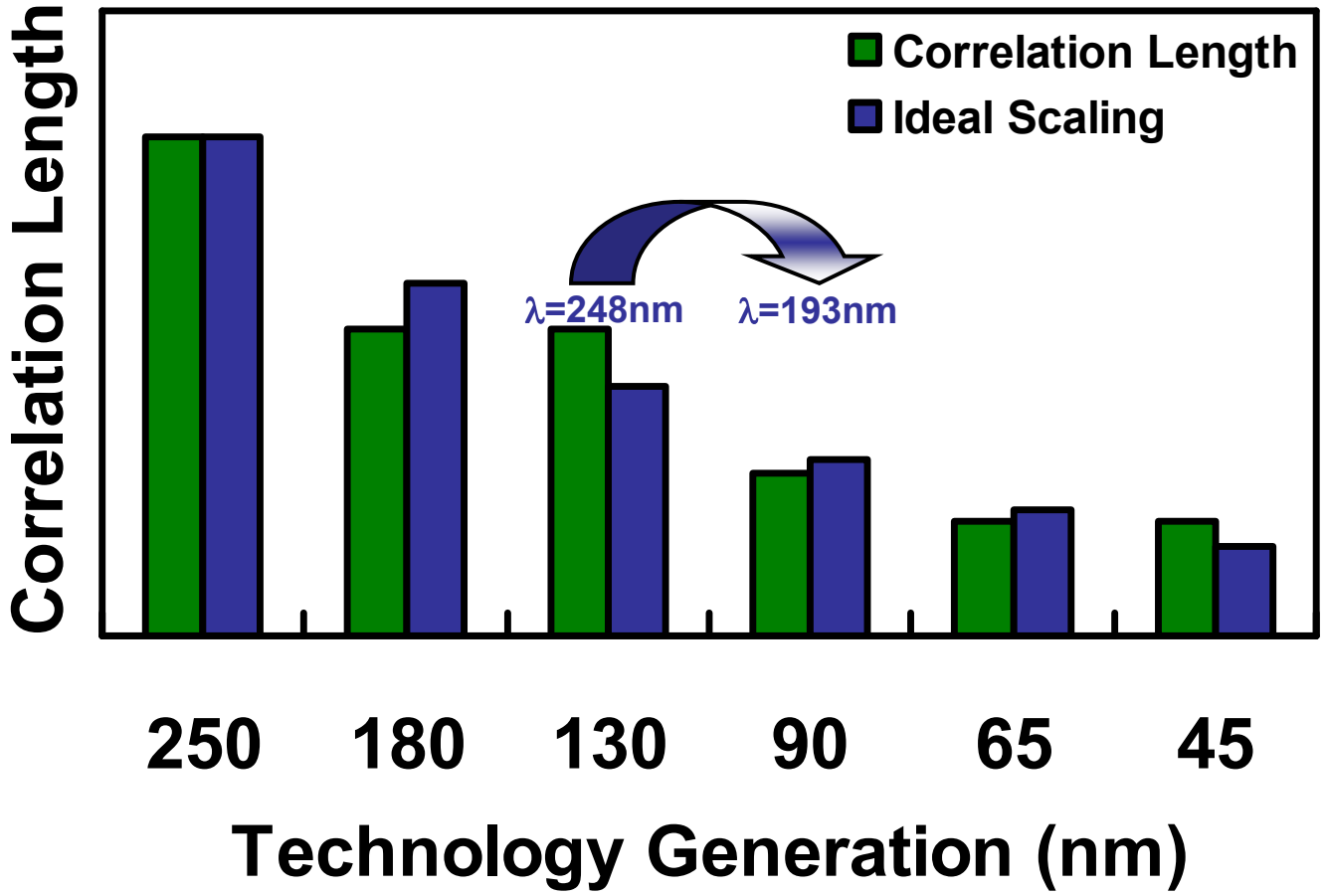
- From circuit design perspective, systematic-WID variation behaves as a correlated random-WID variation

Gate Length Variation Trends



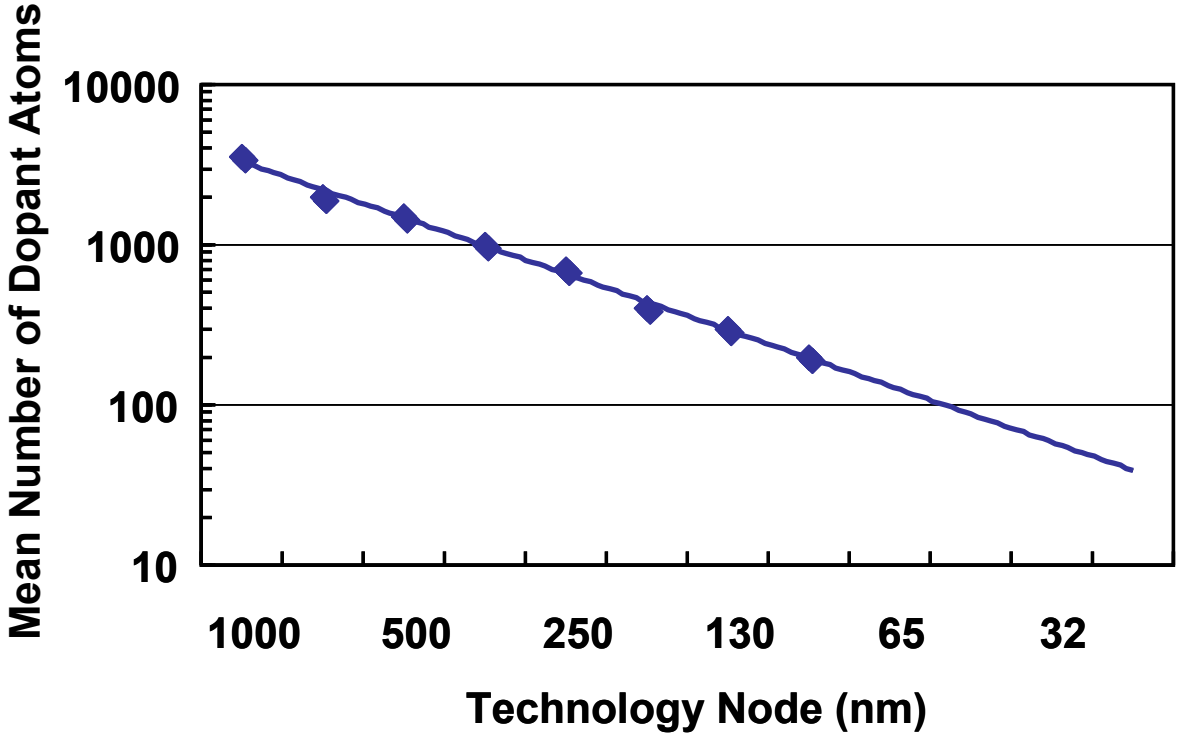
- Total CD control approximately fixed percentage of nominal gate length
- Random-WID variations increase with scaling

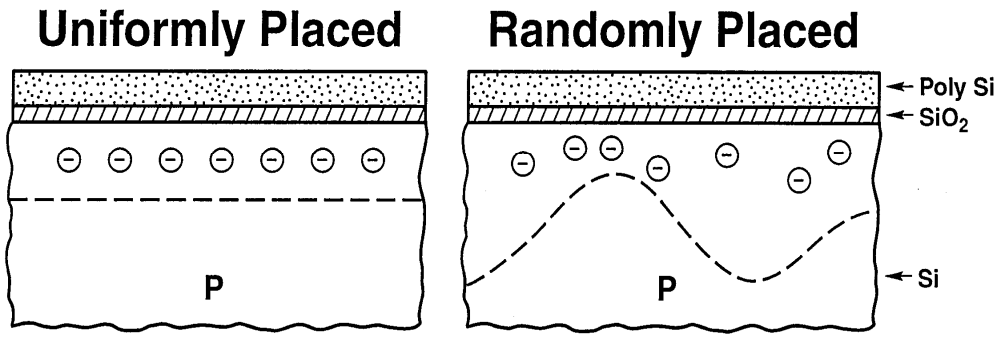
Systematic-WID Correlation Length



- Correlation length scaling by ~1/sqrt(2)

Random Dopant Fluctuation





⊖ Dopant Atoms Source: X. Tang

Interconnect Variations

1) Depth of Focus Variation

- Depends on neighboring interconnects

2) Chemical Mechanical Polishing (CMP)

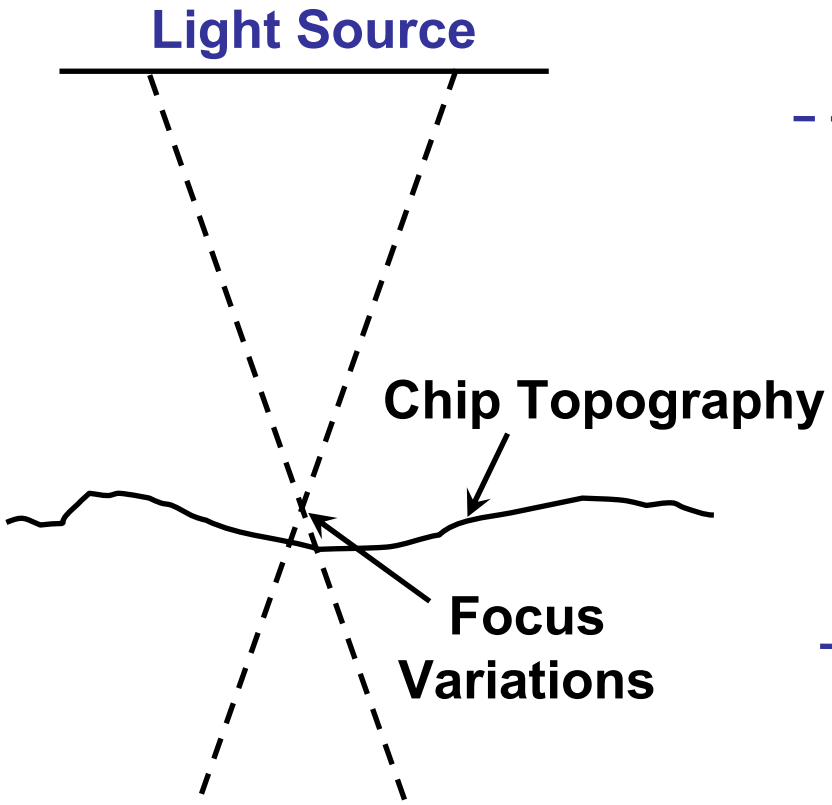
- Depends on metal density

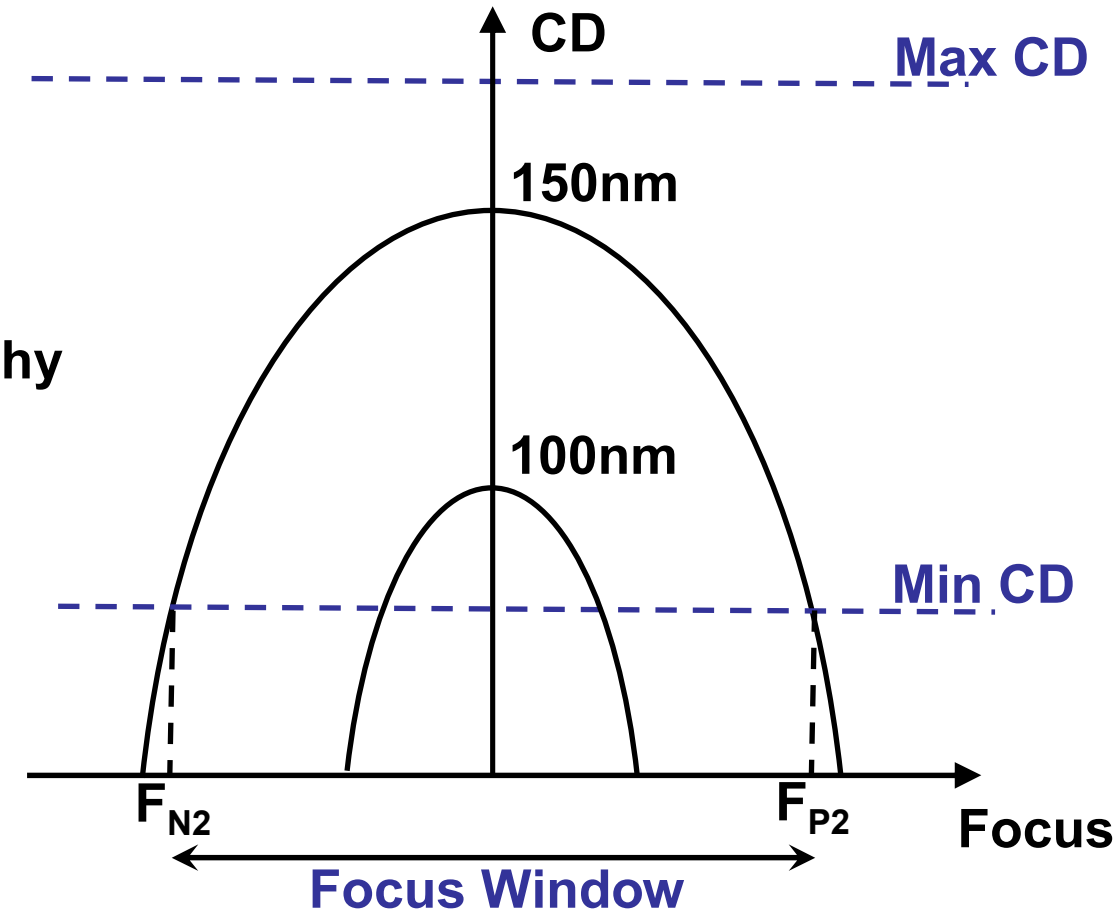
3) Etching

- Smaller than depth of focus & CMP variations

Impact of OPC on Isolated Lines

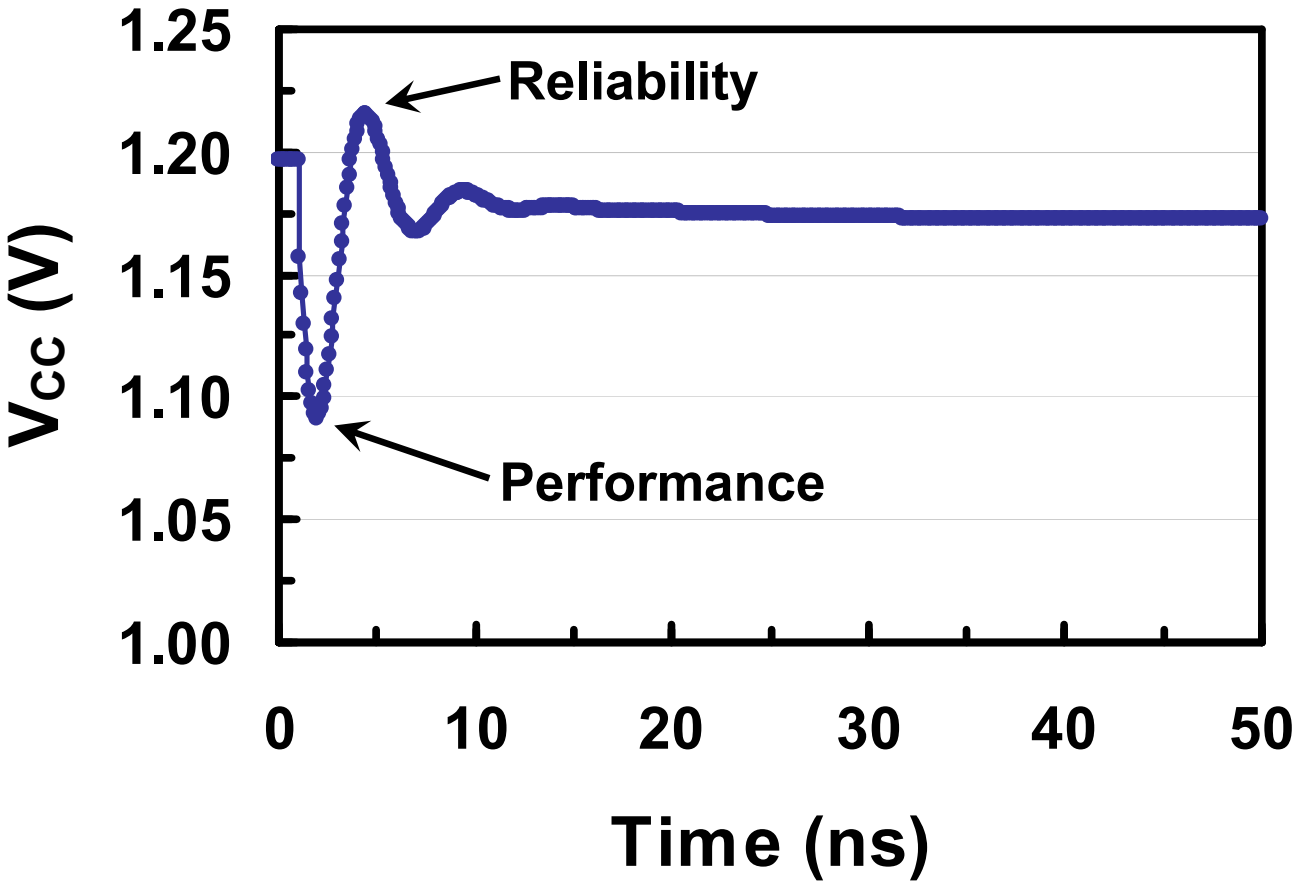
Bossung Plot Example (Isolated Drawn Lines)





Dynamic Variations

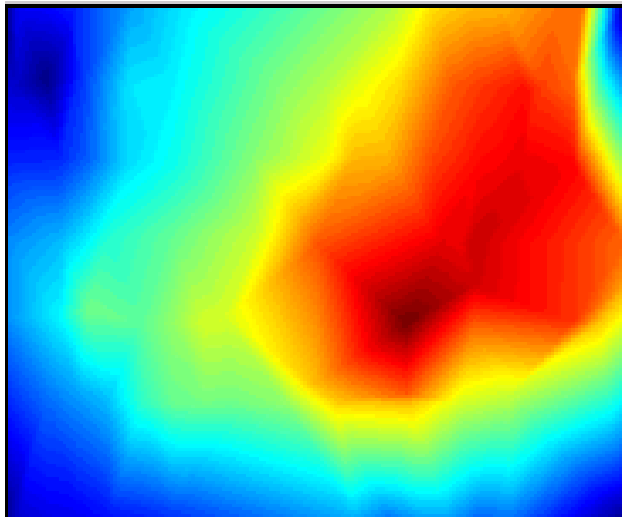
Supply Voltage Variations



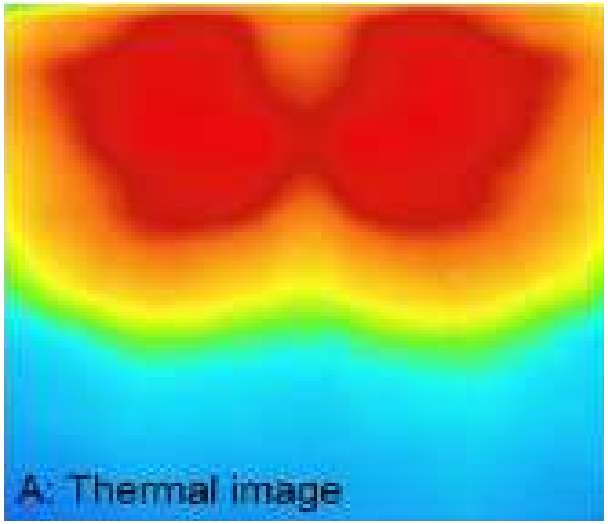
- Processor activity change
- Current delivery (RLC)
- Dynamic: ns – 100μs

Temperature Variations

Single Core



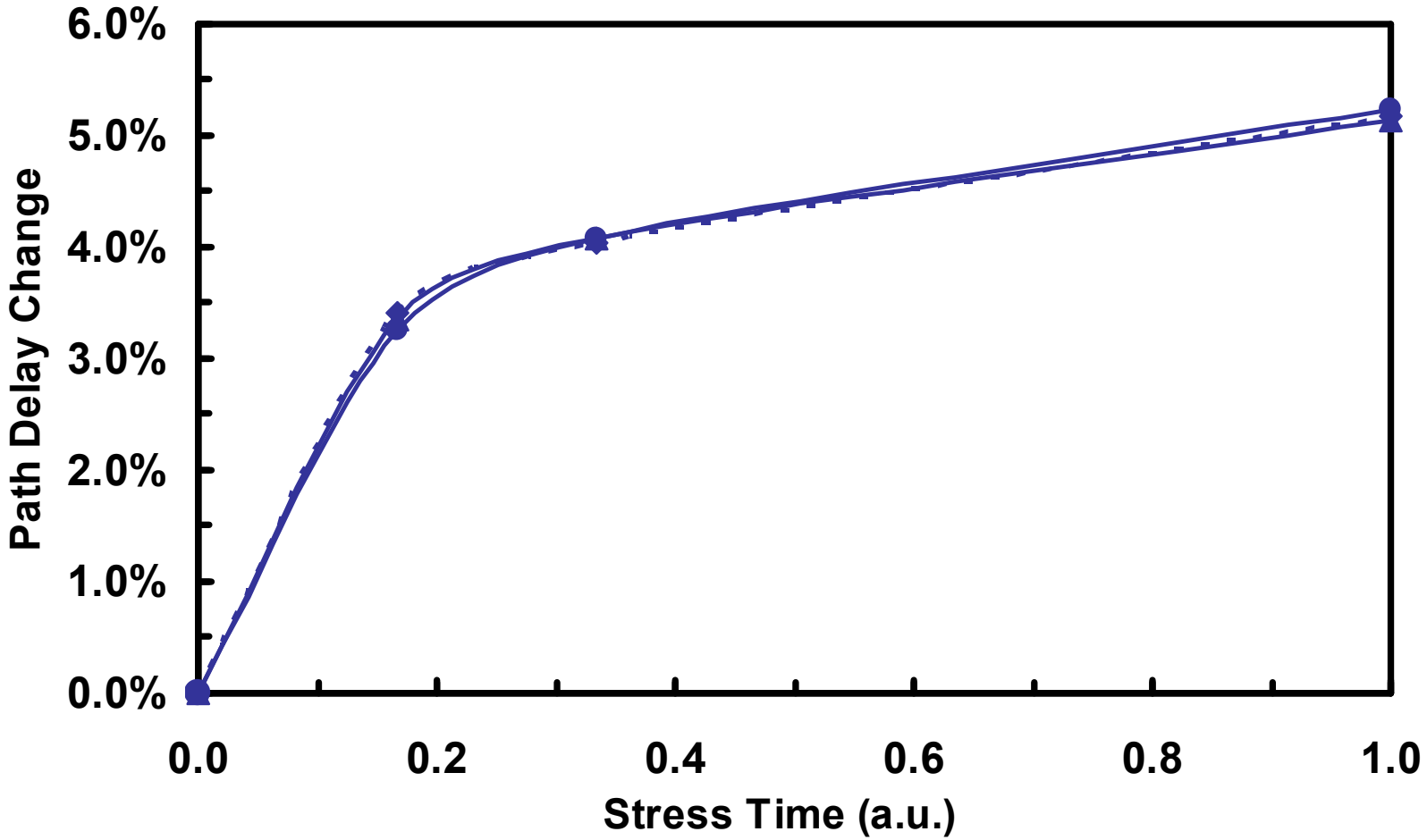
Dual Core



Hamann et. al, *ITHERM*, 2006.

- Processor activity & ambient change
- Dynamic: 100 – 1000μs

Transistor Aging

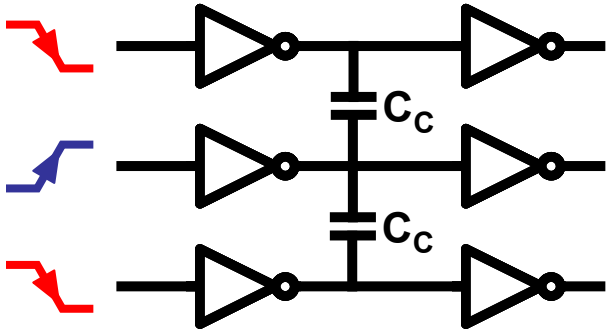


- **NMOS & PMOS threshold voltages degrade from bias & temperature stress**

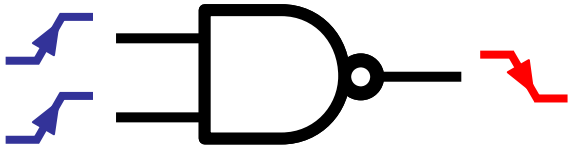
J. Tschanz, et al., *Symp. VLSI Circuits*, 2009.

Additional Dynamic Variations

Cross-Coupling Capacitance



Multiple-Input Switching



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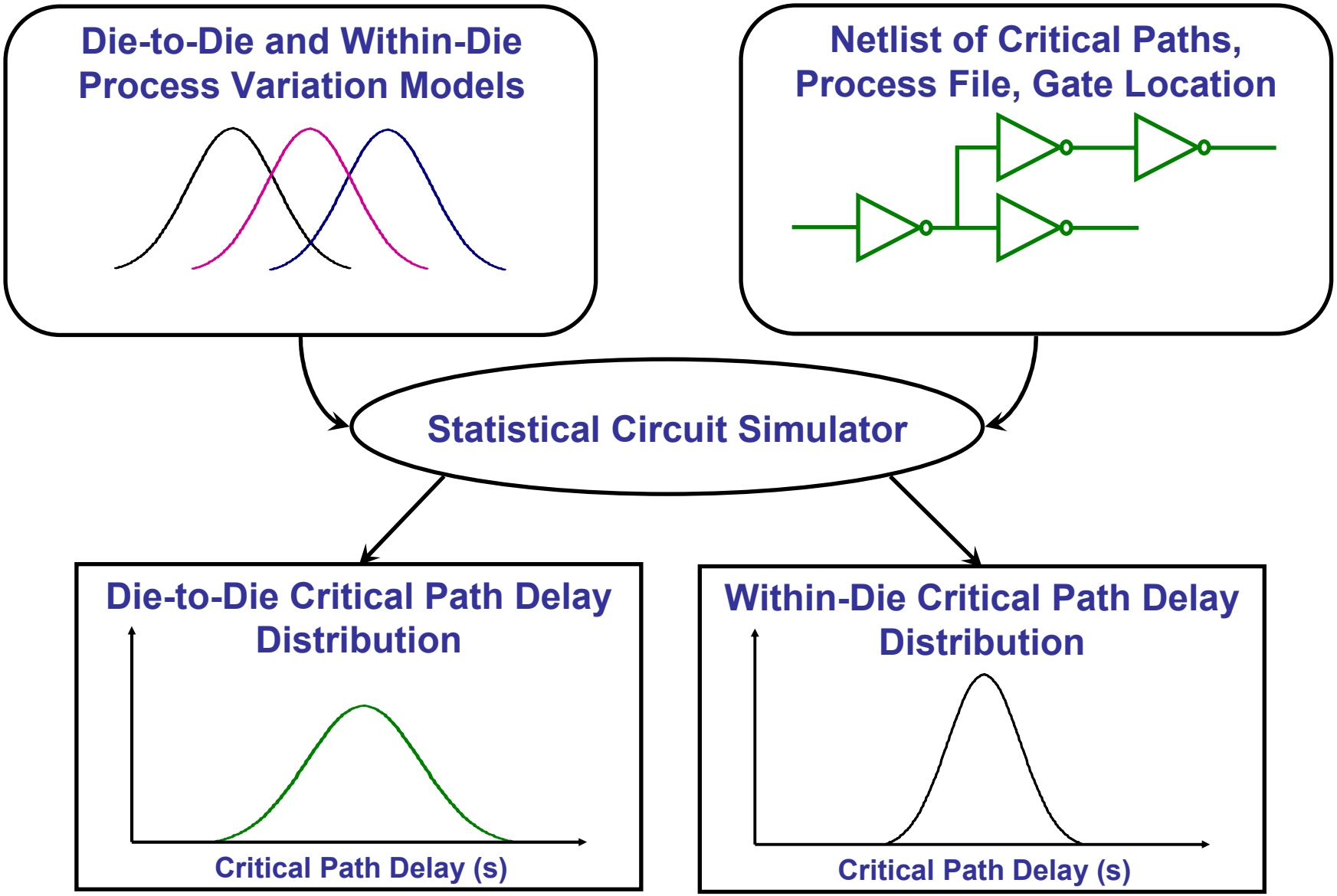
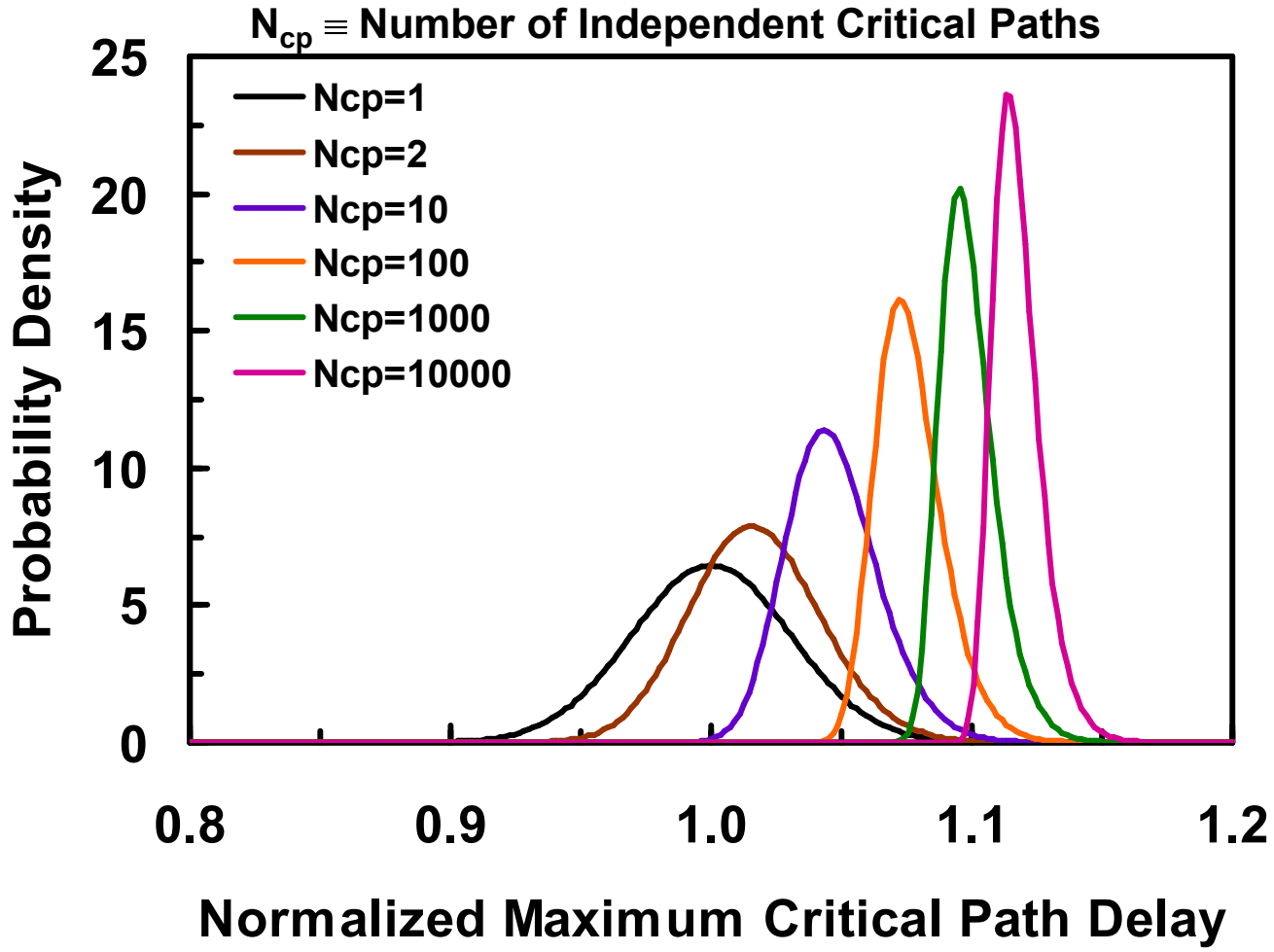
Impact of Variations on Delay



K. Bowman, et al., *JSSC*, 2002.

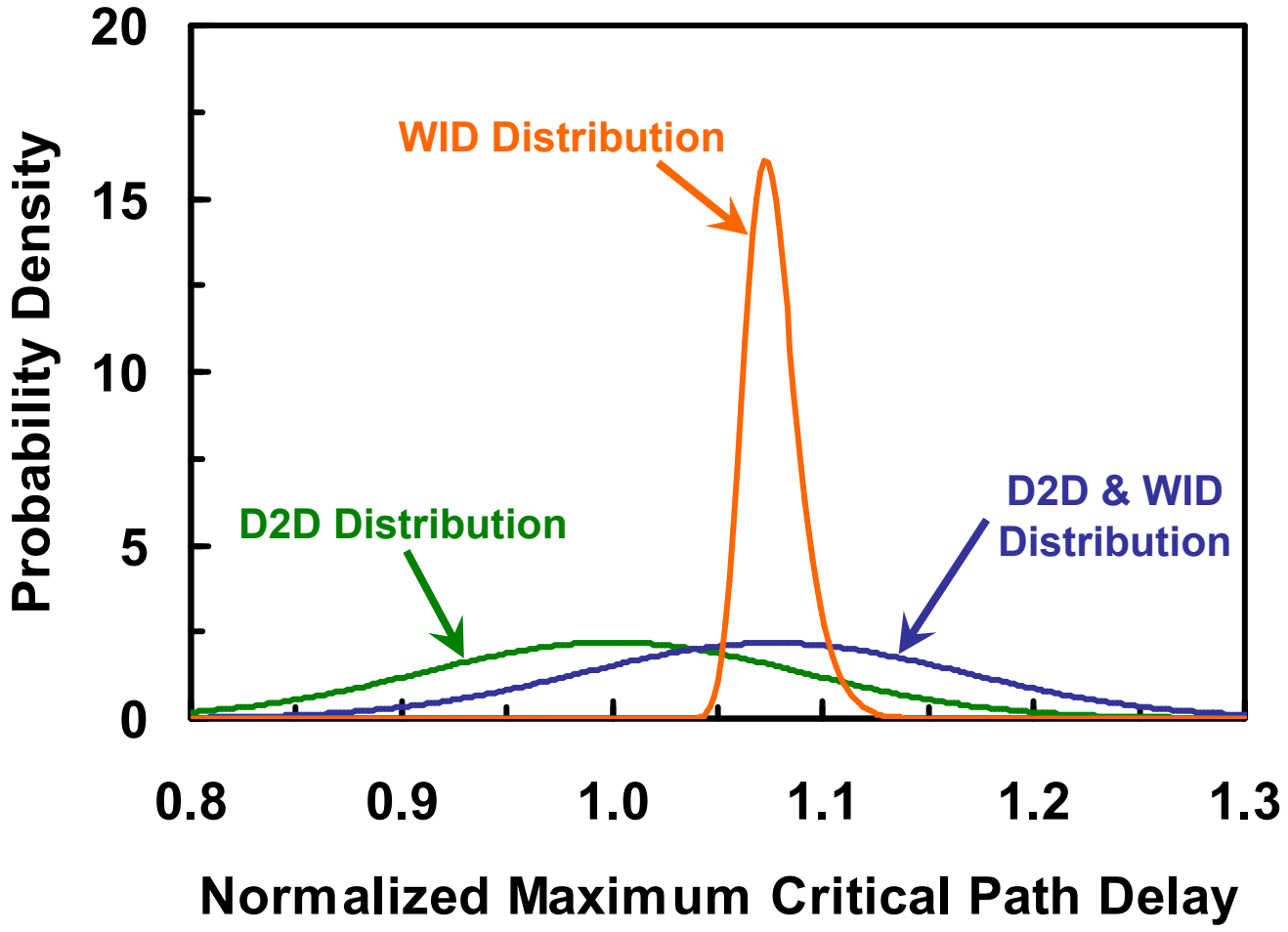
Impact of WID Variations on Delay



- As N_{cp} increases, WID distribution mean increases and variance decreases

K. Bowman, et al., *JSSC*, 2002.

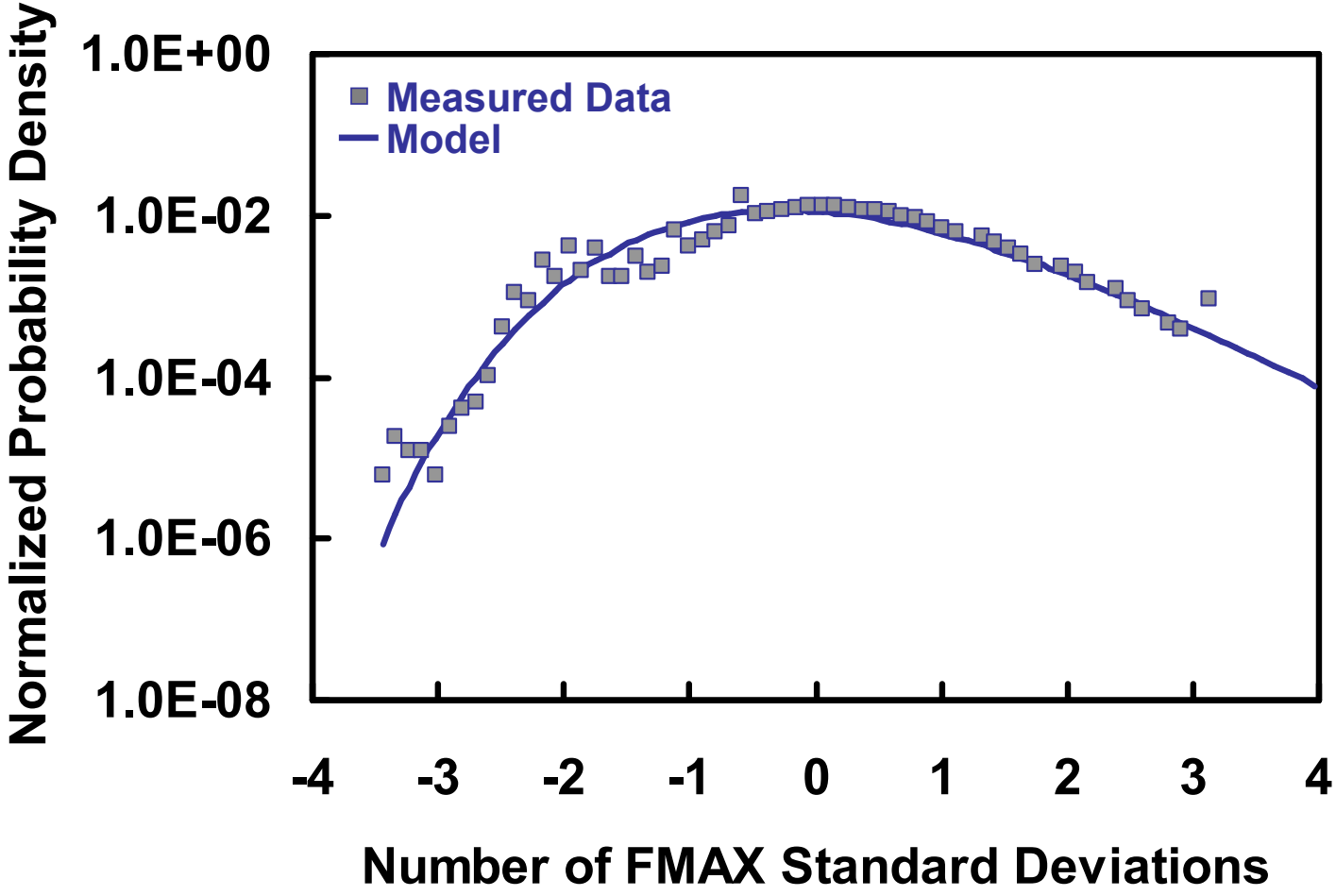
Impact of Variations on Delay



- WID variations impact delay mean
- D2D variations impact delay variance

K. Bowman, et al., *JSSC*, 2002.

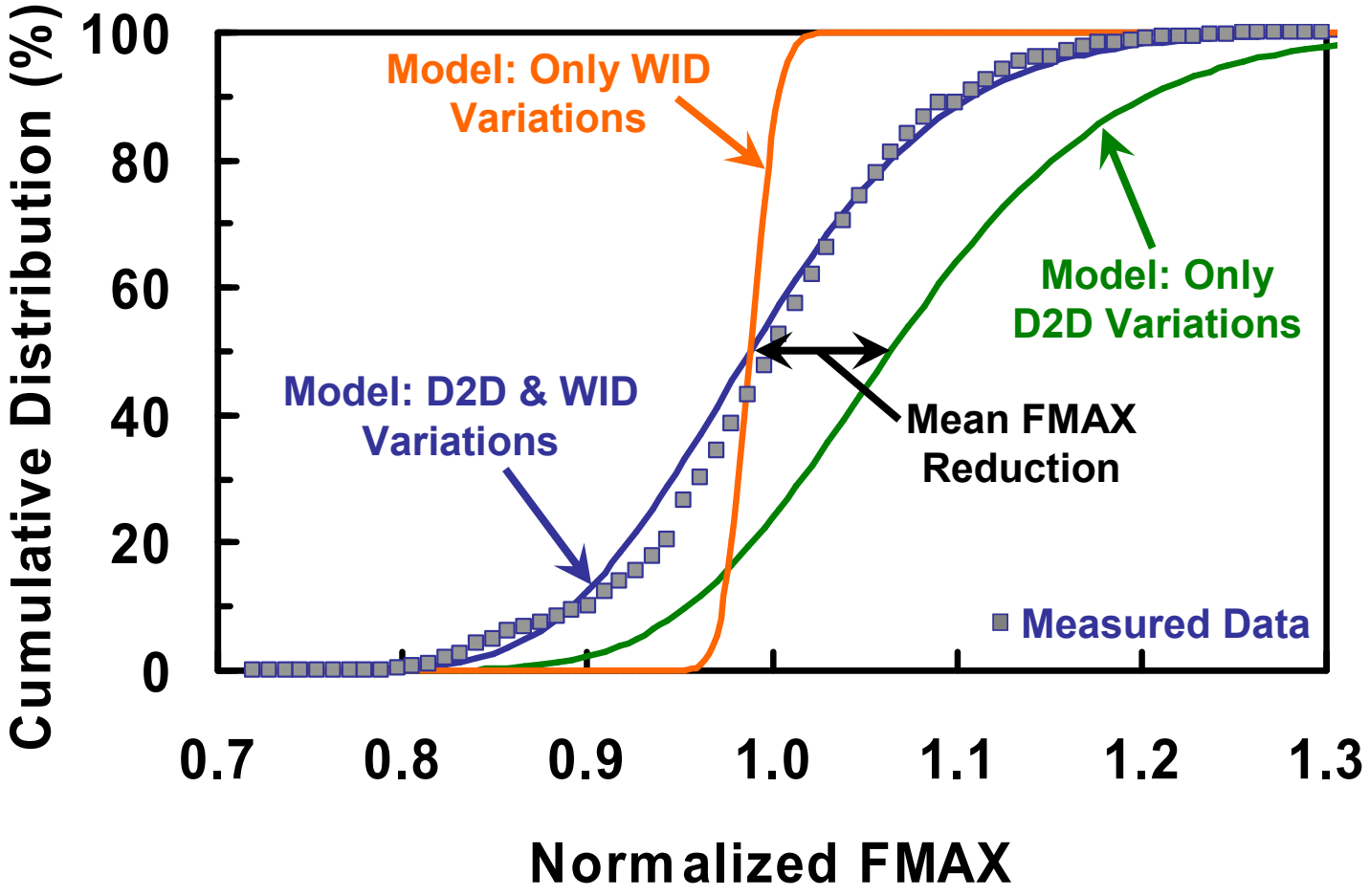
FMAX Distribution Model Validation



- Model agrees closely with measured data from a 0.25μm microprocessor in mean, variance, & shape
- No fitting parameters used in the comparison

K. Bowman, et al., *JSSC*, 2002.

Impact of Variations on FMAX

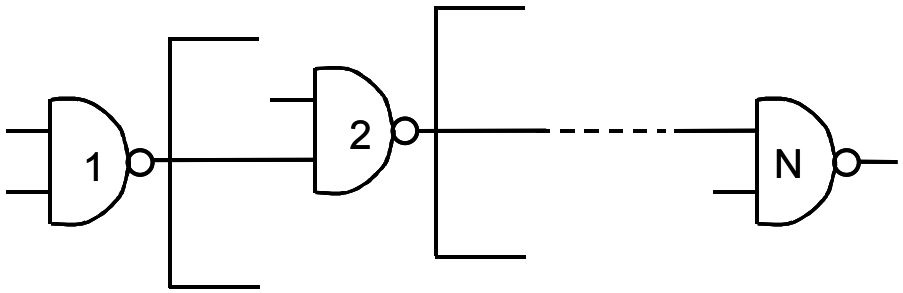


- WID variations impact FMAX mean
- D2D variations impact FMAX variance

K. Bowman, et al., *JSSC*, 2002.

Impact of Variations on Logic Depth

Critical Path



Systematic-WID Variations (ρ=1)

$$\frac{\sigma_{T_{CP}}}{T_{CP}} = \frac{N\sigma_{T_{GATE}}}{NT_{GATE}} = \frac{\sigma_{T_{GATE}}}{T_{GATE}}$$

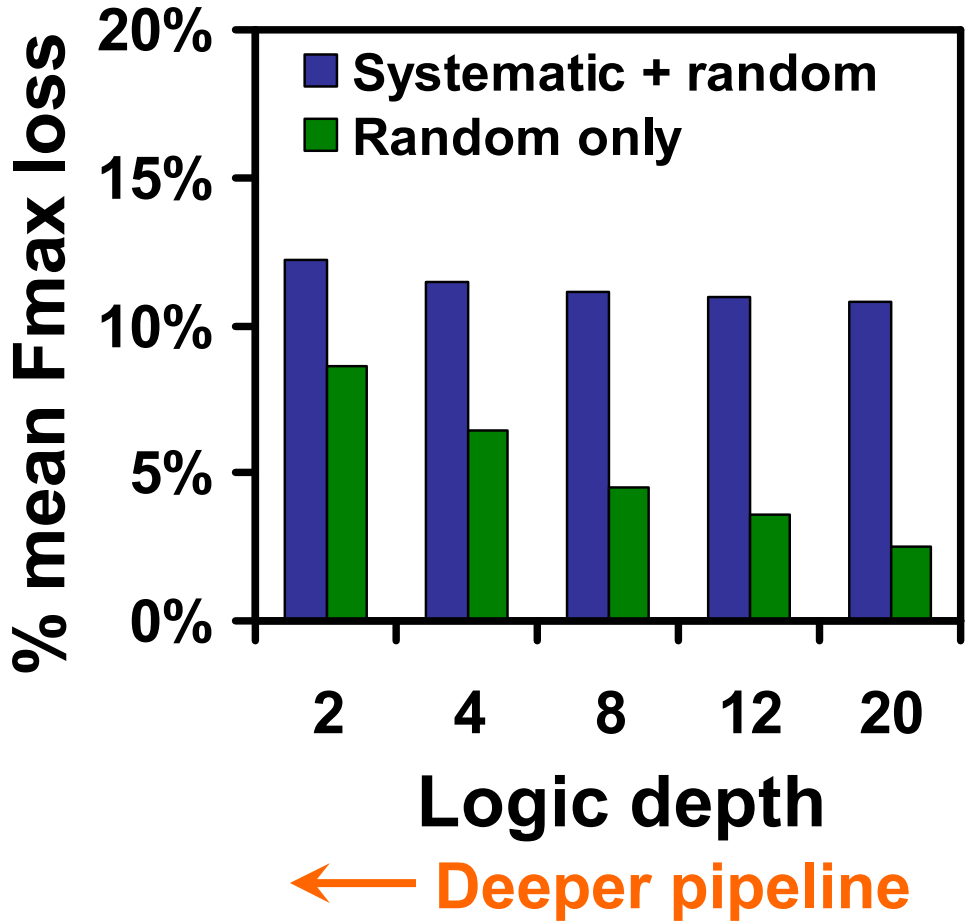
Random-WID Variations

$$\frac{\sigma_{T_{CP}}}{T_{CP}} = \frac{\sqrt{N}\sigma_{T_{GATE}}}{NT_{GATE}} = \frac{1}{\sqrt{N}}\frac{\sigma_{T_{GATE}}}{T_{GATE}}$$

- **Random-WID variations average across N stages**

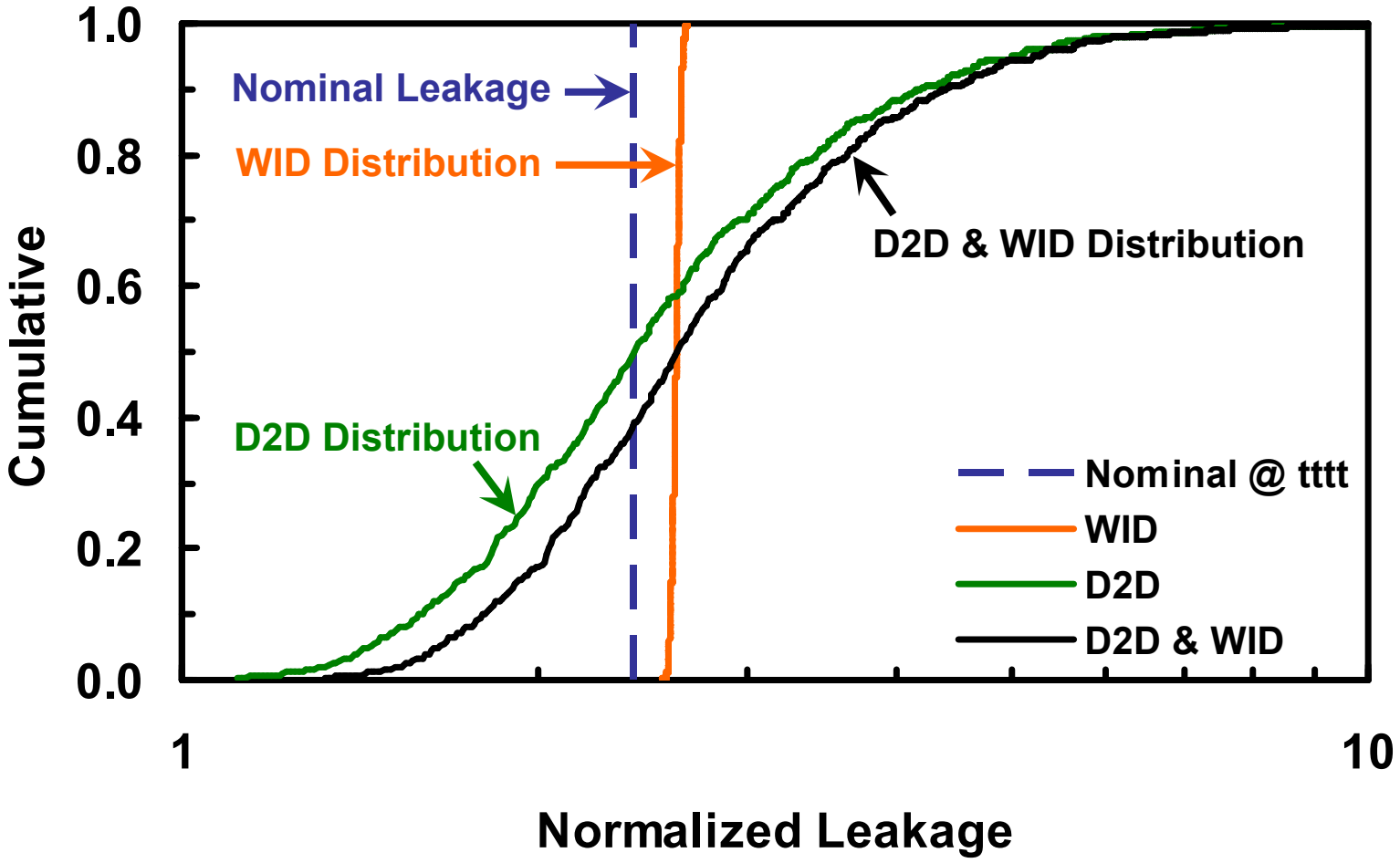
K. Bowman, et al., *JSSC*, 2002.

Impact of Variations on Logic Depth



- Impact of random-WID variation increases with deeper pipelining
- Impact of systematic-WID variation insensitive to pipelining

Impact of Variations on Leakage



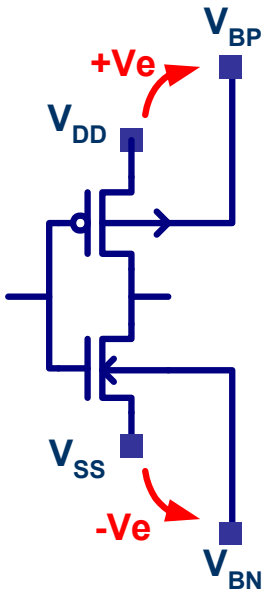
- WID variations impact leakage median
- D2D variations impact leakage variance

S. Burns, et al., DAC, 2007.

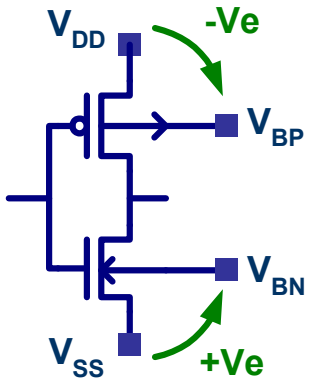
Static Variation Compensation

- **Measure:**
  - Clock Frequency
  - Power
- **Control Knobs:**
  - Supply Voltage
  - Body Bias

Body Bias Review



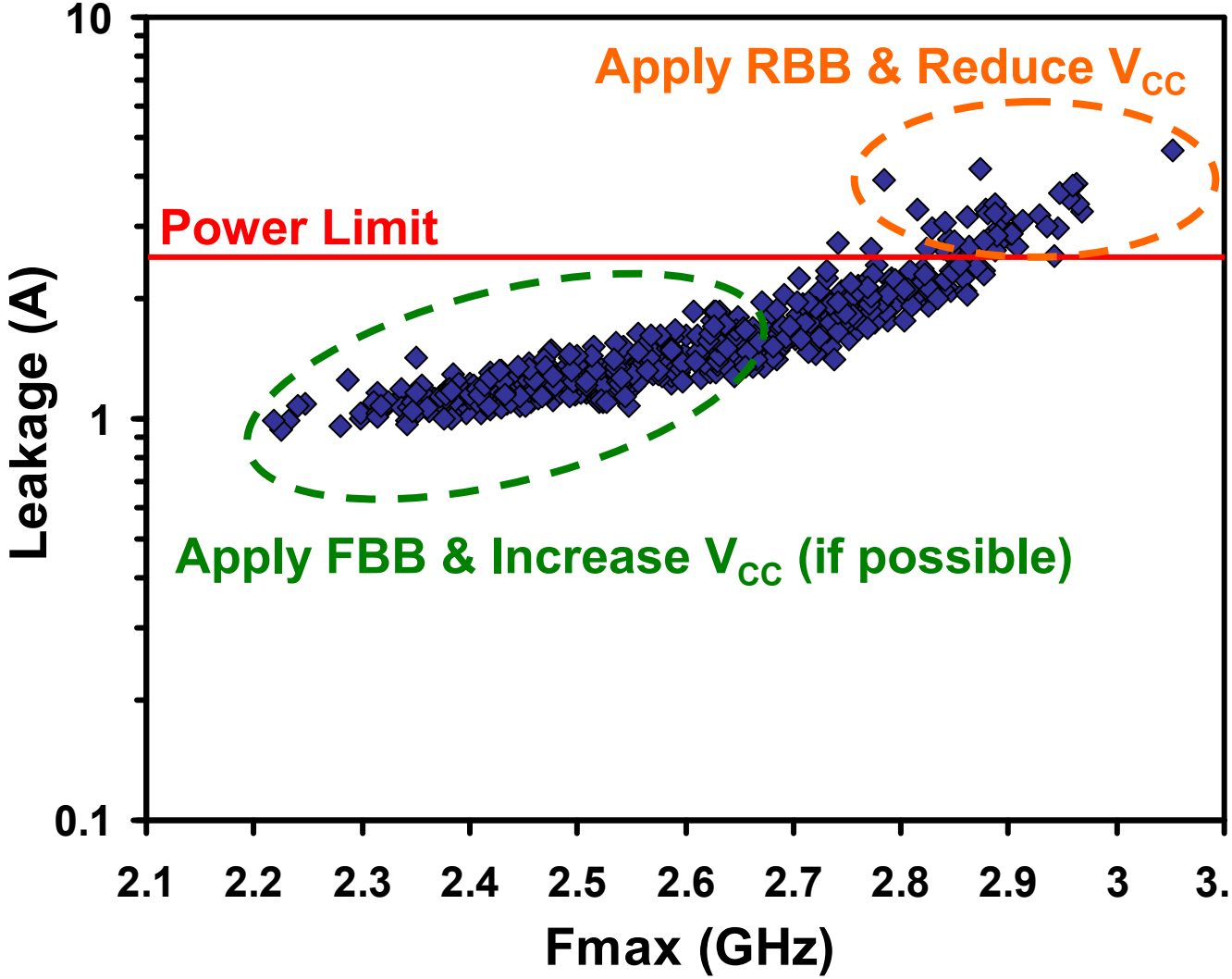
- **Reverse body bias (RBB)**
  - PMOS: $V_{BP} > V_{DD}$
  - NMOS: $V_{BN} < V_{SS}$
  - V_T increases (I_{ON}, I_{OFF} reduce)



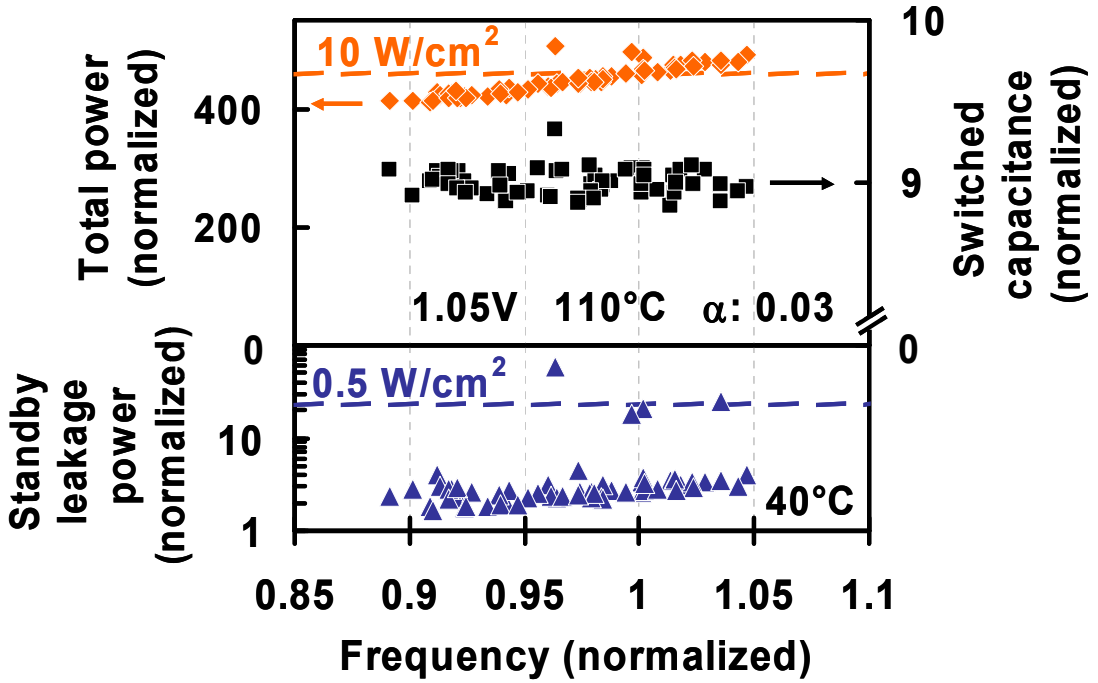
- **Forward body bias (FBB)**
  - PMOS: $V_{BP} < V_{DD}$
  - NMOS: $V_{BN} > V_{SS}$
  - V_T reduces (I_{ON}, I_{OFF} increase)

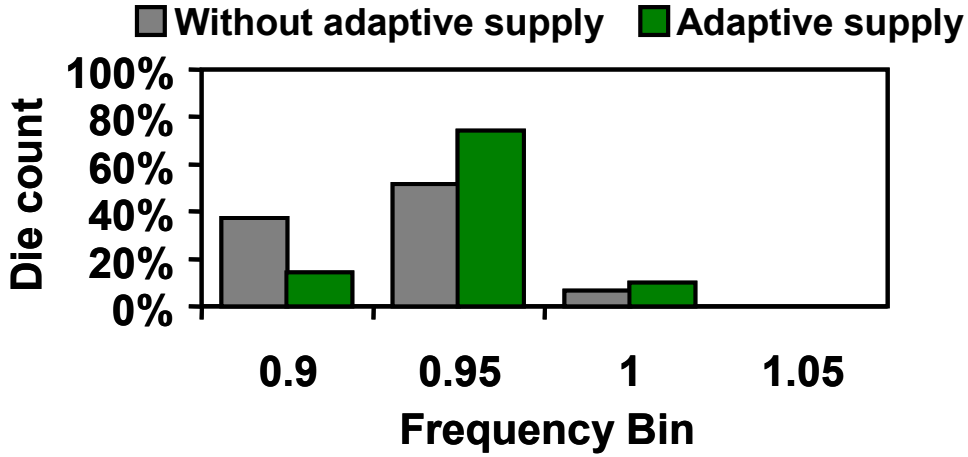
Adaptive V_{CC} & Body Bias

Reduce Impact of D2D Variations



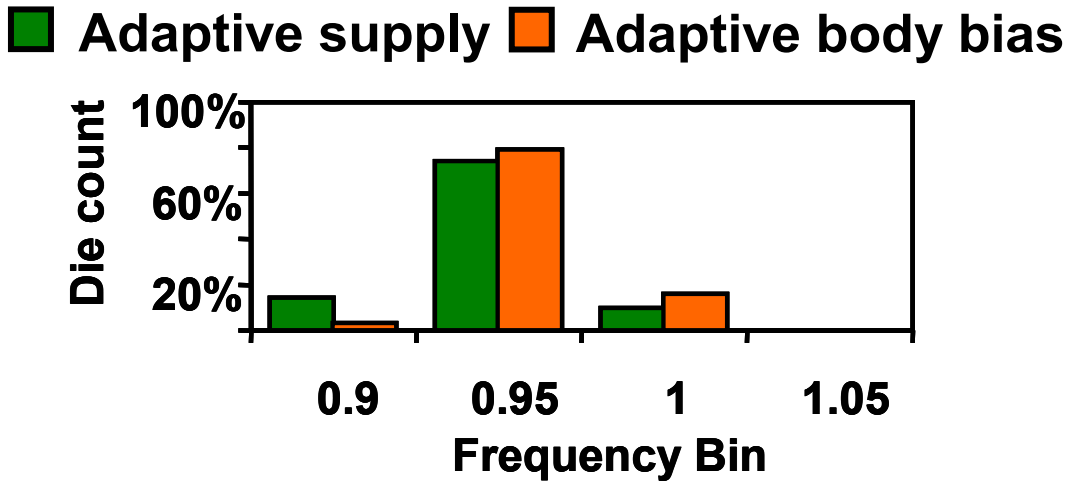
Adaptive Supply Voltage

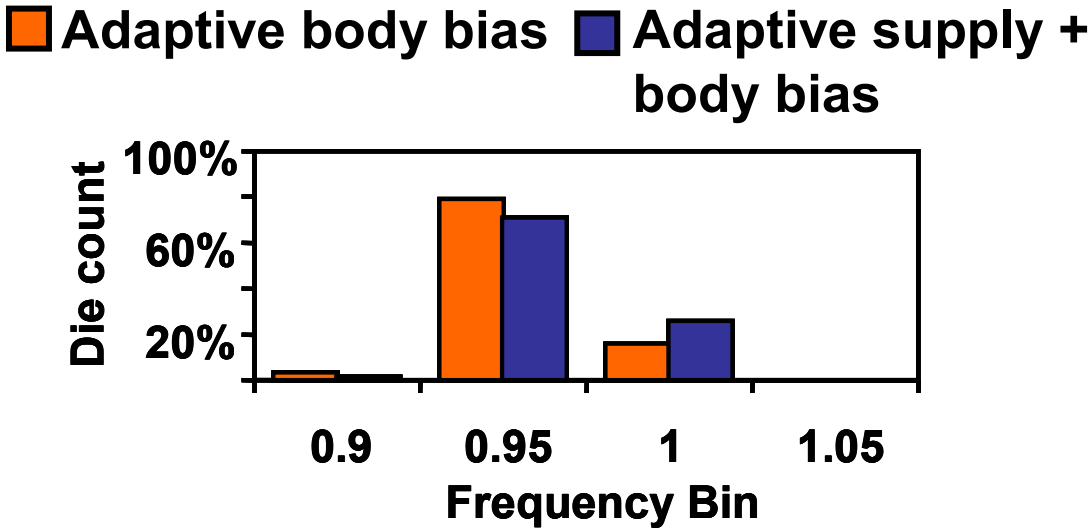


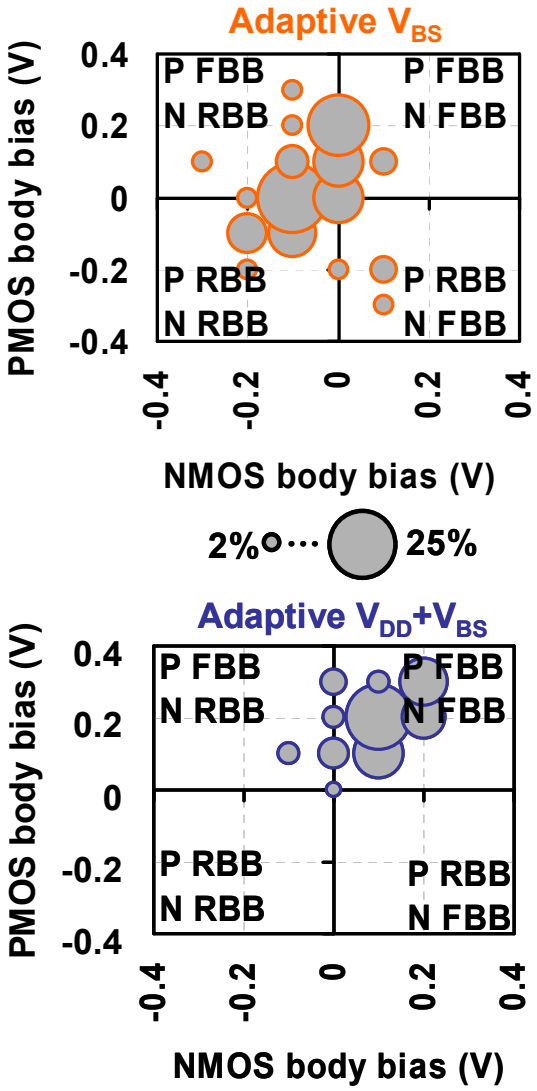


J. Tschanz, et al., *JSSC*, 2003.

Effectiveness of Adaptive Biasing







J. Tschanz, et al., *JSSC*, 2003.

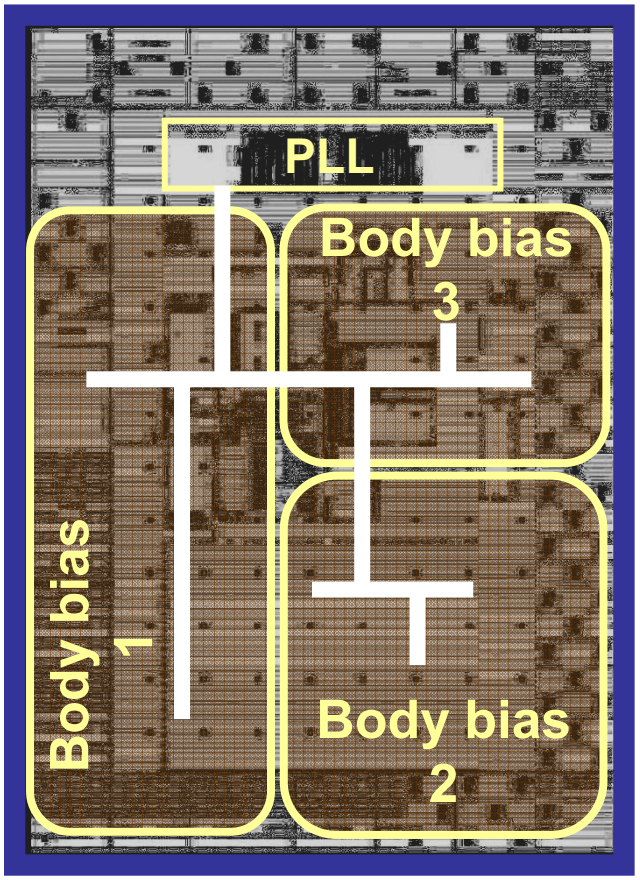
Effectiveness of Adaptive Biasing

- **Slower Parts (Lower Power)**
  - Leakage is a small percentage of total power
  - Trade-off leakage increase for performance gain
  - More effective to apply a forward body bias (FBB)

- **Faster Parts (Higher Power)**
  - Active & leakage contribute significantly to total power
  - V_{CC} reduction lowers both active and leakage power
  - More effective to reduce V_{CC}

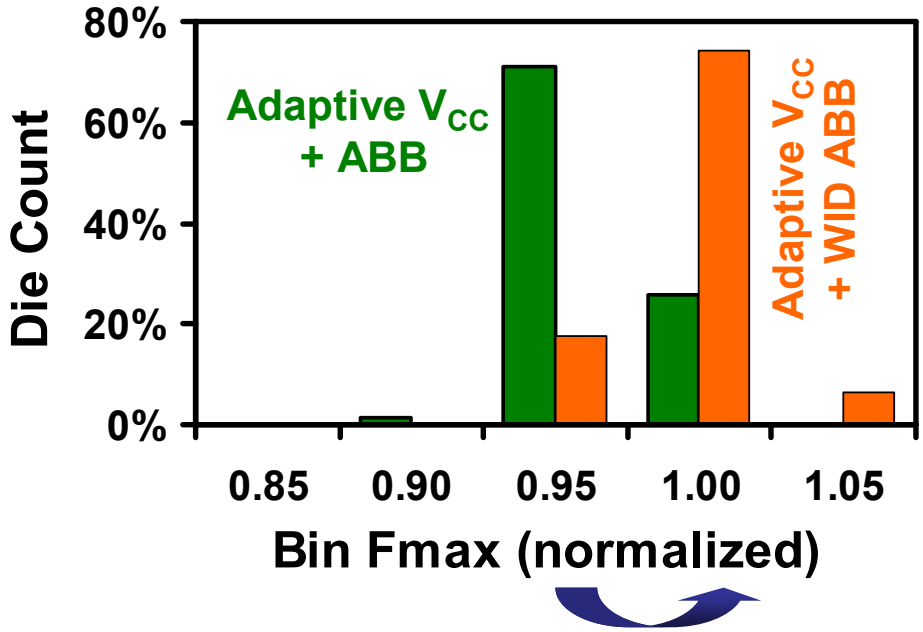
Static ABB for WID Variations

WID ABB Concept



150nm Technology Test-Chip

WID ABB Effectiveness



More parts in higher bins

- No body bias for clock
- Requires triple-well process

J. Tschanz, et al., *JSSC*, 2003.

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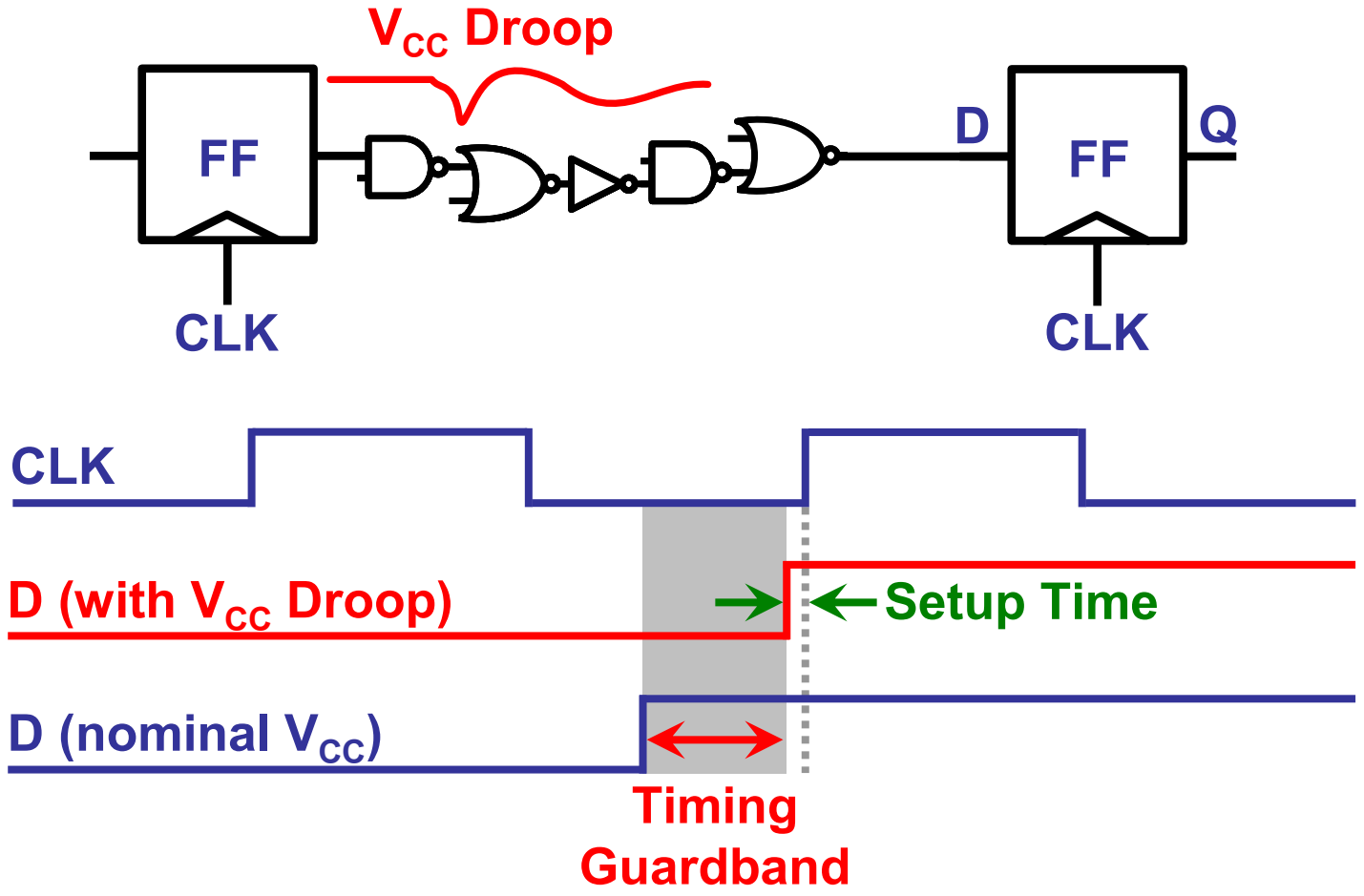
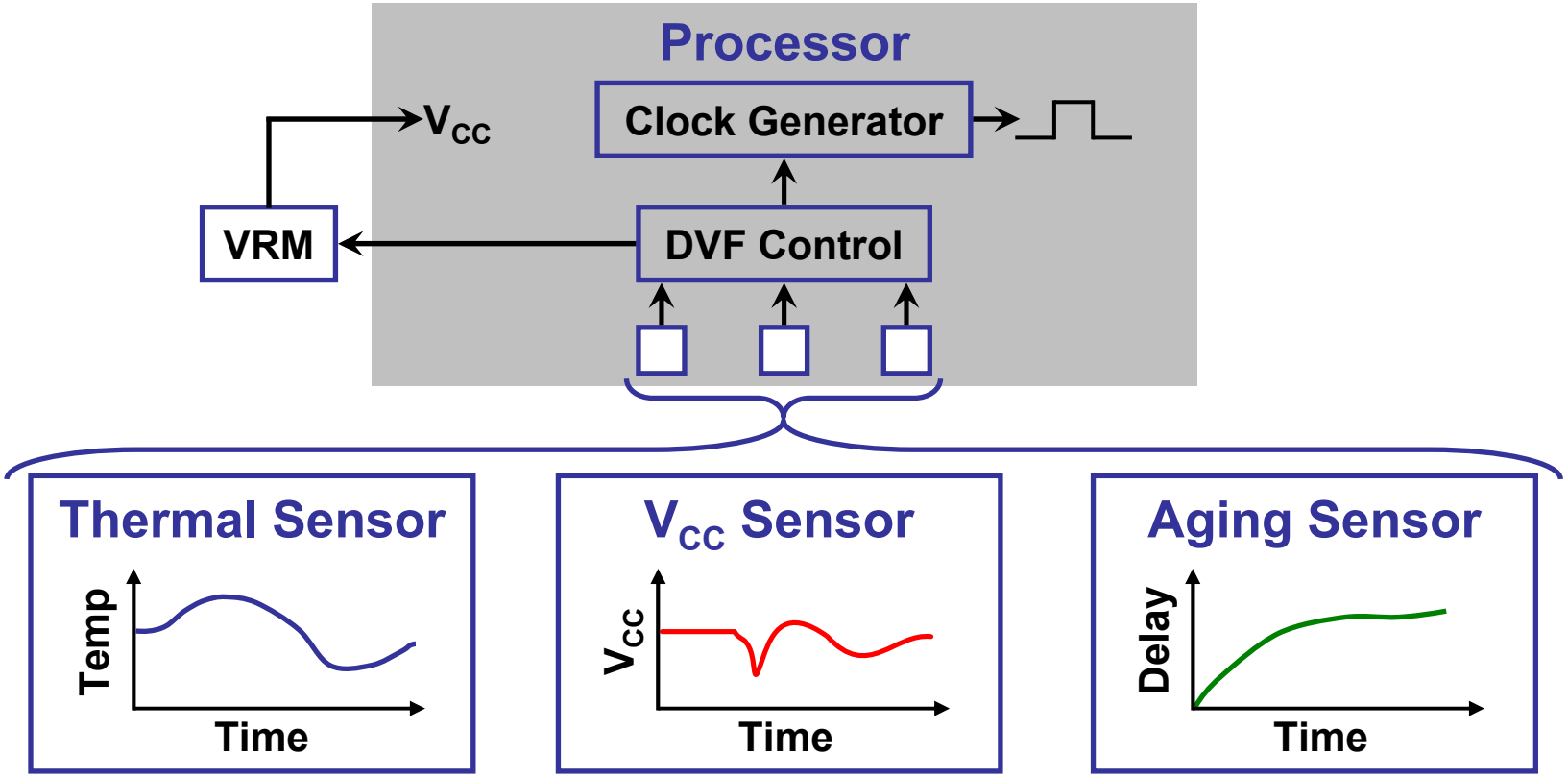
Impact of Dynamic Variations on Conventional Design



- Guardbands required to ensure correct operation within the presence of dynamic variations

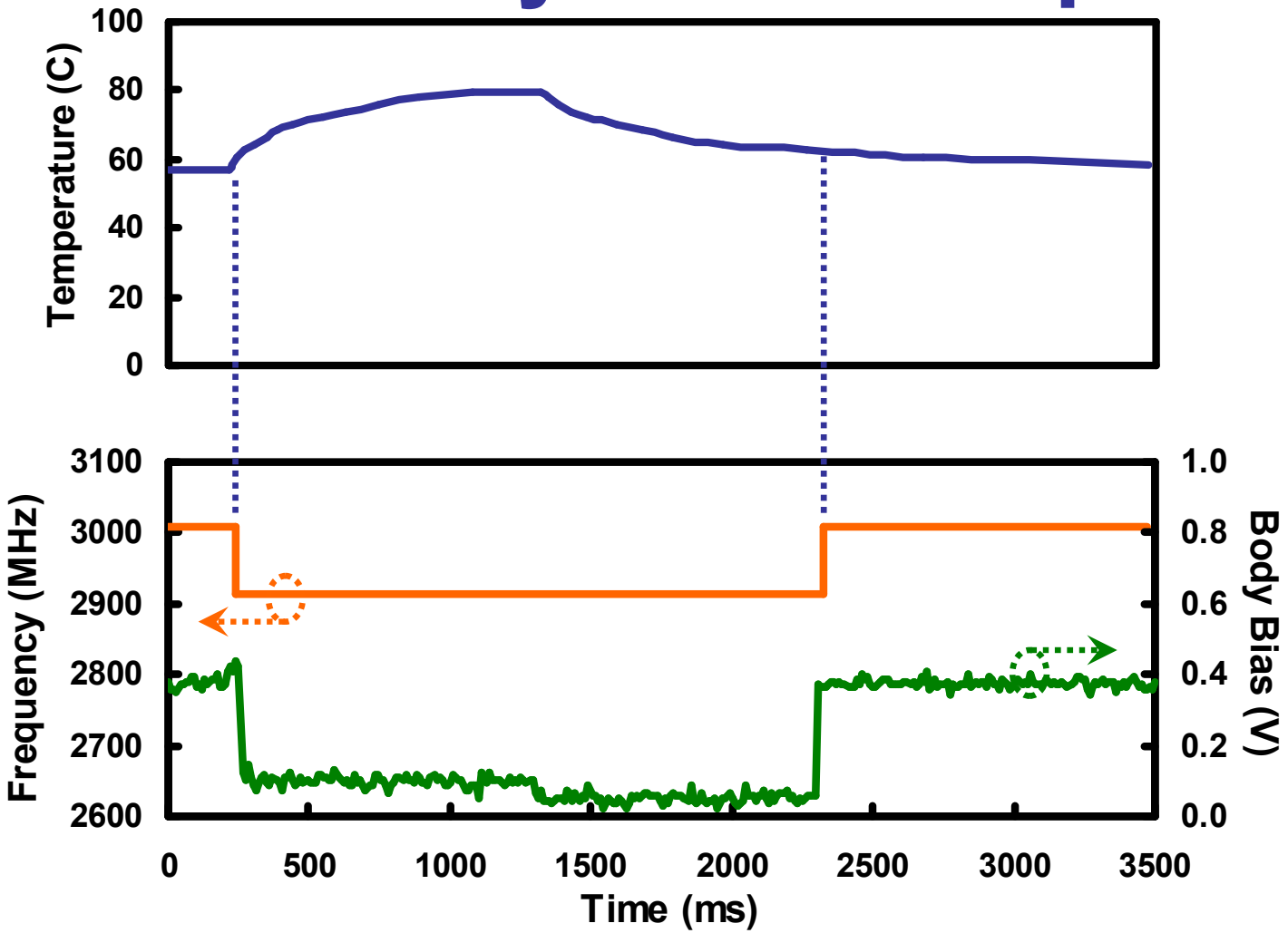
Sensors with Dynamic Voltage & Frequency (DVF) Control



- Detect temperature, V_{CC}, & aging variations
- Adapt F_{CLK} & V_{CC} to avoid timing violations

T. Fisher, et al., *JSSC*, 2006.
R. McGowen, et al., *JSSC*, 2006.
J. Tschanz, et al., *ISSCC*, 2007.

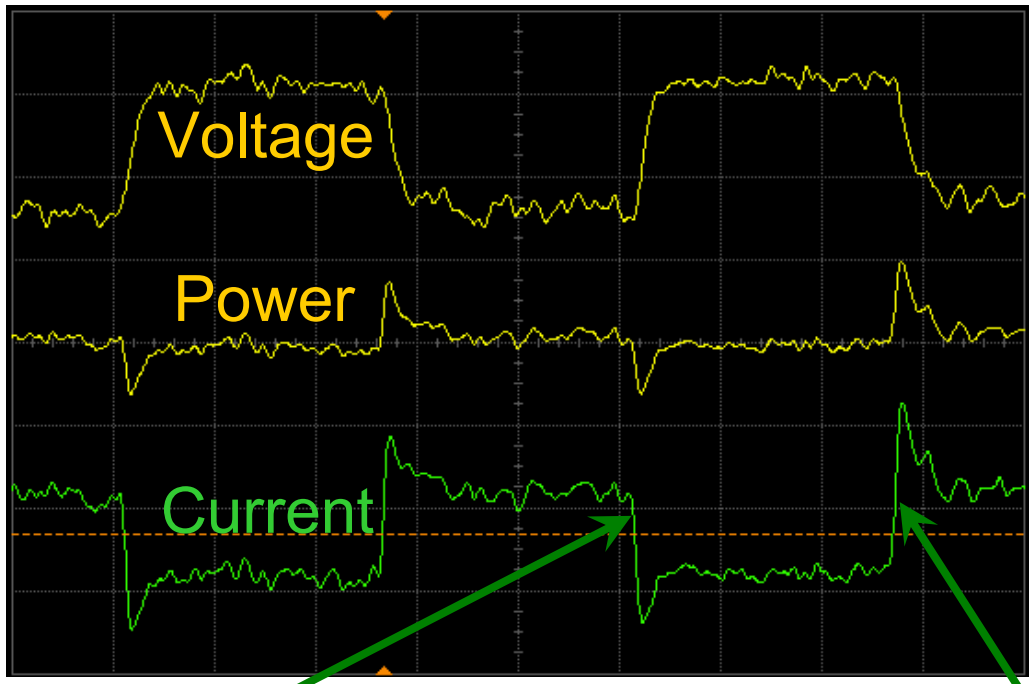
Measured Dynamic Response



- Adaptive F_{CLK} & body bias ensures correct operation & lower leakage at higher temperatures

J. Tschanz, et al., *ISSCC*, 2007.

Power Sensor with DVF



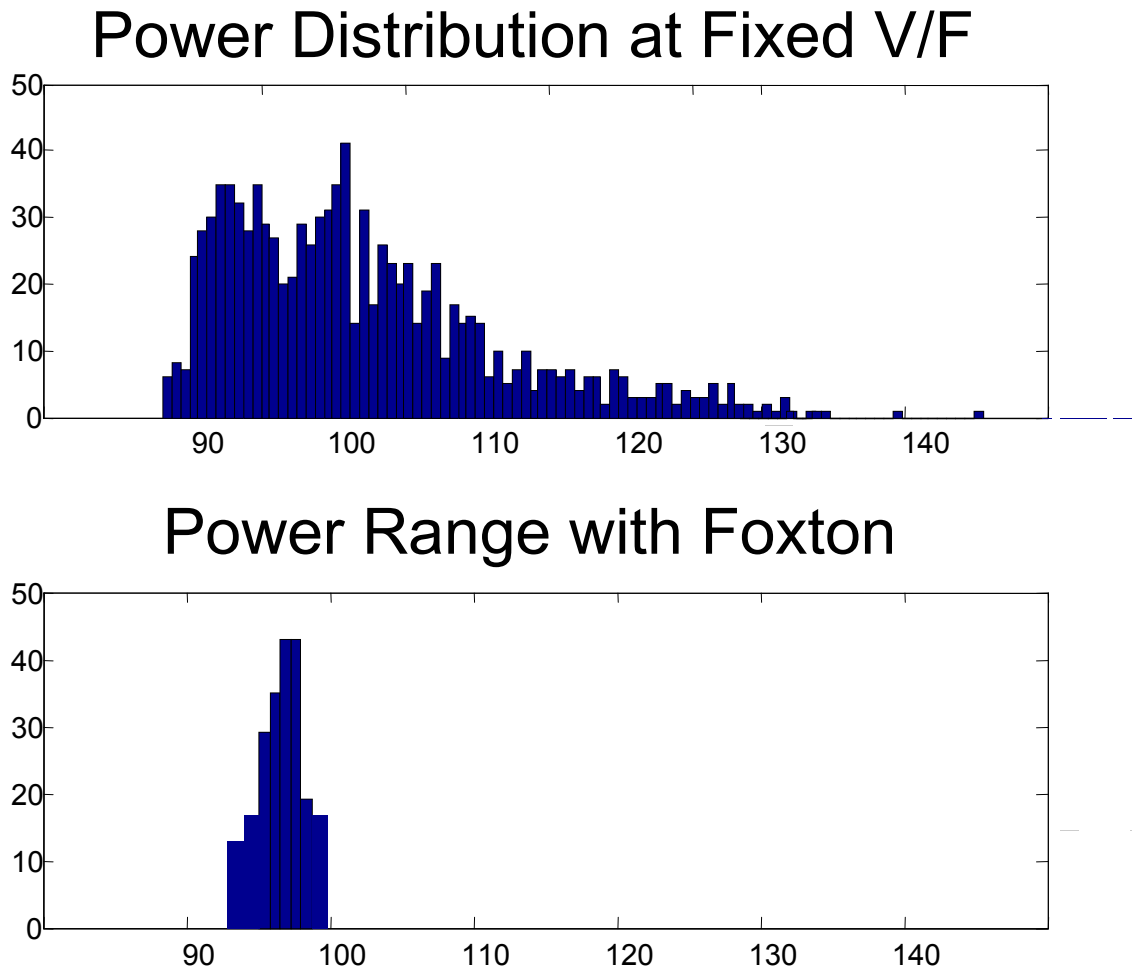
Transition to Low Power Draw

Transition to High Power Draw

- **Power management scheme increases performance within a power & thermal envelope**

T. Fisher, et al., *JSSC*, 2006.
R. McGowen, et al., *JSSC*, 2006.

Power Sensor with DVF



- **Dynamic adaptation to reduce power variation**

T. Fisher, et al., *JSSC*, 2006.
R. McGowen, et al., *JSSC*, 2006.

Sensors with Dynamic Voltage & Frequency (DVF) Control

Advantages:

- ✓ Reduces guardbands for slow-changing global dynamic variations
- ✓ Low design overhead

Disadvantages:

- – Cannot detect fast-changing or local dynamic variations
- – Requires post-silicon calibration

Summary

- **Technology trends amplify microprocessor performance & power variability**
- **Static Variations:**
  - **Within-die impacts F_{MAX} mean & leakage median**
  - **Die-to-die impacts F_{MAX} & leakage variances**
- **Dynamic Variations:**
  - **Impact F_{CLK} guardbands**
- **Variation-tolerant circuits mitigate the impact of variations on performance & power**

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Q&A