Frequency Synthesis

F. Badets

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Outline

- Introduction
  - Frequency Synthesis - Where and Why?
  - Specificactions
- Frequency Synthesizer Architectures
  - Direct Digital Synthesizer
  - Integer N PLL
  - Fractional PLL
- Implementation examples
  - Phase Interpolator based DDS
  - Multimode GSM/DCS/PCS frequency Synthesizer
  - 40 GHz PLL for 60 GHz UWB transceiver

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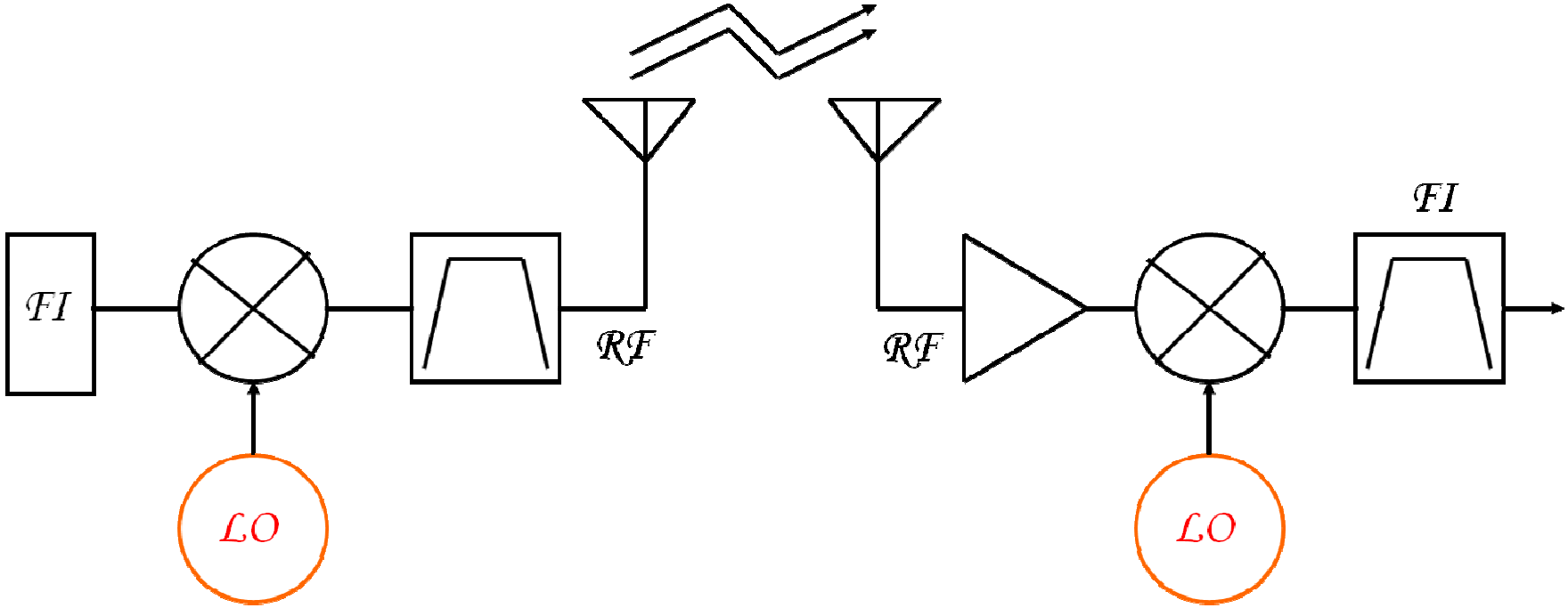
Freaquency Synthesis: Where -Why?

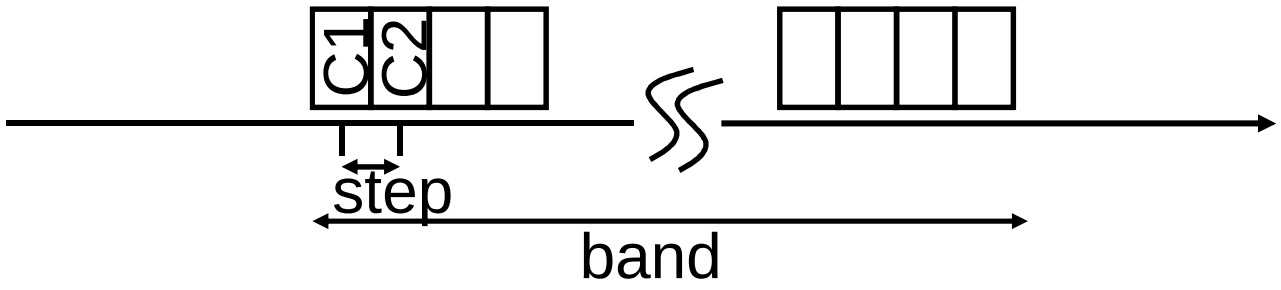


Specifications (1)

- Five principal specifications
  - 1) Frequency range
  - 2) Frequency Step
  - 3) Accuracy
  - 4) Settling time
  - 5) Phase Noise – Spurious

- Specifications are obtained from the standard under consideration and the transceiver architecture.

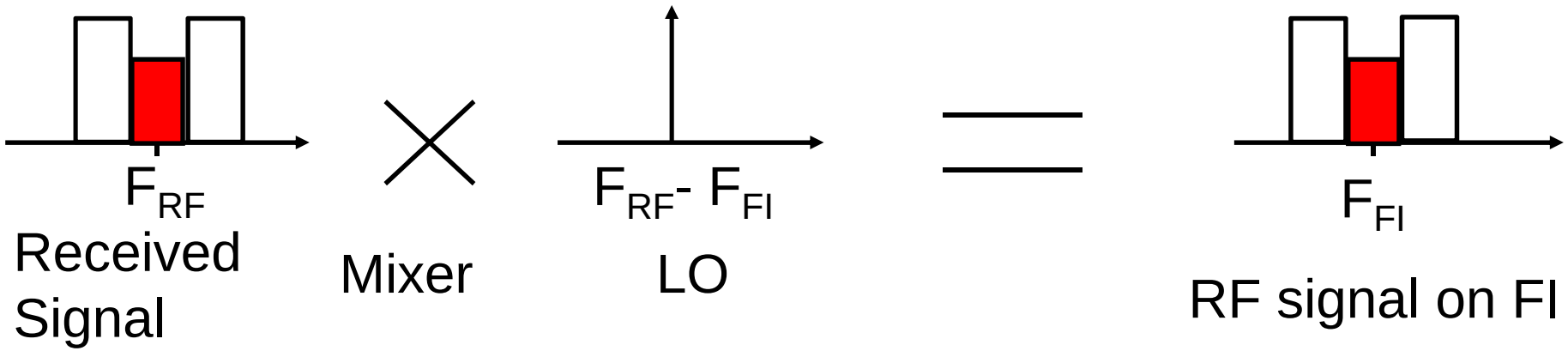
Specifications (2)



GSM example:

- RX band :935-960 MHz
- channel spacing : 200 kHz
- Settling time : 176µs maximum
- accuracy : 0.1 ppm

Phase Noise (1): Ideal Case



Ideal Case: The oscillator delivers a pure sinus

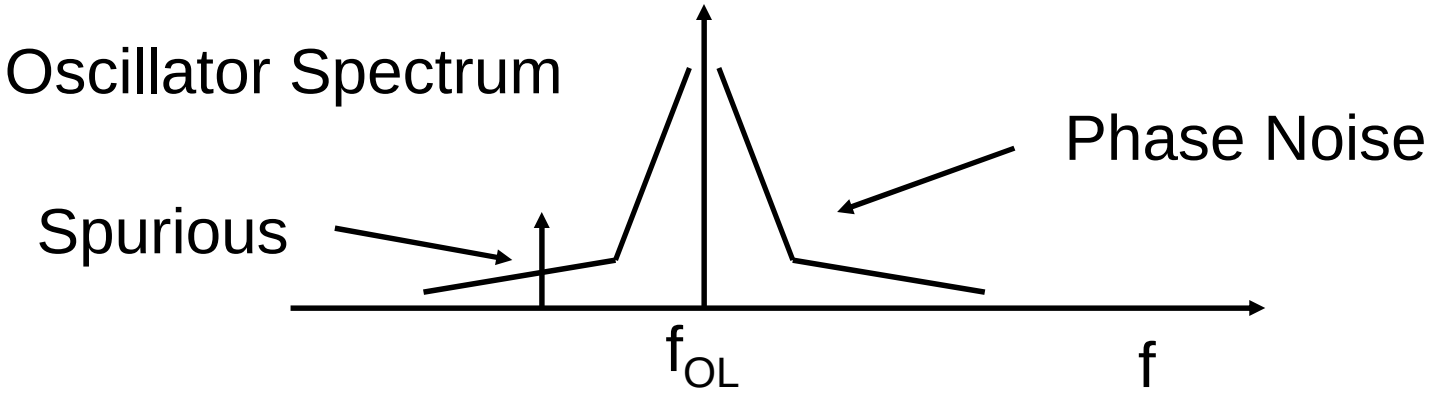
Phase Noise (2): real case

Real oscilator spectrum presents some lobs due to component noise (1/f, thermal noise…)

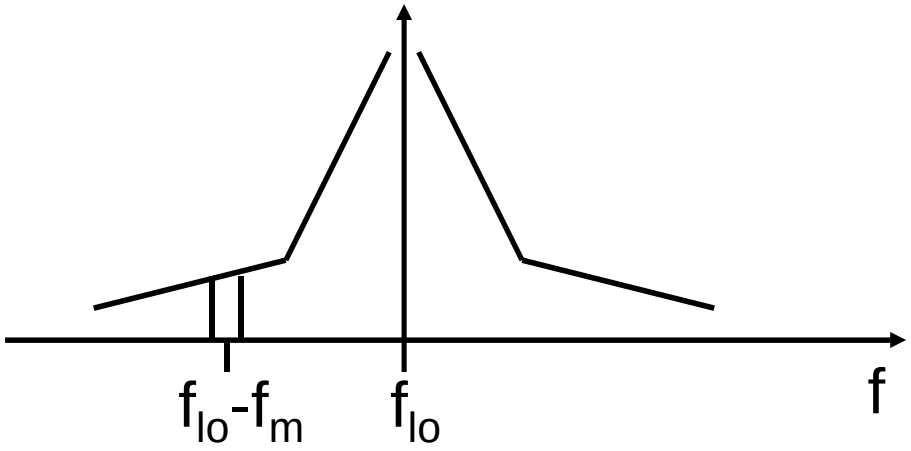
- $V_{LO}(t) = A\,Cos(\omega_{lo}t+\varphi(t))$

$= A\,Cos(\omega_{lo}t)\,Cos(\varphi(t)) - A\,Sin(\omega_{lo}t)\,Sin(\varphi(t))$

$= A\,Cos(\omega_{lo}t) - A\,\varphi(t)\,Sin(\omega_{lo}t)$

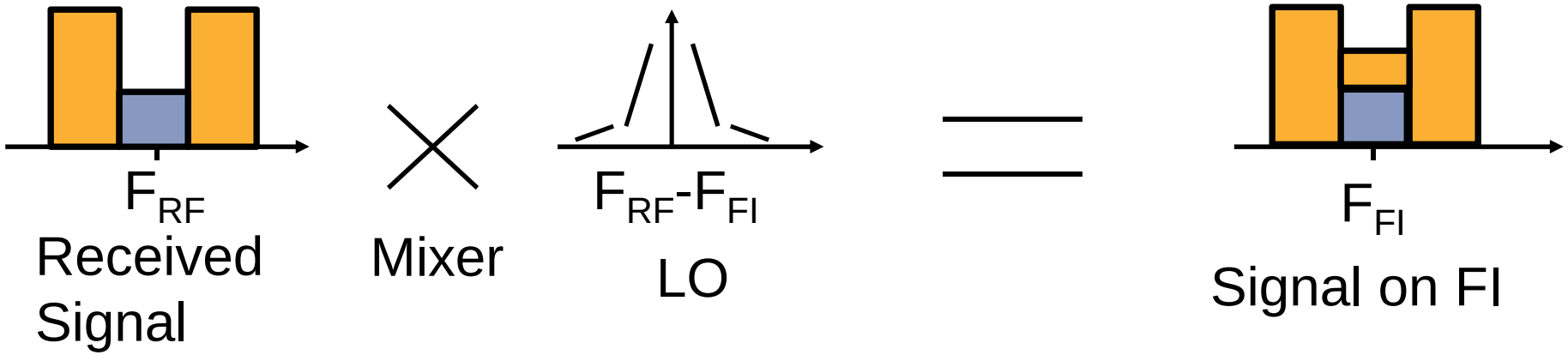


Phase noise (3): measurement unit



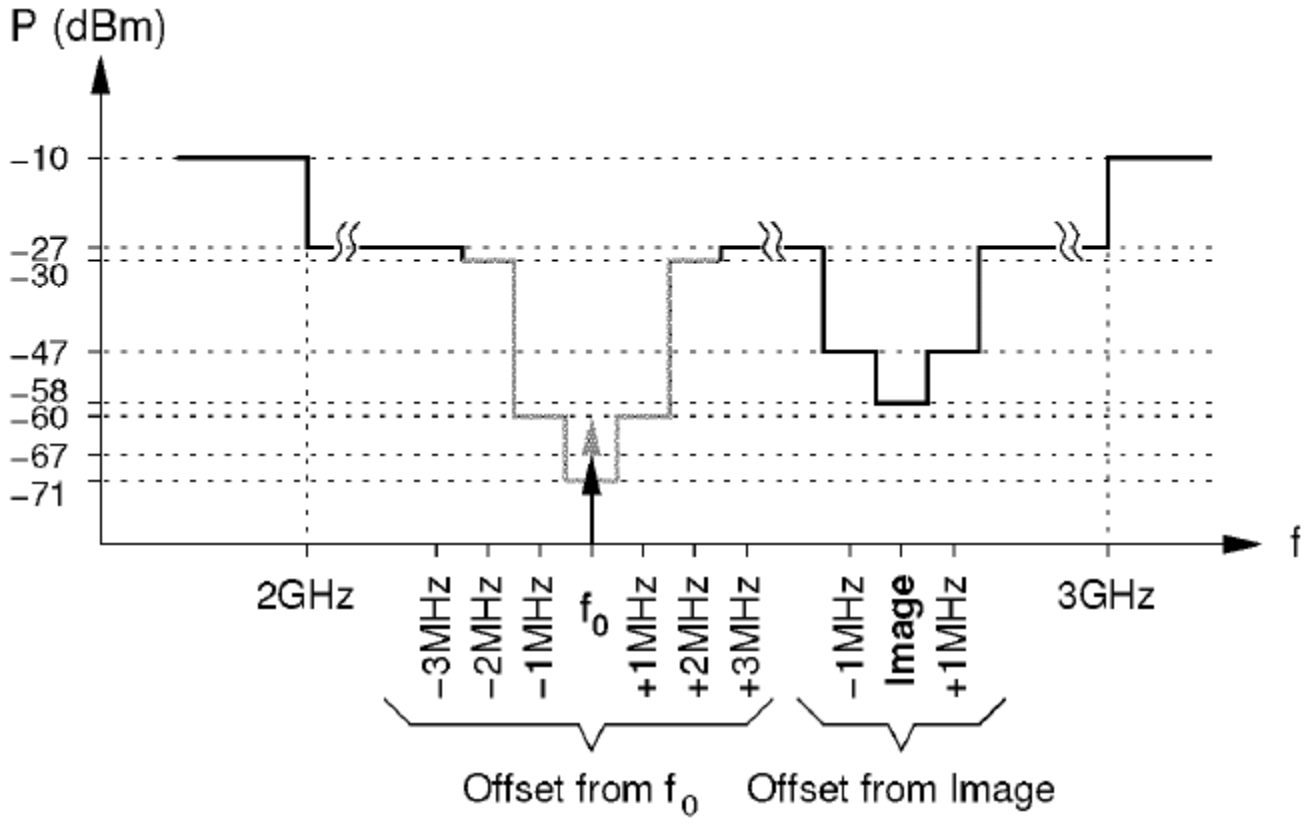
$$L(f_m) = 10\,log_{10}\left(\frac{P(f_0 + f_m)\ in\ 1\ Hz\ band}{P_{carrier}}\right)$$

Phase Noise (4): consequences on mixing



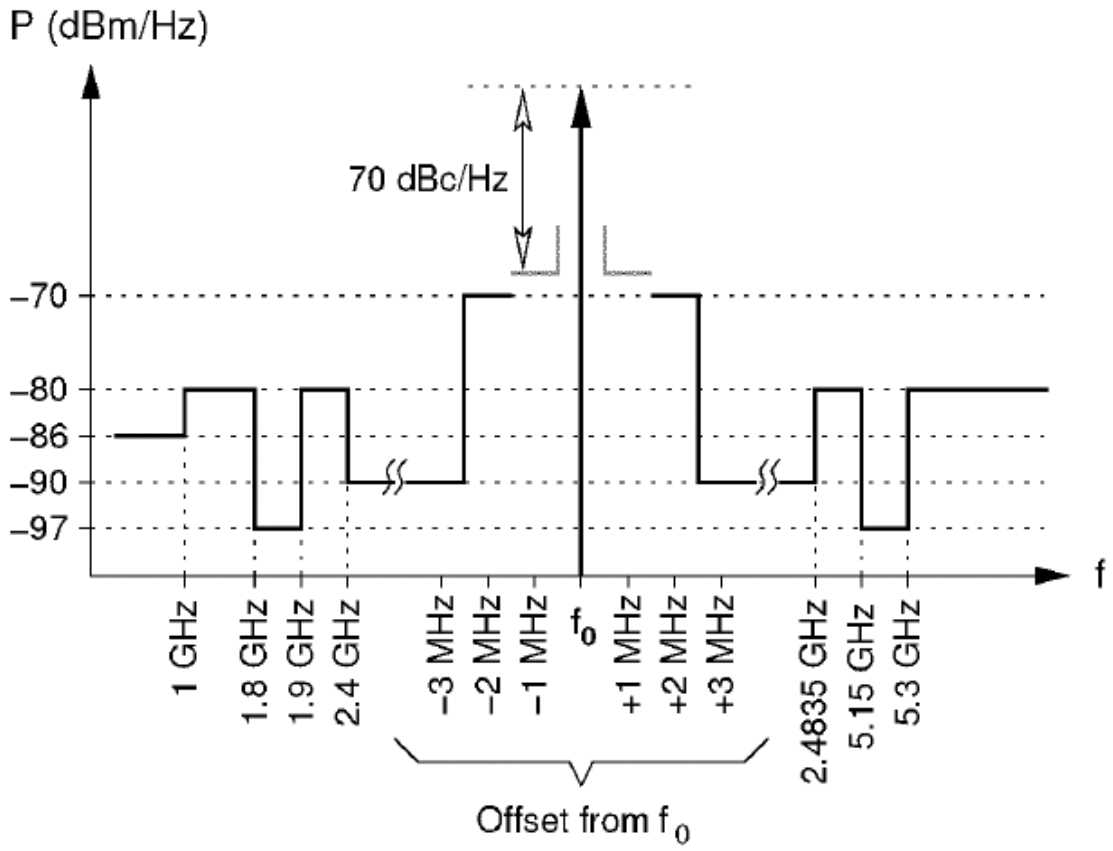
- Signal to be received between strong interferers in adjacent channel
- LO phase noise down-converts interferers in FI : signal corruption

RX specification translation



$$L(fm) = \frac{C}{I(fm)} - \frac{C}{I_{cc}} - 10\log(BW)$$

TX specification translation



$$L(fm) = CP - AP(fm) - 10\log(BW)$$ In dBc/Hz

CP : carrier power

AP : allowed transmitted power in channel considered

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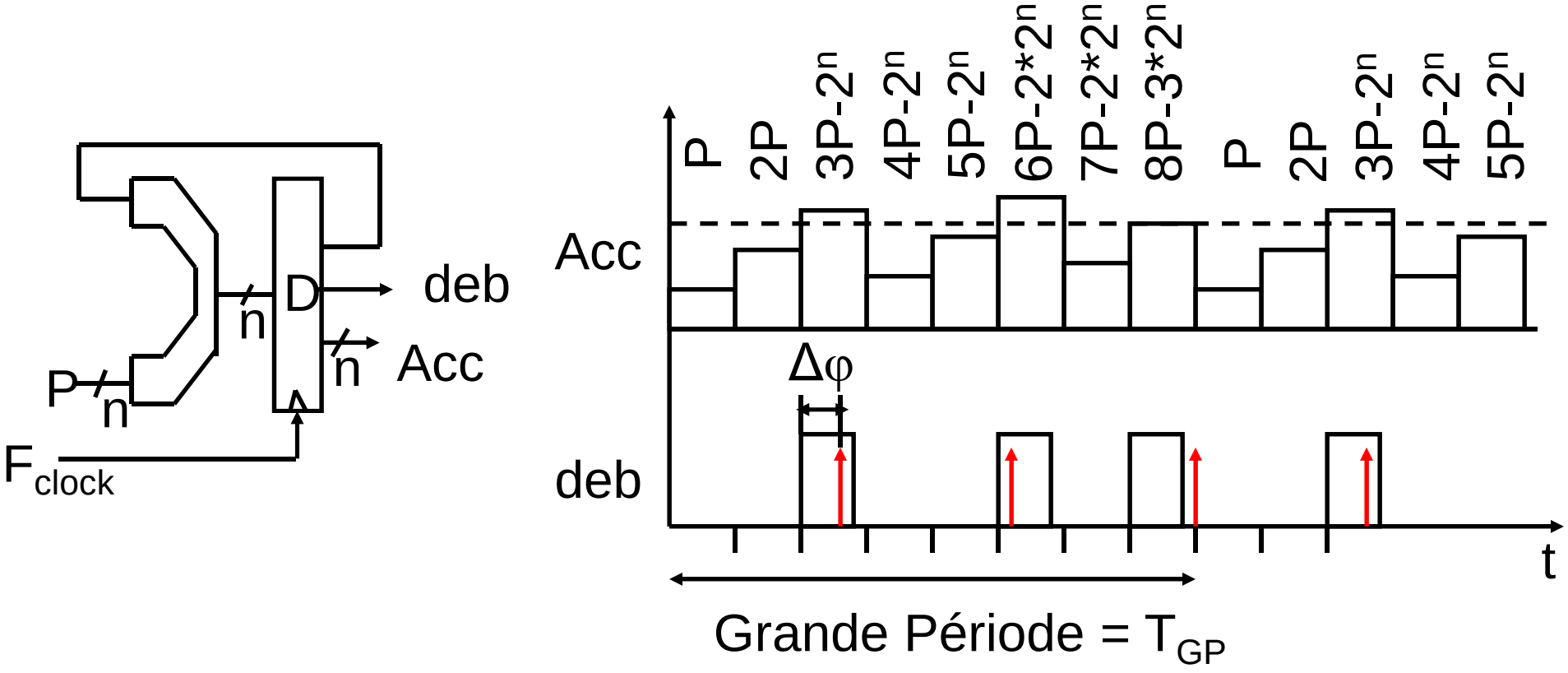
Pulse Output Direct Digital Synthesizer (1)

Key Component : phase accumulator



Pulse Output DDS (2)

- Output is periodic. Period when output comes back to 0. It is equal to x. Tclock, where x is the smallest integer value as:

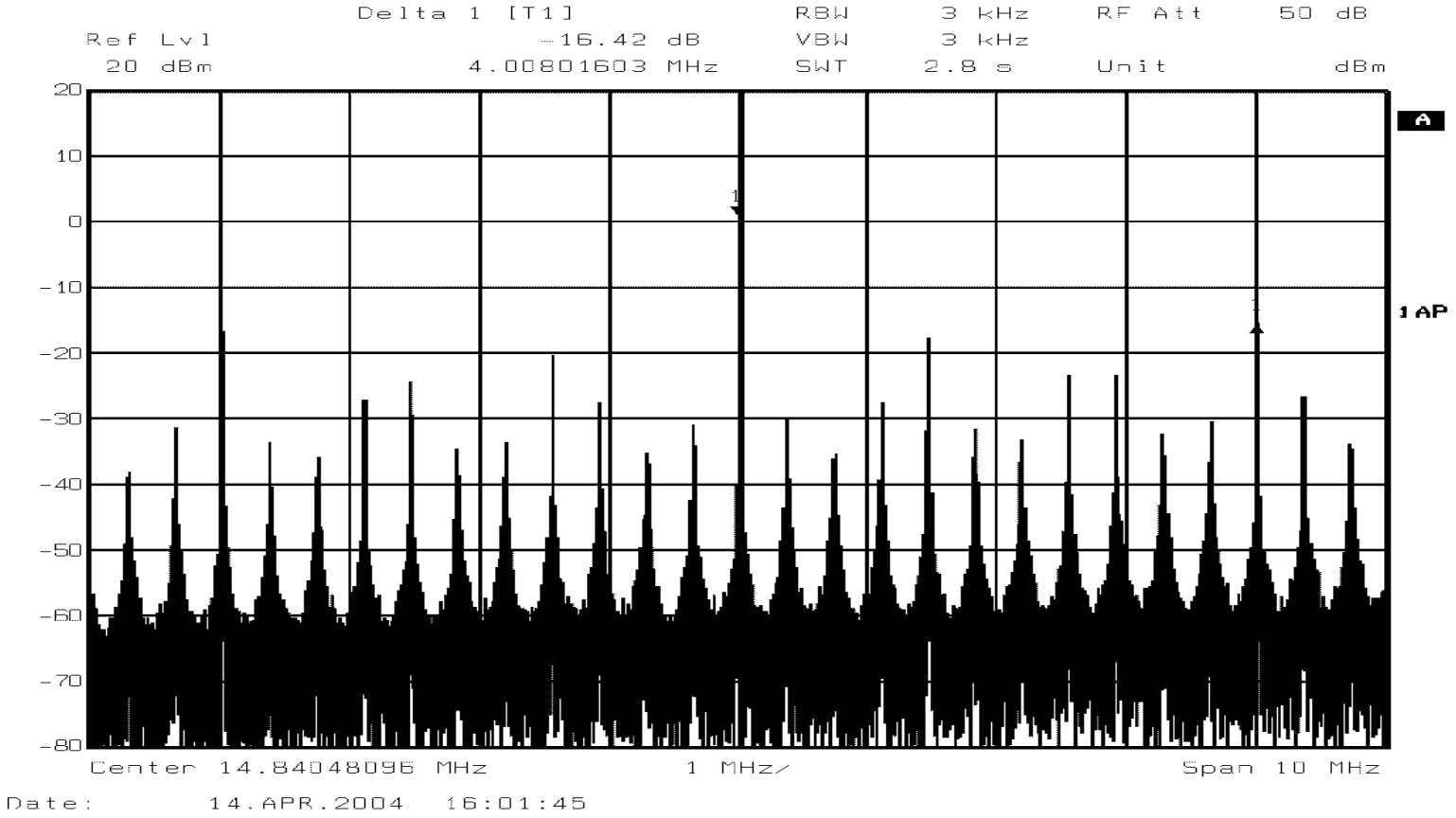
$$x = y\frac{2^n}{p}$$

  - x is the number of time p is added
  - y is the number of time of overflow
- Frequency synthesis possible using overflow bit

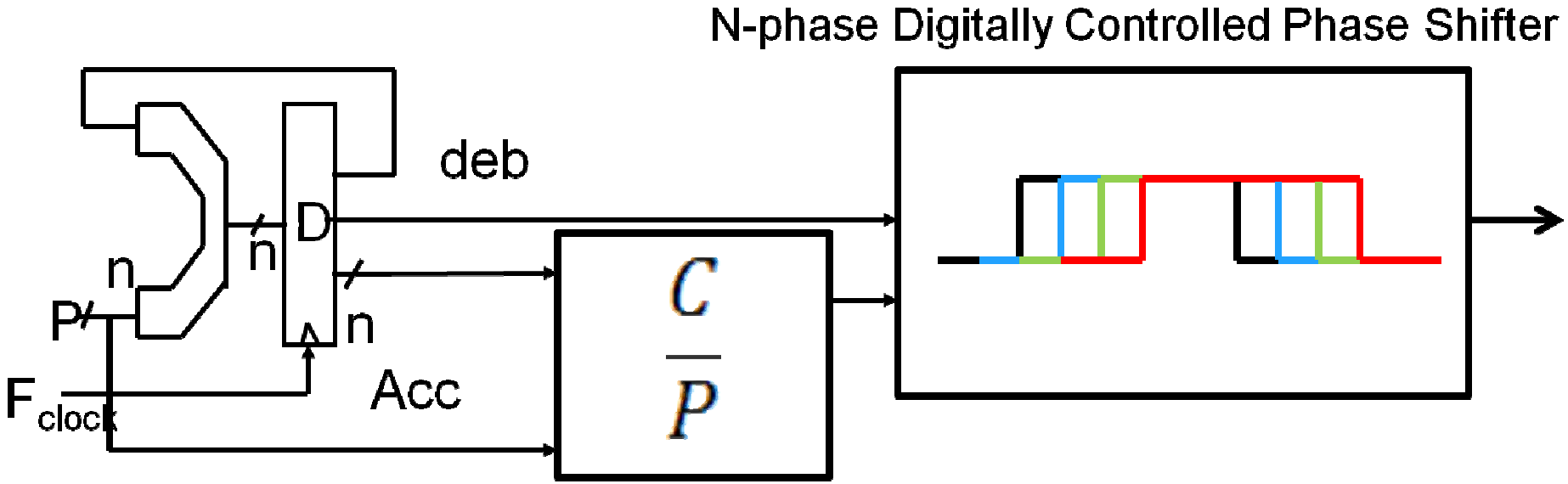
$$f_{ovw} = \frac{p}{2^n} f_{clk}$$

Pulse Output DDS (3)

- Frequency true on average only: lot of spurious tones separated by 1/(x.Tck)



Pulse Output DDS (4): Phase Interpolator

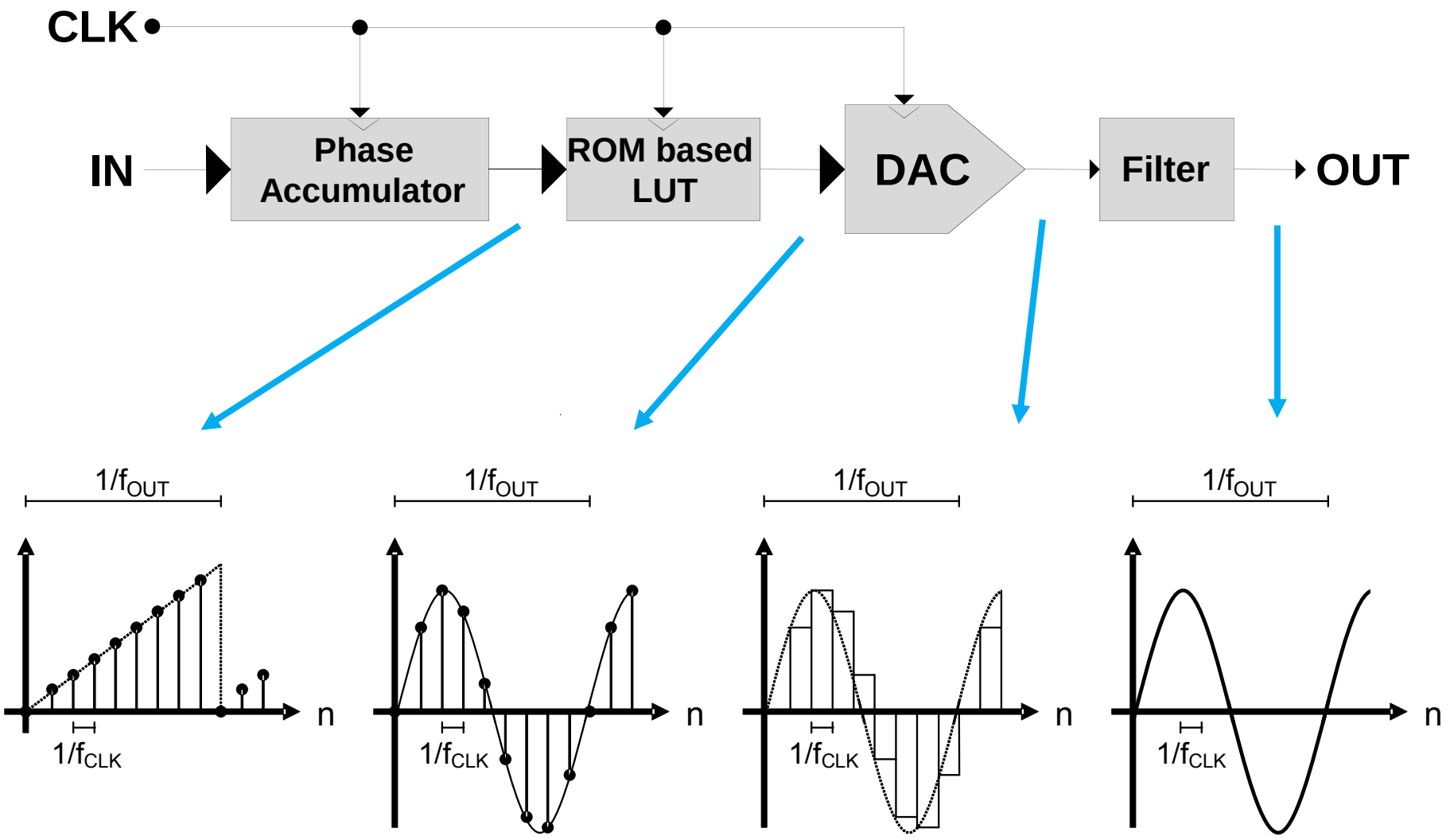


- Every overflow occurence, phase accumulator value is a digital information of the phase error between generated signal and spuriousless ideal signal
- Solution to decrease spurious tones:
  - Calculation C/P (not trivial as P could take any value between 1 and 2^(n-1)
  - Ratio value is used to select the phase that interpolates the best the ideal signal.

Pulse Output DDS (5): Advantages / Drawbacks

- Advantages
  - High resolution++
  - Good Phase noise+
  - Switching time++
  - Easy phase and frequency modulation++
- Drawbacks
  - High level spurious tones

ROM based DDS (1)



ROM based DDS (2)

- Advantages
  - High resolution++
  - Good phase noise+
  - Switching time++
  - Easy phase and frequency modulation++
- Drawbacks
  - Low Frequency due to ROM based LUT acces time. Fout limited to Fclk /10 for better filtering
  - Power increases with DDS bandwidth
  - DAC degrades performances at high frequencies

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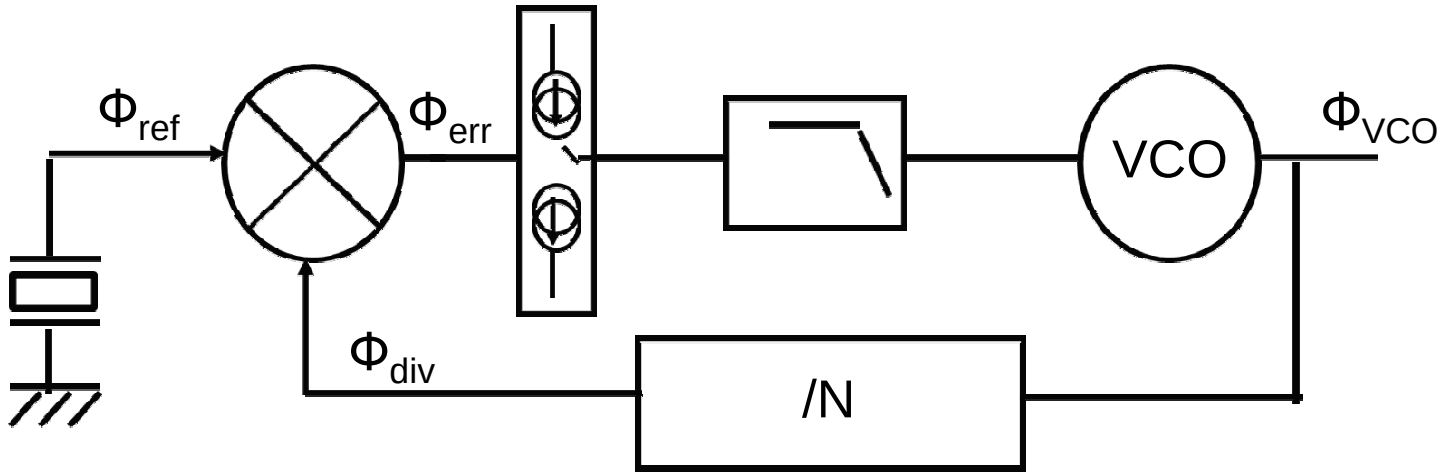
Integer-N Frequency Synthesizer (1)



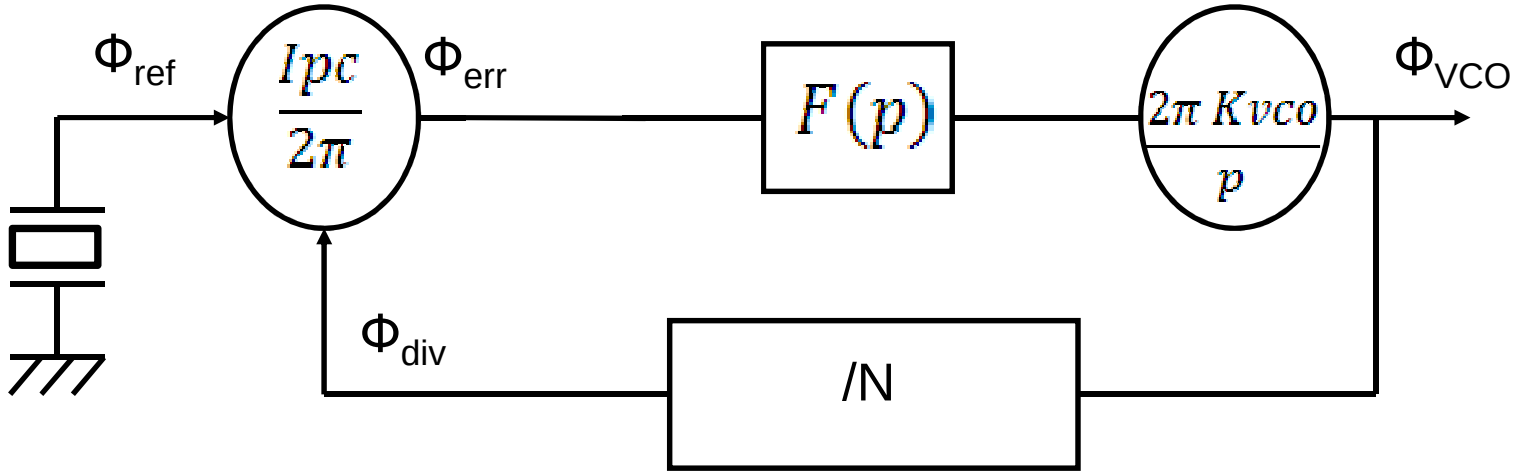
- Once Loop Locked Φ_{div} tracks Φ_{ref} variations

$$\varphi_{err} = \varphi_{ref} - \frac{\varphi_{VCO}}{N} = Cste \Rightarrow f_{VCO} = N f_{ref}$$

Integer-N frequency synthesizer (2)

- Frequency range: N should be programmable with a sufficent range.
- Step = Fref -> should be equal to channel width
- Accuracy = will copy the reference accuracy (usually a pure crystal based oscillator)
- Settling time will constrain loop bandwidth (need small signal analysis)
- Phase noise will constrain the PLL block contributions (need of a loop noise analysis)

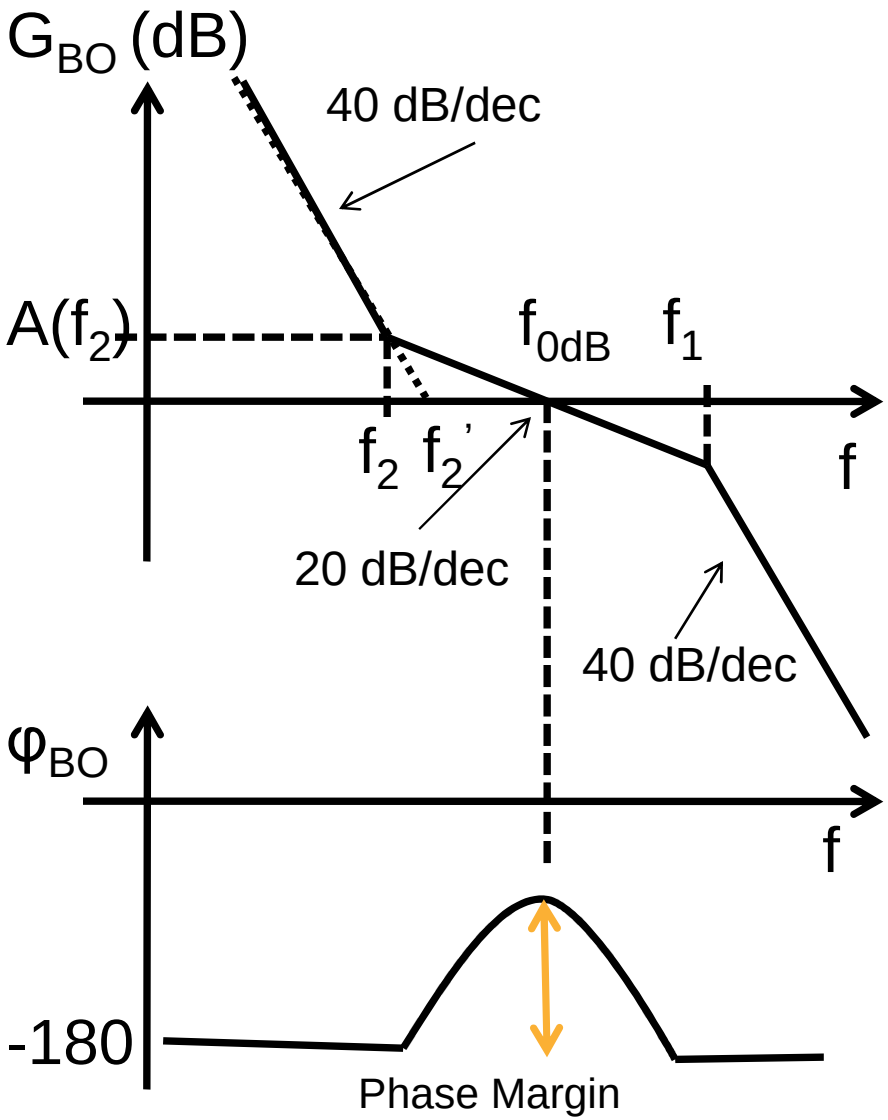
Integer–N : small signal analysis



$$BO(p) = \frac{I_{pc}.F(p).Kvco}{N.p}$$

$$H(p) = N.\frac{BO(p)}{1 + BO(p)}$$

Open Loop Bode Diagramm



- PLL order = loop filter order +1 due to VCO pole
- To ensure robustness over process variations:

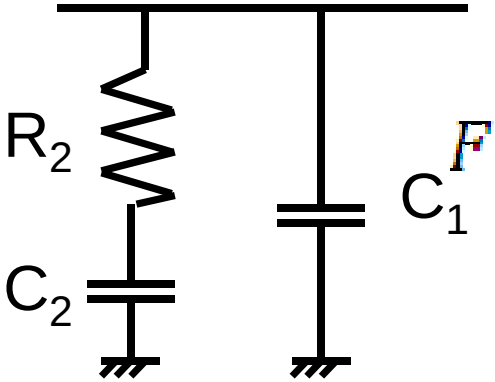
$$f_{0dB} = \sqrt{f_1.f_2}$$

- Phase margin depends on f_2/f_1 ratio (should be greater than 10 for PM > 45º)
- Relation between f_2 f'_2 and f_{0dB}

$$40 \log \frac{f'_2}{f_0} = 20 \log \frac{f_0}{f_2}$$

Example 3rd order Type II PLL (1)

- Loop filter structure:



$$F(p) \approx \frac{1}{C_2 p}.\frac{1+R_2C_2p}{1+R_2C_1p} = \frac{1}{C_2 p}.\frac{1+2\pi.f_2p}{1+2\pi.f_1p}$$

$$f_{0dB} = \sqrt{f_1.f_2} \quad \& \quad f_1 = 10.f_2 \Rightarrow f_{0dB} = \frac{f_2}{\sqrt{10}}$$

$$f_2' = 10^{\frac{-1}{4}}.f_0$$

- At low frequencies open loop :

$$BO(p) \approx \frac{I_{pc}.Kvco}{C_2.N.p^2} \Rightarrow 1 = \frac{I_{pc}.Kvco}{C_2.N.(2\pi.f_2')^2}$$

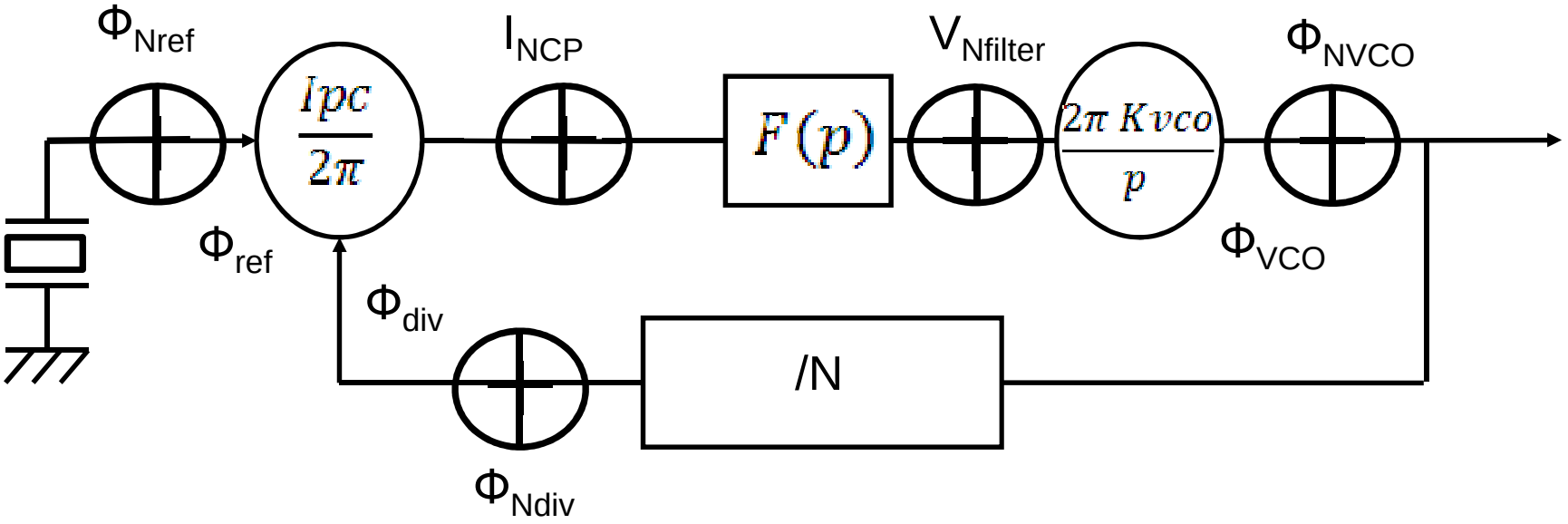
Example 3rd Type II PLL (2): summary

- Calculation of needed filter:
  - Fixed parameters : VCO gain, Loop divider ratio
  - 1st step : determination of needed lopp bandwidth (~f_{0dB})
  - 2nd step: from f_{0dB} calculation of f_1, f_2 and f'_2
  - 3rd step: fixing charge pump current value (PFD gain), calculation of C_2
  - 4th step :from expression of f_2 calculation of R_2
- Of course, fixing resistor value in step 3 and determining charge pump current in step 4 is another option
- Loop bandwidth, resistor and charge pump current values are to be compliant with overall frequency synthesizer specification in term of settling time, phase noise, power consumption etc.

Integer-N small signal analysis

- PLL : time-sampled system -> should be modeled using z-transform! Non trivial modelization.
- Sampling process arises in feedback loop divider. Linear modelisation possible for $f < f_{outDiv}/10$
- PLL is non linear. Transfer function could be used to predict the settling time from one locking state to another one only if the PFD doesn't enter frequency discrimination process
- Small signal analysis could be implemented on math software or in electrical simulators using verilog-A models

Integer- N PLL noise analysis (1)



- Noise analysis: using small signal model
- All contribution are additive noises
- Calculation mode:
  - Noise of each blocks simulated at transistor level
  - Determination of the contribution of each noise source to the overall output noise

Integer-N phase Noise Analysis (2)

- Reference and Divider output noise contribution

$$\varphi^2_{outNref} = N^2\left(\frac{BO(p)}{1+BO(p)}\right)^2.\varphi^2_{Nref}$$

$$\varphi^2_{outDiv} = N^2\left(\frac{BO(p)}{1+BO(p)}\right)^2.\varphi^2_{NDiv}$$

  - Reference and Divider noise are low pass filtered

Integer-N phase Noise Analysis (3)

- Charge Pump output noise contribution

$$\varphi^2_{outNicp} - \left(\frac{N.2\pi}{I_{cp}}\right)^2 \left(\frac{BO(p)}{1+BO(p)}\right)^2 . i^2_{NCP}$$

  - Low pass filtering

- Filter resistors output noise contribution

$$\varphi^2_{outNfilter} = \left(\frac{N.2\pi}{I_{cp}F(p)}\right)^2 \left(\frac{BO(p)}{1+BO(p)}\right)^2 . v^2_{Nfilter}$$

  - Bandpass filtering

- VCO output noise contribution

$$\varphi^2_{outNVCO} = \left(\frac{1}{1+BO(p)}\right)^2 . \varphi^2_{NVCO}$$

  - High pass filtering

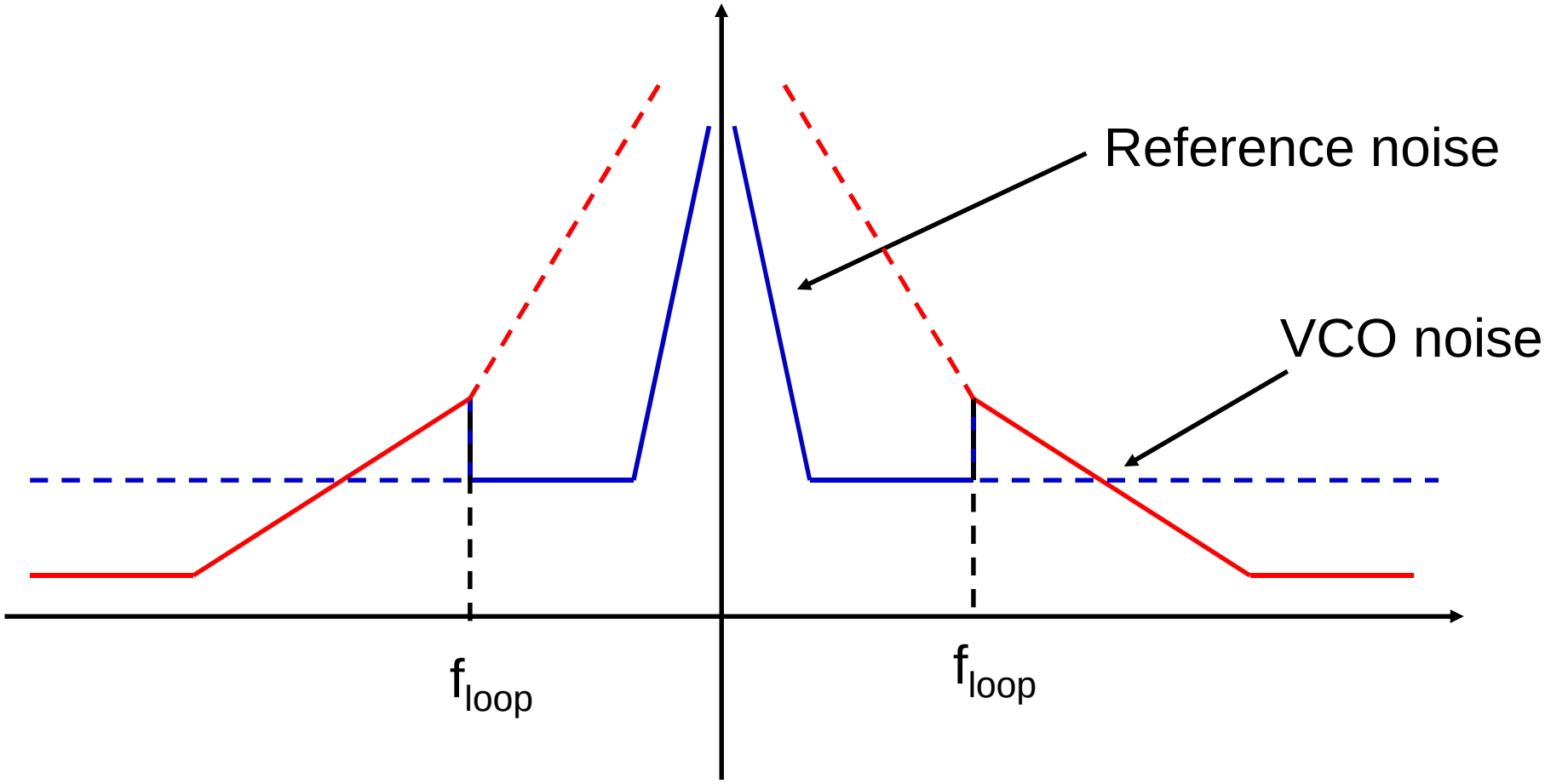
Integer-N phase Noise Analysis (4)

- Total PLL output noise:

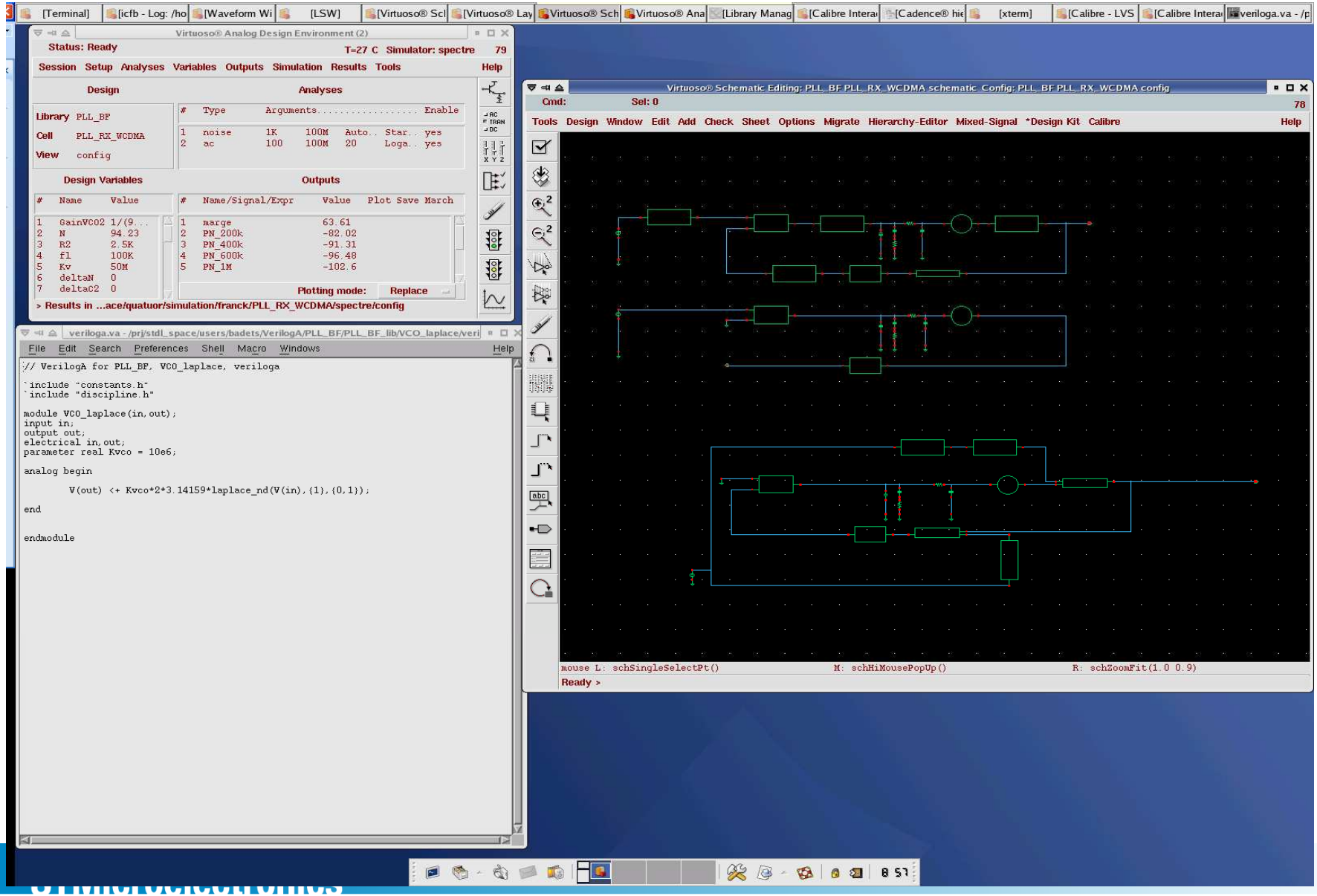
$$\varphi^2_{Total} = \varphi^2_{outNVCO} + \varphi^2_{outNfilter} + \varphi^2_{outNicp} + \varphi^2_{outDiv} + \varphi^2_{outNref}$$

- Total PLL output phase noise could be easy calculated using a math software or using an electrical simulator with parametrised verilog-A models
- Phase noise analysis and small signal analysis has to take into account PVT, non linearity of VCO gain

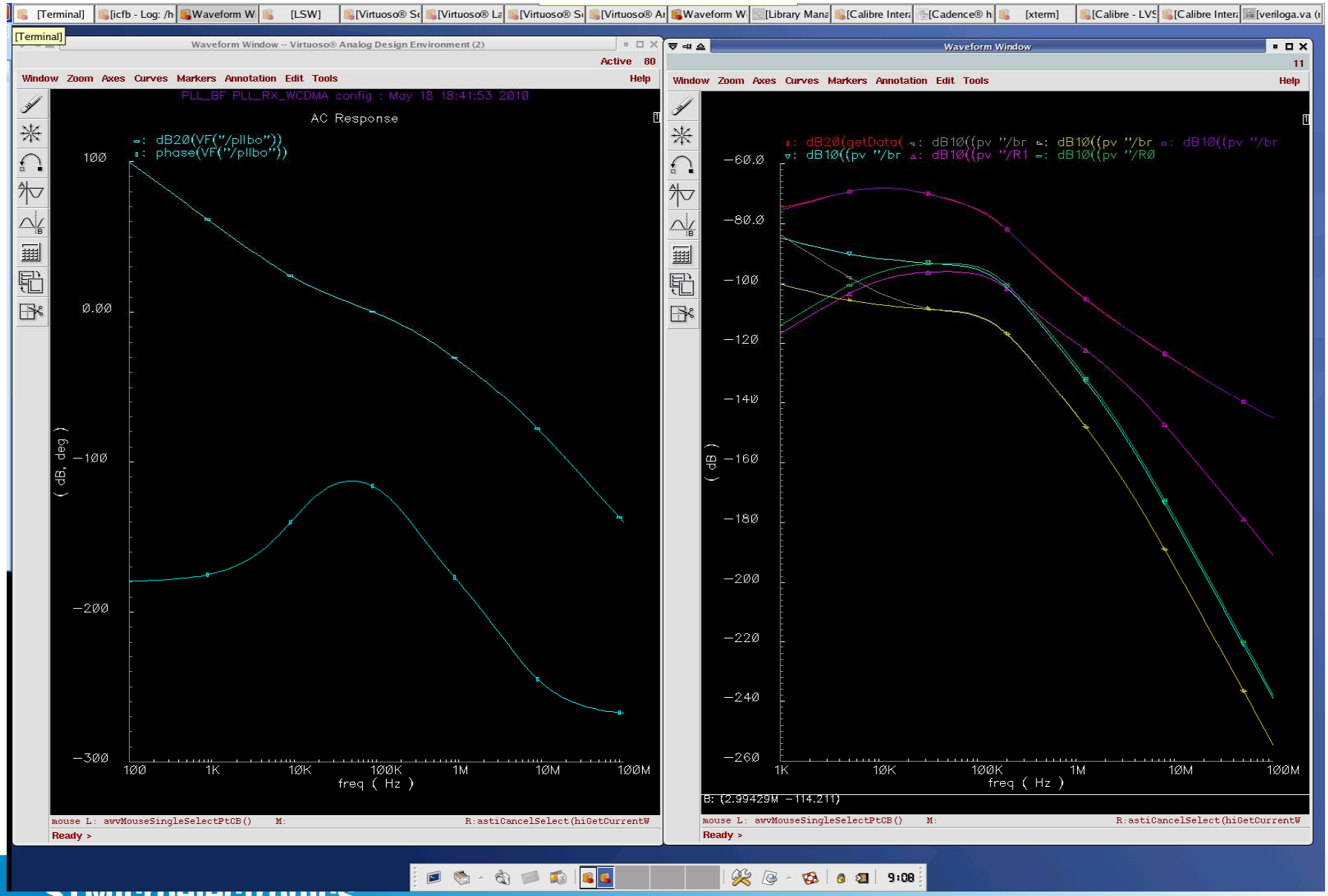
Integer-N PLL: Output Phase Noise



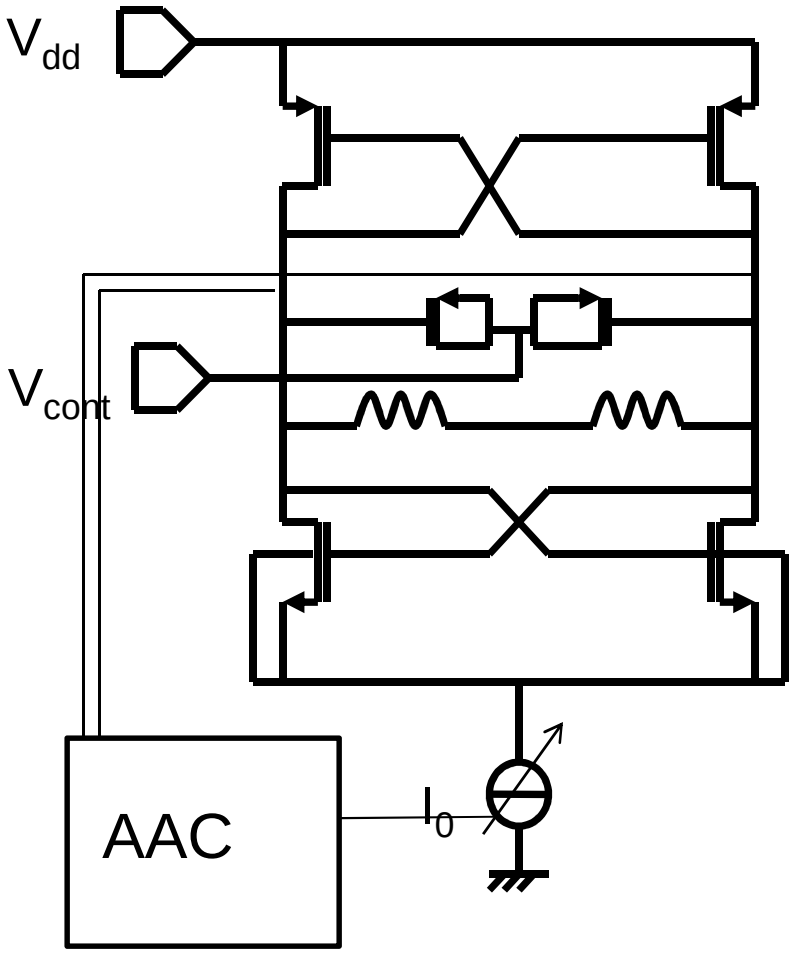
VerilogA Small Signal Analysis (1)



VerilogA Small Signal Analysis (2)

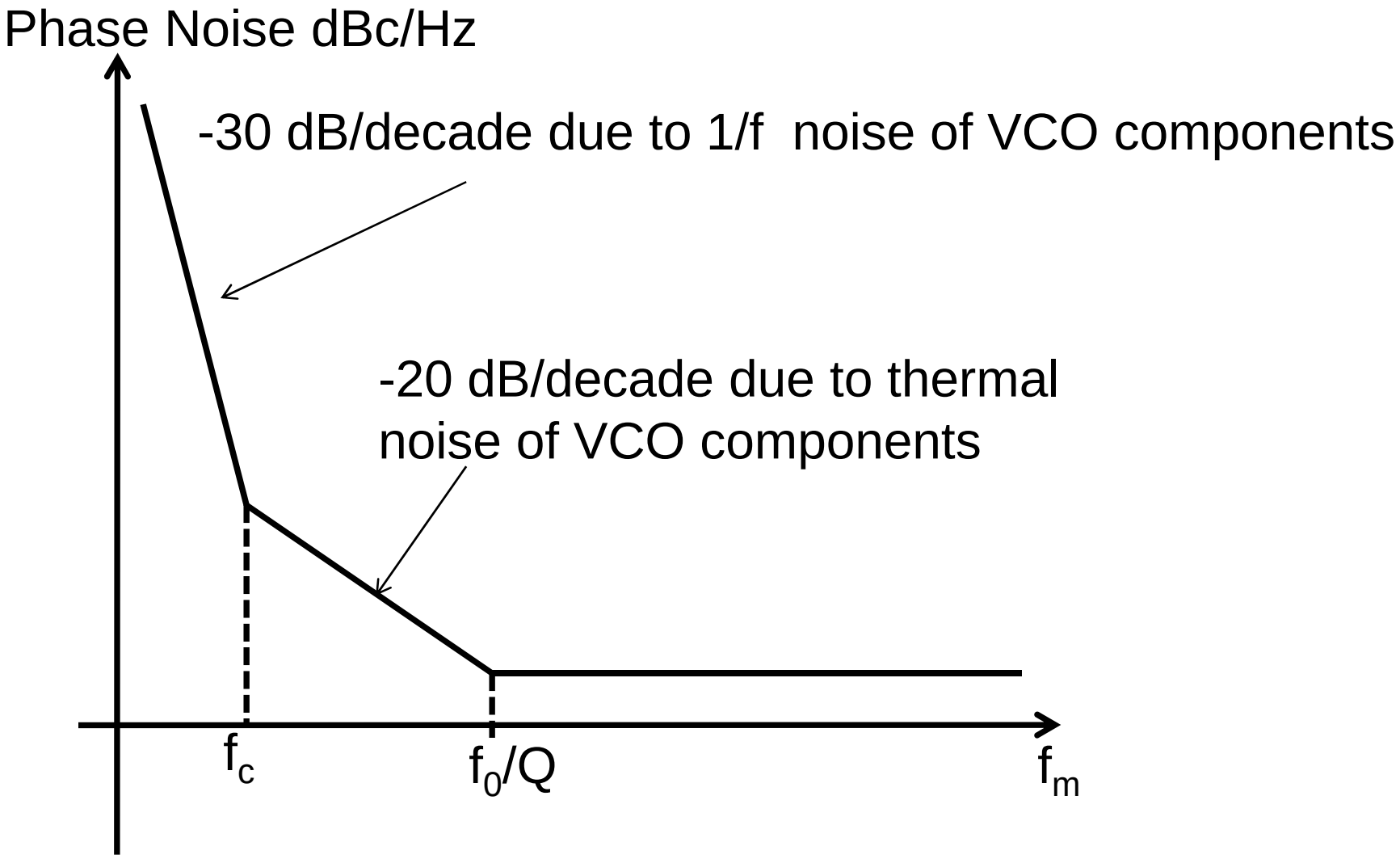


Block Design : VC0 (1)

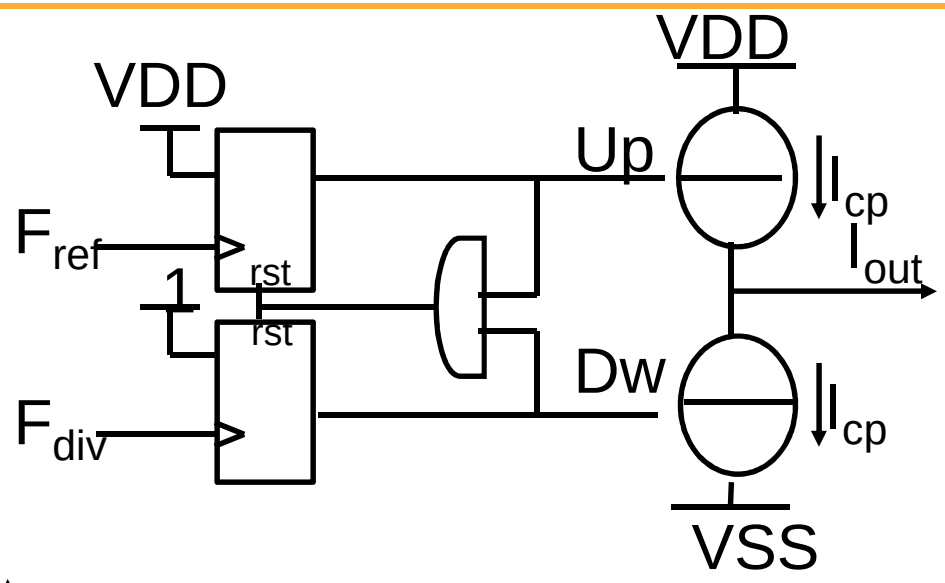


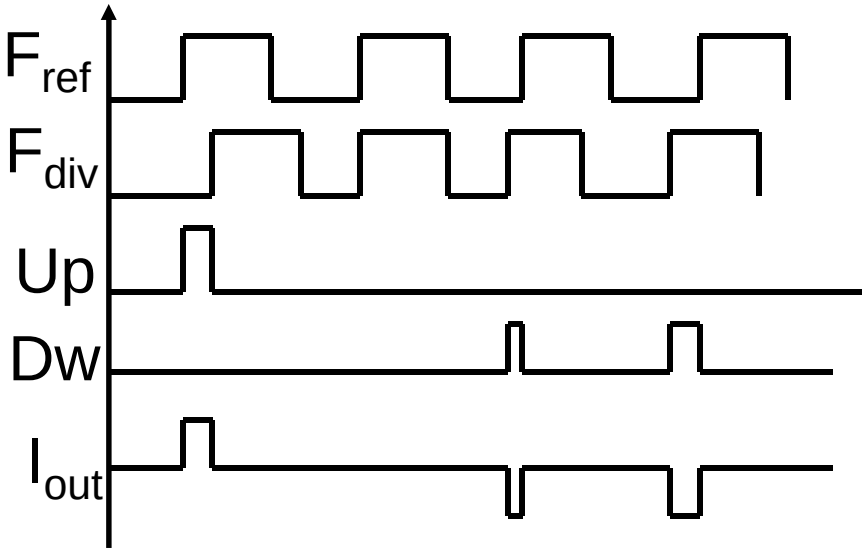
- Usually VCO are LC CMOS oscillators.
  - Silicon inductor Q is about 20
  - Tuning using MOS varactor or Diode Varactor Q ~ 50
  - PVT covered thanks to a bank of capacitor
  - For better noise immunity an automatic amplitude control is used

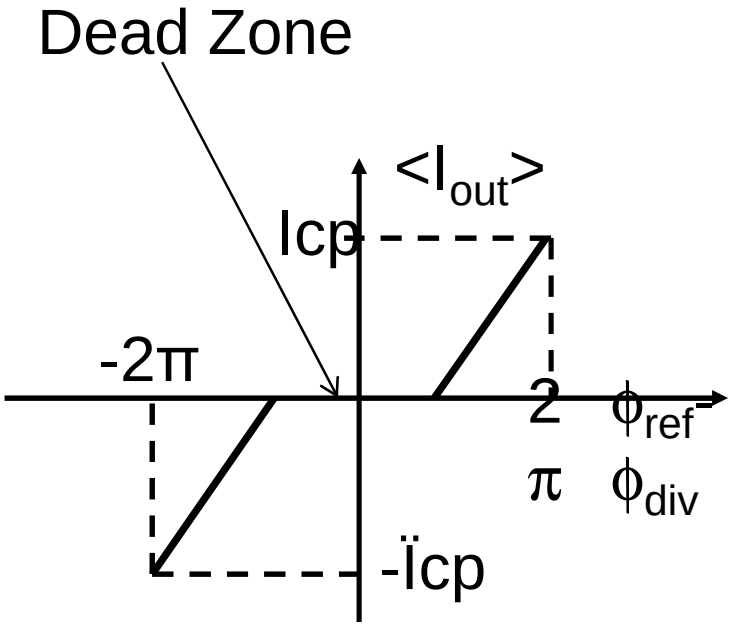
Block Design: VCO phase Noise Profile



Phase Frequency Detector (1)







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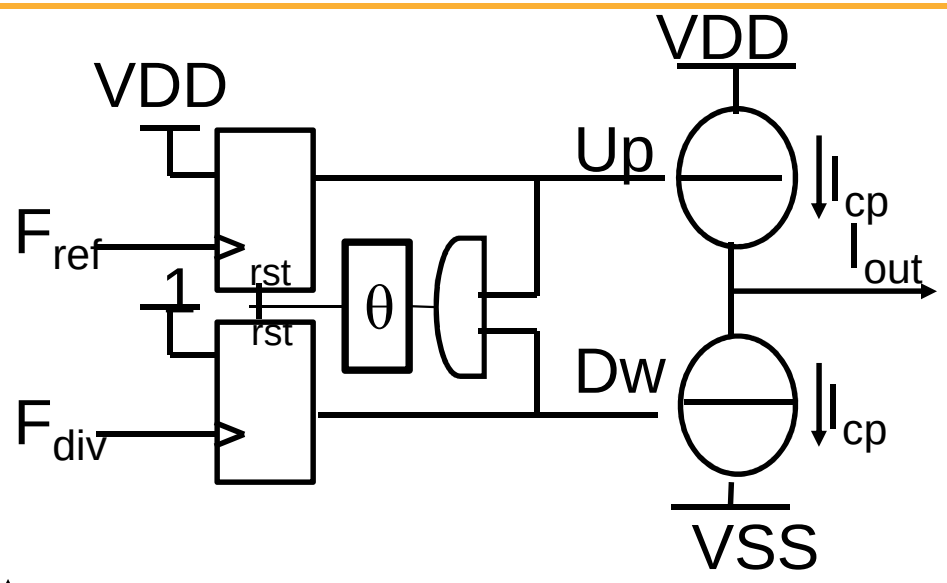
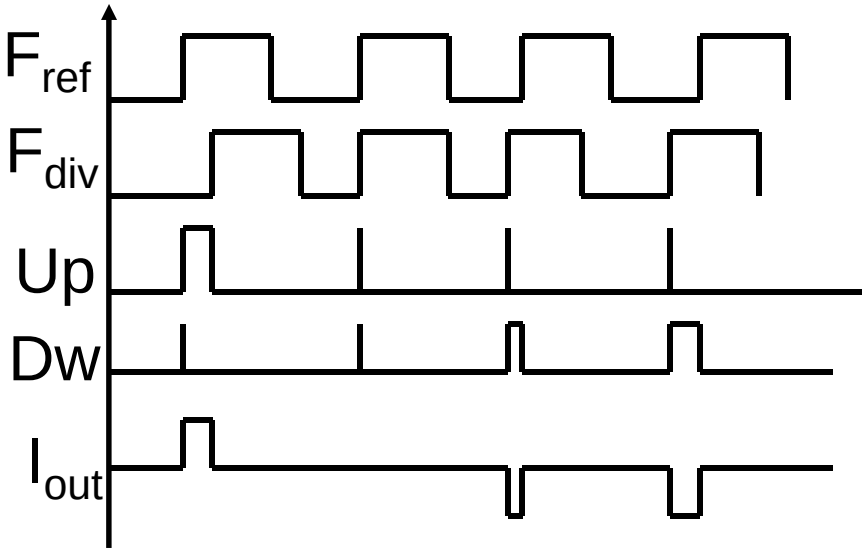
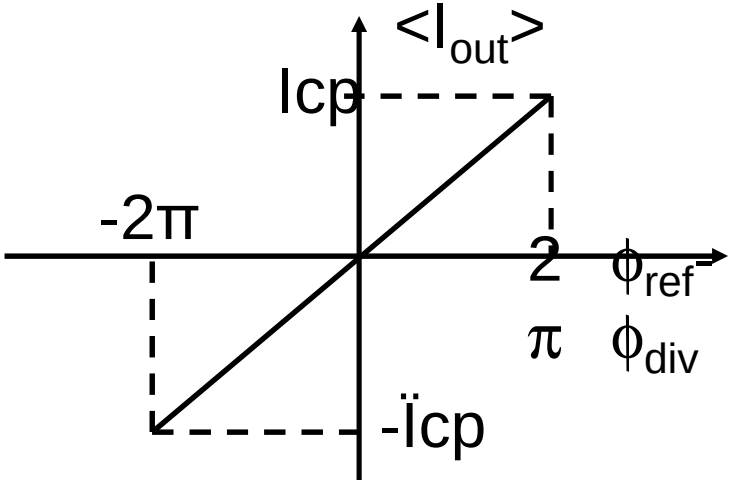
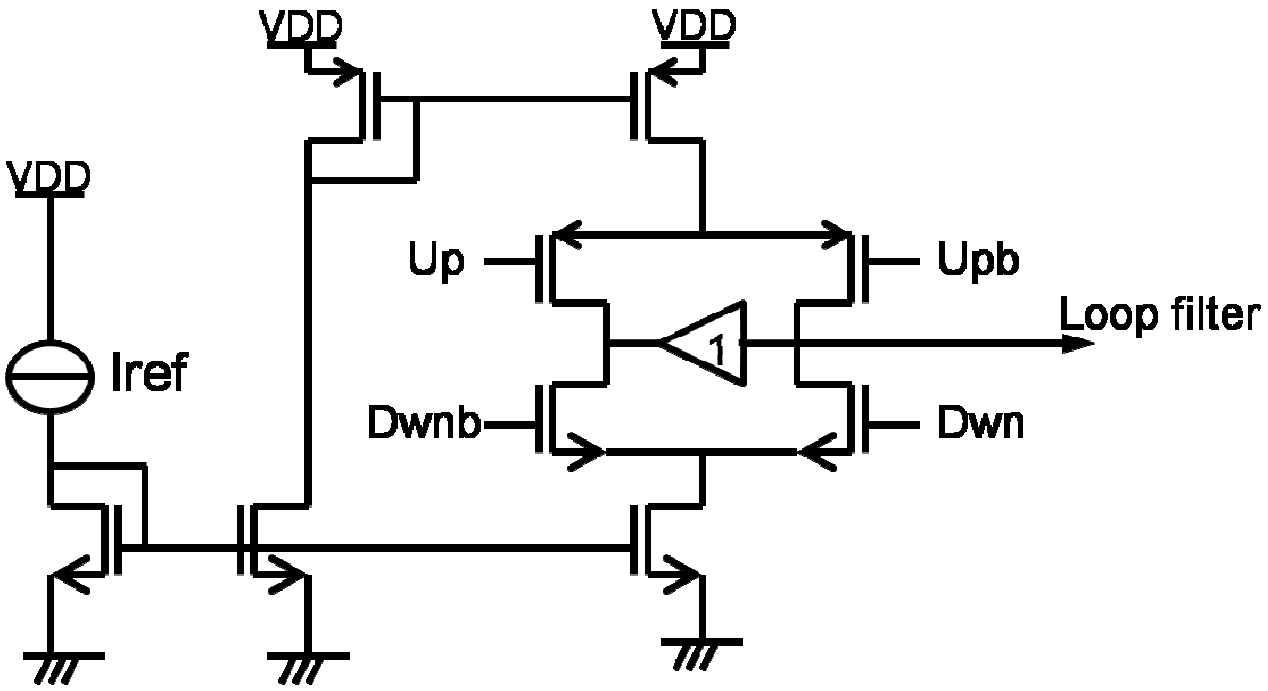




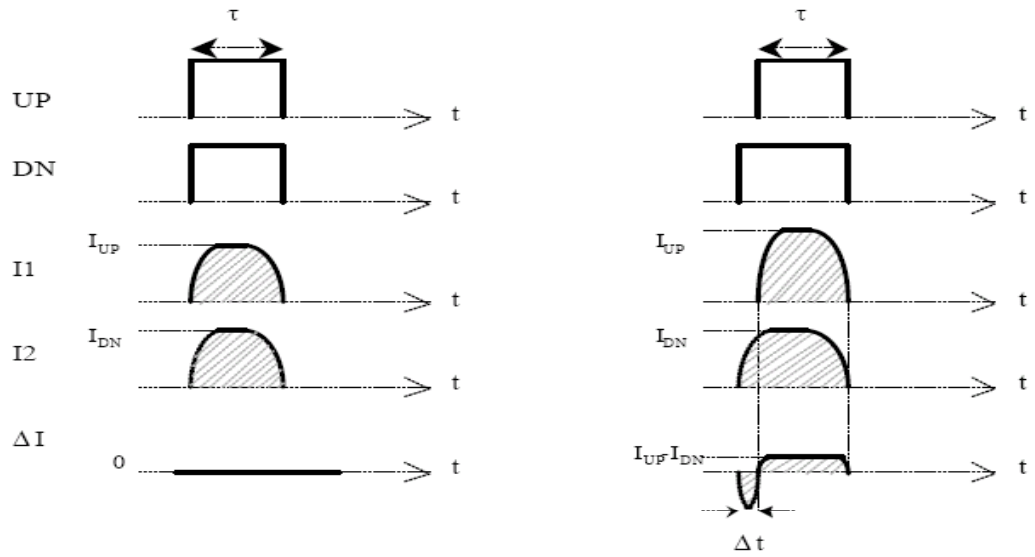


Charge Pump Design (1)



- Charge pump:
  - Permits a control of the PFD/loop filter gain
  - Enhances power supply noise rejection
- Needs good matching of current sources

Charge Pump Design (2): Mismatch issue



- Mismatch in charge pump Up and Down Current and filter current leakage are responsible of reference spurious tone in PLL output

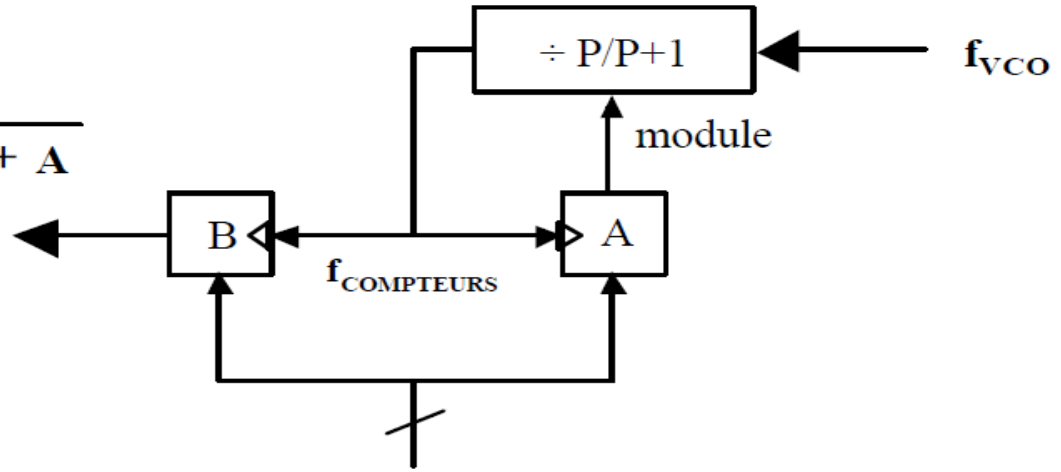
$$A_{sp}(f_{lo} \pm nf_{ref}) = A_{LO} \frac{I_m |Z_f(j2\pi nf_{ref})| K_{VCO}}{nf_{ref}}$$

$$I_m = I_{cp} \frac{\Delta\Phi}{2\pi}$$

Loop Divider (1)

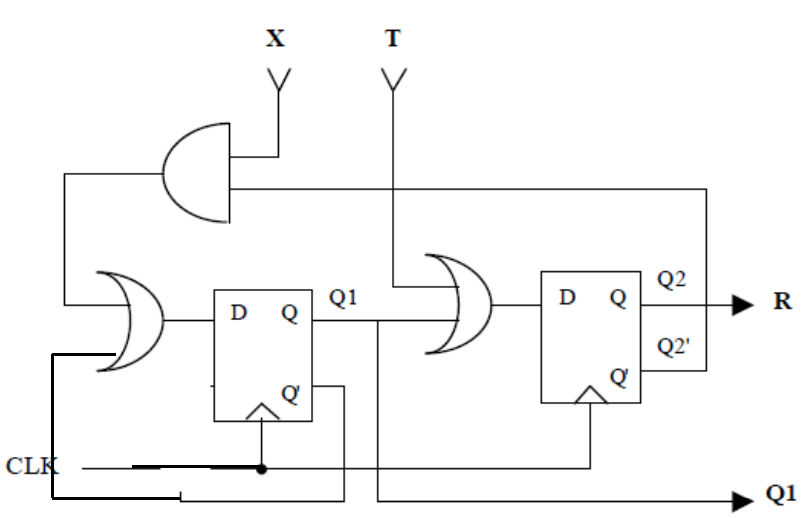
$$M = A \cdot (P+1) + (B-A) \cdot P = B \cdot P + A$$

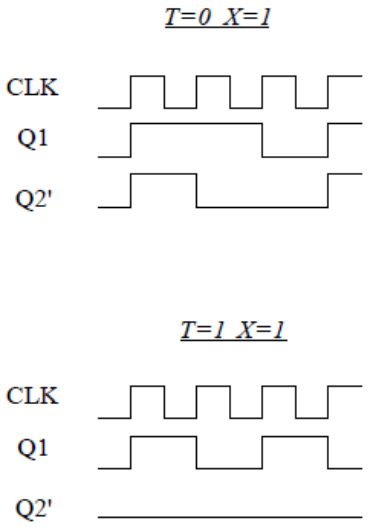
$$f_{DIV} = \frac{f_{IN}}{B * P + A}$$

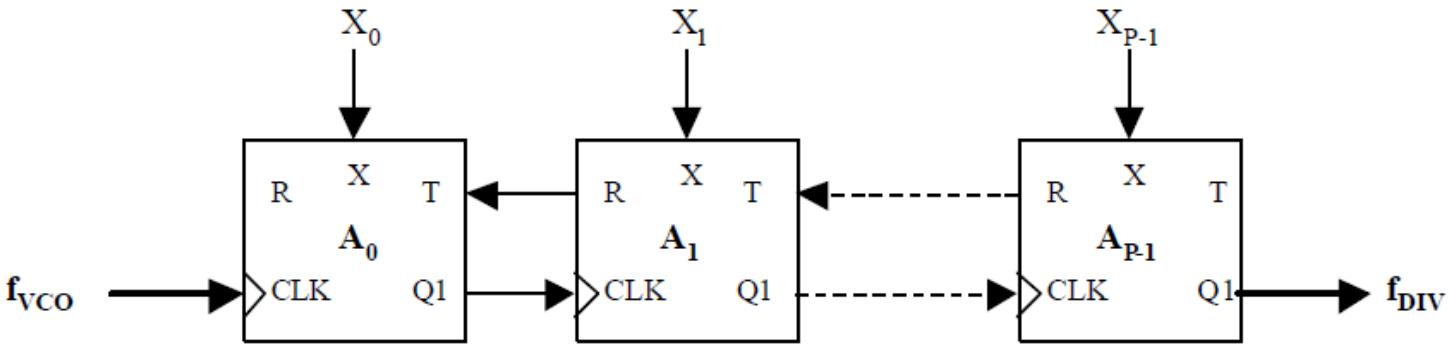


- Main Drawback: has only (P+1)Tvco to change from P+1 to P modulus. Could be problematic for low P values

Loop Divider (2)







Integer-N PLL: transient simulation

- Small signal analysis: stability, filter and charge pump current determination
- Noise analysis: verification of loop bandwidth choice and gives some specifications to designers
- Transient analysis: to verify feedback connection.
- At transistor level : VCO in the GHz range (need a few ps precision), loop bandwidth very small, settling time in the us range...simulation time prohibitive!
  - Solution: mixed solution with realistic verilog-A model of at least VCO and loop feedback divider
  - Merging VCO and loop feedback divider in one model fastens simulations
  - Noise behaviour in transient: need some simulation using Math simulators or C models.

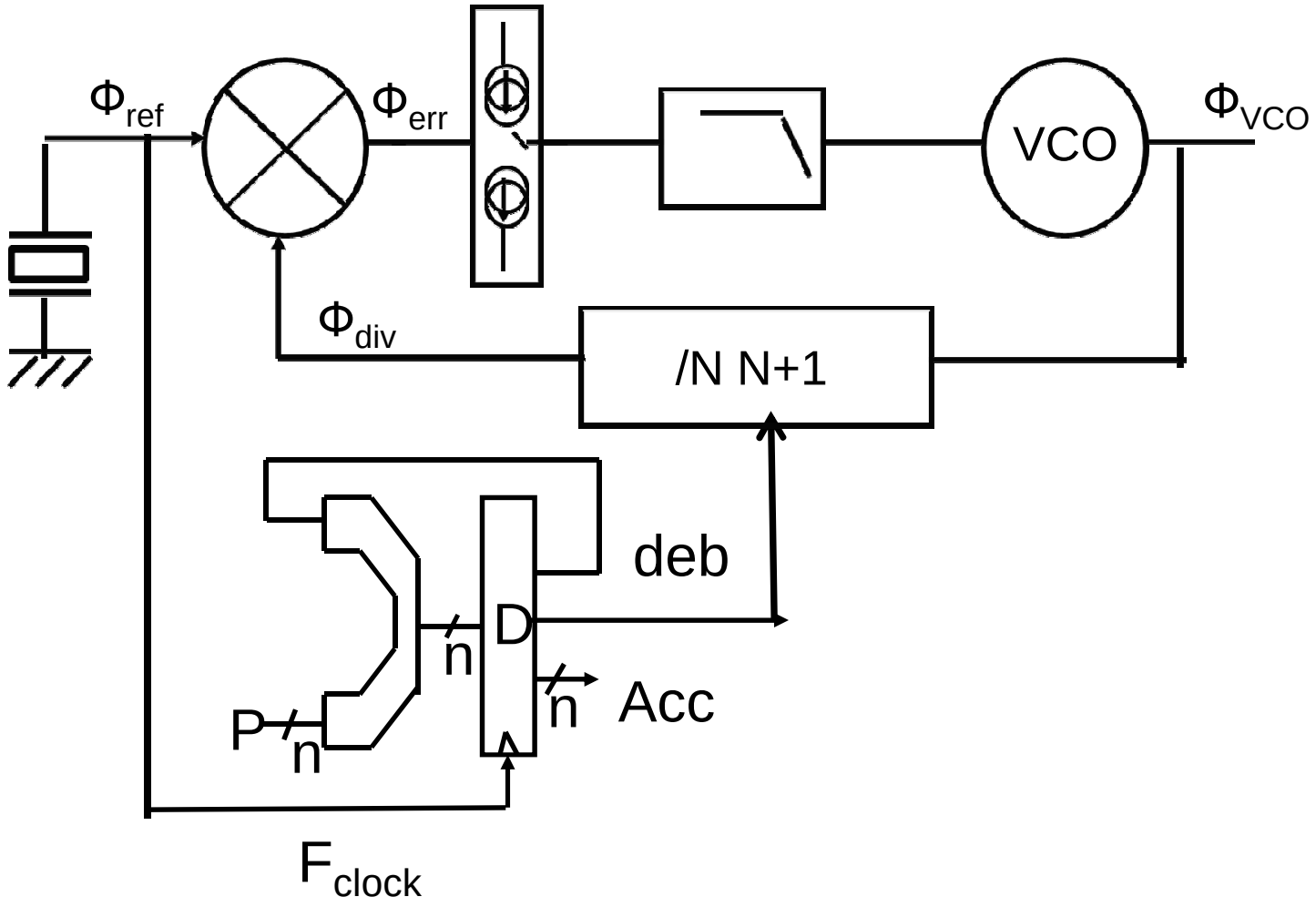
Integer-N Frequency Synthesizer

- Advantages
  - Easy to setup for GHz frequency synthesis
  - Only one spurious @ reference frequency
- Drawbacks
  - Low speed System
    - Frequency Step= Fref
    - Fref Max = channel width
    - Loop bandwidth < Channelwidth /10
  - Spurious in adjacent channel!! Big constraints on CP mismatch, loop filter leakage current
  - Power consumption(VCO+ dividers)
  - Low bandwidth modulation
  - Loop transfer function depends on process variations (especially if the loop filter is integrated)

Outline

- Introduction
  - Frequency Synthesis - Where and Why?
  - Specifications
- Frequency Synthesizer Architectures
  - Direct Digital Synthesizer
  - Integer N PLL
  - Fractional PLL
- Implementation examples
  - Phase Interpolator Based DDS
  - Multimode GSM/DCS/PCS frequency Synthesizer
  - 40 GHz PLL for 60 GHz UWB transceiver

Fractional-N synthesizer Principle (1)



Fractional-N synthesizer Principle (2)

- Dual modulus N/N+1 divider
  - When Deb = 0 division by N
  - When Deb = 0 division by N+1
- In 2^n reference clocks (period of phase accumulator) the divider divide P time by N+1 and 2^n-P time by N

$$N_{avg} = \frac{p.(N+1) - (2^n - P).N}{2^n} = N + \frac{p}{2^n}$$

- Thus Frac-N PLL output frequency is given by:

$$f_{vco} = \left(N + \frac{p}{2^n}\right) f_{ref}$$

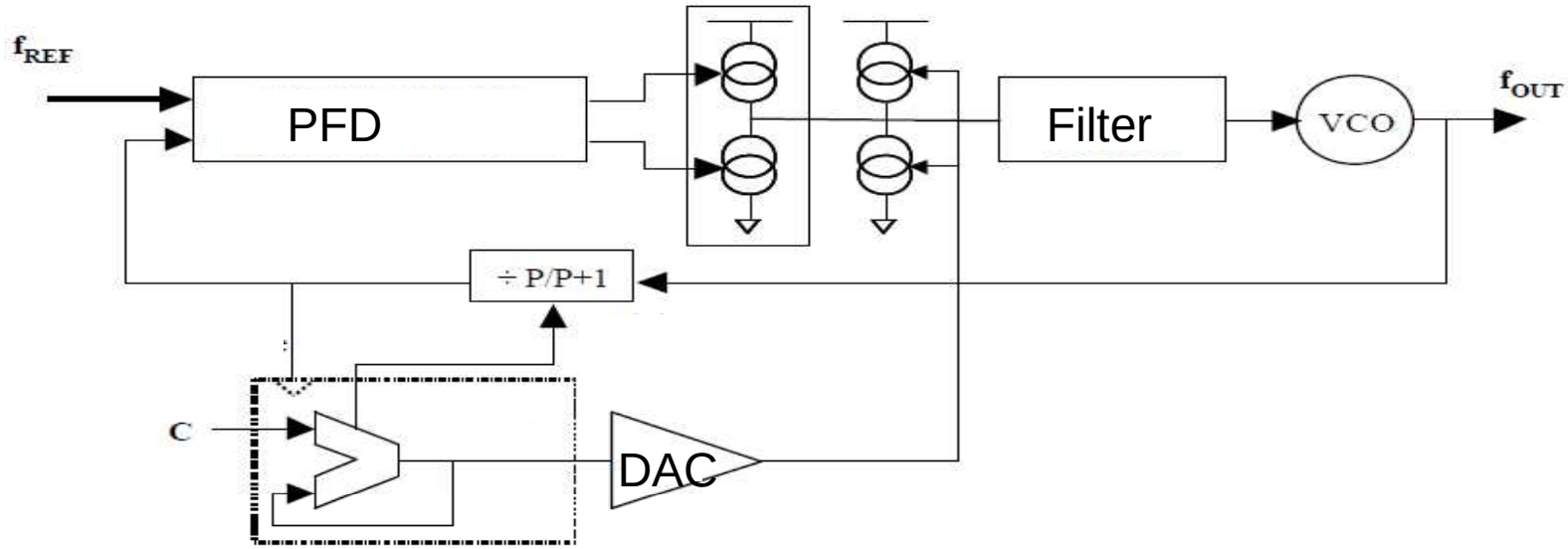
- Drawbacks: overflow signal of phase accumulator presents suprious tones. Those that lies into PLL bandwdith are not filtered and are present in PLL output

Fractional-N principle (2)

- Advantages:
  - divider ratio fractional permits to use a reference frequency greater than the channel spacing
  - Larger bandwidth could be reached (floop ~4MHz for a 38.4 MHz quartz reference) highly desirable for modulation purpose.

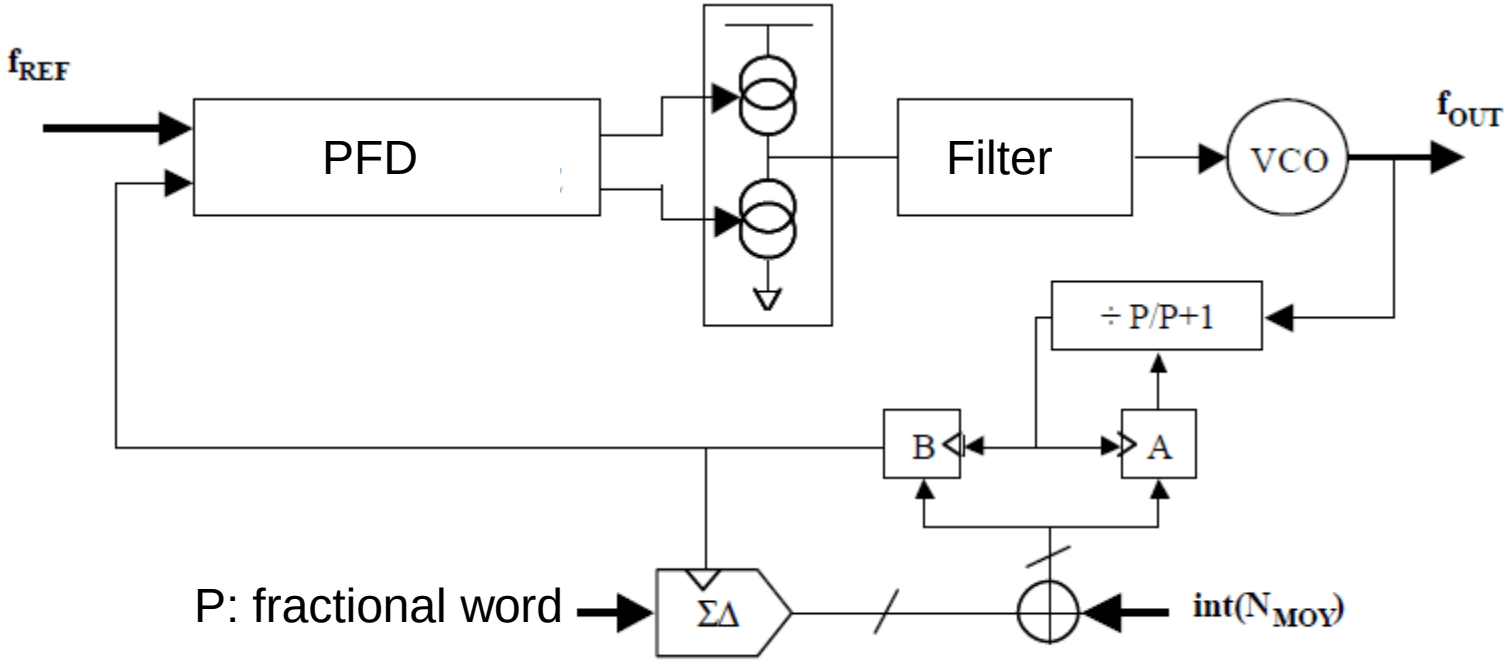
- Drawback:
  - Phase accumulator spurious tones are not filtered out in the loop bandwidth -> high suprious level in the VCO output

Compensated Frac-N synthesizer



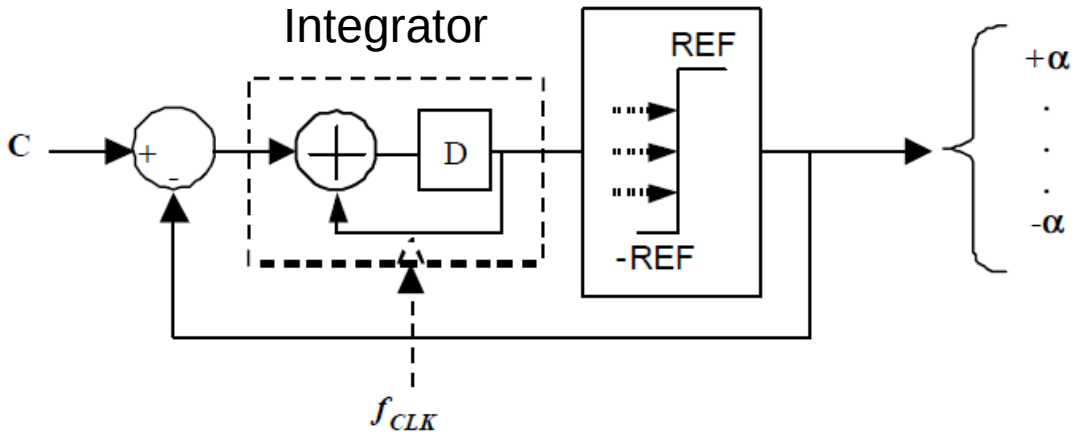
- Phase accumulator output is used to inject current in loop filter to compensate spurious
- Solution very sensitive to accuracy, DAC speed. Extra noise added onto the loop filter.

ΣΔ Fractional-N synthesizer (1)



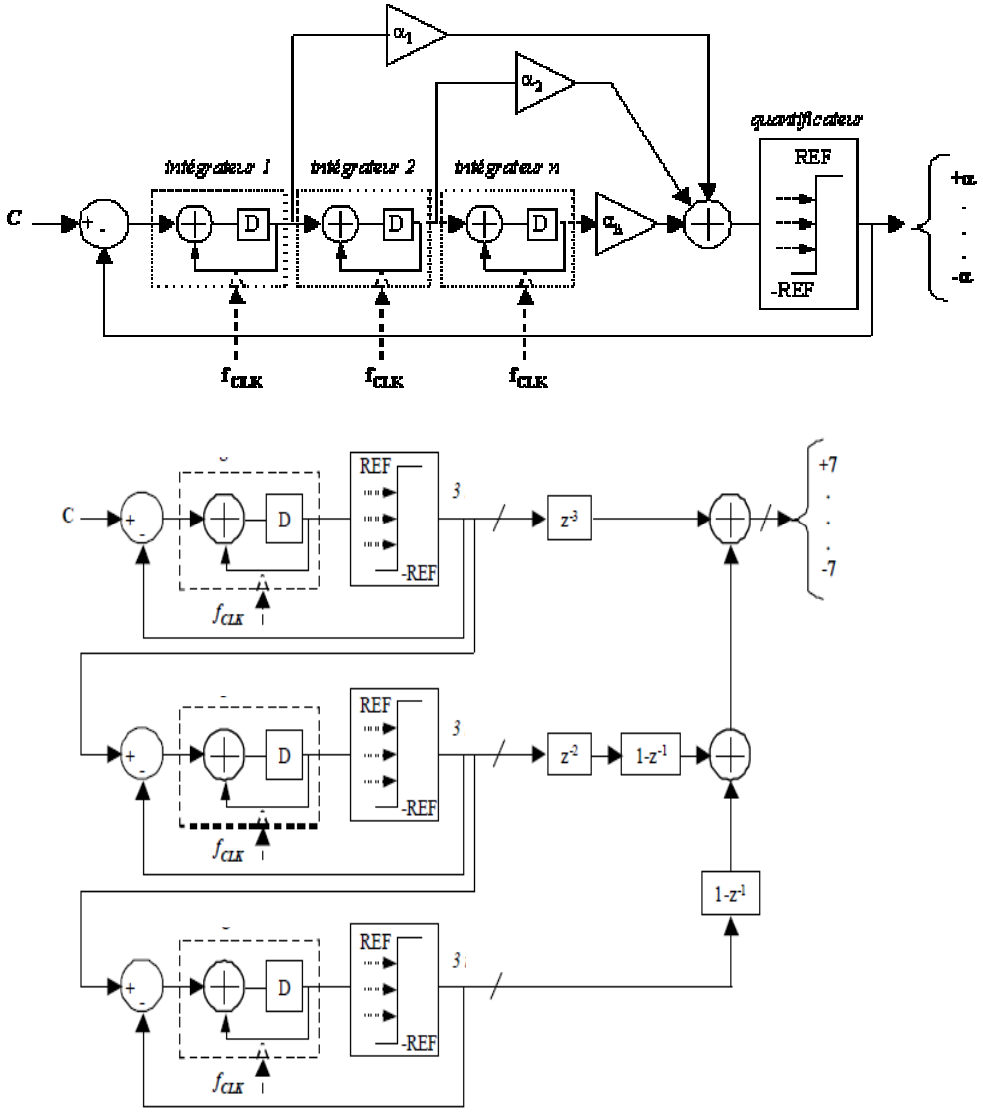
- ΣΔ modulator is used to deliver a fractional word proportional to the frequency fraction to be synthesized
- Same function as Frac-N but using the noise shaping property of ΣΔ modulator to reject quantization noise out of PLL loop bandwidth

ΣΔ modulator (1)



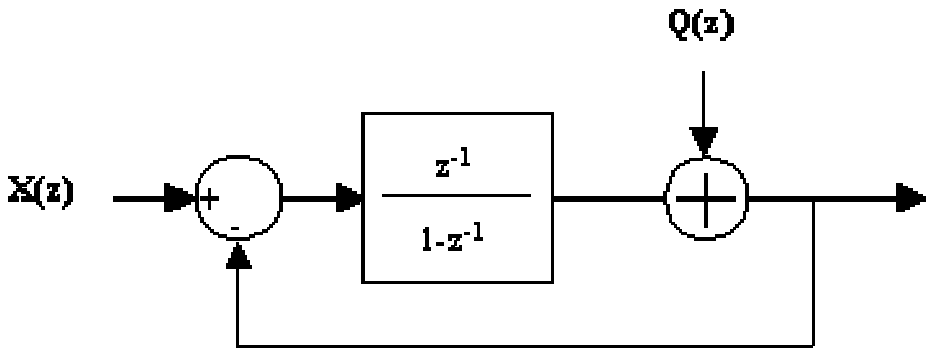
- ΣΔ converter:
  - Sampled feedback loop
  - Composed of an integrator and a quantisizer.
  - At each clock occurrence, difference between output and input is integrated and quantified. The loop tends to minimize this error
- ΣΔ modulator
  - Digital implementation
  - N order ΣΔ modulator : N ΣΔ modulator in series or in parallel (MASH)

Example of 3rd order ΣΔ



- Series structure
  - Stability issue
- Parallel structure: MASH
  - No stability issue

ΣΔ modulator noise shaping (1)



$$Y(z) = z^{-1} \cdot X(z) + \left(1 - z^{-1}\right) \cdot Q(z)$$

- For a Nth order MASH, transfer function is:

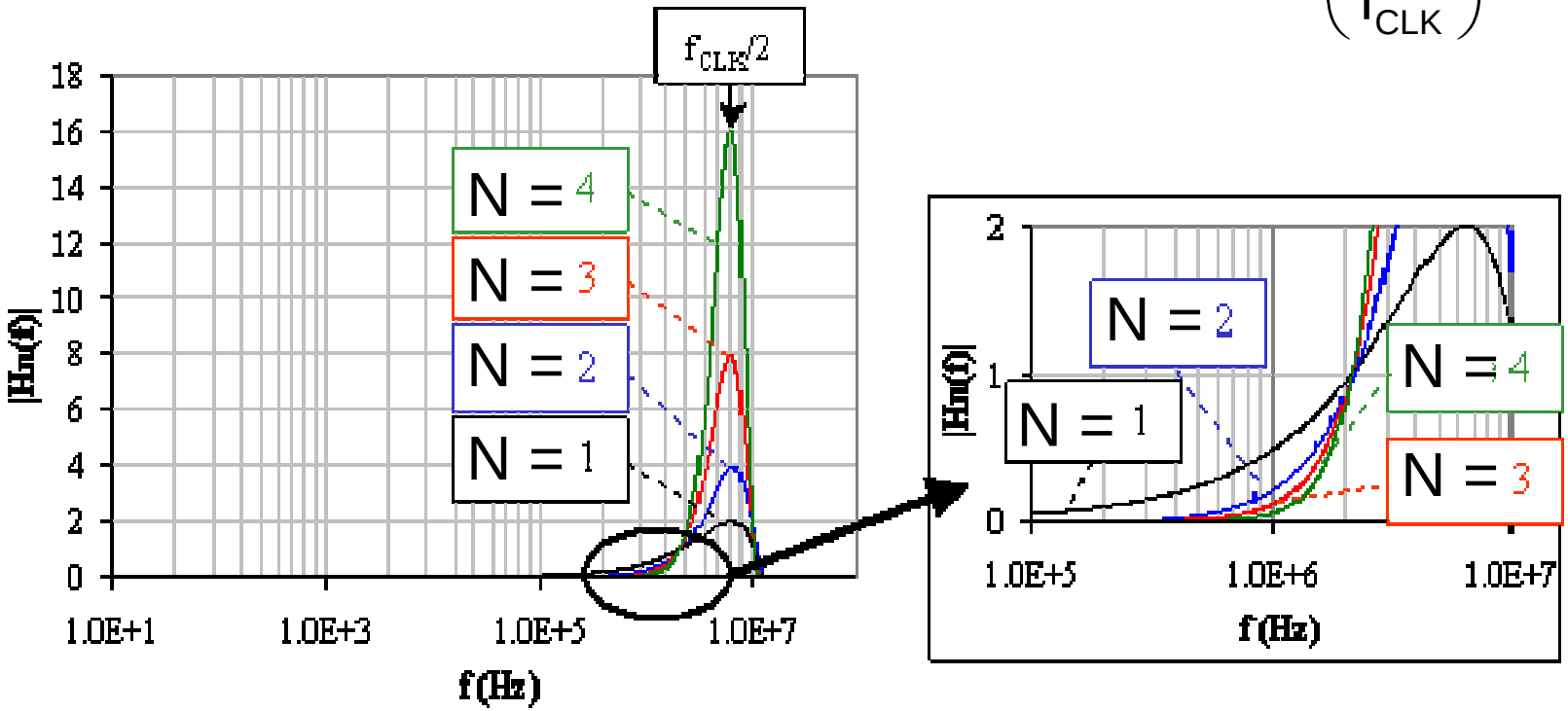
$$Y(z) = z^{-n} \cdot X(z) + \left(1 - z^{-1}\right)^{n} \cdot Q_n(z)$$

- Only the quantification of the last converter is of interest

ΣΔ modulator noise shaping (2)

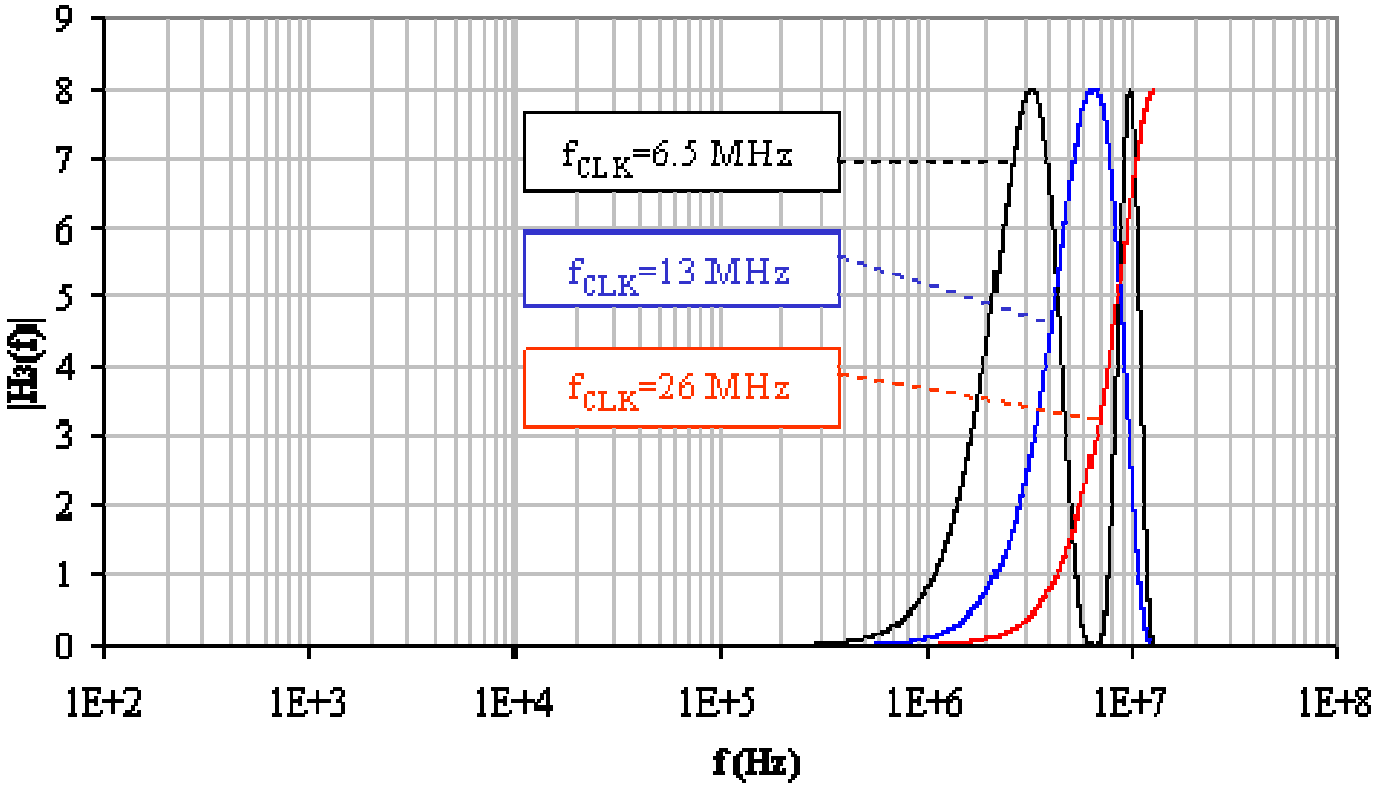
$$H_n(z) = (1 - z^{-1})^n$$

$$|H_n(f)| = |2 * \sin\left(\frac{\pi \cdot f}{f_{CLK}}\right)|^n$$



- As order N increases the noise is more and more rejected near Fclk/2

ΣΔ modulator noise shaping (3)



ΣΔ modulated divider model (3)

- Output Frequency divider expression:

$$f_{out} = \frac{f_{VCO}}{N_{avg} + q(t)} \approx \frac{f_{VCO}}{N_{avg}}\left(1 - \frac{q(t)}{N_{avg}}\right)$$

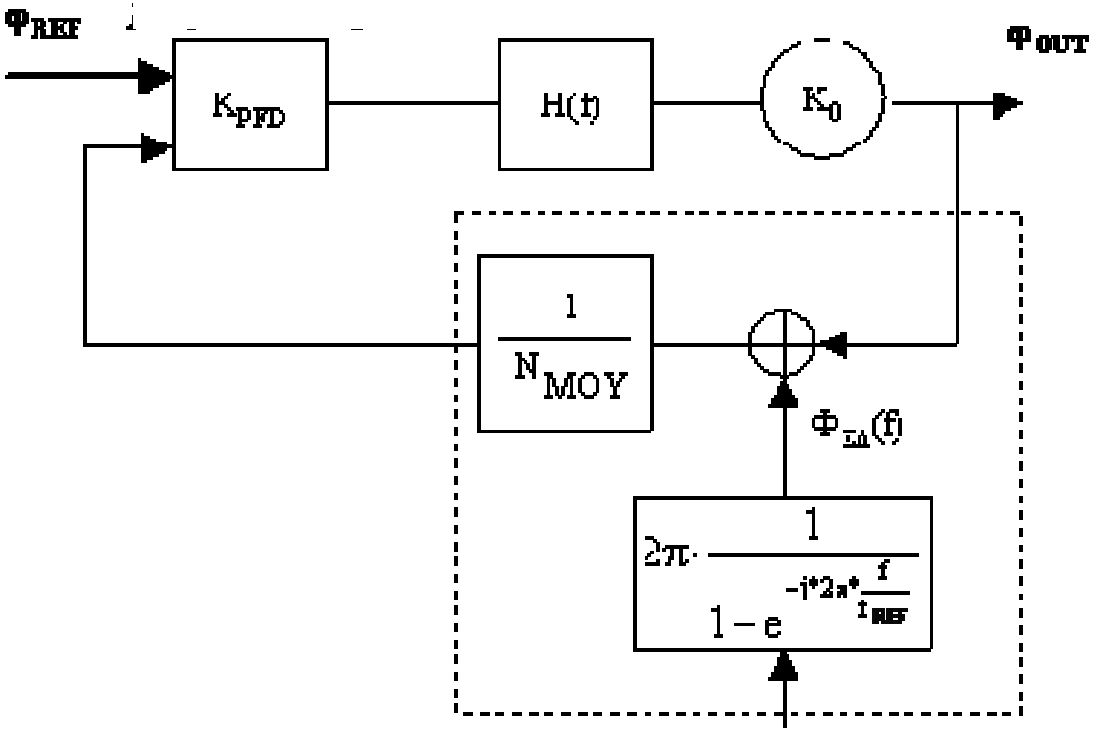
- Z domain transform:

$$f_{out} = \frac{f_{vco}}{N_{avg}} - \frac{f_{vco}}{N_{avg}^{2}} . \frac{q}{\sqrt{12.f_{ref}}}(1 - z^{-1})^{3} \approx \frac{f_{vco}}{N_{avg}} - \frac{f_{REF}}{N_{avg}} \frac{q}{\sqrt{12.f_{ref}}}(1 - z^{-1})^{3}$$

- Integration to get the phase domain expression

$$\Phi_{out} = \frac{\Phi_{VCO}}{N_{avg}} - \frac{f_{ref}}{N_{avg}} \frac{q}{\sqrt{12 \cdot f_{ref}}}(1 - z^{-1})^{3} . \frac{2\pi . T_{ref}}{(1 - z^{-1})} = \frac{\Phi_{VCO}}{N_{avg}} - \frac{2\pi}{N_{avg}} \frac{q}{\sqrt{12 \cdot f_{ref}}}(1 - z^{-1})^{2}$$

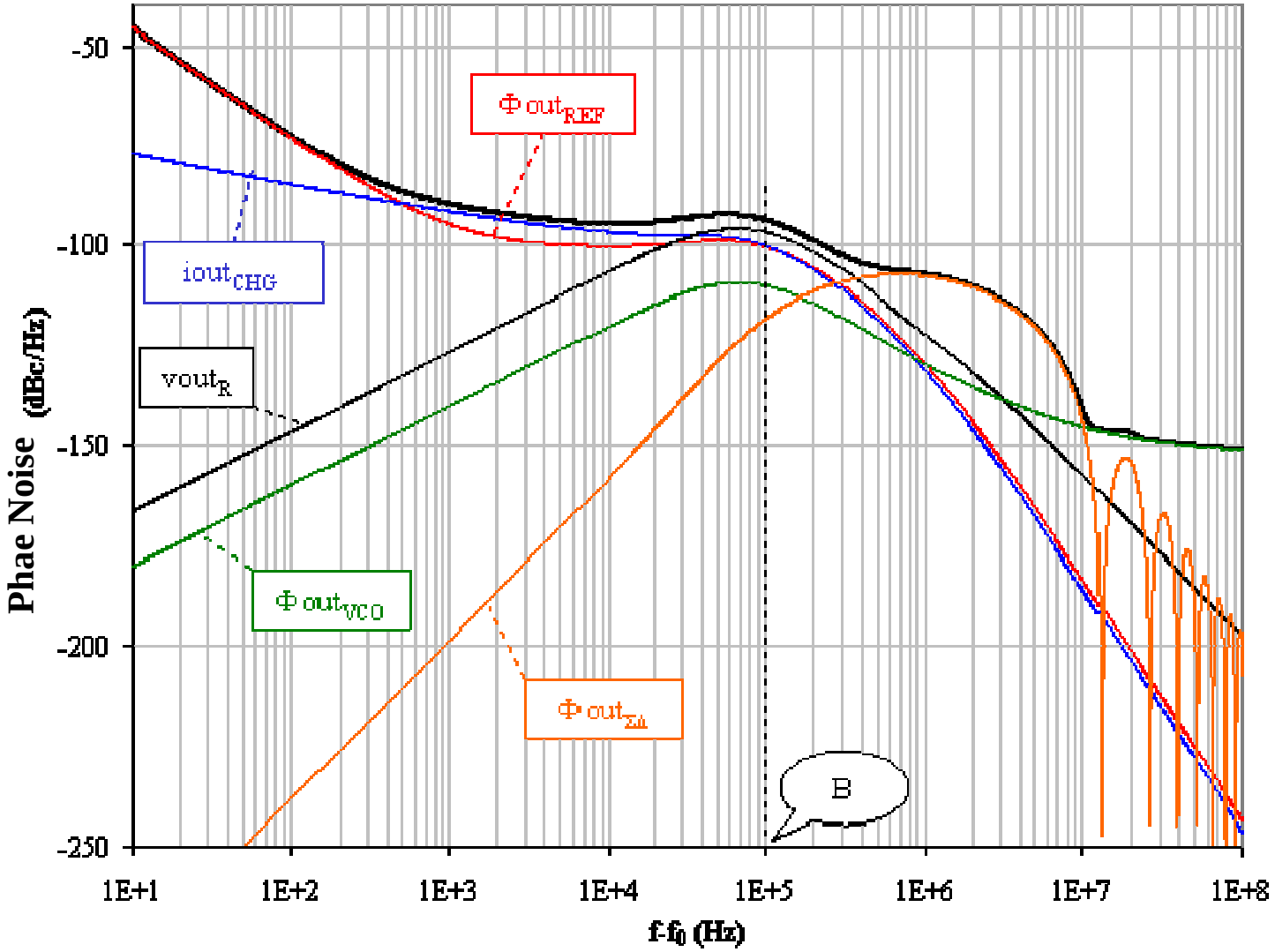
Noise Model of ΣΔ Frac-N PLL



Shaped Quantification noise

$$\Phi_{\Sigma\Delta}(f) = \left(1 - e^{-j2\pi\frac{f}{f_{REF}}}\right)^n * \frac{1}{\sqrt{12 \cdot f_{REF}}}$$

Example of ΣΔ Frac-N PLL noise plot



ΣΔ Frac-N PLL : conclusion

Advantages

- Frequency step as small as possible
- High reference frequency:
  - Spurious tone far from carrier and thus better filtered
- Frequency and phase modulation possible

Drawbacks

- ΣΔ noise shaping doesn't permit to reach fref/10 loop bandwidth
- ΣΔ: digital circuit -> noise coupling.

Classical Frequency Synthesizer: Conclusion

	1-bit DDS	DDS	Integer-N	Frac- N	ΣΔ
Bandwidth	☺ ☺	☺ ☺	☹	☺	☺
Phase Noise	☺	☺	☺	☺	☺
Spurious	☹ ☹	☹	☺ ☺	☹ ☹	☺
RF ability	☹ ☹	☹ ☹	☺	☺	☺
consumption	☺	☹ ☹	☺	☺	☺
modulation	☺ ☺	☺ ☺	☹	☺	☺
Accuracy	☺	☺	☺	☺	☺

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A 100MHz DDS With Synchronous Oscillator-Based Phase Interpolator

Franck Badets, Didier Belot

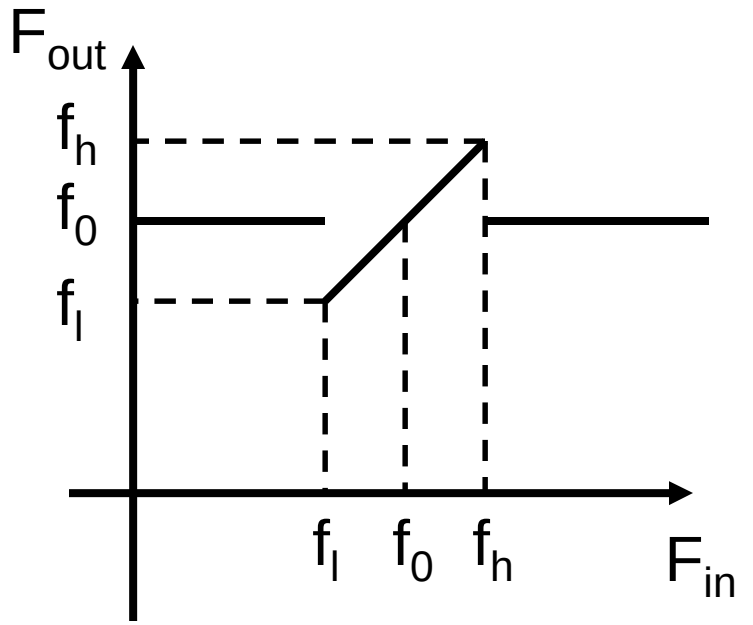
STMicroelectronics,
Central R&D Crolles

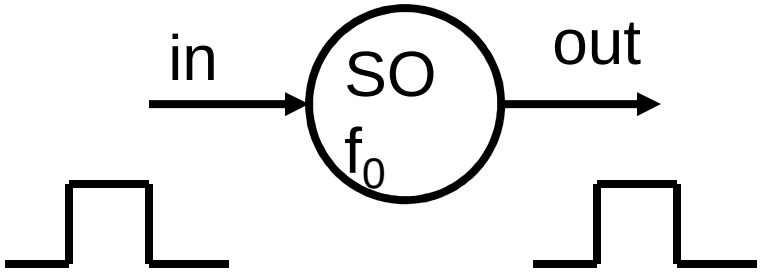
OUTLINE

- Synchronous Oscillator Based Phase Interpolator
- Synchronous Oscillator Locked Loop (SOLL)
- SOLL based phase interpolator
- 100 MHz 16 bits DDS with SOLL based phase interpolator

Injection Locked Oscillator (ILO)

- Oscillator able to lock on an incoming signal whose frequency (or an harmonic) lies into the oscillator synchronization range

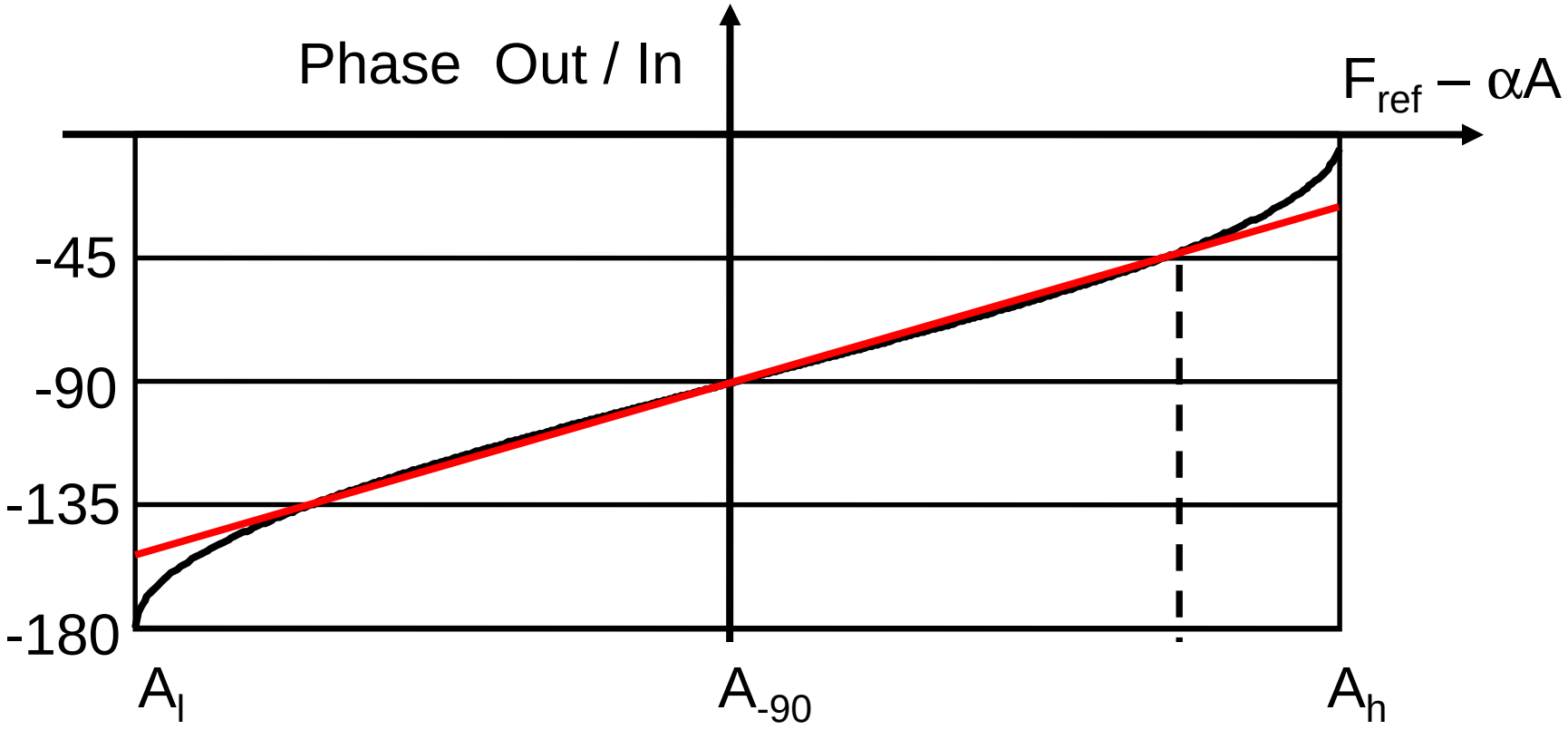




ILO Properties

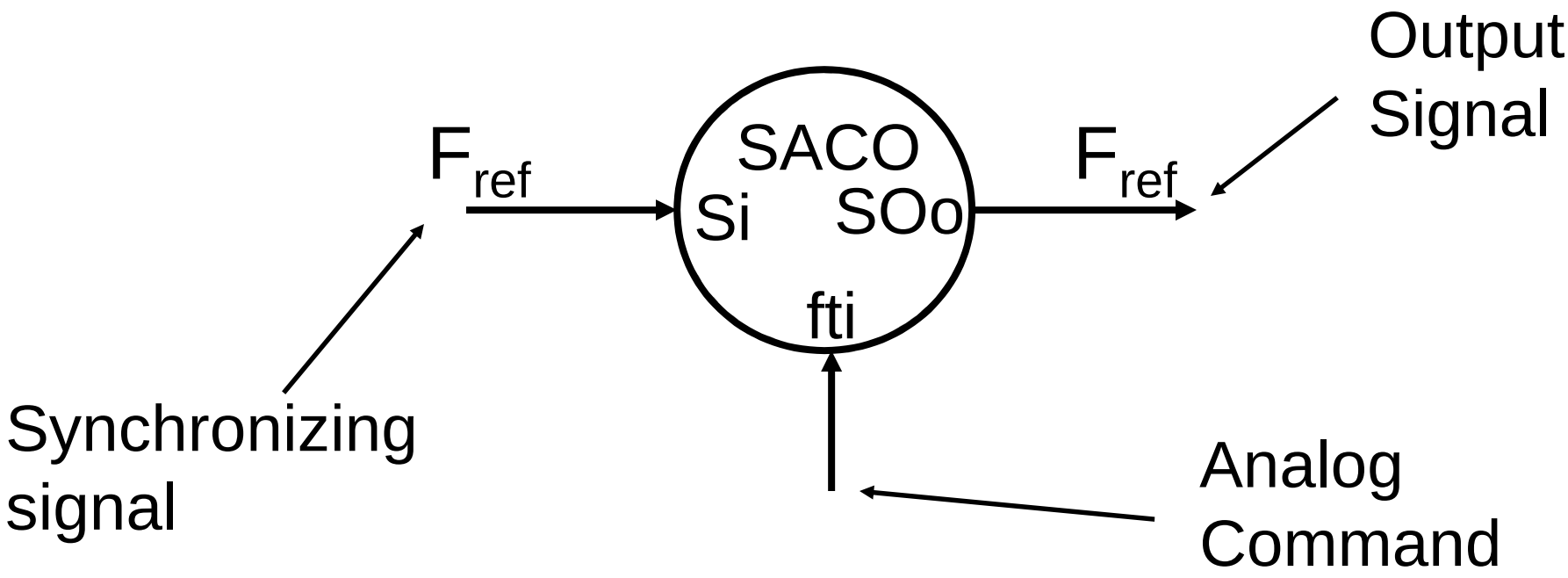
- Synchronization range depends only on synchronizing signal amplitude and oscillator topology
- Fast frequency acquisition
- Output SO phase noise is a copy of the synchronizing signal phase noise
- Once synchronized there is a phase relationship between the SO output signal and its synchronizing signal.

ILO properties con't

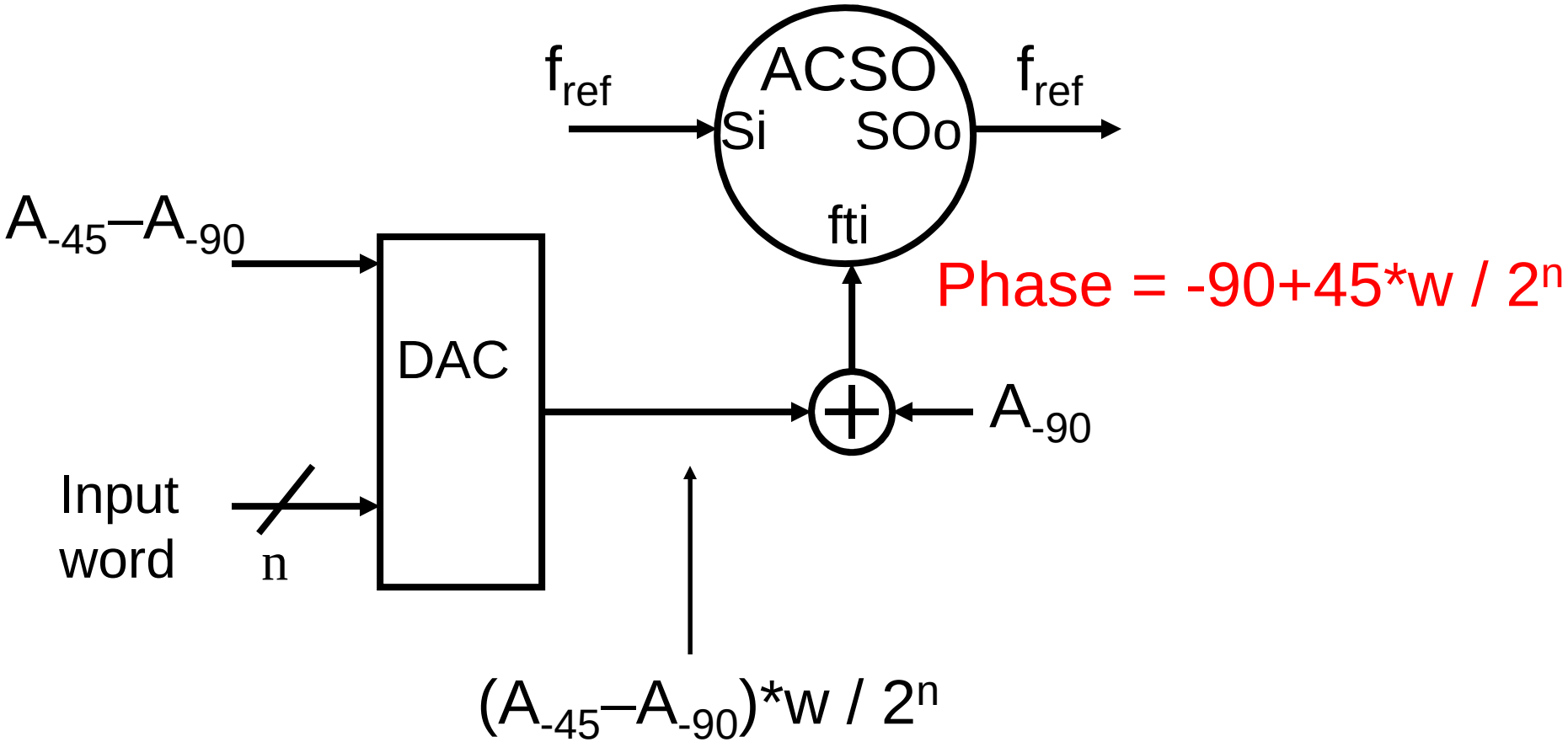


ILO based Phase Interpolator(SOPI) (1)

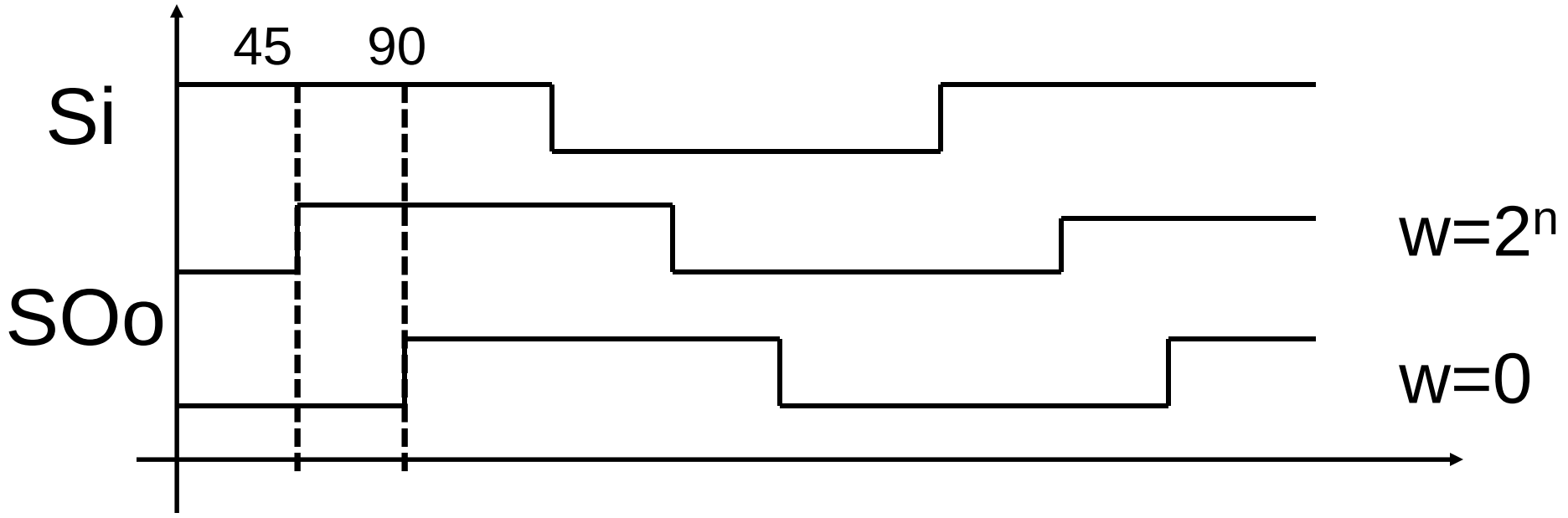
- Oscillator with linearly tunable free running frequency (Synchronous VCO or ICO (ACO))
- Fixed synchronization frequency



Digital Accurate SOPI (API)



API : Chronogram

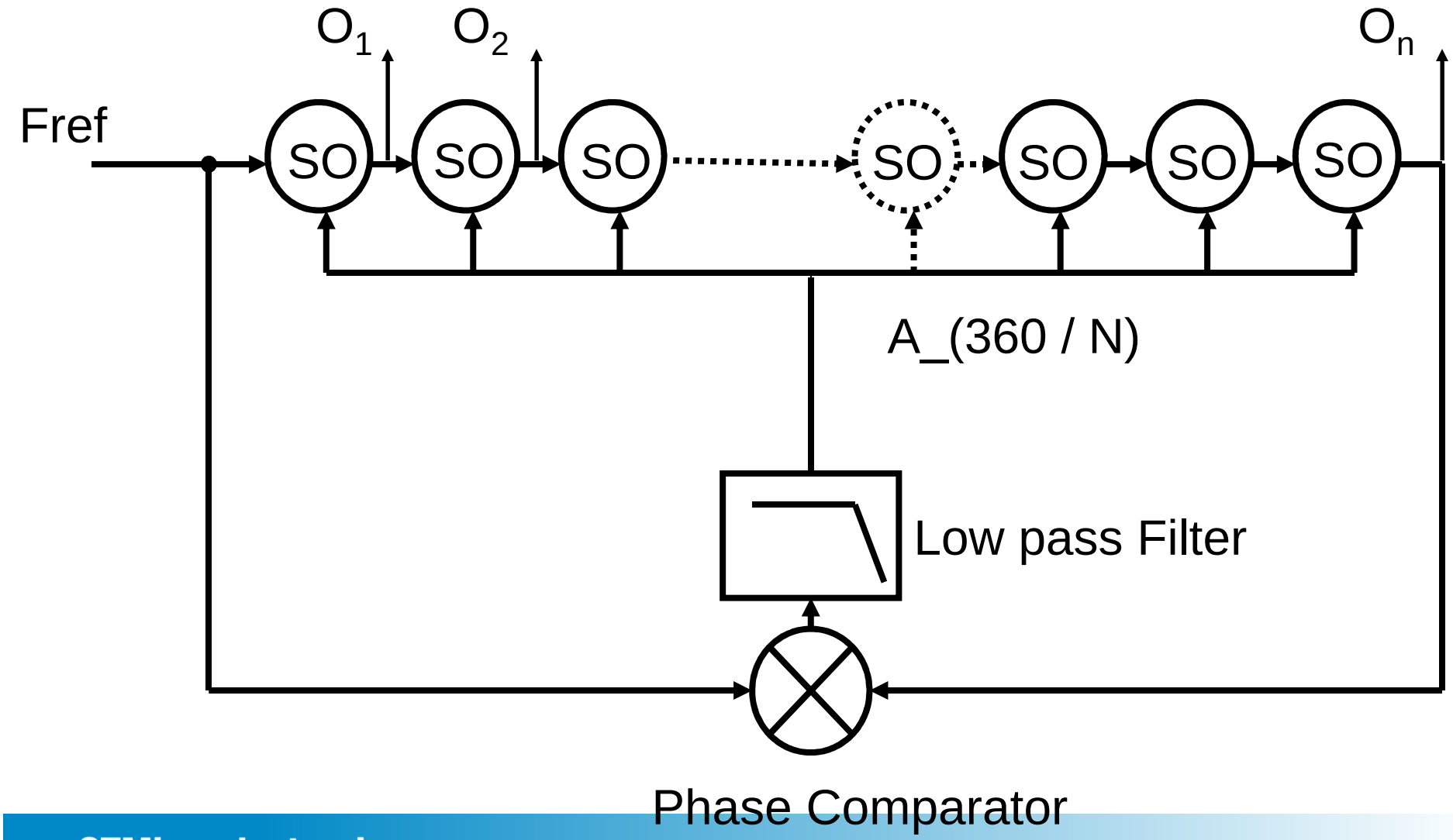


w : DAC input word

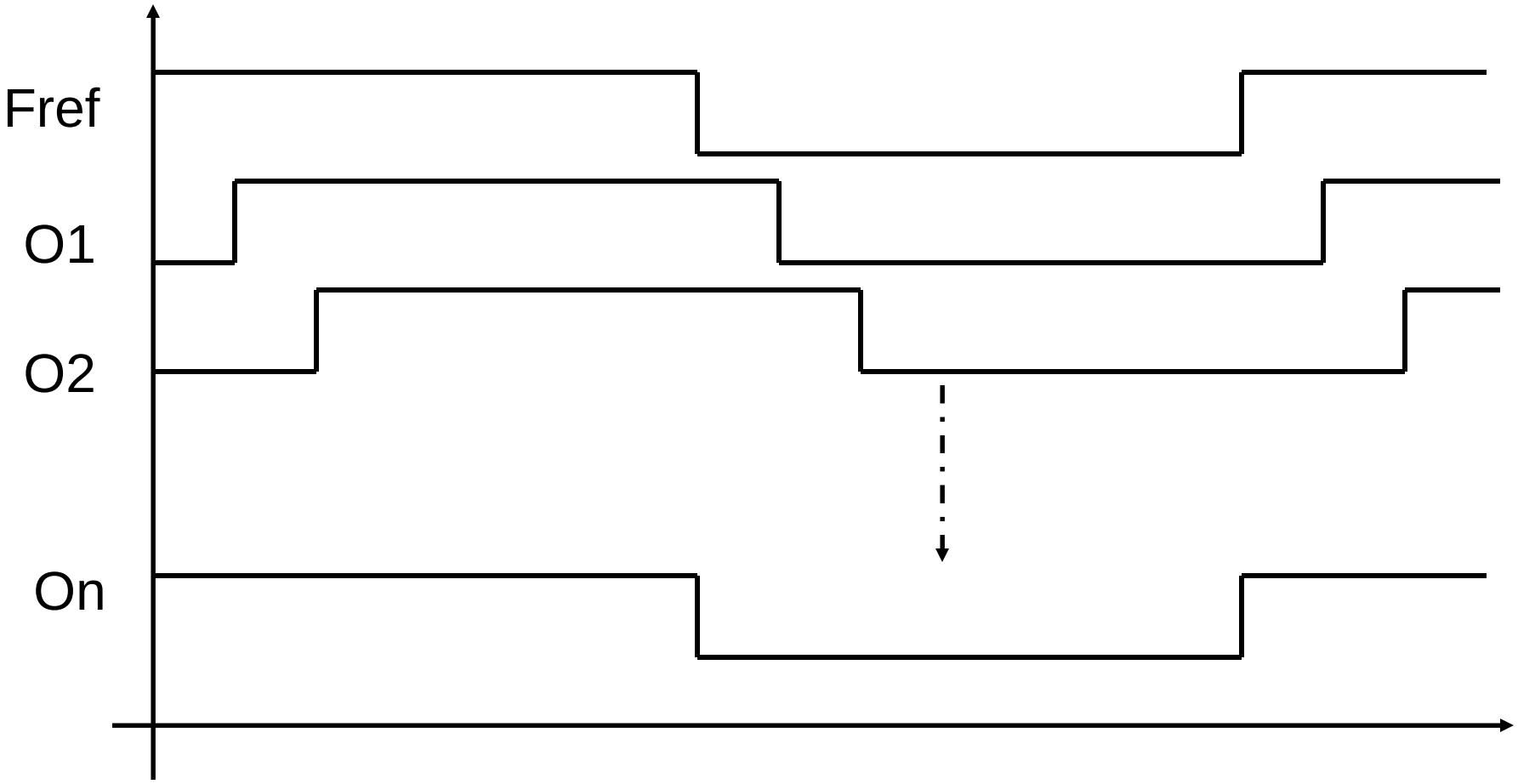
Digital Accurate SOPI (API)

- Good linearity in the –90, -45 degrees range
- Fast phase acquisition
- Needs the analog commands A_{-90} and A_{-45} for calibration

ILO Locked Loop SOLL (1)



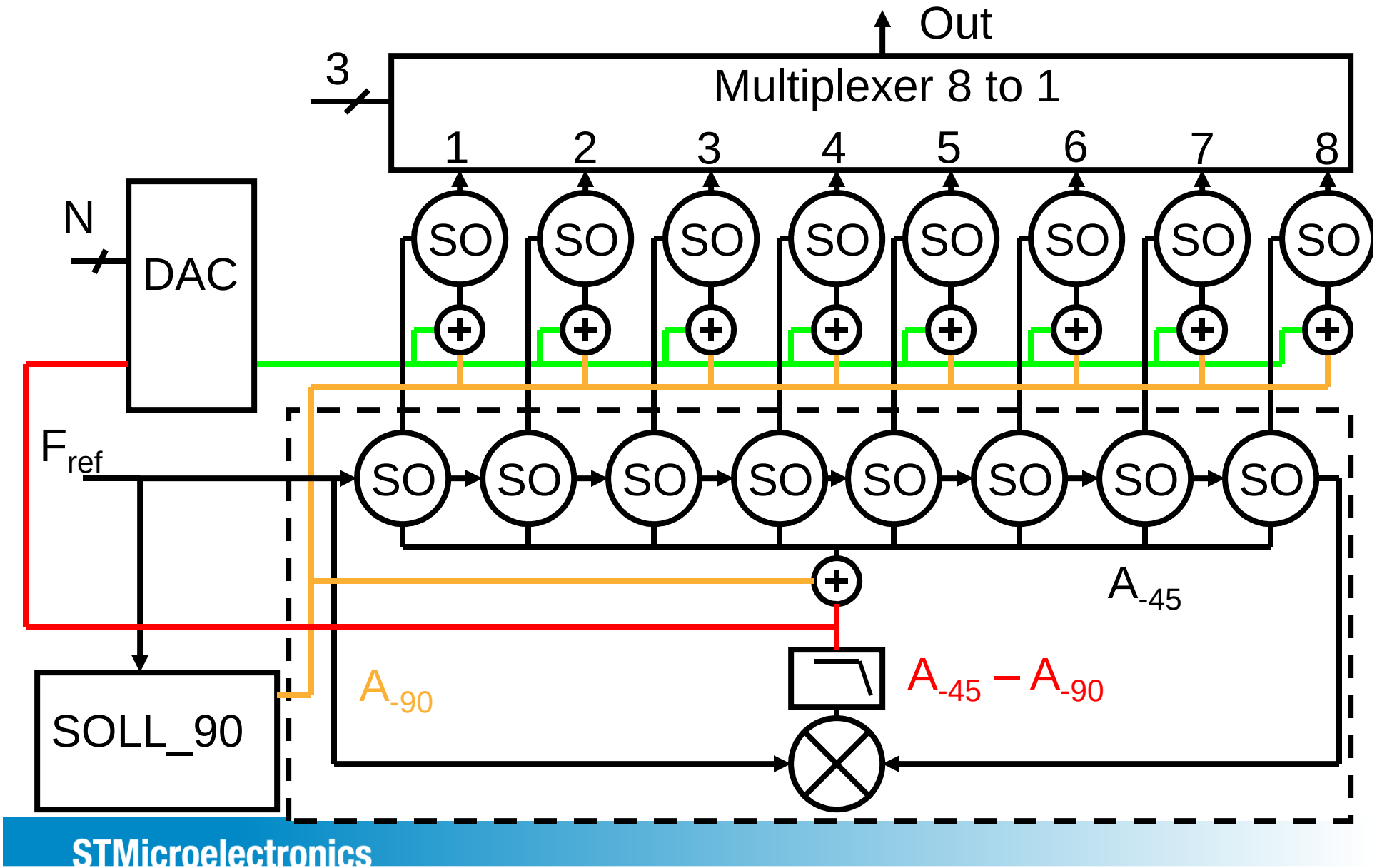
SOLL (2) : Chronogram



SOLL (2)

- DLL with SOs as delay elements
- Once Locked all SOs are fed with the analog command that ensures a 360/N phase for each SO.
- SOLL_90 : 4 SOs. Gives A_-90 command
- SOLL_45 : 8 SOs. Gives A_-45 command

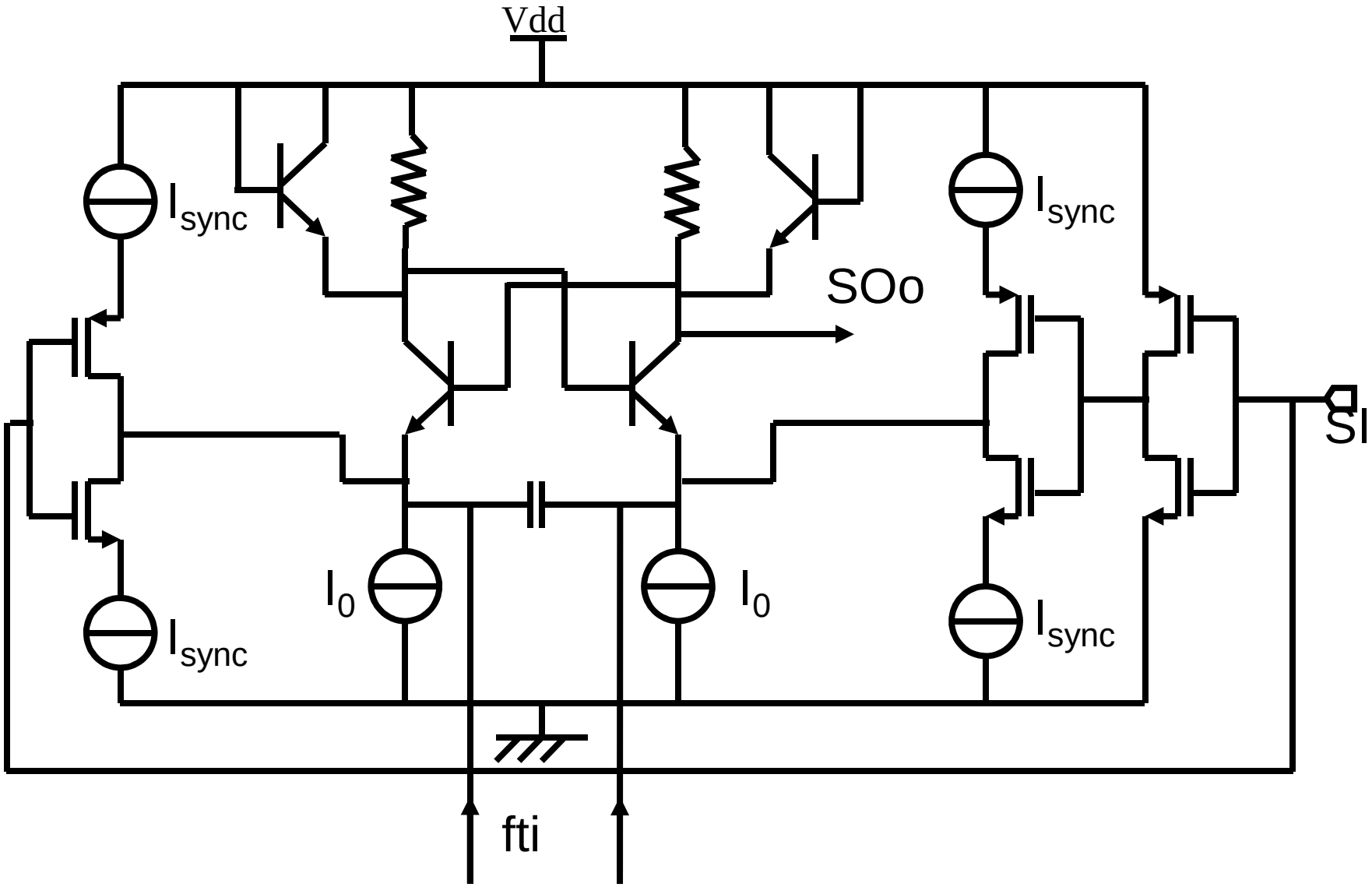
SOLL based Phase Interpolator (1)



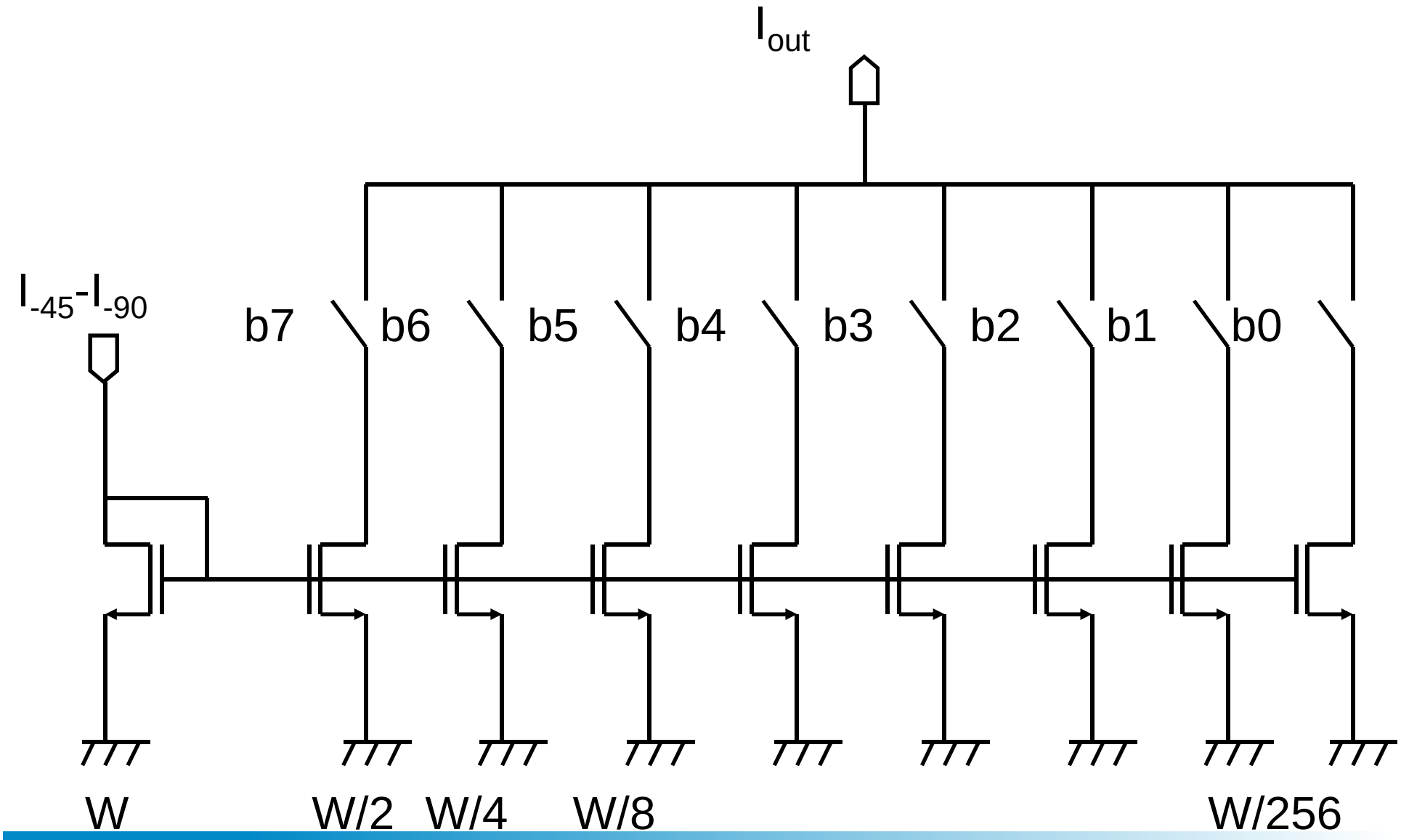
SOLL Based Phase Interpolator (2)

- SOLL_45 provides 8 outputs with a 45 phase step (multiphase clock): coarse phase interpolation
- 8 DAPI are coupled with the 8 SOLL_45 outputs to provide complementary accurate phase interpolation
- SOLL_45 and the 8 DAPI provide phase interpolation from 0 to 360 degrees with a N+3 bits accuracy

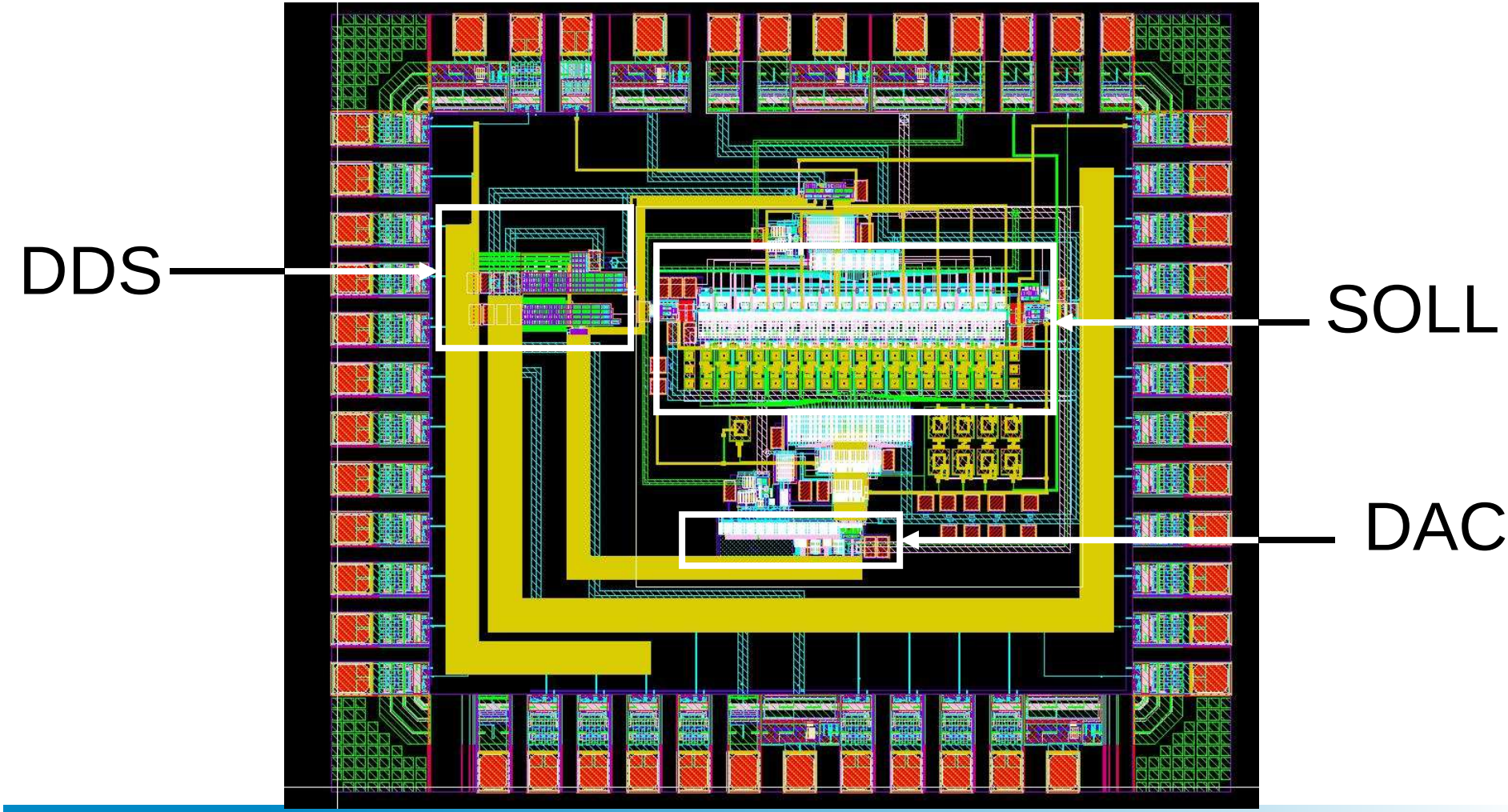
ILO implementation



DAC implementation

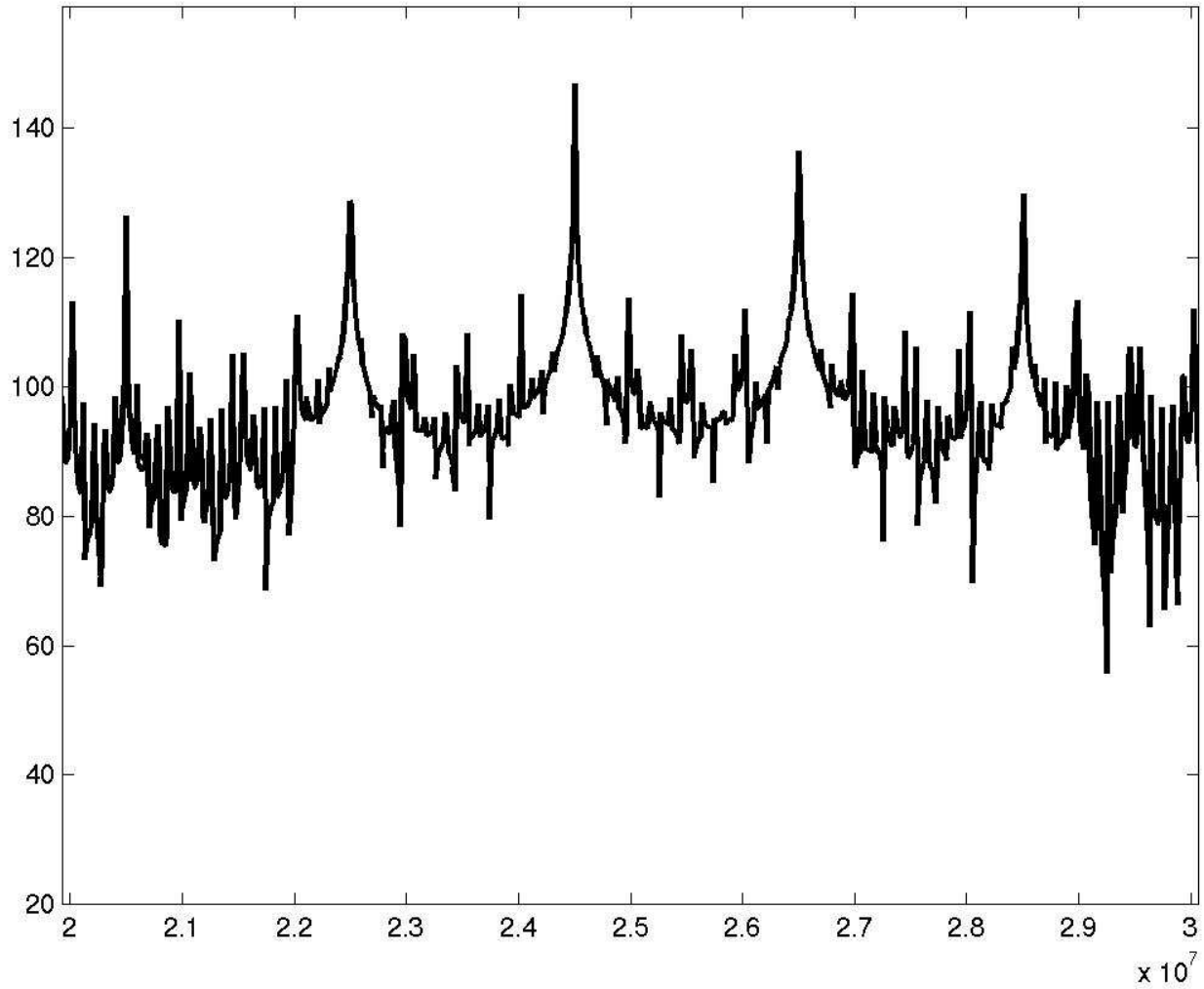


Circuit Layout



Behavioral Modeling : DDS alone

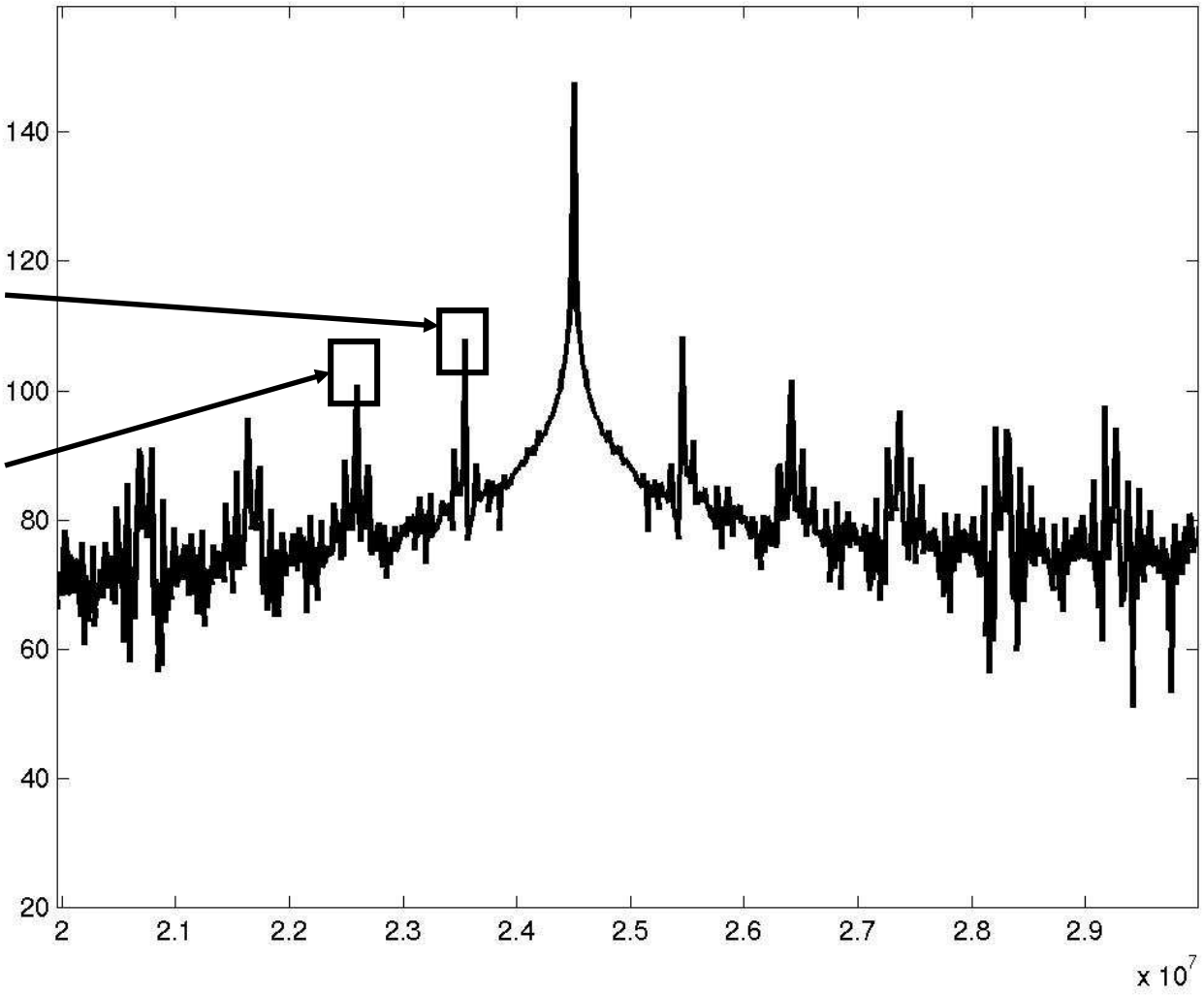
P=16056
M= 5355
f = 24.498 MHz



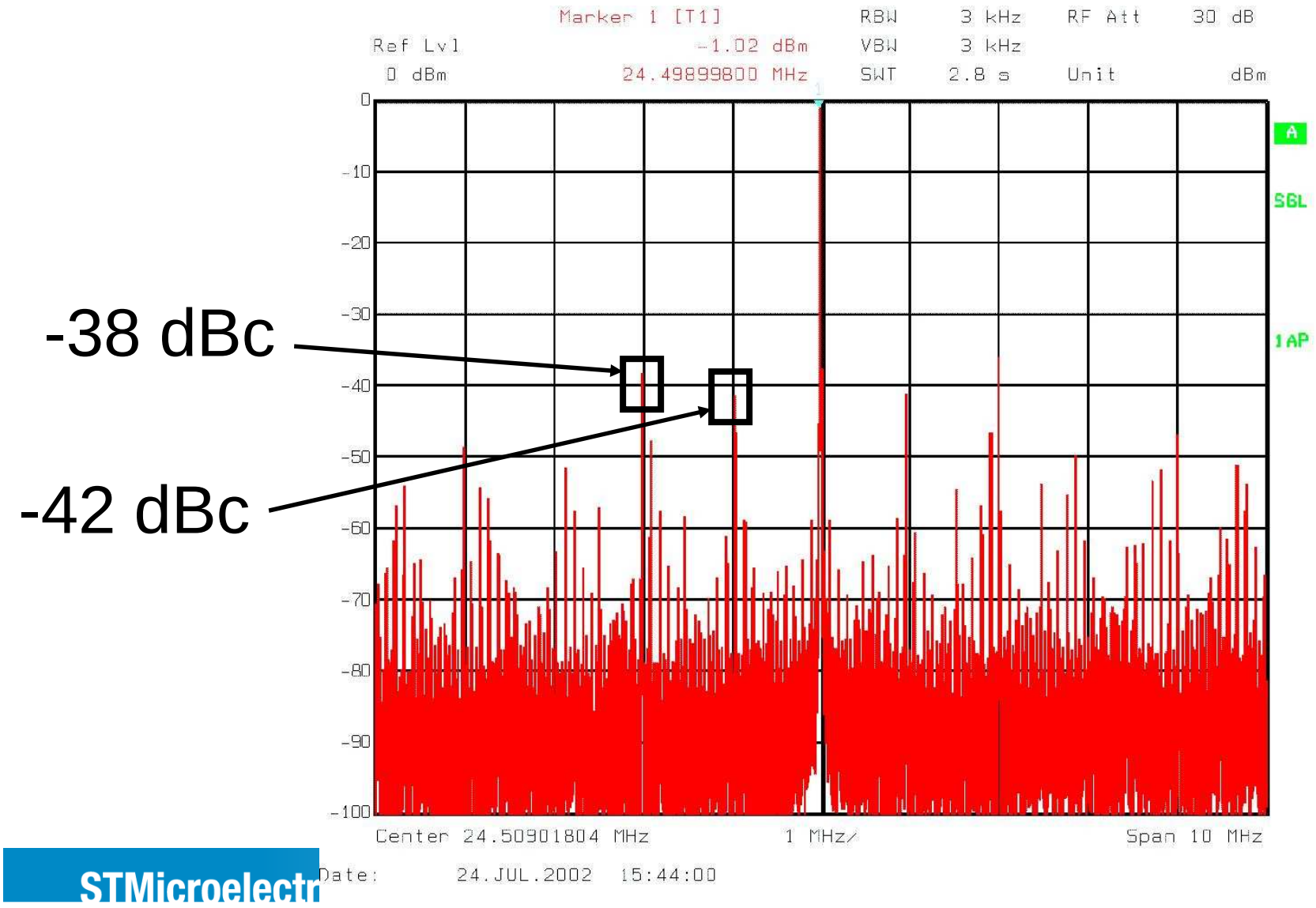
Behavioral Modeling :Coarse PI alone

-37 dBc

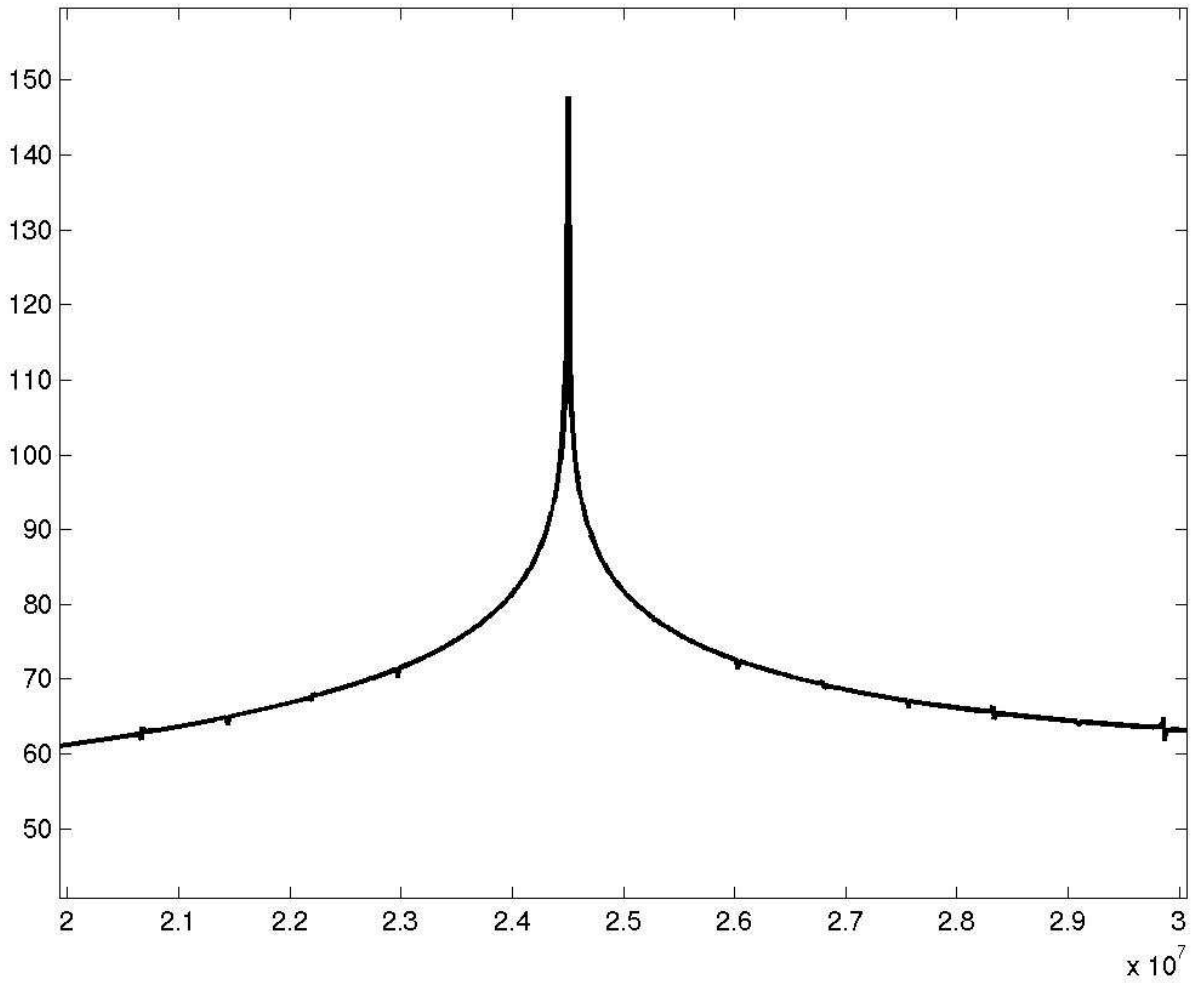
-45 dBc



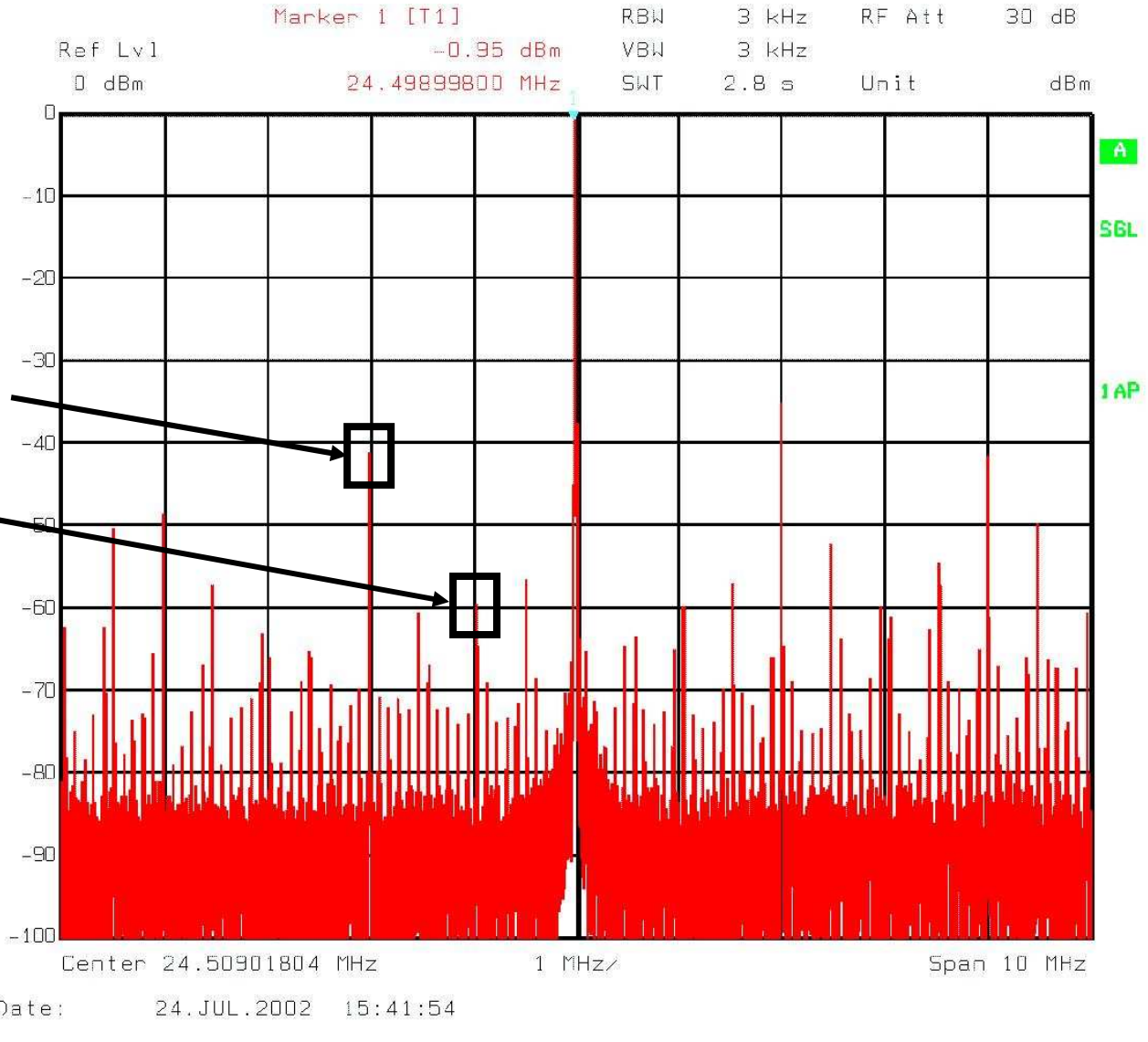
Measurement Results : Coarse Interpolation



Behavioral Modeling :
Coarse and Accurate PI enabled



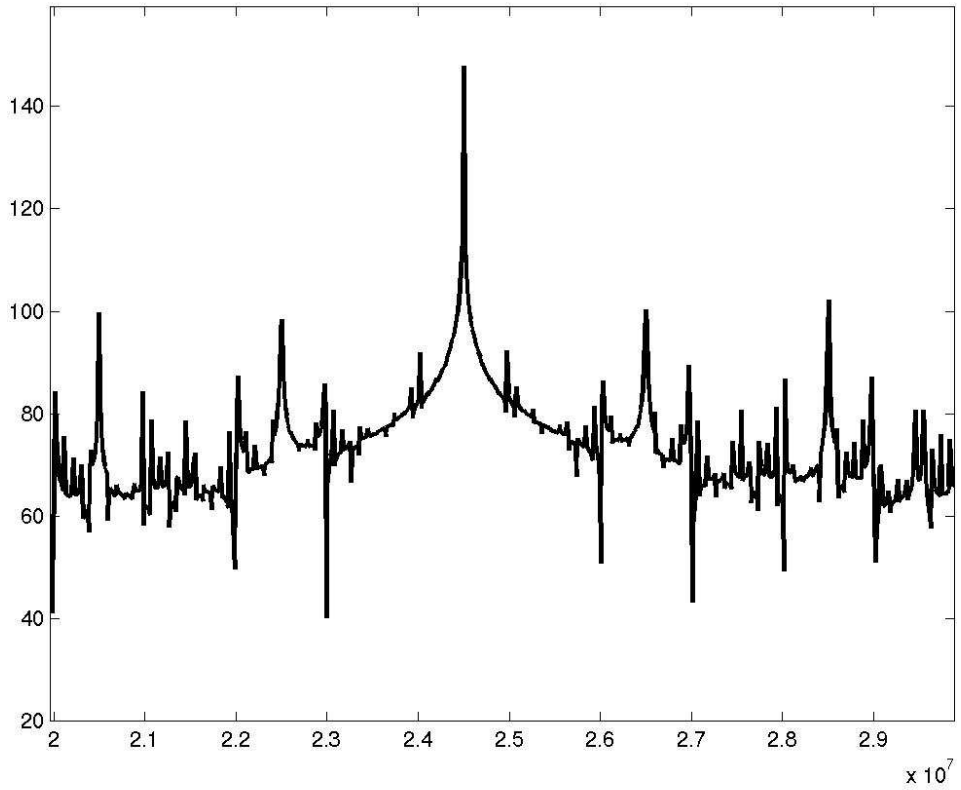
Measurement results : Accurate interpolation



-40dBc

-60 dBc

Behavioral Modeling :SOLL problem



The First SO of SOLL_45 synchronized by the external clock is responsible of a large amount of the accumulative phase error in SOLL_45

Conclusions (1)

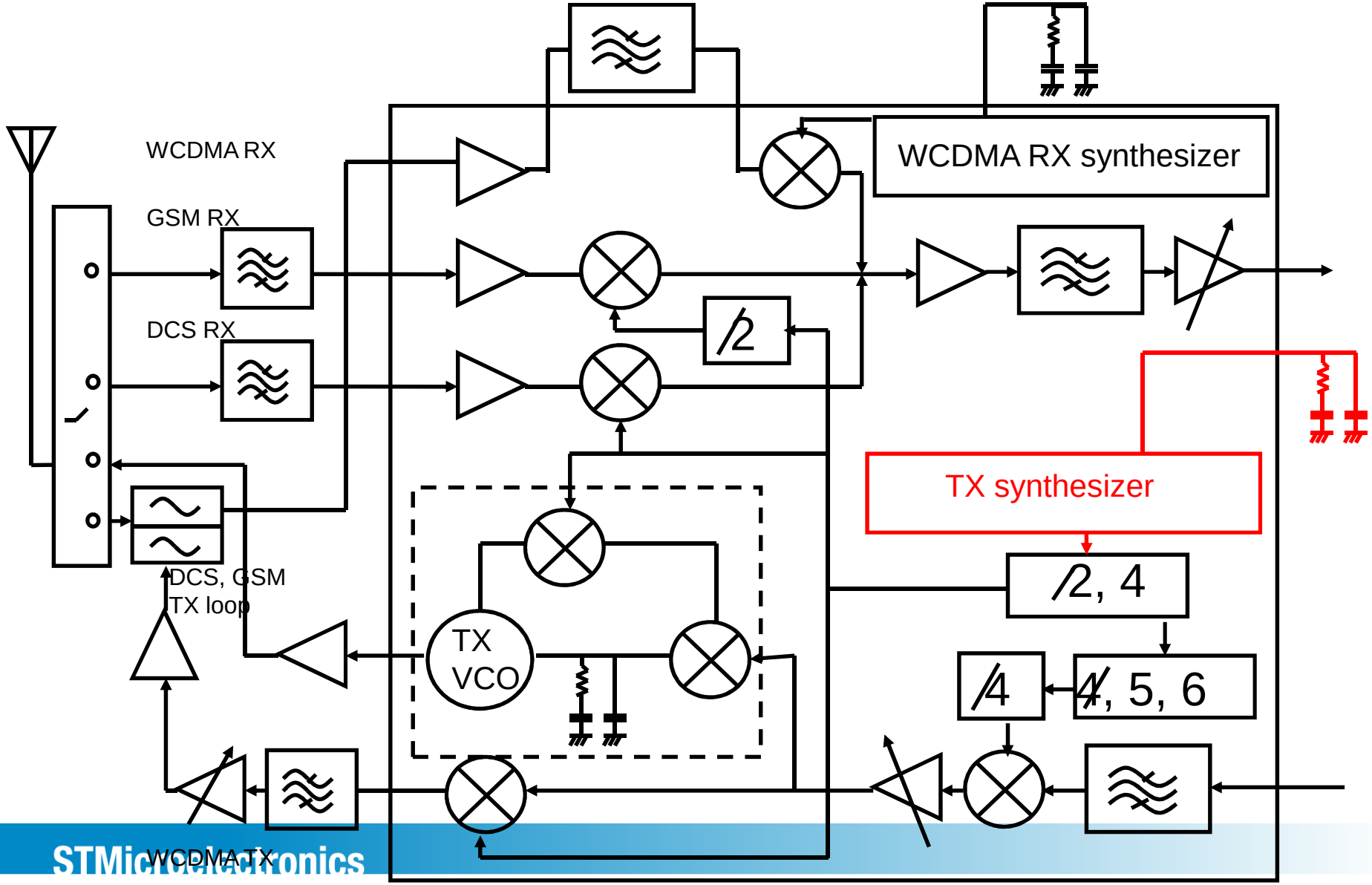
- Synchronous oscillator as Phase interpolator
- DLL with SO as delay element (SOLL)
- Application to decreases spurious tones in DDS
- Prototype: validation of principle

A Multimode GSM/DCS/WCDMA Double Loop Frequency Synthesizer

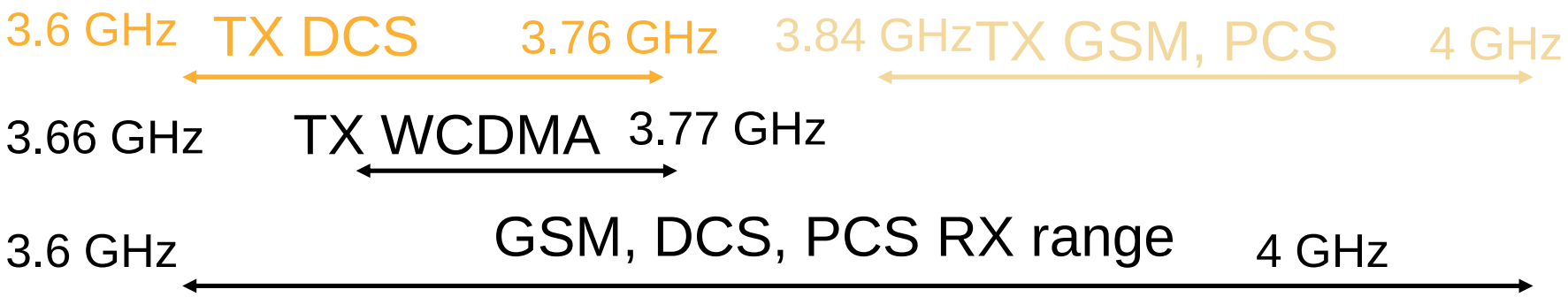
Franck Badets, Sebastien Rieubon, Laurent Camino, Thierry Divel, Sebastien Dedieu, Patrick Cerisier and Didier Belot

STMicroelectronics

GSM/DCS/WCDMA Transceiver Architecture



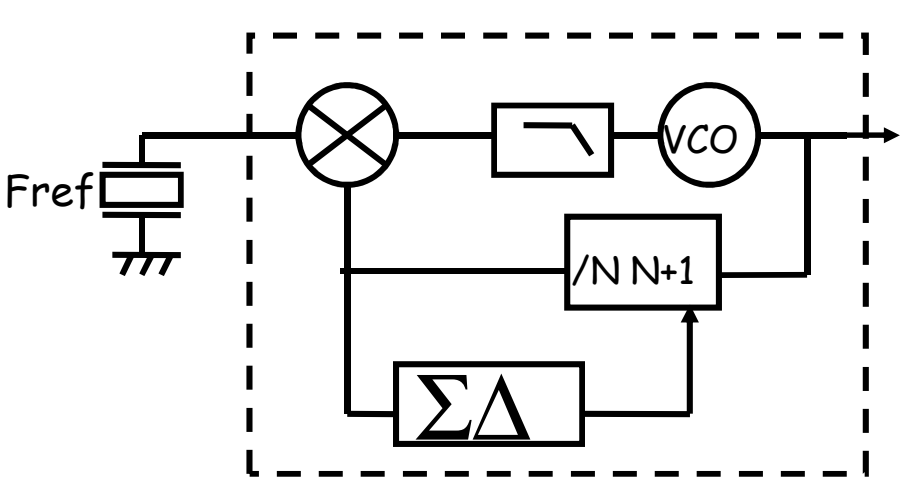
TX synthesizer Specifications

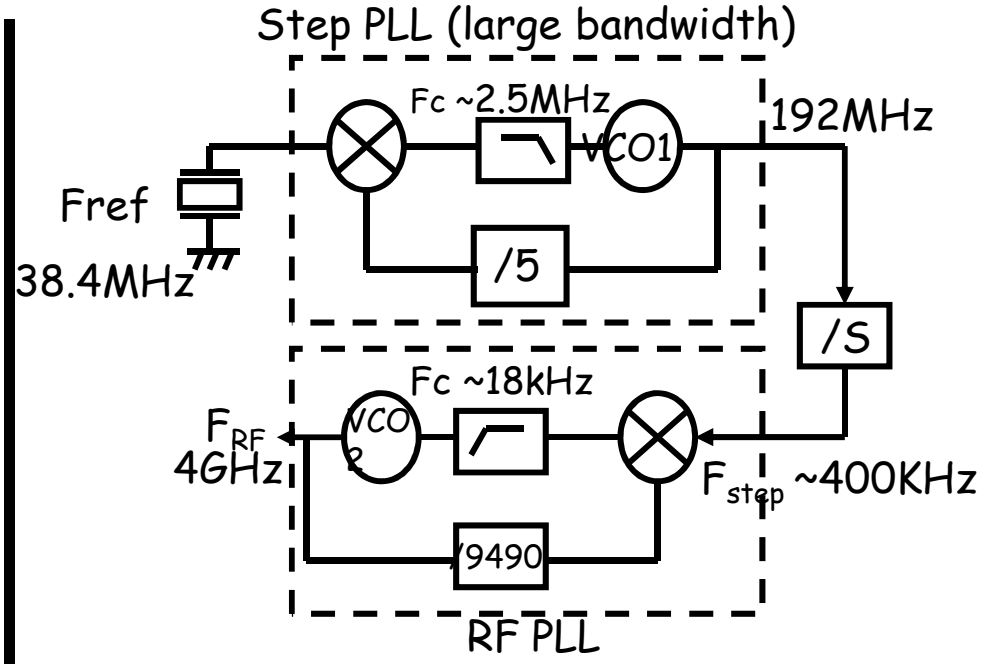


Mode	F_{step}
TX WCDMA	**32/34*(400 kHz) or 48/50*(400 kHz)**
TX GSM	**24/22*(400 kHz)**
TX DCS	**40/38*(400 kHz)**
TX PCS	**48/46*(400 kHz)**
RX GSM/DCS/PCS	**400 kHz**

TX synthesizer architecture choice (1)

Fractionnal Synthesizer VS Rationnal Synthesizer





$$F_{out} = (N + \frac{p}{2^n})F_{ref}$$

$$F_{step} = \frac{F_{ref}}{2^n}$$

$$F_{out} = (\frac{5N}{S})F_{ref}$$

$$F_{step} = (\frac{5}{S})F_{ref} = \frac{480}{S} * 400kHz$$

TX synthesizer architecture choice (2)

	Advantages	Drawbacks
Fractionnal Synthesizer	**- Seetling time requirement easily obtainable**	**-Spurious (noise coupling)** **-Complexity (SD modulation needed)**
Rationnal synthesizer	**- No fractionnal spurious**	**- Narrow bandwidth**

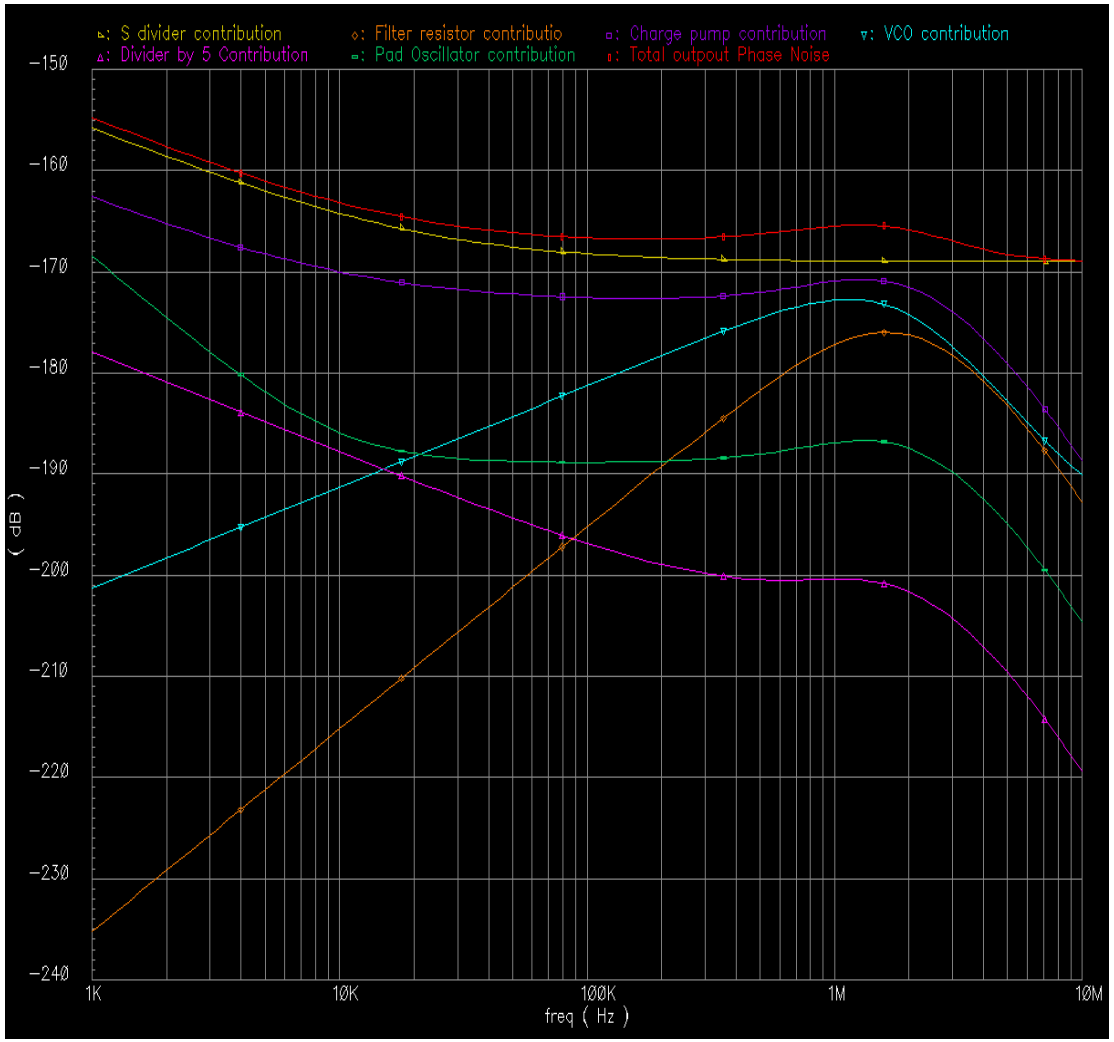
Rationnal Synthesizer good solution if :

-Step PLL fully integrable (with its loop filter)

-No significant added power consumption

-Silicon area comparable with ΣΔ modulator

PLL Step Implementation (1) : Noise



Phase noise floors :

- VCO : -142 dBc/Hz
- CP : -230 dBA
- S Divider : -169 dBc/Hz
- Loop Divider : -169 dBC/Hz
- Reference : -150 dBc/Hz

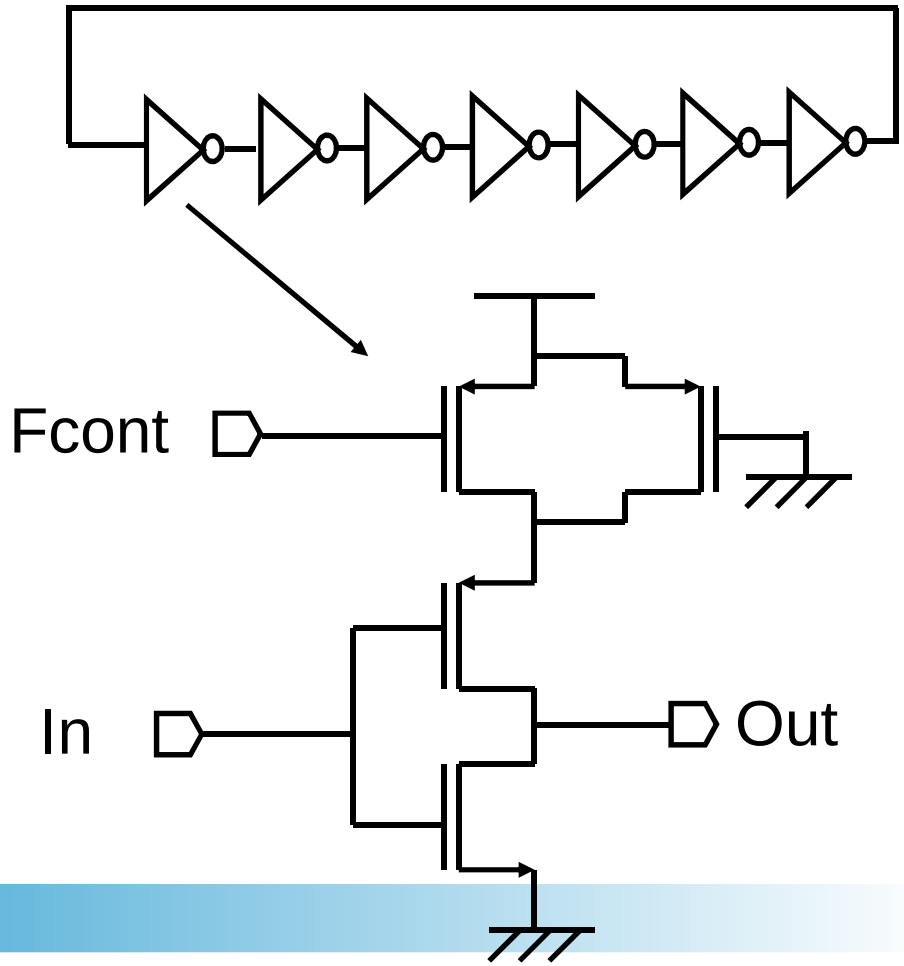
PLL Step Implementation (2) : Simulation Results

	Min	Typ	Max	Unit
CP current	80	100	120	µA
VCO gain	77	180	290	MHz/V
R2	3360	4200	5040	Ω
C2	37	46.8	56	pF
C1	4.2	5.2	6.2	pF
Phase Margin	32	55		degree
PN @1 kHz		-155	-155	dBc/Hz
PN @100 kHz		-167	-165	dBc/Hz
PN @1 MHz		-166	-160	dBc/Hz
PN @ 10 MHz		-169	-169	dBc/Hz

PLL step Implementation (3) : VCO

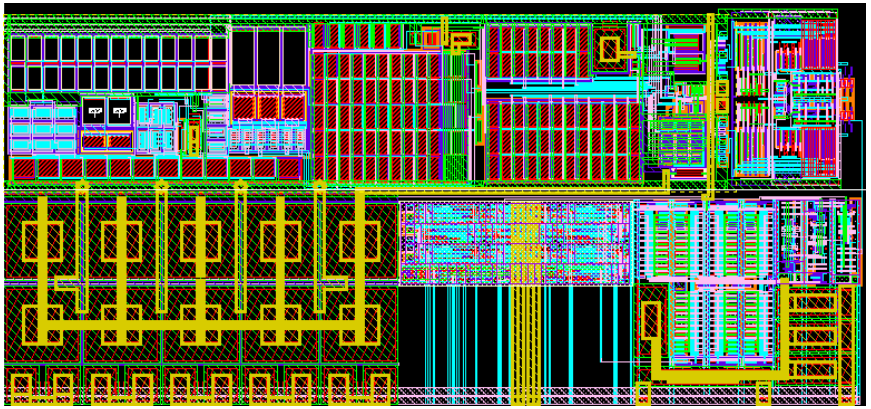
	Min	Typ	Max	Unit
alim	2.5	2.6	2.7	V
Temperature	-30	27	100	°C
$f_{0\ (vcon\ \ t=1.3\ V)}$	118	190	324	MHz
$f_{min\ (vcont\ =\ 2.2V)}$	46	74	136	MHz
$f_{max(vcont\ =\ 0.6\ V)}$	224	310	476	MHz
VCO gain @192 MHz	77	180	290	MHz/V
PN @ 1 kHz		-28	-25	dBc/Hz
PN @ 10 kHz		-58	-55	dBc/Hz
PN @ 100 kHz		-88	-85	dBc/Hz
PN @ 1 MHz		-117	-115	dBc/Hz
PN @ 10 MHz		-142	-141	dBc/Hz

Full CMOS Seven Stages Ring Oscillator



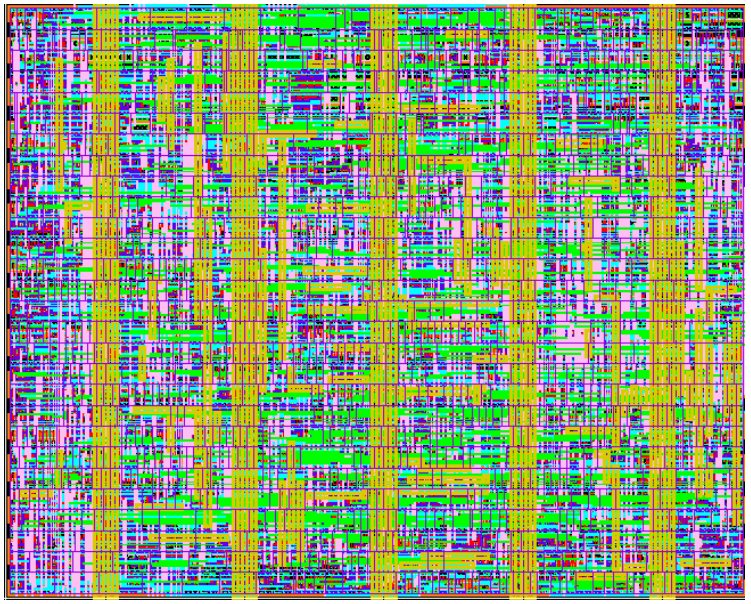
PLL step Implementation (4) : layout

PLL step layout



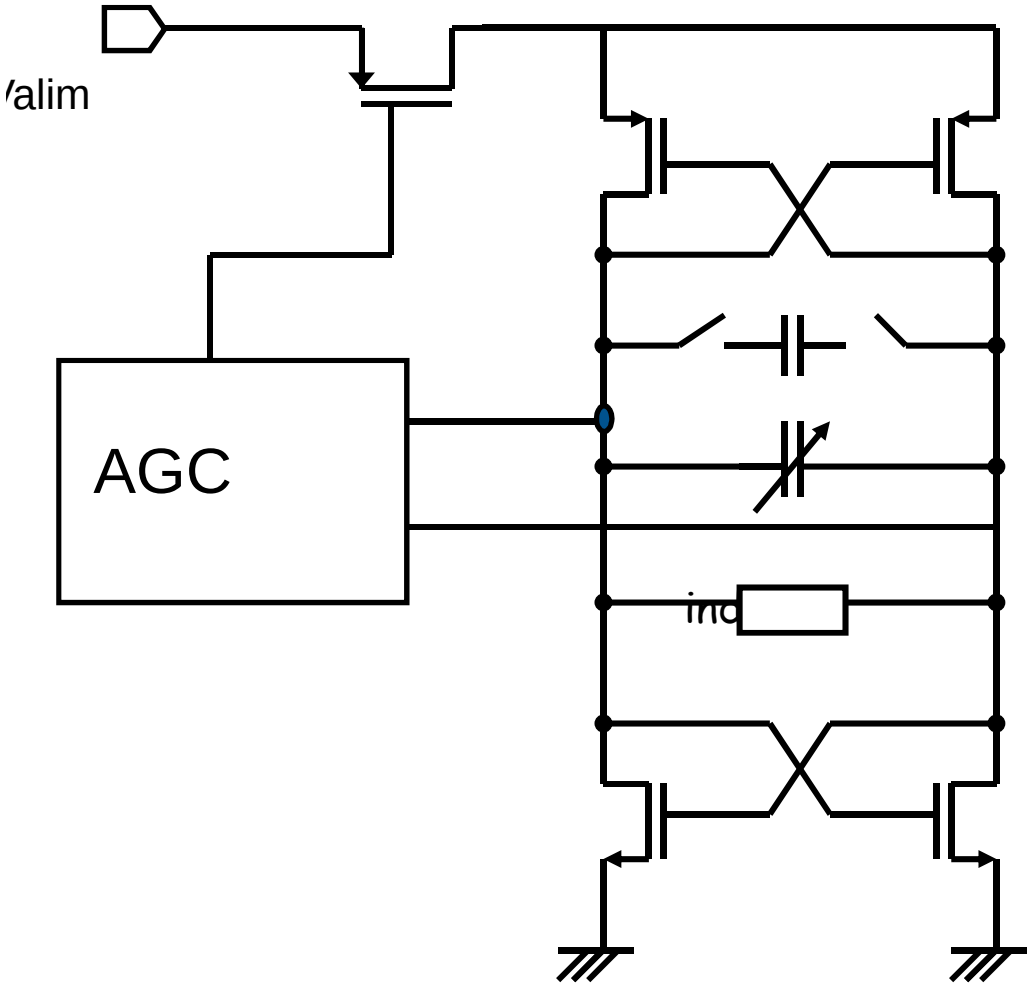
Dx = 380 µm
Dy = 180 µm

ΣΔ layout
(4th order MASH)



Dx = 320 µm
Dy = 260 µm

RF VCO Implementation (1)



-Amplitude control loop

- 5 bits bank capacitors

- 0.55nH inductor

- 3.6 - 4 GHz band (3.2 -4.4 GHz for PVT purpose)

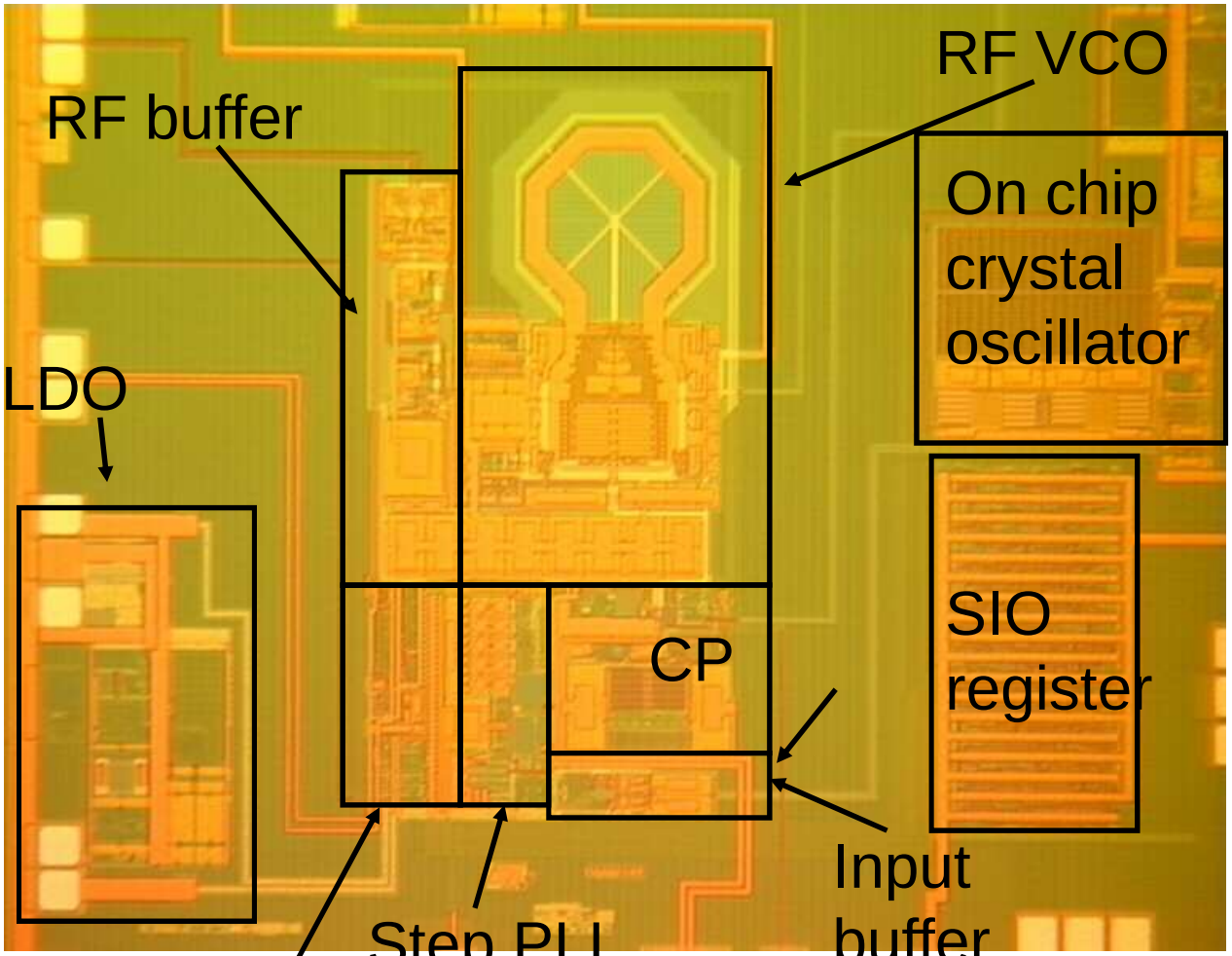
- -117 dBc/Hz @ 400 kHz

RF VCO Implementation (2)

Temperature (°C)	Process	Consumption (mA)	Magnitude (V)	PN @ 400kHz (dBc/Hz)
-30	S	6.7	1.47	-117
	T	6.5	1.47	-120
	F	6.8	1.47	-118
27	S	8	1.5	-119.5
	T	7.6	1.5	-120
	F	7.8	1.5	-119.5
100	S	9.8	1.48	-119
	T	9.3	1.53	-119
	F	9.3	1.53	-118.5

- Frequency band : 3.04 – 4.8 GHz;
- Post extract simulation : 2.8 – 4.15 Ghz

TX Synthesizer Implementation

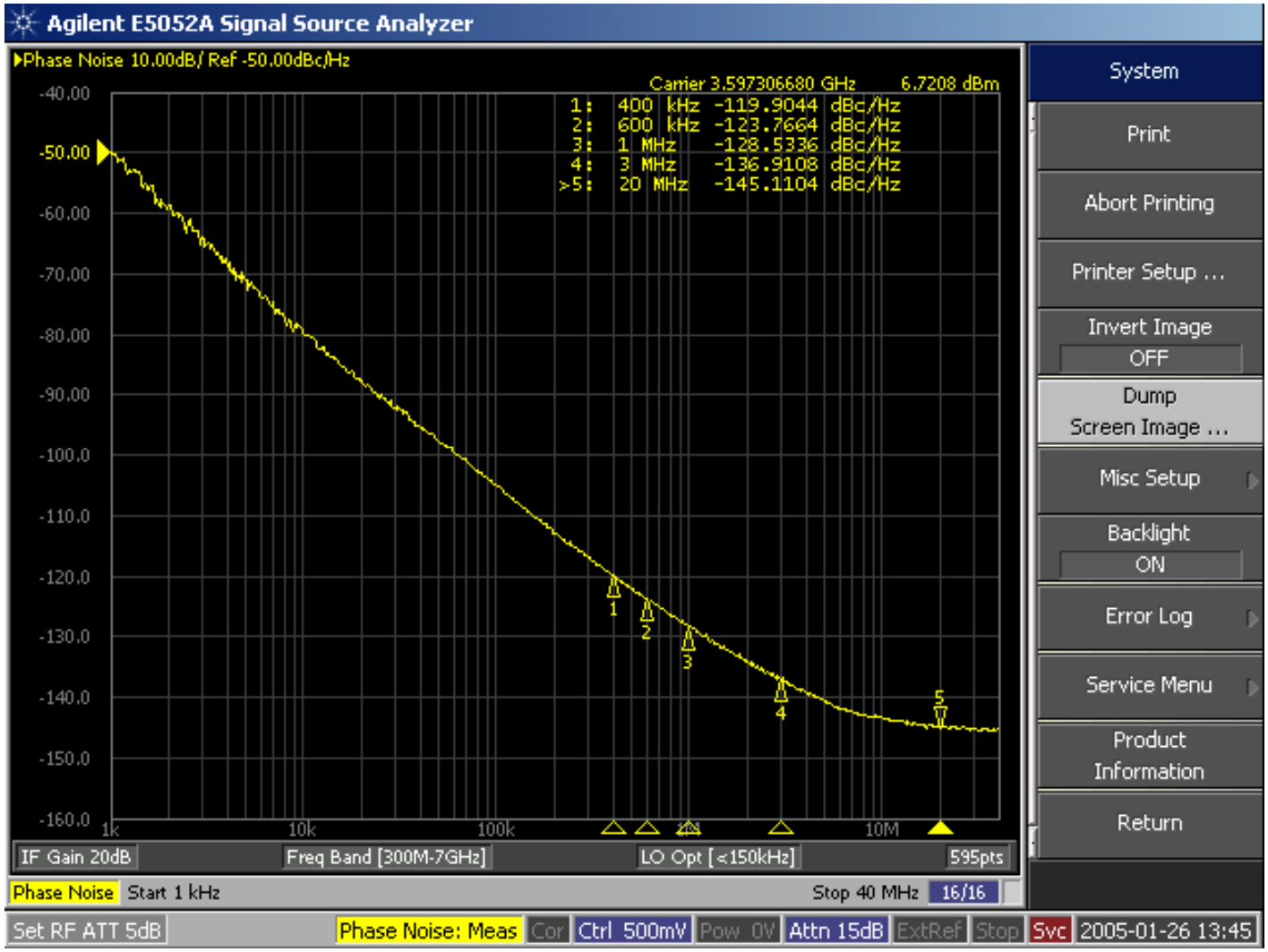


- RF 0.25un ST BiCMOS technology

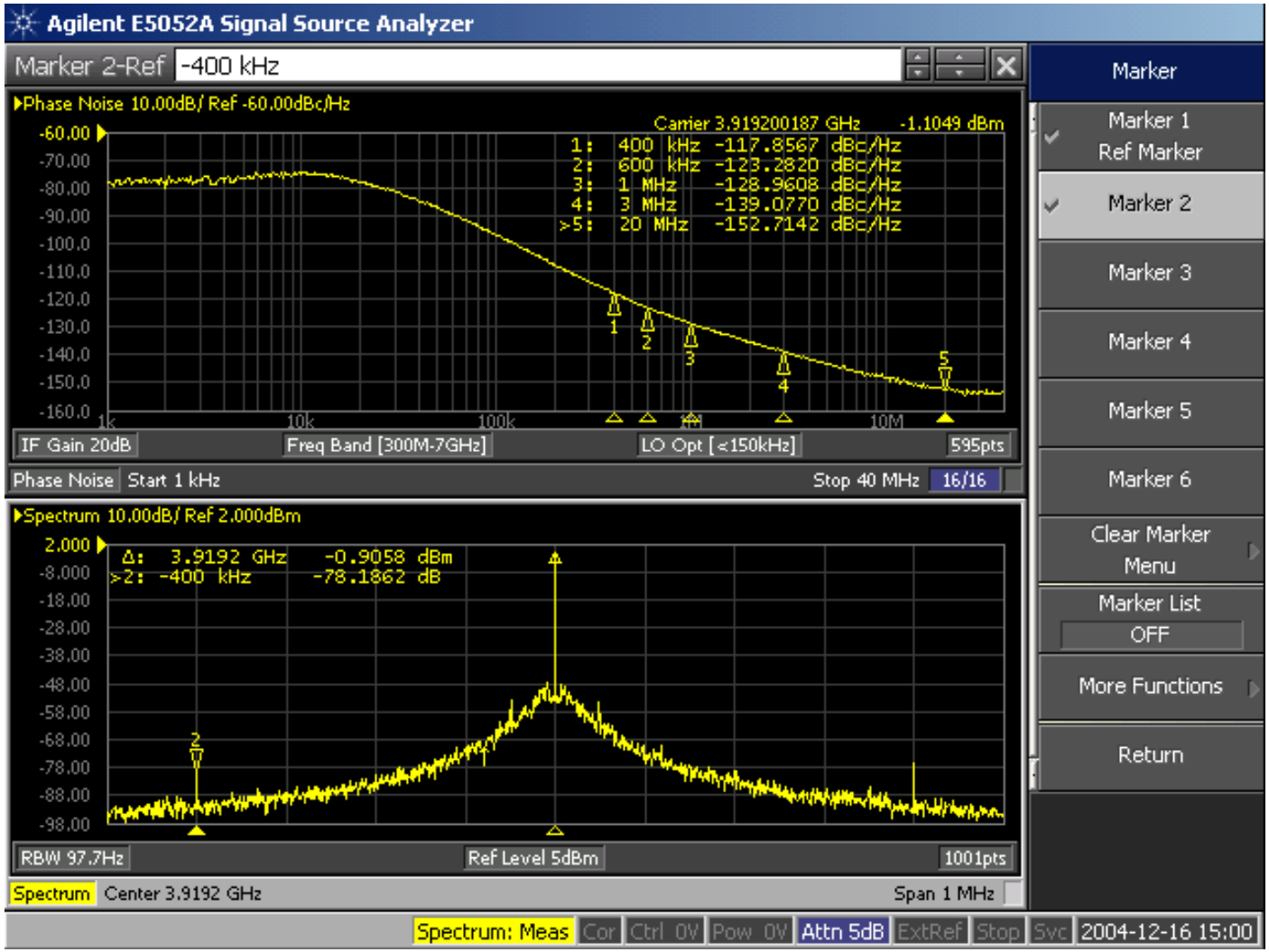
-Three LDOS (RF VCO, Crystal oscillator and PLLs)

-700 µm x 1300 µm

Measurement results (1) RF VCO phase noise



Measurement results (2): TX phase noise



Main Measurement Results (3)

Parameter	Specification	Measured value
Tuning range	3.6 – 4 Ghz	3.6 – 4. GHz
PN in band	-80 dBc/Hz	-76 dBc
Pn @ 400 kHz	-117 dBc/hz	-118 dBc / Hz
PN @ 600 kHz	-122 dBc/Hz	-123 dBc /Hz
PN @ 3 MHz	-136 dBc/Hz	-137 dBc /Hz
Integrated noise (400 Hz -1.92 MHz)	-32 dBc	-30 dBc
Power consumption (under 2.7 V)		~ 21 mA

Outline

- Introduction
  - Frequency Synthesis - Where and Why?
  - Specificactions
- Frequency Synthesizer Architectures
  - Direct Digital Synthesizer
  - Integer N PLL
  - Fractional PLL
- Implementation examples
  - Phase Interpolator based DDS
  - Multimode GSM/DCS/PCS frequency Synthesizer
  - 40 GHz PLL for 60 GHz UWB transceiver

A 17.5-to-20.94GHz and 35-to-41.88GHz PLL in 65nm CMOS for Wireless HD Applications

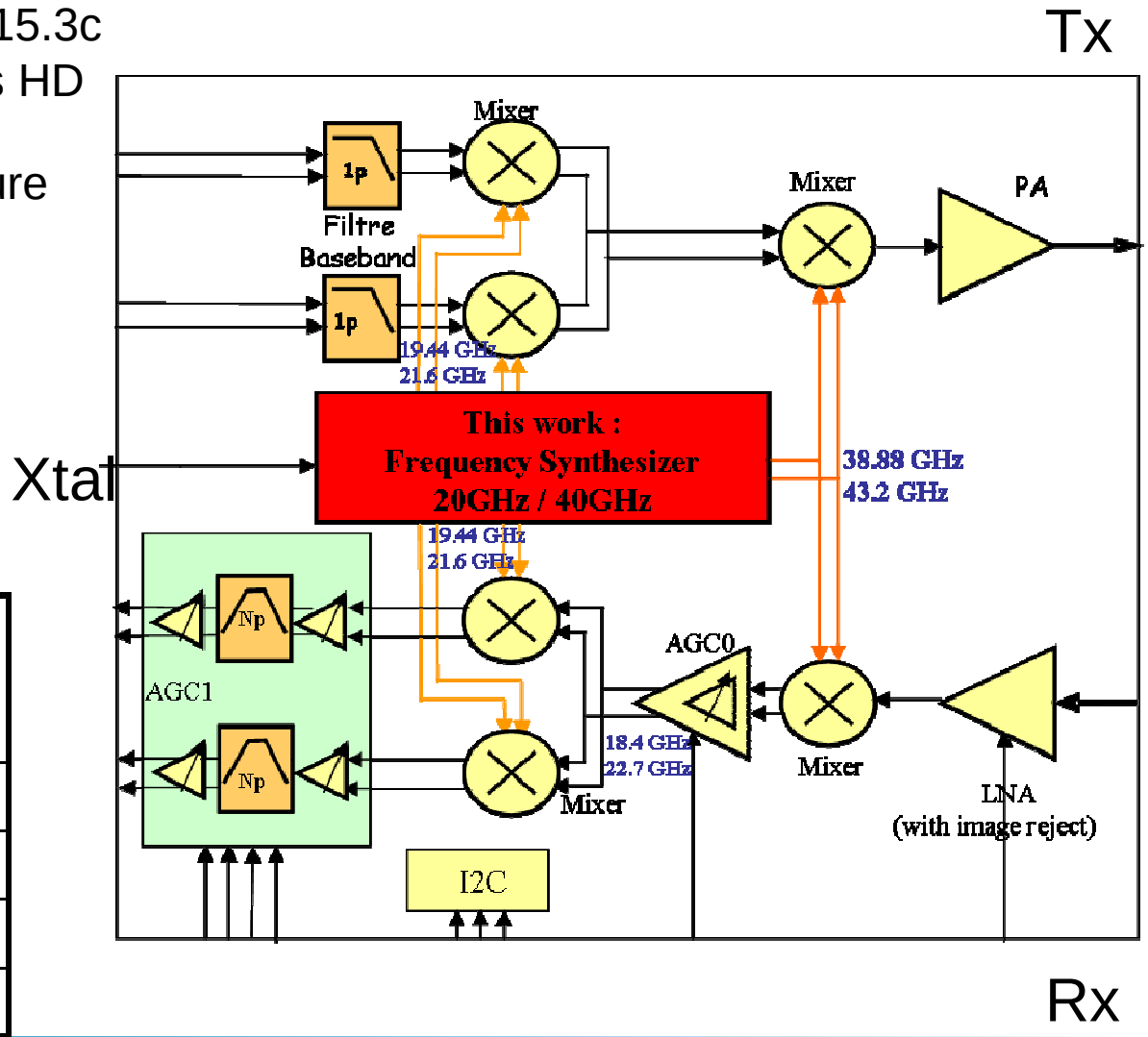
Olivier Richard[1], Alexandre Siligaris[2], Franck Badets[3], Cedric Dehos[2], Cedric Dufis[1], Pierre Busson[1], Pierre Vincent[2], Didier Belot[1], Pascal Urard[1]

[1]STMicroelectronics, Crolles France
[2]CEA-LETI-MINATEC, Grenoble France
[3]STMicroelectronics, Grenoble France

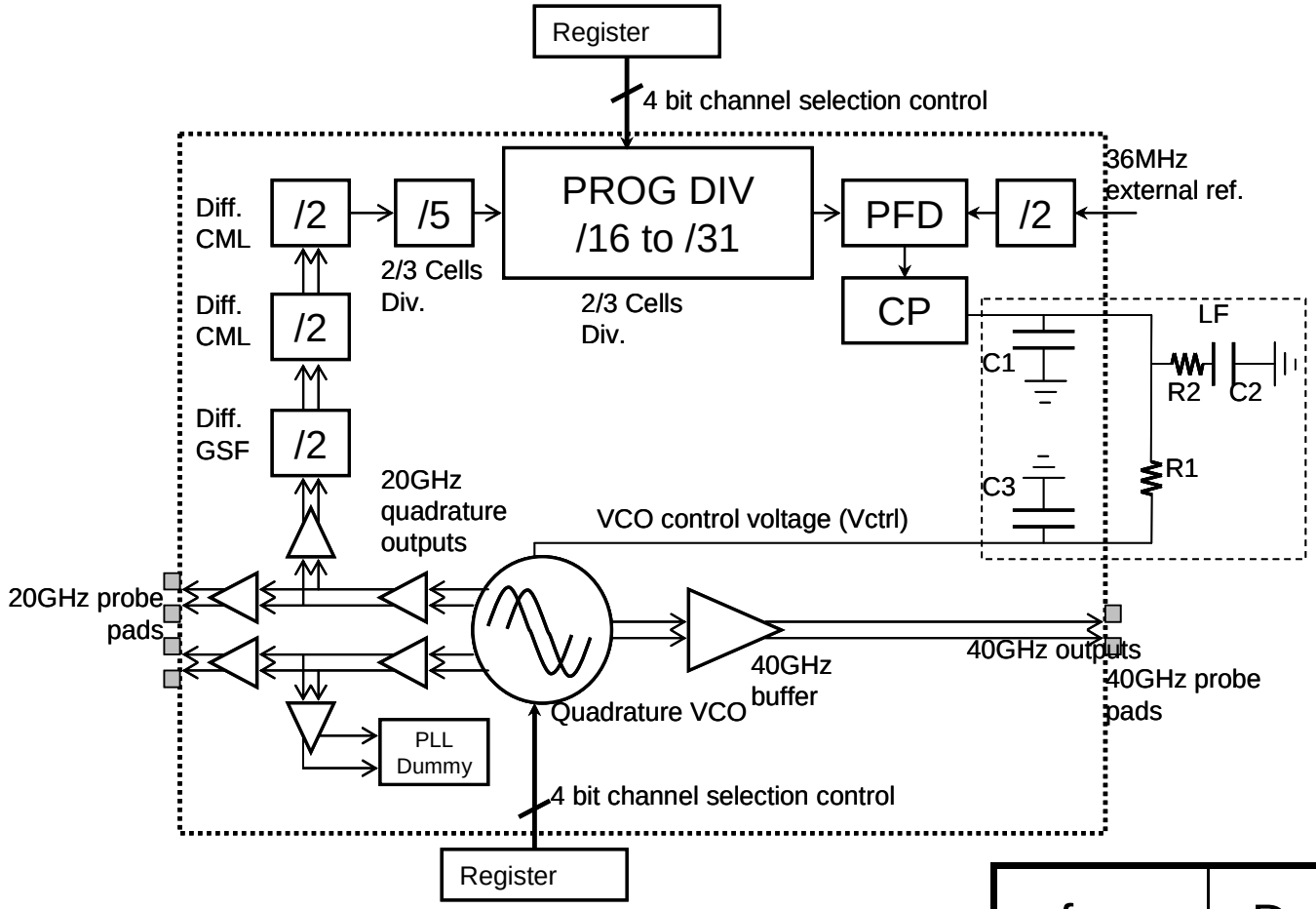
Introduction

- The frequency synthesizer must be compliant with IEEE 802.15.3c standard for 60GHz Wireless HD
- Double conversion architecture with zero IF final stage
- The frequency synthesizer delivers 20GHz and 40GHz signals
- 65nm CMOS technology

Standard Channel	LO1 Freq. (GHz)	LO2 Freq. (GHz)
A1	19.44	38.88
A2	20.16	40.32
A3	20.88	41.76
A4	21.6	43.2



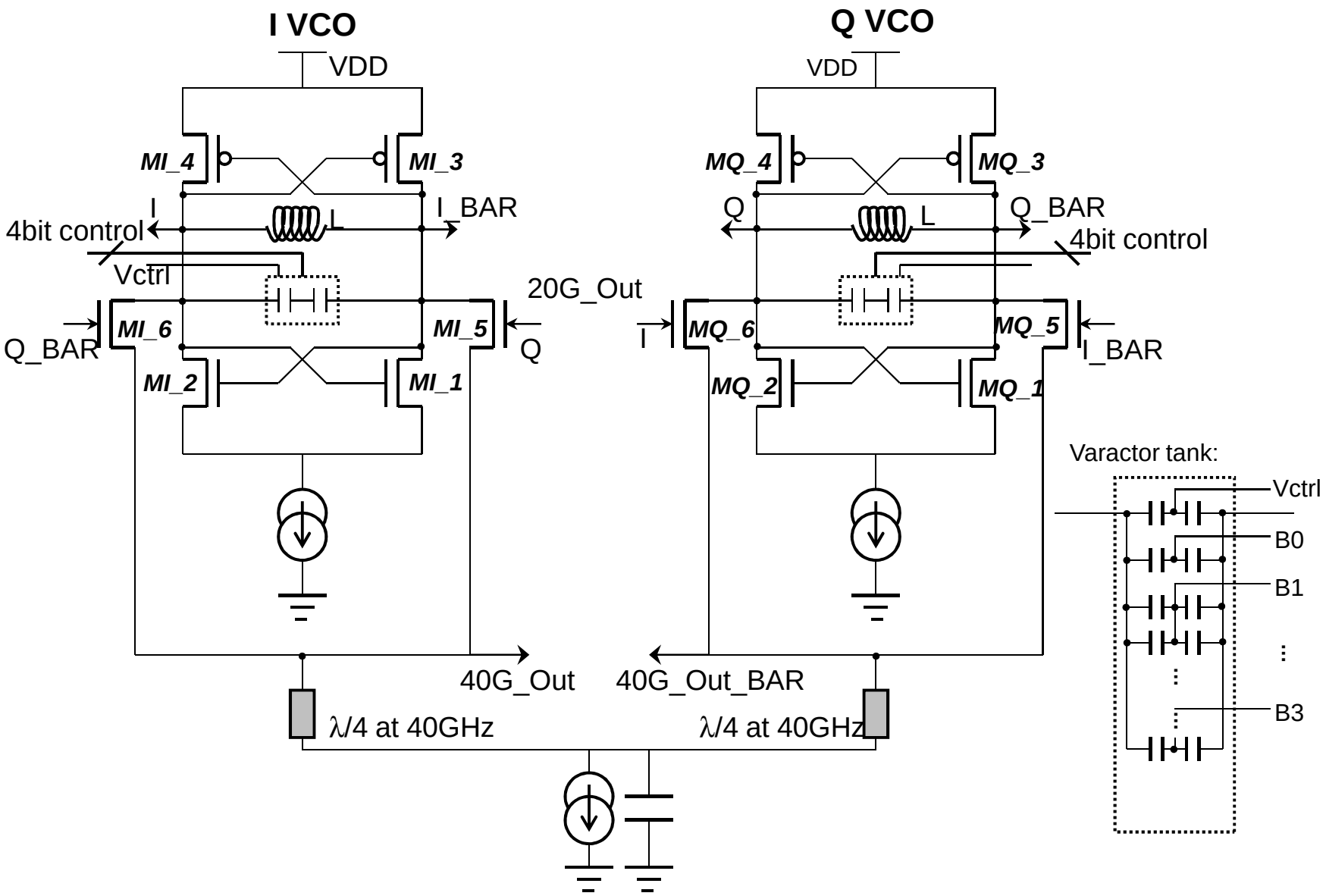
PLL architecture



$$f_{LOCK} \frac{f_{REF}}{2} \cdot D_{DIV} \cdot D_{PROG}$$

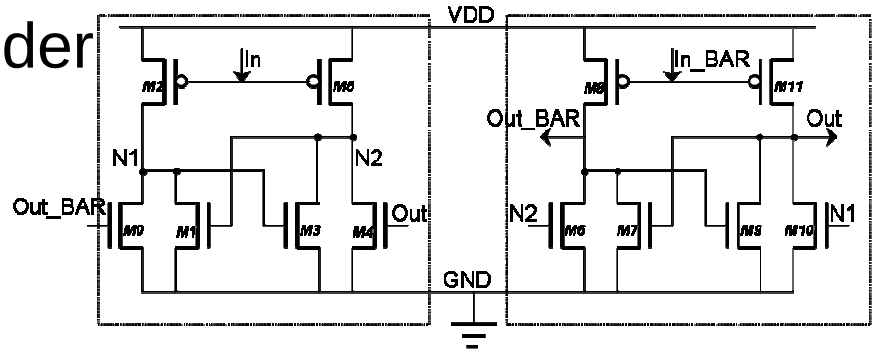
f_{REF}	D_{DIV}	D_{PROG}
36MHz	40	16 to 31

Circuit design: quadrature VCO

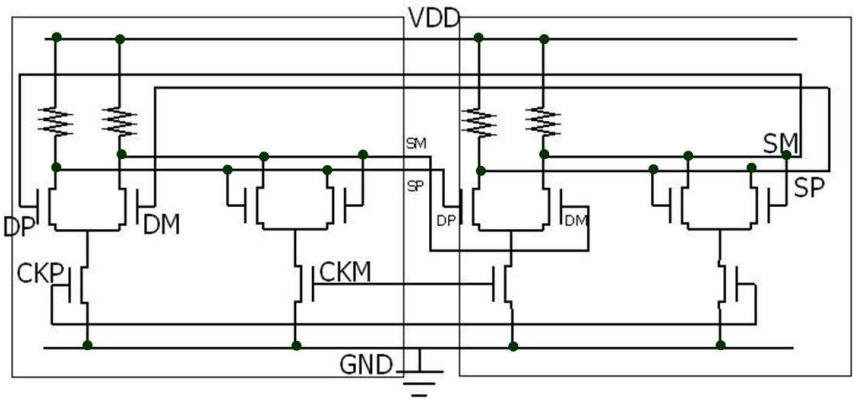


Circuit design: Dividers' schematics

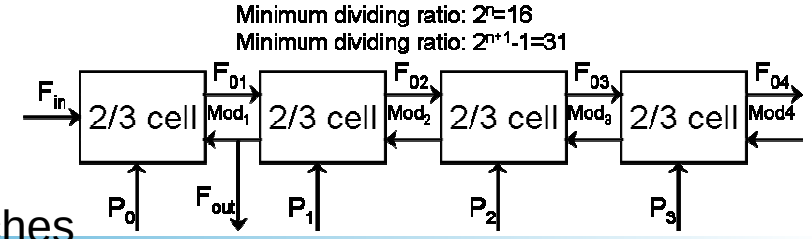
- Grounded Source Frequency Divider
  - Divider by 2 @20GHz
  - 2 D-Latches in master-slave
  - DC supply 1.2V
  - N and P MOS low power RF



- Current Mode Logic Divider
  - Divider by 2 @10GHz and @5GHz
  - 2 D-Latches in master-slave
  - DC supply 1.2V
  - N & P MOS low power RF

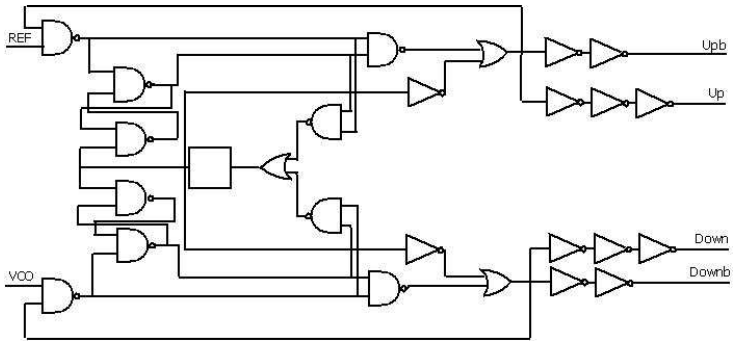


- Modular Programmable Prescaler
  - Programmable divider using 2/3 cell based modular architecture
  - Division range : 16-to-31 with 4 cells
  - 2/3 cell is composed to 3 NAND and 2 D-Latches

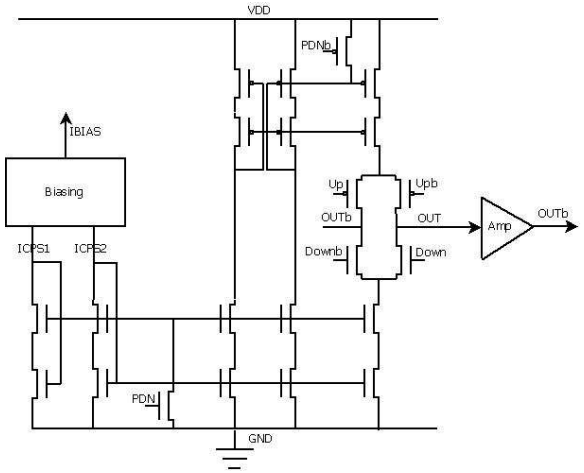


Circuit design: other blocks of the PLL

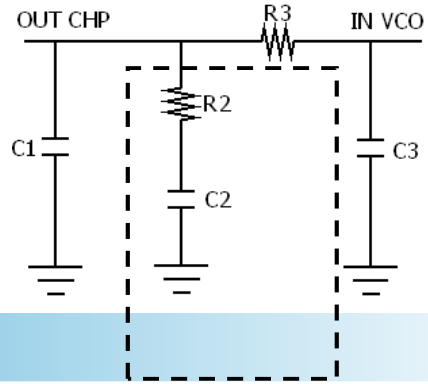
- Phase-Frequency Detector design
  - Sequential Phase detector
  - DC supply 1.8V
  - N and P MOS Thick gate oxide
  - Core Library



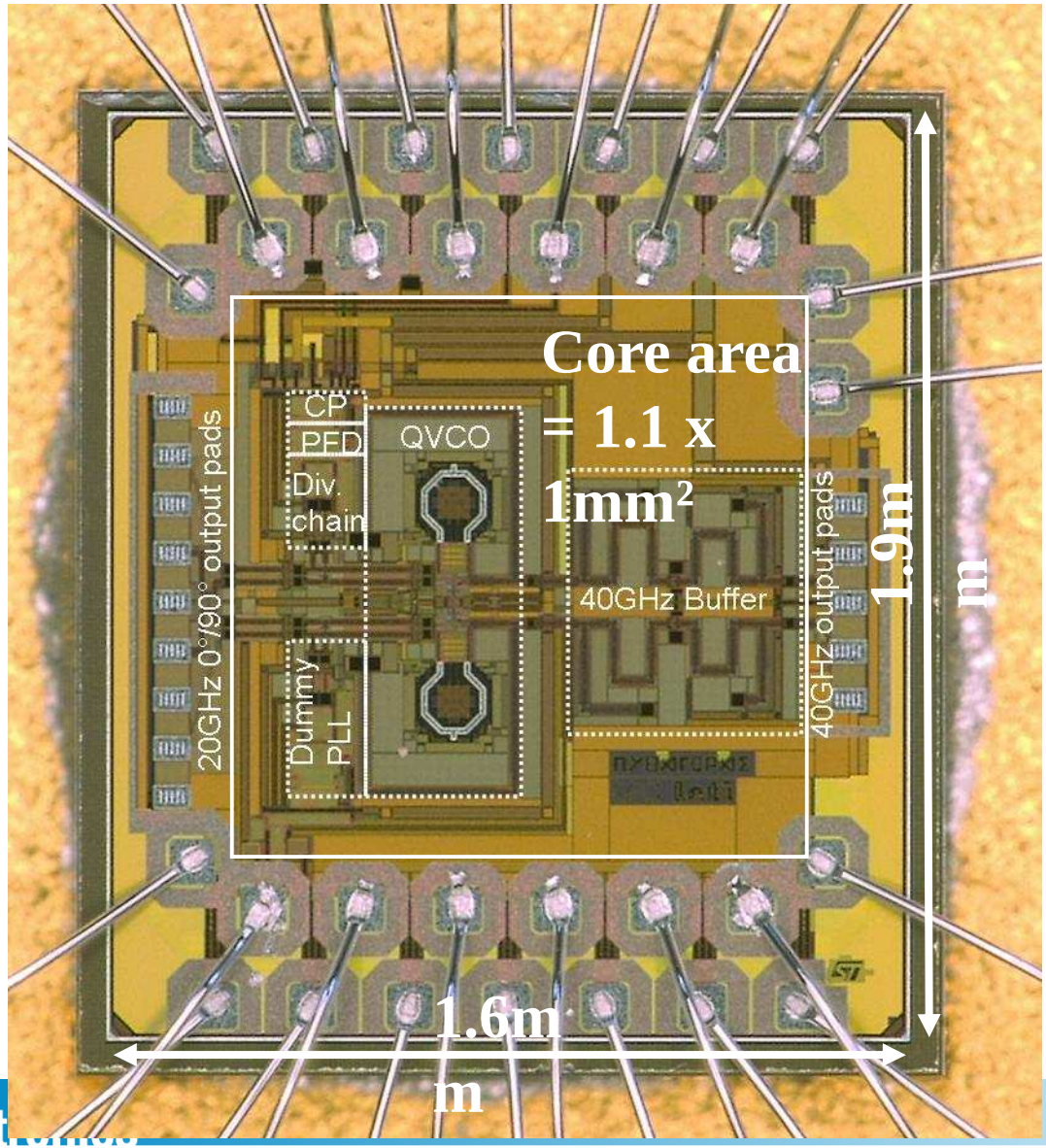
- Charge Pump
  - External current biasing
  - DC supply 1.8V
  - N and P MOS Thick gate oxide



- Loop filter
  - 3rd order Loop Filter
  - External components : C2, R2 and R3
  - Integrated components : C1 and C3
  - Chosen to allow a better rejection of spurious out of the range ($\omega > \omega_c$)



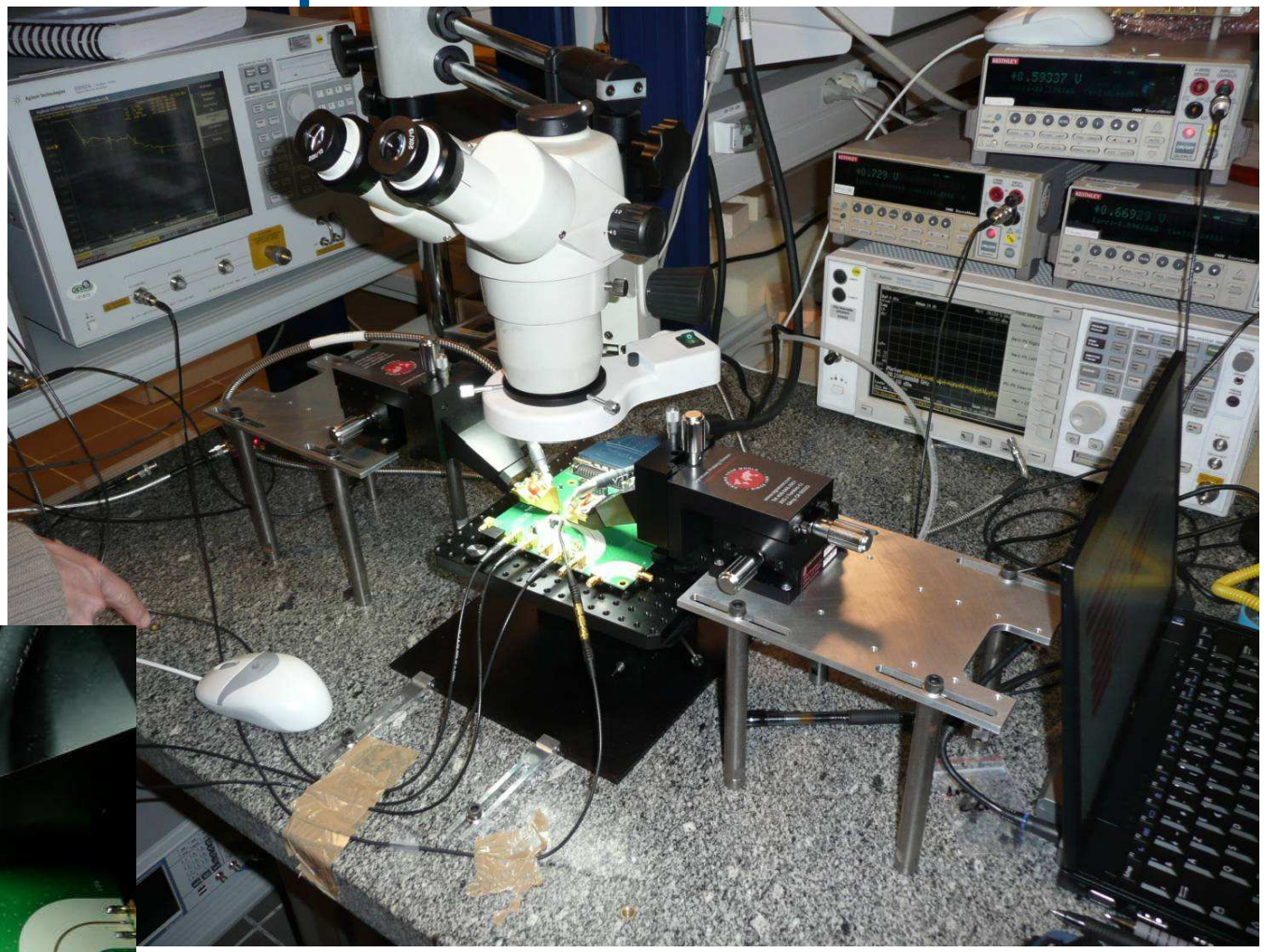
Circuit design: Die Photograph

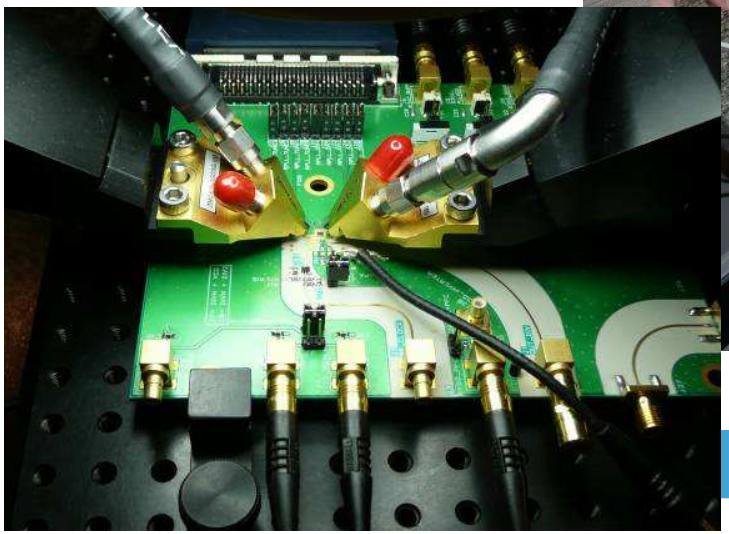


Experimental Results

PLL measurement setup

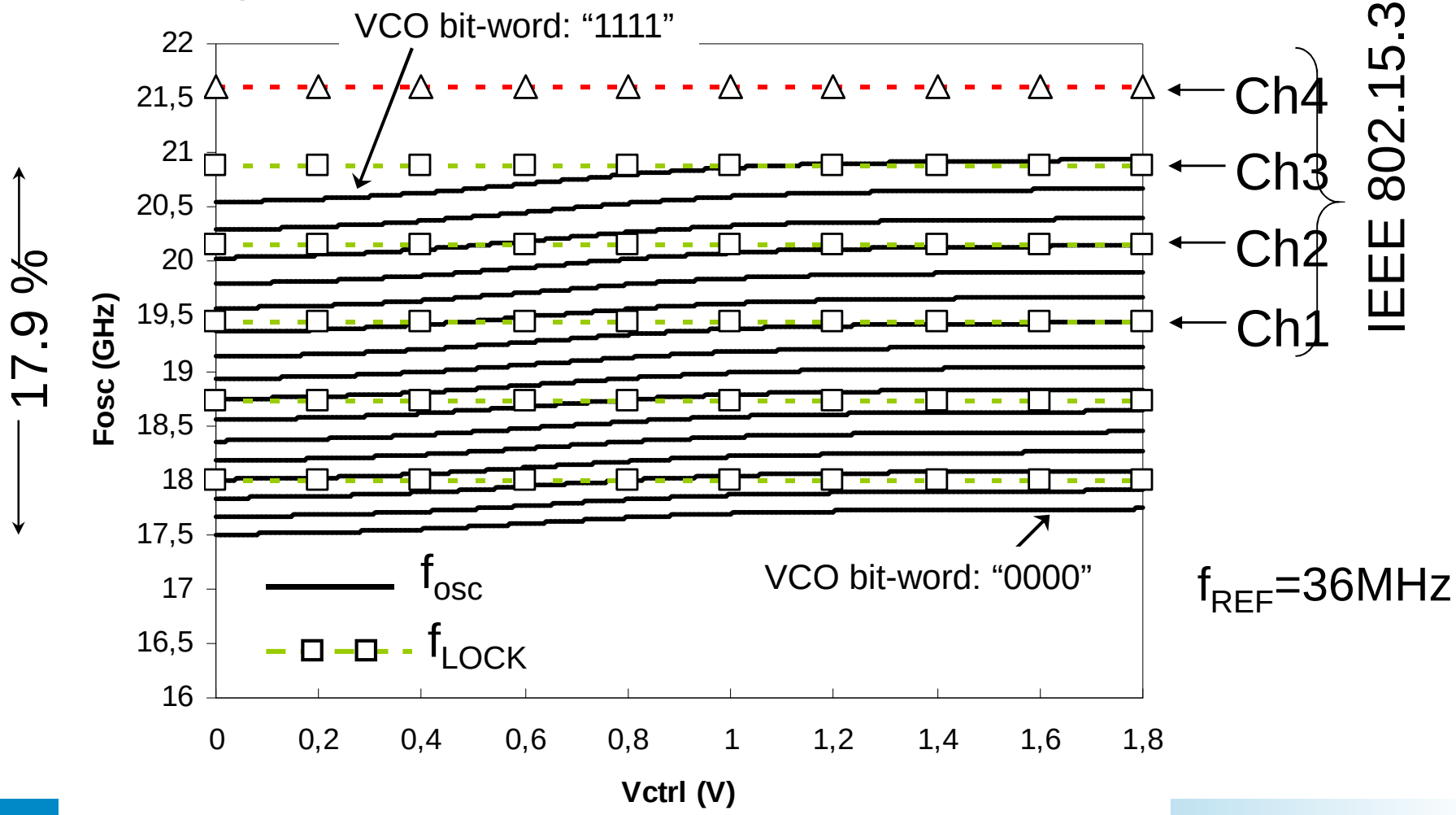
- PLL on Roger 4003 PCB
- Low frequency signals wire bonded
- 20GHz and 40GHz signals measured on chip with differential probes





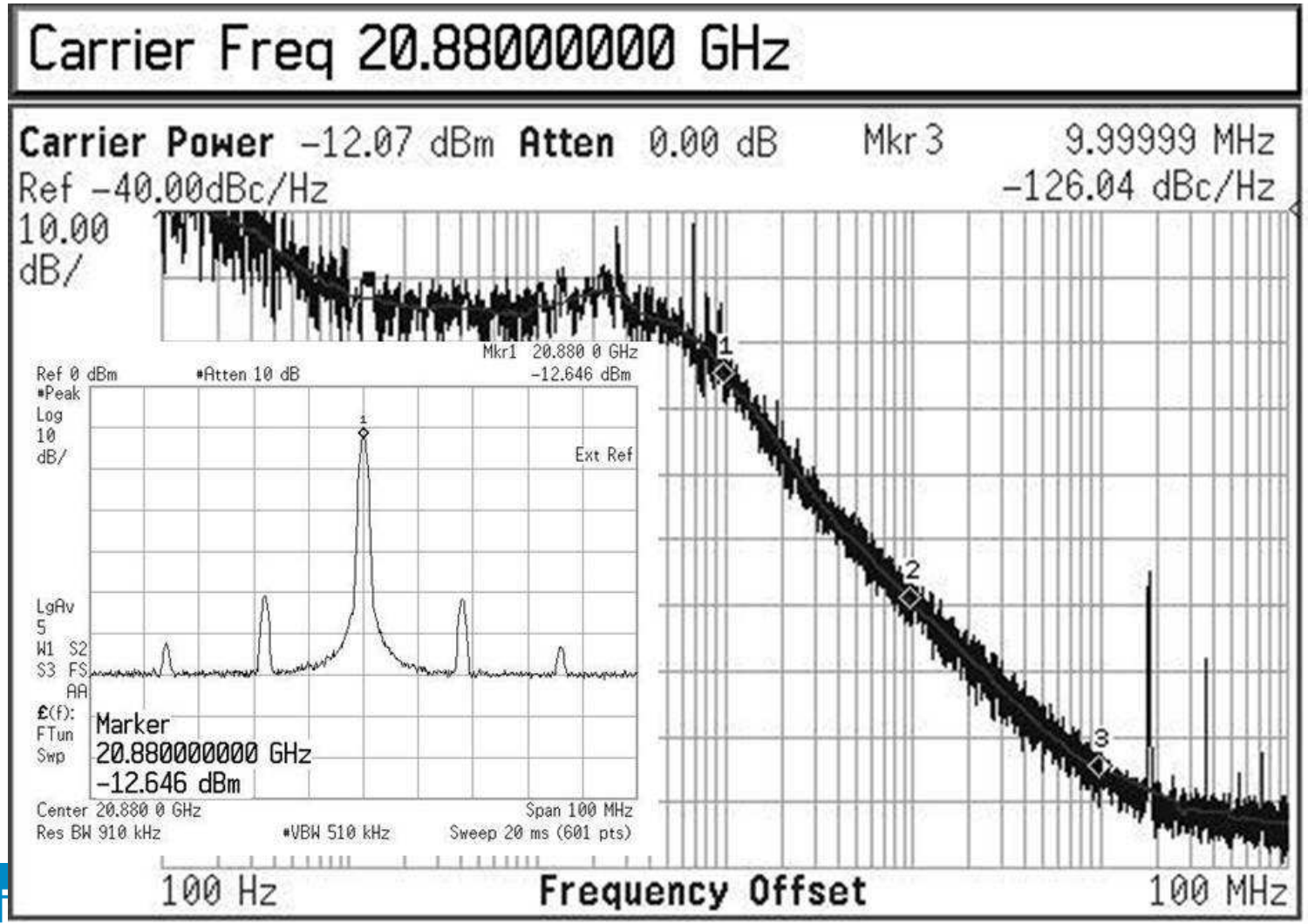
Experimental results

Locking frequencies of the synthesizer



Experimental results

Measured Phase Noise at the 3rd channel (20.88GHz)



Experimental results

Phase Noise Measurement table

Channels Frequency (GHz)	19.44	20.16	20.88	21.6
PN @100kHz (dBc/Hz)	-66.4	-66.1	-71.2	n.a
PN @1MHz (dBc/Hz)	-100.2	-100.4	-100.6	n.a
PN @10MHz (dBc/Hz)	-125.5	-125.6	-126.7	n.a
PN @40MHz (dBc/Hz)	-133.3	-132	-135.2	n.a

Comparison of CMOS PLL

	This work	[1]	[2]	[3]	[4]
Tech. [nm]	65 CMOS	90 CMOS	45 CMOS	90 CMOS	65 CMOS
Supply [V]	1.2**	1.2	1.1	1.2	1.2
Frequency range [GHz]	17.5 to 20.94 **(17.9%)** 35 to 41.88 **(17.9%)**	39.1 to 41.6 (6.2%)	57 to 66 (14.6%)	58 to 60.4 (4%)	96
Phase noise [dBc/Hz]	**-100 (20.88GHz) -97.5 (41.76GHz)**	-90	-75	-85	-75.2
Calculated @ 20GHz Phase noise [dBc/Hz]	**-100**	-96	-84.6	-94.6	-88.9
F_{ref} [MHz]	36	50	100	234.1	375
Loop Type	Integer	Fractional	Integer	Integer	Integer
Division Ratio(s)	640 to 1240	512 to 2032	512 to 8184	256 to 258	256
Ref. Spur [dBc]	<-50	-54	-42	-50.4	-51.7
Power [mW]	80	64*	78	80	43.7*

*Without Output Buffer

**The supply voltage of PFD and CP is 1.8V

[1] S. Pellerano and al., ISSCC2008

[2] K. Scheir and al., ISSCC2009

[3] C. Lee and al., ISSCC2007

[4] K. Tsai and al., ISSCC2009

Conclusion

- PLL in 65nm CMOS LP technology compliant with IEEE 802.15.3c standard for 60GHz Wireless HD
- 20GHz and 40GHz bands for double conversion transceivers
- 17.9% tuning range
- -100dBc/Hz phase noise at 1MHz of the carrier