Frequency Synthesis

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Outline

- Introduction
  - Frequency Synthesis - Where and Why?
  - Specifications
- Frequency Synthesizer Architectures
  - Direct Digital Synthesizer
  - Integer N PLL
  - Fractional PLL
- Implementation examples
  - Phase Interpolator based DDS
  - Multimode GSM/DCS/PCS frequency Synthesizer
  - 40 GHz PLL for 60 GHz UWB transceiver
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- **Introduction**
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- **Frequency Synthesizer Architectures**
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- **Implementation examples**
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Frequency Synthesis: Where - Why?

Diagram:

- FI
- LO
- RF
- FL

STMicroelectronics
Specifications (1)

- Five principal specifications
  - 1) Frequency range
  - 2) Frequency Step
  - 3) Accuracy
  - 4) Settling time
  - 5) Phase Noise – Spurious

- Specifications are obtained from the standard under consideration and the transceiver architecture.
Specifications (2)

GSM example:

- RX band: 935-960 MHz
- Channel spacing: 200 kHz
- Settling time: 176µs maximum
- Accuracy: 0.1 ppm
Phase Noise (1): Ideal Case

Ideal Case: The oscillator delivers a pure sinus
Phase Noise (2): real case

Real oscillator spectrum presents some lobes due to component noise (1/f, thermal noise...)

\[- V_{\text{LO}} (t) = A \cos(\omega_{\text{lo}} t + \phi(t))\]

\[= A \cos (\omega_{\text{lo}} t) \cos(\phi (t)) - A \sin (\omega_{\text{lo}} t) \sin (\phi (t))\]

\[= A \cos (\omega_{\text{lo}} t) - A \phi (t) \sin (\omega_{\text{lo}} t)\]
Phase noise (3): measurement unit

\[ L(f_m) = 10 \log_{10} \left( \frac{P(f_0 + f_m) \text{ in } 1 \text{ Hz band}}{P_{\text{carrier}}} \right) \]
Phase Noise (4): consequences on mixing

- Signal to be received between strong interferers in adjacent channel
- LO phase noise down-converts interferers in FI: signal corruption
RX specification translation

\[ L(fm) = \frac{C}{l(fm)} - \frac{C}{l_{cc}} - 10\log(BW) \]
TX specification translation

\[ L(fm) = CP - AP(fm) - 10\log(BW) \text{ in } \text{dBc/Hz} \]

- **CP**: carrier power
- **AP**: allowed transmitted power in channel considered
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Key Component: phase accumulator

Grande Période = $T_{GP}$
Pulse Output DDS (2)

- Output is periodic. Period when output comes back to 0. It is equal to $x \cdot T_{\text{clock}}$, where $x$ is the smallest integer value as:

$$x = y \frac{2^n}{p}$$

- $x$ is the number of time $p$ is added
- $y$ is the number of time of overflow

- Frequency synthesis possible using overflow bit

$$f_{\text{ovw}} = \frac{p}{2^n f_{\text{clk}}}$$
Pulse Output DDS (3)

- Frequency true on average only: lot of spurious tones separated by $1/(x \cdot Tck)$
Pulse Output DDS (4): Phase Interpolator

- Every overflow occurrence, phase accumulator value is a digital information of the phase error between generated signal and spuriousless ideal signal.
- Solution to decrease spurious tones:
  - Calculation $C/P$ (not trivial as $P$ could take any value between 1 and $2^{(n-1)}$)
  - Ratio value is used to select the phase that interpolates the best the ideal signal.
Pulse Output DDS (5): Advantages / Drawbacks

**Advantages**
- High resolution++
- Good Phase noise+
- Switching time++
- Easy phase and frequency modulation++

**Drawbacks**
- High level spurious tones
ROM based DDS (1)
ROM based DDS (2)

- **Advantages**
  - High resolution++
  - Good phase noise+
  - Switching time++
  - Easy phase and frequency modulation++

- **Drawbacks**
  - Low Frequency due to ROM based LUT access time. Fout limited to Fclk/10 for better filtering
  - Power increases with DDS bandwidth
  - DAC degrades performances at high frequencies
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Once Loop Locked $\Phi_{\text{div}}$ tracks $\Phi_{\text{ref}}$ variations

$$\Phi_{\text{err}} = \Phi_{\text{ref}} - \frac{\Phi_{\text{VCO}}}{N} = \text{Cste}$$

$$f_{\text{VCO}} = Nf_{\text{ref}}$$
Integer-N frequency synthesizer (2)

- Frequency range: N should be programmable with a sufficient range.
- Step = Fref -> should be equal to channel width
- Accuracy = will copy the reference accuracy (usually a pure crystal based oscillator)
- Settling time will constrain loop bandwidth (need small signal analysis)
- Phase noise will constrain the PLL block contributions (need of a loop noise analysis)
Integer–N : small signal analysis

\[ BO(p) = \frac{I_{pc} \cdot F(p) \cdot K_{vco}}{N \cdot p} \]

\[ H(p) = N \cdot \frac{BO(p)}{1 + BO(p)} \]
Open Loop Bode Diagramm

- PLL order = loop filter order +1 due to VCO pole
- To ensure robustness over process variations:
  \[ f_{0\text{dB}} = \sqrt{f_1 \cdot f_2} \]
- Phase margin depends on \( f_2/f_1 \) ratio (should be greater than 10 for PM > 45°)
- Relation between \( f_2, f'_2 \) and \( f_{0\text{dB}} \)

\[ 40 \log \frac{f'_2}{f_0} = 20 \log \frac{f_0}{f_2} \]
Example 3\textsuperscript{rd} order Type II PLL (1)

- Loop filter structure:

\[
F(p) \approx \frac{1}{C_2 p} \cdot \frac{1 + R_2 C_2 p}{1 + R_2 C_1 p} = \frac{1}{C_2 p} \cdot \frac{1 + 2\pi f_2 p}{1 + 2\pi f_1 p}
\]

\[
f_{0dB} = \sqrt{f_1 \cdot f_2} \quad \& \quad f_1 = 10 \cdot f_2 \quad \Rightarrow \quad f_{0dB} = \frac{f_2}{\sqrt{10}}
\]

\[
f'_2 = 10^{\frac{-1}{4}} \cdot f_0
\]

- At low frequencies open loop:

\[
BO(p) \approx \frac{I_{pc} \cdot K_{vco}}{C_2 \cdot N \cdot p^2}
\]

\[
1 = \frac{I_{pc} \cdot K_{vco}}{C_2 \cdot N \cdot (2\pi f'_2)^2}
\]
Example 3\textsuperscript{rd} Type II PLL (2): summary

- Calculation of needed filter:
  - Fixed parameters: VCO gain, Loop divider ratio
  - 1\textsuperscript{st} step: determination of needed loop bandwidth ($\sim f_{0\text{dB}}$)
  - 2\textsuperscript{nd} step: from $f_{0\text{dB}}$ calculation of $f_1$, $f_2$ and $f'_2$
  - 3\textsuperscript{rd} step: fixing charge pump current value (PFD gain), calculation of $C_2$
  - 4\textsuperscript{th} step: from expression of $f_2$ calculation of $R_2$

- Of course, fixing resistor value in step 3 and determining charge pump current in step 4 is another option

- Loop bandwidth, resistor and charge pump current values are to be compliant with overall frequency synthesizer specification in term of settling time, phase noise, power consumption etc.
 Integer-N small signal analysis

- PLL: time-sampled system -> should be modeled using z-transform! Non trivial modelization.
- Sampling process arises in feedback loop divider. Linear modelisation possible for \( f < \frac{f_{\text{outDiv}}}{10} \)
- PLL is non linear. Transfer function could be used to predict the settling time from one locking state to another one only if the PFD doesn’t enter frequency discrimination process
- Small signal analysis could be implemented on math software or in electrical simulators using verilog-A models
Noise analysis: using small signal model
- All contribution are additive noises
- Calculation mode:
  - Noise of each blocks simulated at transistor level
  - Determination of the contribution of each noise source to the overall output noise
Reference and Divider output noise contribution

\[ \varphi_{out_{Nref}}^2 = N^2 \left( \frac{BO(p)}{1 + BO(p)} \right)^2 \cdot \varphi_{Nref}^2 \]

\[ \varphi_{out_{Div}}^2 = N^2 \left( \frac{BO(p)}{1 + BO(p)} \right)^2 \cdot \varphi_{NDiv}^2 \]

- Reference and Divider noise are low pass filtered
Integer-N phase Noise Analysis (3)

- Charge Pump output noise contribution

\[
\varphi_{\text{outNCP}}^2 = \left(\frac{N \cdot 2\pi}{I_{cp}}\right)^2 \left(\frac{BO(p)}{1 + BO(p)}\right)^2 \cdot \varphi_{NCP}^2
\]

- Low pass filtering

- Filter resistors output noise contribution

\[
\varphi_{\text{outFilter}}^2 = \left(\frac{N \cdot 2\pi}{I_{cp} F(p)}\right)^2 \left(\frac{BO(p)}{1 + BO(p)}\right)^2 \cdot \varphi_{\text{Filter}}^2
\]

- Bandpass filtering

- VCO output noise contribution

\[
\varphi_{\text{outNVCO}}^2 = \left(\frac{1}{1 + BO(p)}\right)^2 \cdot \varphi_{\text{NVCO}}^2
\]

- High pass filtering
Total PLL output noise:

\[ \varphi_{\text{Total}}^2 = \varphi_{\text{outNVCO}}^2 + \varphi_{\text{outNfilter}}^2 + \varphi_{\text{outNicp}}^2 + \varphi_{\text{outDiv}}^2 + \varphi_{\text{outNref}}^2 \]

Total PLL output phase noise could be easily calculated using a math software or using an electrical simulator with parametrised Verilog-A models.

Phase noise analysis and small signal analysis have to take into account PVT, non linearity of VCO gain.
Integer-N PLL: Output Phase Noise

Reference noise

VCO noise

$f_{\text{loop}}$

$f_{\text{loop}}$
VerilogA Small Signal Analysis (1)
VerilogA Small Signal Analysis (2)
- Usually VCO are LC CMOS oscillators.
  - Silicon inductor Q is about 20
  - Tuning using MOS varactor or Diode Varactor Q ~ 50
  - PVT covered thanks to a bank of capacitor
  - For better noise immunity an automatic amplitude control is used
Block Design: VCO phase Noise Profile

Phase Noise dBc/Hz

-30 dB/decade due to 1/f noise of VCO components

-20 dB/decade due to thermal noise of VCO components

Graph with axes:
- Vertical axis: Phase Noise dBc/Hz
- Horizontal axis: fm, fc, f0/Q

Diagram shows the phase noise profile with two distinct noise components.
Phase Frequency Detector (1)

VDD

\[ F_{\text{ref}} \]

\[ F_{\text{div}} \]

\[ \text{Up} \]

\[ \text{Dw} \]

\[ \text{I}_{\text{cp}} \]

\[ \text{I}_{\text{out}} \]

\[ \phi_{\text{ref}} \]

\[ \phi_{\text{div}} \]

Dead Zone

\[ -2\pi \]

\[ 2\pi \]

\[ \langle \text{I}_{\text{out}} \rangle \]
Phase Frequency Detector (2)
Charge Pump Design (1)

- Charge pump:
  - Permits a control of the PFD/loop filter gain
  - Enhances power supply noise rejection
- Needs good matching of current sources
Mismatch in charge pump Up and Down Current and filter current leakage are responsible for reference spurious tone in PLL output.

\[ A_{sp}(f_{lo} \pm nf_{ref}) = A_{LO} \frac{I_m |Z_f(j2\pi nf_{ref})|K_{VCO}}{nf_{ref}} \]

\[ I_m = I_{cp} \frac{\Delta \Phi}{2\pi} \]
Loop Divider (1)

\[ M = A \cdot (P + 1) + (B - A) \cdot P = B \cdot P + A \]

\[ f_{\text{DIV}} = \frac{f_{\text{IN}}}{B \cdot P + A} \]

- Main Drawback: has only \((P+1)Tvco\) to change from \(P+1\) to \(P\) modulus. Could be problematic for low \(P\) values
Loop Divider (2)

![Diagram of loop divider circuit](image)

- **T=0, X=1**
  - CLK
  - Q1
  - Q2'

- **T=1, X=1**
  - CLK
  - Q1
  - Q2'

- **Inputs:**
  - X_0
  - X_1
  - X_{P-1}

- **Outputs:**
  - f_{VCO}
  - f_{DIV}

- **Gates:**
  - D
  - Q
  - Q'

- **States:**
  - R
  - X
  - T
  - A_0
  - A_1
  - A_{P-1}
  - CLK
  - Q1
Integer-N PLL: transient simulation

- Small signal analysis: stability, filter and charge pump current determination
- Noise analysis: verification of loop bandwidth choice and gives some specifications to designers
- Transient analysis: to verify feedback connection.
- At transistor level: VCO in the GHz range (need a few ps precision), loop bandwidth very small, settling time in the us range...simulation time prohibitive!
  - Solution: mixed solution with realistic verilog-A model of at least VCO and loop feedback divider
  - Merging VCO and loop feedback divider in one model fastens simulations
  - Noise behaviour in transient: need some simulation using Math simulators or C models.
Advantages

- Easy to setup for GHz frequency synthesis
- Only one spurious @ reference frequency

Drawbacks

- Low speed System
  - Frequency Step= Fref
  - Fref Max = channel width
  - Loop bandwidth < Channelwidth /10
- Spurious in adjacent channel!! Big constraints on CP mismatch, loop filter leakage current
- Power consumption(VCO+ dividers)
- Low bandwidth modulation
- Loop transfer function depends on process variations (especially if the loop filter is integrated)
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Fractional-N synthesizer Principle (1)
Fractional-N synthesizer Principle (2)

- Dual modulus N/N+1 divider
  - When Deb = 0 division by N
  - When Deb = 0 division by N+1
- In $2^n$ reference clocks (period of phase accumulator) the divider divide $P$ time by N+1 and $2^n-P$ time by N

$$N_{avg} = \frac{p \cdot (N + 1) - (2^n - P) \cdot N}{2^n} = N + \frac{p}{2^n}$$

- Thus Frac-N PLL output frequency is given by:

$$f_{VCO} = \left(N + \frac{p}{2^n}\right) f_{ref}$$

- Drawbacks: overflow signal of phase accumulator presents spurious tones. Those that lies into PLL bandwidth are not filtered and are present in PLL output
Fractional-N principle (2)

- Advantages:
  - divider ratio fractional permits to use a reference frequency greater than the channel spacing
  - Larger bandwidth could be reached (floop ~4MHz for a 38.4 MHz quartz reference) highly desirable for modulation purpose.

- Drawback:
  - Phase accumulator spurious tones are not filtered out in the loop bandwidth -> high suprious level in the VCO output
- Phase accumulator output is used to inject current in loop filter to compensate spurious.
- Solution very sensitive to accuracy, DAC speed. Extra noise added onto the loop filter.
\( \Sigma \Delta \) Fractional-N synthesizer (1)

- \( \Sigma \Delta \) modulator is used to deliver a fractional word proportional to the frequency fraction to be synthesized
- Same function as Frac-N but using the noise shaping property of \( \Sigma \Delta \) modulator to reject quantization noise out of PLL loop bandwidth
**ΣΔ modulator (1)**

- **ΣΔ converter:**
  - Sampled feedback loop
  - Composed of an integrator and a quantisizer.
  - At each clock occurrence, difference between output and input is integrated and quantified. The loop tends to minimize this error

- **ΣΔ modulator**
  - Digital implementation
  - N order ΣΔ modulator: N ΣΔ modulator in series or in parallel (MASH)
Example of 3\textsuperscript{rd} order $\Sigma\Delta$

- Series structure
  - Stability issue

- Parallel structure: MASH
  - No stability issue
\[ Y(z) = z^{-1} \cdot X(z) + \left(1 - z^{-1}\right) \cdot Q(z) \]

For a Nth order MASH, transfer function is:

\[ Y(z) = z^{-n} \cdot X(z) + \left(1 - z^{-1}\right)^n \cdot Q_n(z) \]

• Only the quantification of the last converter is of interest
\( H_n(z) = (1 - z^{-1})^n \)

\[ |H_n(f)| = 2 \cdot \sin \left( \frac{\pi \cdot f}{f_{CLK}} \right) \]

- As order \( N \) increases the noise is more and more rejected near \( f_{CLK}/2 \)
ΣΔ modulator noise shaping (3)
**ΣΔ modulated divider model (3)**

- Output Frequency divider expression:

\[
f_{\text{out}} = \frac{f_{\text{VCO}}}{N_{\text{avg}} + q(t)} \approx \frac{f_{\text{VCO}}}{N_{\text{avg}}} \left(1 - \frac{q(t)}{N_{\text{avg}}}\right)
\]

- Z domain transform:

\[
f_{\text{out}} = \frac{f_{\text{VCO}}}{N_{\text{avg}}} - \frac{f_{\text{VCO}}}{N_{\text{avg}}^2} \cdot \frac{q}{\sqrt{12} f_{\text{ref}}} (1 - z^{-1})^3 \approx \frac{f_{\text{VCO}}}{N_{\text{avg}}} - \frac{f_{\text{REF}}}{N_{\text{avg}}} \frac{q}{\sqrt{12} f_{\text{ref}}} (1 - z^{-1})^3
\]

- Integration to get the phase domain expression

\[
\Phi_{\text{out}} = \frac{\Phi_{\text{VCO}}}{N_{\text{avg}}} - \frac{f_{\text{ref}}}{N_{\text{avg}}} \frac{q}{\sqrt{12} f_{\text{ref}}} (1 - z^{-1})^3 \cdot \frac{2\pi T_{\text{ref}}}{(1 - z^{-1})^2} = \frac{\Phi_{\text{VCO}}}{N_{\text{avg}}} - \frac{2\pi}{N_{\text{avg}}} \frac{q}{\sqrt{12} f_{\text{ref}}} (1 - z^{-1})^2
\]
Noise Model of $\Sigma\Delta$ Frac-N PLL

Shaped Quantification noise

$$Q_{\Sigma\Delta}(F) = \left(1 - e^{-\frac{j\pi f_i}{f_{	ext{ref}}}}\right)^2 \ast \frac{1}{\sqrt{12 \cdot f_{	ext{ref}}}}$$
Example of $\Sigma \Delta$ Frac-N PLL noise plot
**ΣΔ Frac-N PLL: conclusion**

**Advantages**
- Frequency step as small as possible
- High reference frequency:
  - Spurious tone far from carrier and thus better filtered
- Frequency and phase modulation possible

**Drawbacks**
- ΣΔ noise shaping doesn’t permit to reach $f_{ref}/10$ loop bandwidth
### Classical Frequency Synthesizer: Conclusion

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<th>1-bit DDS</th>
<th>DDS</th>
<th>Integer-N</th>
<th>Frac- N</th>
<th>ΣΔ</th>
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<td>Bandwidth</td>
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<td>Spurious</td>
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<td>Accuracy</td>
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*Note: Smiley faces indicate better performance, while sad faces indicate worse performance.*
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A 100MHz DDS With Synchronous Oscillator-Based Phase Interpolator

Franck Badets, Didier Belot
STMicroelectronics,
Central R&D Crolles
- Synchronous Oscillator Based Phase Interpolator
- Synchronous Oscillator Locked Loop (SOLL)
- SOLL based phase interpolator
- 100 MHz 16 bits DDS with SOLL based phase interpolator
Injection Locked Oscillator (ILO)

- Oscillator able to lock on an incoming signal whose frequency (or an harmonic) lies into the oscillator synchronization range.
ILO Properties

- Synchronization range depends only on synchronizing signal amplitude and oscillator topology
- Fast frequency acquisition
- Output SO phase noise is a copy of the synchronizing signal phase noise
- Once synchronized there is a phase relationship between the SO output signal and its synchronizing signal.
ILO properties con’t

Phase Out / In

$F_{\text{ref}} - \alpha A$

$A_l$ $A_{-90}$ $A_h$
ILO based Phase Interpolator (SOPI)

- Oscillator with linearly tunable free running frequency (Synchronous VCO or ICO (ACO))
- Fixed synchronization frequency

![Diagram of SOPI](image)
Digital Accurate SOPI (API)

Phase = \(-90 + 45 \frac{w}{2^n}\)

(A_{-45} - A_{-90}) \frac{w}{2^n}

Input word

DAC

\(f_{\text{ref}}\)

ACSO

SOo

\(f_{\text{ref}}\)

\(A_{-90}\)
w : DAC input word

Si

SOo

w = 2^n

w = 0
Digital Accurate SOPI (API)

- Good linearity in the –90, -45 degrees range
- Fast phase acquisition
- Needs the analog commands $A_{-90}$ and $A_{-45}$ for calibration
ILO Locked Loop SOLL (1)

Phase Comparator

Low pass Filter

$A_{(360/N)}$
SOLL (2) : Chronogram

Diagram showing the relationship between Fref, O1, O2, and On.
SOLL (2)

- DLL with SOs as delay elements
- Once Locked all SOs are fed with the analog command that ensures a 360/N phase for each SO.
  - SOLL_90 : 4 SOs. Gives A_-90 command
  - SOLL_45 : 8 SOs. Gives A_-45 command
SOLL based Phase Interpolator (1)
SOLL Based Phase Interpolator (2)

- SOLL_45 provides 8 outputs with a 45 phase step (multiphase clock): coarse phase interpolation
- 8 DAPI are coupled with the 8 SOLL_45 outputs to provide complementary accurate phase interpolation
- SOLL_45 and the 8 DAPI provide phase interpolation from 0 to 360 degrees with a N+3 bits accuracy
ILO implementation

\[ V_{dd} \]

\[ I_{sync} \quad I_0 \quad I_{sync} \quad I_{sync} \quad I_0 \quad I_{sync} \quad I_{sync} \]

\[ SO_0 \]

\[ fti \]
DAC implementation

I_{out}

I_{-45} - I_{-90}

b7  b6  b5  b4  b3  b2  b1  b0

W  W/2  W/4  W/8  W/256
Behavioral Modeling : DDS alone

$P = 16056$
$M = 5355$
$f = 24.498 \text{ MHz}$
Behavioral Modeling: Coarse PI alone

-37 dBc

-45 dBc
Measurement Results: Coarse Interpolation

-38 dBc
-42 dBc
Behavioral Modeling:
Coarse and Accurate PI enabled
Measurement results:
Accurate interpolation

-40 dBc
-60 dBc
The First SO of SOLL_45 synchronized by the external clock is responsible of a large amount of the accumulative phase error in SOLL_45.
Conclusions (1)

- Synchronous oscillator as Phase interpolator
- DLL with SO as delay element (SOLL)
- Application to decreases spurious tones in DDS
- Prototype: validation of principle
A Multimode GSM/DCS/WCDMA Double Loop Frequency Synthesizer

Franck Badets, Sebastien Rieubon, Laurent Camino, Thierry Divel, Sebastien Dedieu, Patrick Cerisier and Didier Belot

STMicroelectronics
TX synthesizer Specifications

3.6 GHz  TX DCS  3.76 GHz  3.84 GHz TX GSM, PCS  4 GHz

3.66 GHz  TX WCDMA  3.77 GHz

3.6 GHz  GSM, DCS, PCS RX range  4 GHz

<table>
<thead>
<tr>
<th>Mode</th>
<th>(F_{\text{step}})</th>
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<tr>
<td>TX WCDMA</td>
<td>32/34*(400 kHz) or 48/50*(400 kHz)</td>
</tr>
<tr>
<td>TX GSM</td>
<td>24/22*(400 kHz)</td>
</tr>
<tr>
<td>TX DCS</td>
<td>40/38*(400 kHz)</td>
</tr>
<tr>
<td>TX PCS</td>
<td>48/46*(400 kHz)</td>
</tr>
<tr>
<td>RX GSM/DCS/PCS</td>
<td>400 kHz</td>
</tr>
</tbody>
</table>
TX synthesizer architecture choice (1)

Fractionnal Synthesizer VS Rationnal Synthesizer

Fractionnal Synthesizer

- VCO1
- \( \frac{F_{\text{ref}}}{5} \)
- \( F_c \sim 2.5 \text{MHz} \)
- \( \sum \Delta \)
- \( F_{\text{RF}} \sim 4 \text{GHz} \)

Rationnal Synthesizer

- Step PLL (large bandwidth)
- Fref 38.4MHz
- Fref 192MHz
- \( F_c \sim 18 \text{kHz} \)
- \( F_{\text{RF}} \sim 9490 \)
- \( F_{\text{step}} \sim 400 \text{kHz} \)

Mathematical Expressions:

\[
F_{\text{out}} = \left( N + \frac{p}{2^n} \right) F_{\text{ref}}
\]

\[
F_{\text{step}} = \frac{F_{\text{ref}}}{2^n}
\]

\[
F_{\text{out}} = \left( \frac{5N}{S} \right) F_{\text{ref}}
\]

\[
F_{\text{step}} = \left( \frac{5}{S} \right) F_{\text{ref}} = \frac{480}{S} * 400 \text{kHz}
\]
## TX synthesizer architecture choice (2)

<table>
<thead>
<tr>
<th></th>
<th>Advantages</th>
<th>Drawbacks</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fractionnal Synthesizer</strong></td>
<td><em>- Seetling time requirement easily obtainable</em></td>
<td><em>- Spurious (noise coupling)</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td><em>- Complexity (SD modulation needed)</em></td>
</tr>
<tr>
<td><strong>Rationnal synthesizer</strong></td>
<td><em>- No fractionnal spurious</em></td>
<td><em>- Narrow bandwidth</em></td>
</tr>
</tbody>
</table>

Rationnal Synthesizer good solution if:

- Step PLL fully integrable (with its loop filter)
- No significant added power consumption
- Silicon area comparable with ΣΔ modulator
PLL Step Implementation (1) : Noise

Phase noise floors:
- VCO : -142 dBc/Hz
- CP : -230 dBA
- S Divider : -169 dBc/Hz
- Loop Divider : -169 dBC/Hz
- Reference : -150 dBC/Hz
## PLL Step Implementation (2): Simulation Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP current</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>µA</td>
</tr>
<tr>
<td>VCO gain</td>
<td>77</td>
<td>180</td>
<td>290</td>
<td>MHz/V</td>
</tr>
<tr>
<td>R2</td>
<td>3360</td>
<td>4200</td>
<td>5040</td>
<td>Ω</td>
</tr>
<tr>
<td>C2</td>
<td>37</td>
<td>46.8</td>
<td>56</td>
<td>pF</td>
</tr>
<tr>
<td>C1</td>
<td>4.2</td>
<td>5.2</td>
<td>6.2</td>
<td>pF</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>32</td>
<td>55</td>
<td></td>
<td>degree</td>
</tr>
<tr>
<td>PN @1 kHz</td>
<td>-155</td>
<td>-155</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>PN @100 kHz</td>
<td>-167</td>
<td>-165</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>PN @1 MHz</td>
<td>-166</td>
<td>-160</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>PN @10 MHz</td>
<td>-169</td>
<td>-169</td>
<td></td>
<td>dBc/Hz</td>
</tr>
</tbody>
</table>
## PLL step Implementation (3) : VCO

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>alim</td>
<td>2.5</td>
<td>2.6</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>Temperature</td>
<td>-30</td>
<td>27</td>
<td>100</td>
<td>°C</td>
</tr>
<tr>
<td>( f_0 ) (vcont = 1.3 V)</td>
<td>118</td>
<td>190</td>
<td>324</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{min}} ) (vcont = 2.2V)</td>
<td>46</td>
<td>74</td>
<td>136</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{max}} ) (vcont = 0.6 V)</td>
<td>224</td>
<td>310</td>
<td>476</td>
<td>MHz</td>
</tr>
<tr>
<td>VCO gain @192 MHz</td>
<td>77</td>
<td>180</td>
<td>290</td>
<td>MHz/V</td>
</tr>
<tr>
<td>PN @ 1 kHz</td>
<td>-28</td>
<td>-25</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>PN @ 10 kHz</td>
<td>-58</td>
<td>-55</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>PN @ 100 kHz</td>
<td>-88</td>
<td>-85</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>PN @ 1 MHz</td>
<td>-117</td>
<td>-115</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>PN @ 10 MHz</td>
<td>-142</td>
<td>-141</td>
<td></td>
<td>dBC/Hz</td>
</tr>
</tbody>
</table>

Full CMOS Seven Stages Ring Oscillator

![Ring Oscillator Diagram]
PLL step Implementation (4) : layout

PLL step layout

ΣΔ layout
(4th order MASH)

Dx = 380 µm
Dy = 180 µm

Dx = 320 µm
Dy = 260 µm
RF VCO Implementation (1)

- Amplitude control loop
- 5 bits bank capacitors
- 0.55nH inductor
- 3.6 - 4 GHz band (3.2 - 4.4 GHz for PVT purpose)
- -117 dBc/Hz @ 400 kHz
## RF VCO Implementation (2)

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Process</th>
<th>Consumption (mA)</th>
<th>Magnitude (V)</th>
<th>PN @ 400kHz (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-30</td>
<td>S</td>
<td>6.7</td>
<td>1.47</td>
<td>-117</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td>6.5</td>
<td>1.47</td>
<td>-120</td>
</tr>
<tr>
<td></td>
<td>F</td>
<td>6.8</td>
<td>1.47</td>
<td>-118</td>
</tr>
<tr>
<td>27</td>
<td>S</td>
<td>8</td>
<td>1.5</td>
<td>-119.5</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td>7.6</td>
<td>1.5</td>
<td>-120</td>
</tr>
<tr>
<td></td>
<td>F</td>
<td>7.8</td>
<td>1.5</td>
<td>-119.5</td>
</tr>
<tr>
<td>100</td>
<td>S</td>
<td>9.8</td>
<td>1.48</td>
<td>-119</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td>9.3</td>
<td>1.53</td>
<td>-119</td>
</tr>
<tr>
<td></td>
<td>F</td>
<td>9.3</td>
<td>1.53</td>
<td>-118.5</td>
</tr>
</tbody>
</table>

- Frequency band: 3.04 – 4.8 GHz;
- Post extract simulation: 2.8 – 4.15 Ghz
TX Synthesizer Implementation

- RF 0.25um ST BiCMOS technology
- Three LDOS (RF VCO, Crystal oscillator and PLLs)
- 700 µm x 1300 µm

RF buffer - RF 0.25um ST BiCMOS technology - Three LDOS (RF VCO, Crystal oscillator and PLLs) - 700 µm x 1300 µm
Measurement results (1) RF VCO phase noise
Measurement results (2): TX phase noise
## Main Measurement Results (3)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Measured value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tuning range</td>
<td>3.6 – 4 Ghz</td>
<td>3.6 – 4. GHz</td>
</tr>
<tr>
<td>PN in band</td>
<td>-80 dBC/Hz</td>
<td>-76 dBC</td>
</tr>
<tr>
<td>Pn @ 400 kHz</td>
<td>-117 dBC/Hz</td>
<td>-118 dBC / Hz</td>
</tr>
<tr>
<td>PN @ 600 kHz</td>
<td>-122 dBC/Hz</td>
<td>-123 dBC /Hz</td>
</tr>
<tr>
<td>PN @ 3 MHz</td>
<td>-136 dBC/Hz</td>
<td>-137 dBC /Hz</td>
</tr>
<tr>
<td>Integrated noise</td>
<td>-32 dBC</td>
<td>-30 dBC</td>
</tr>
<tr>
<td>(400 Hz -1.92 MHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power consumption (under 2.7 V)</td>
<td></td>
<td>~ 21 mA</td>
</tr>
</tbody>
</table>
Outline

- Introduction
  - Frequency Synthesis - Where and Why?
  - Specifications
- Frequency Synthesizer Architectures
  - Direct Digital Synthesizer
  - Integer N PLL
  - Fractional PLL
- Implementation examples
  - Phase Interpolator based DDS
  - Multimode GSM/DCS/PCS frequency Synthesizer
  - 40 GHz PLL for 60 GHz UWB transceiver
A 17.5-to-20.94GHz and 35-to-41.88GHz PLL in 65nm CMOS for Wireless HD Applications

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¹STMicroelectronics, Crolles France
²CEA-LETI-MINATEC, Grenoble France
³STMicroelectronics, Grenoble France
Introduction

- The frequency synthesizer must be compliant with IEEE 802.15.3c standard for 60GHz Wireless HD
- Double conversion architecture with zero IF final stage
- The frequency synthesizer delivers 20GHz and 40GHz signals
- 65nm CMOS technology

<table>
<thead>
<tr>
<th>Standard Channel</th>
<th>LO1 Freq. (GHz)</th>
<th>LO2 Freq. (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>19.44</td>
<td>38.88</td>
</tr>
<tr>
<td>A2</td>
<td>20.16</td>
<td>40.32</td>
</tr>
<tr>
<td>A3</td>
<td>20.88</td>
<td>41.76</td>
</tr>
<tr>
<td>A4</td>
<td>21.6</td>
<td>43.2</td>
</tr>
</tbody>
</table>

This work: Frequency Synthesizer 20GHz / 40GHz
PLL architecture

\[
f_{\text{LOCK}} = \frac{f_{\text{REF}}}{2} \cdot D_{\text{DIV}} \cdot D_{\text{PROG}}
\]

<table>
<thead>
<tr>
<th>( f_{\text{REF}} )</th>
<th>( D_{\text{DIV}} )</th>
<th>( D_{\text{PROG}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>36MHz</td>
<td>40</td>
<td>16 to 31</td>
</tr>
</tbody>
</table>
Circuit design: quadrature VCO

I VCO

Q VCO

Varactor tank:

B0
B1
B3
Circuit design: Dividers’ schematics

- Grounded Source Frequency Divider
  - Divider by 2 @20GHz
  - 2 D-Latches in master-slave
  - DC supply 1.2V
  - N and P MOS low power RF

- Current Mode Logic Divider
  - Divider by 2 @10GHz and @5GHz
  - 2 D-Latches in master-slave
  - DC supply 1.2V
  - N & P MOS low power RF

- Modular Programmable Prescaler
  - Programmable divider using 2/3 cell based modular architecture
  - Division range: 16-to-31 with 4 cells
  - 2/3 cell is composed to 3 NAND and 2 D-Latches
Circuit design: other blocks of the PLL

- **Phase-Frequency Detector design**
  - Sequential Phase detector
  - DC supply 1.8V
  - N and P MOS Thick gate oxide
  - Core Library

- **Charge Pump**
  - External current biasing
  - DC supply 1.8V
  - N and P MOS Thick gate oxide

- **Loop filter**
  - 3rd order Loop Filter
  - External components : C2, R2 and R3
  - Integrated components : C1 and C3
  - Chosen to allow a better rejection of spurious out of the range ($\omega > \omega_c$)
Circuit design: Die Photograph

Core area = 1.1 x 1mm²
Experimental Results

PLL measurement setup

- PLL on Roger 4003 PCB
- Low frequency signals wire bonded
- 20GHz and 40GHz signals measured on chip with differential probes
Experimental results

Locking frequencies of the synthesizer

VCO bit-word: “1111”

VCO bit-word: “0000”

f_{REF}=36MHz
Experimental results

Measured Phase Noise at the 3rd channel (20.88GHz)
# Experimental results

## Phase Noise Measurement Table

<table>
<thead>
<tr>
<th>Channels Frequency (GHz)</th>
<th>19.44</th>
<th>20.16</th>
<th>20.88</th>
<th>21.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>PN @100kHz (dBc/Hz)</td>
<td>-66.4</td>
<td>-66.1</td>
<td>-71.2</td>
<td>n.a</td>
</tr>
<tr>
<td>PN @1MHz (dBc/Hz)</td>
<td>-100.2</td>
<td>-100.4</td>
<td>-100.6</td>
<td>n.a</td>
</tr>
<tr>
<td>PN @10MHz (dBc/Hz)</td>
<td>-125.5</td>
<td>-125.6</td>
<td>-126.7</td>
<td>n.a</td>
</tr>
<tr>
<td>PN @40MHz (dBc/Hz)</td>
<td>-133.3</td>
<td>-132</td>
<td>-135.2</td>
<td>n.a</td>
</tr>
</tbody>
</table>
## Comparison of CMOS PLL

<table>
<thead>
<tr>
<th>Tech. [nm]</th>
<th>This work</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply [V]</td>
<td>65 CMOS</td>
<td>90 CMOS</td>
<td>45 CMOS</td>
<td>90 CMOS</td>
<td>65 CMOS</td>
</tr>
<tr>
<td>1.2**</td>
<td>1.2</td>
<td>1.1</td>
<td>1.2</td>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>Frequency range [GHz]</td>
<td>17.5 to 20.94 (17.9%)</td>
<td>39.1 to 41.6 (6.2%)</td>
<td>57 to 66 (14.6%)</td>
<td>58 to 60.4 (4%)</td>
<td>96</td>
</tr>
<tr>
<td>Phase noise [dBc/Hz]</td>
<td>-100 (20.88GHz)</td>
<td>-90</td>
<td>-75</td>
<td>-85</td>
<td>-75.2</td>
</tr>
<tr>
<td>Calculated @ 20GHz Phase noise [dBc/Hz]</td>
<td>-100</td>
<td>-96</td>
<td>-84.6</td>
<td>-94.6</td>
<td>-88.9</td>
</tr>
<tr>
<td>$F_{ref}$ [MHz]</td>
<td>36</td>
<td>50</td>
<td>100</td>
<td>234.1</td>
<td>375</td>
</tr>
<tr>
<td>Loop Type</td>
<td>Integer</td>
<td>Fractional</td>
<td>Integer</td>
<td>Integer</td>
<td>Integer</td>
</tr>
<tr>
<td>Division Ratio(s)</td>
<td>640 to 1240</td>
<td>512 to 2032</td>
<td>512 to 8184</td>
<td>256 to 258</td>
<td>256</td>
</tr>
<tr>
<td>Ref. Spur [dBc]</td>
<td>&lt;-50</td>
<td>-54</td>
<td>-42</td>
<td>-50.4</td>
<td>-51.7</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>80</td>
<td>64*</td>
<td>78</td>
<td>80</td>
<td>43.7*</td>
</tr>
</tbody>
</table>

*Without Output Buffer

**The supply voltage of PFD and CP is 1.8V

Conclusion

- PLL in 65nm CMOS LP technology compliant with IEEE 802.15.3c standard for 60GHz Wireless HD

- 20GHz and 40GHz bands for double conversion transceivers

- 17.9% tuning range

- -100dBc/Hz phase noise at 1MHz of the carrier