RF Transmitter based on Frequency Synthesizer

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Outline

- Introduction
  - Transmitter integration challenges
- Frequency Synthesizer Modulation
  - Translationnal TX loop
  - Modulation of sigma delta frequency synthesizer
  - Two point modulation
- DDS and ILO based RF transmitter
  - Injection Locked Oscillator
  - 400 MHz DDS
  - Bluetooth DDS/ILO based transmitter

I Q based RF transmitter

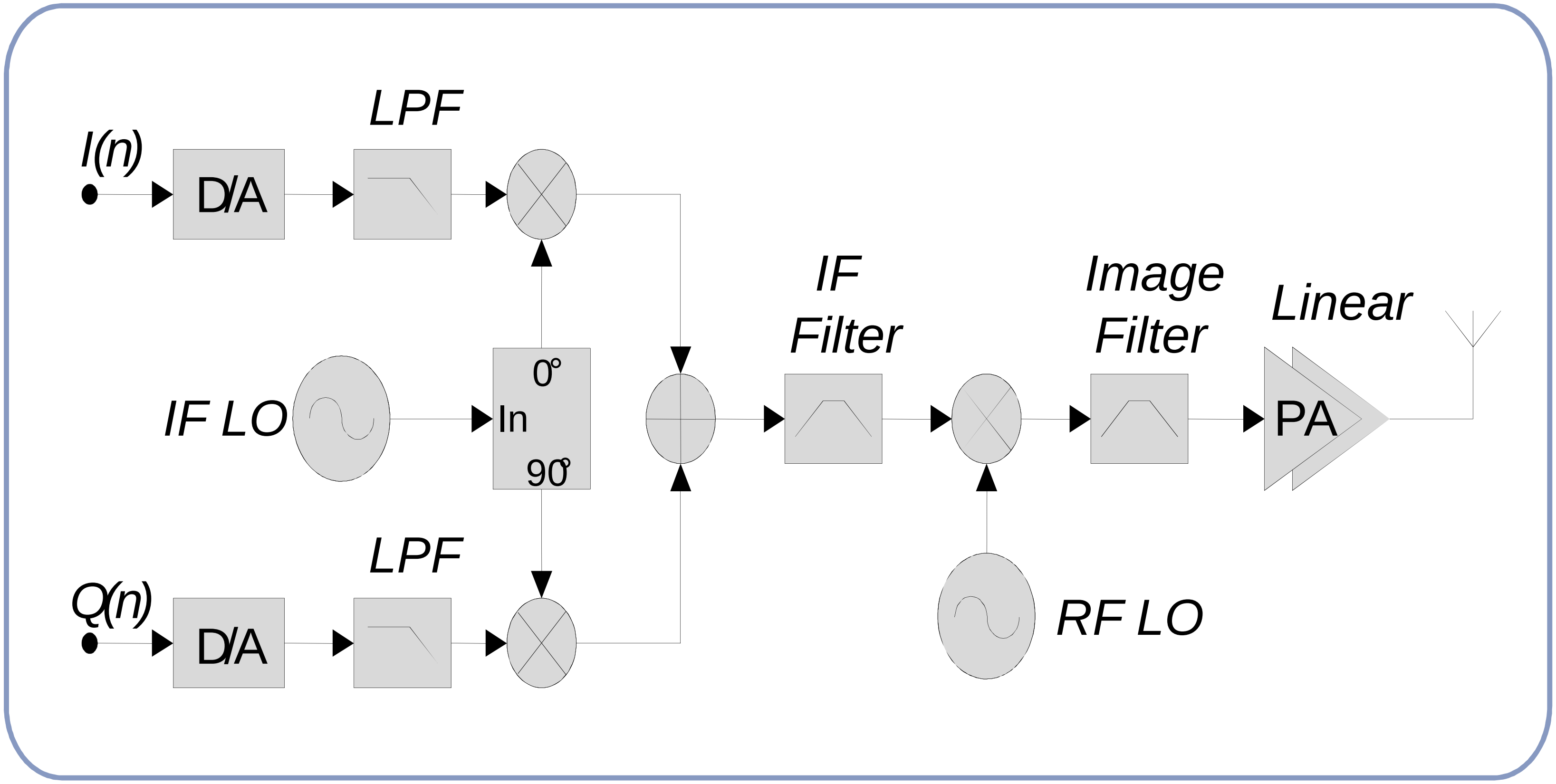
- General expression of signal to be transmitted

$$\text{RF(t)} = A(t)\cos\big(\omega t + \varphi(t)\big) = A(t)cos\big(\varphi(t)\big)\cos(\omega t) - A(t)\sin\big(\varphi(t)\big)\sin(\omega t)$$

$$\text{RF(t)} = I(t)\cos(\omega t) - Q(t)\sin(\omega t)$$

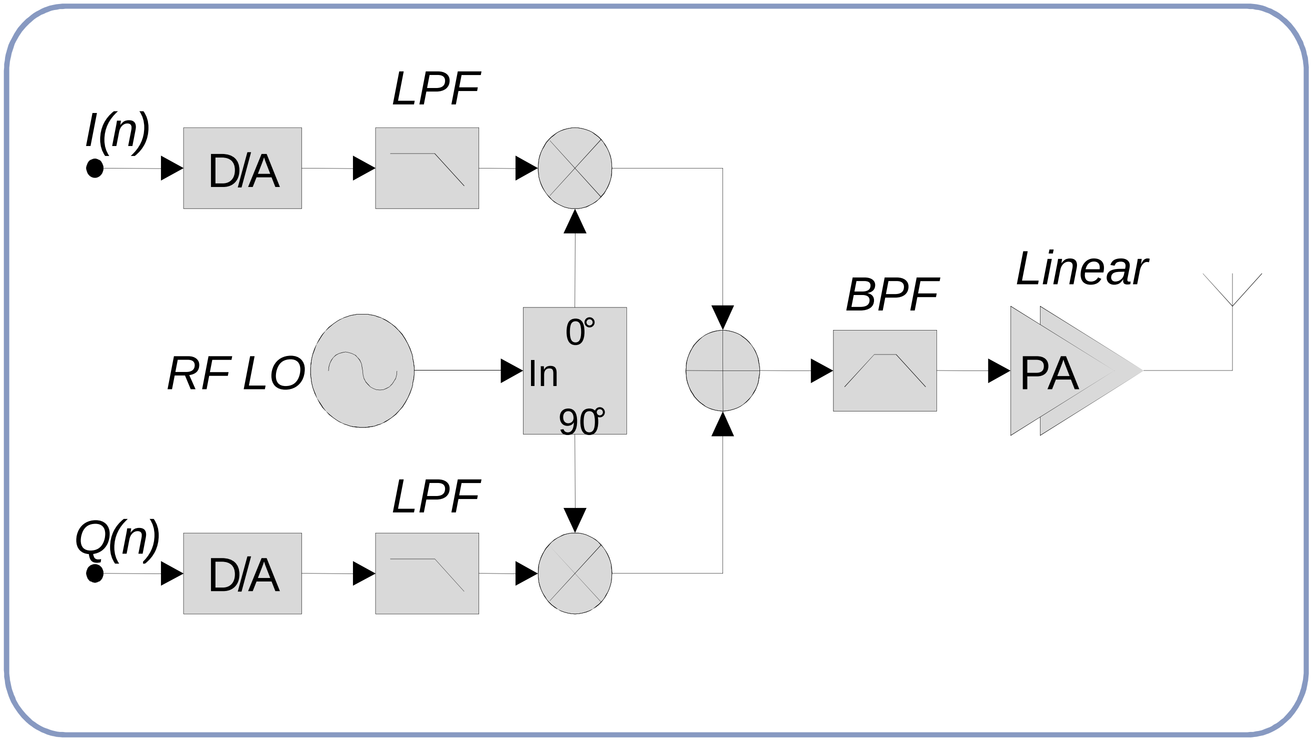
- Principle :
  - Generation of I and Q in baseband
  - Generation of RF signal using in phase and quadrature Local Oscillator

Heterodyne Transmitter Architecture



Drawbacks : - needs one external high Q RF filter
- Precision needed on IF image rejection mixer
- 2 LOs : 2 PLLs
- Linear PA : Power hungry

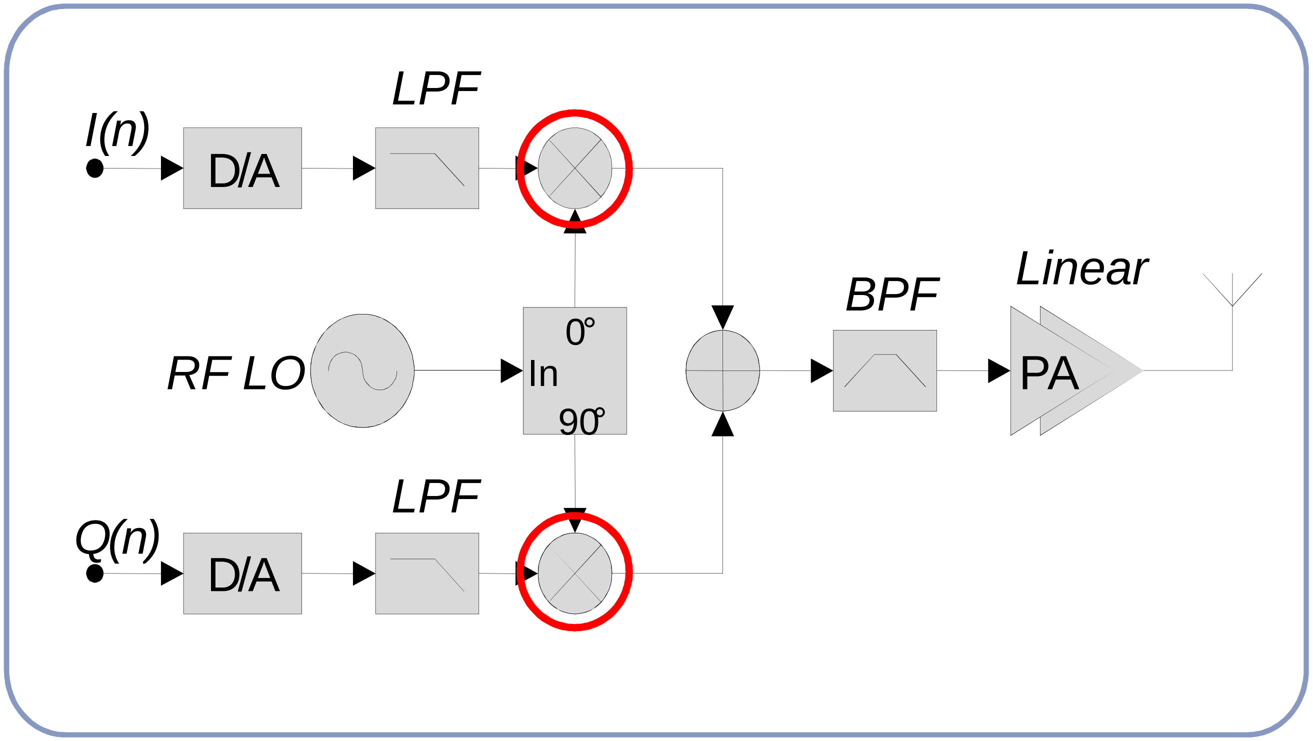
Homodyne Transmitter(1)



Architecture :

- Zero IF -> eliminates a filter
- IQ modulator shifts the spectrum of baseband signal directly to the Rf carrier frequency

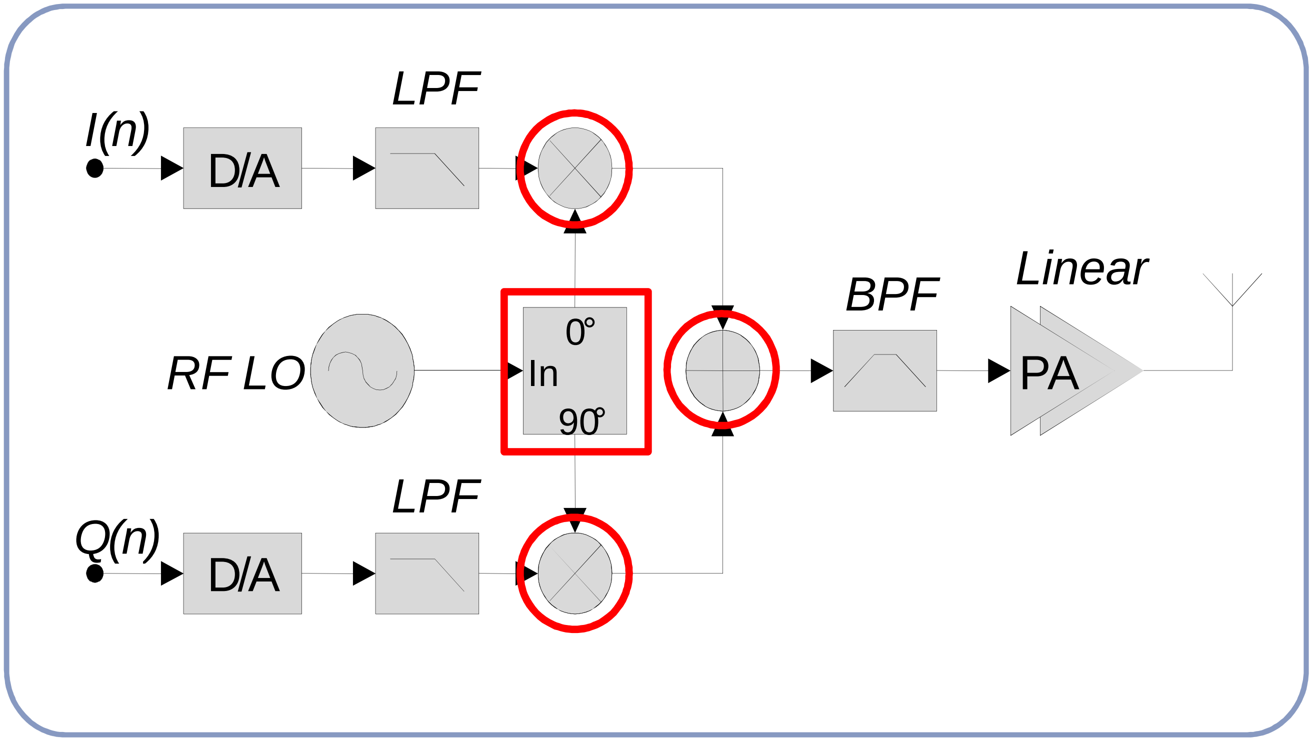
Homodyne Transmiter(2)



Mixers :

- act as switches (lower noise)
- work better when quickly switched
- -> responsible for genration of odd harmonics
- non linearity -> intermodulation products

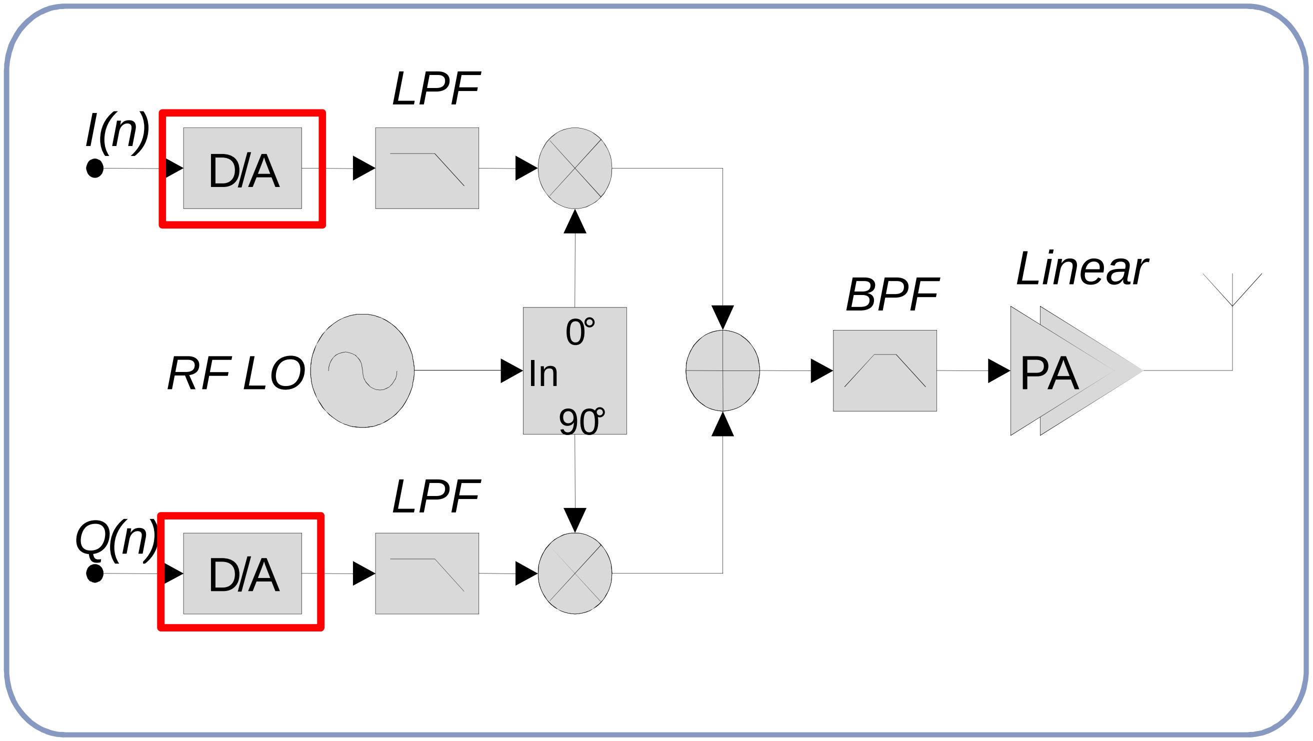
Homodyne Transmitter(3)



Mismatches:

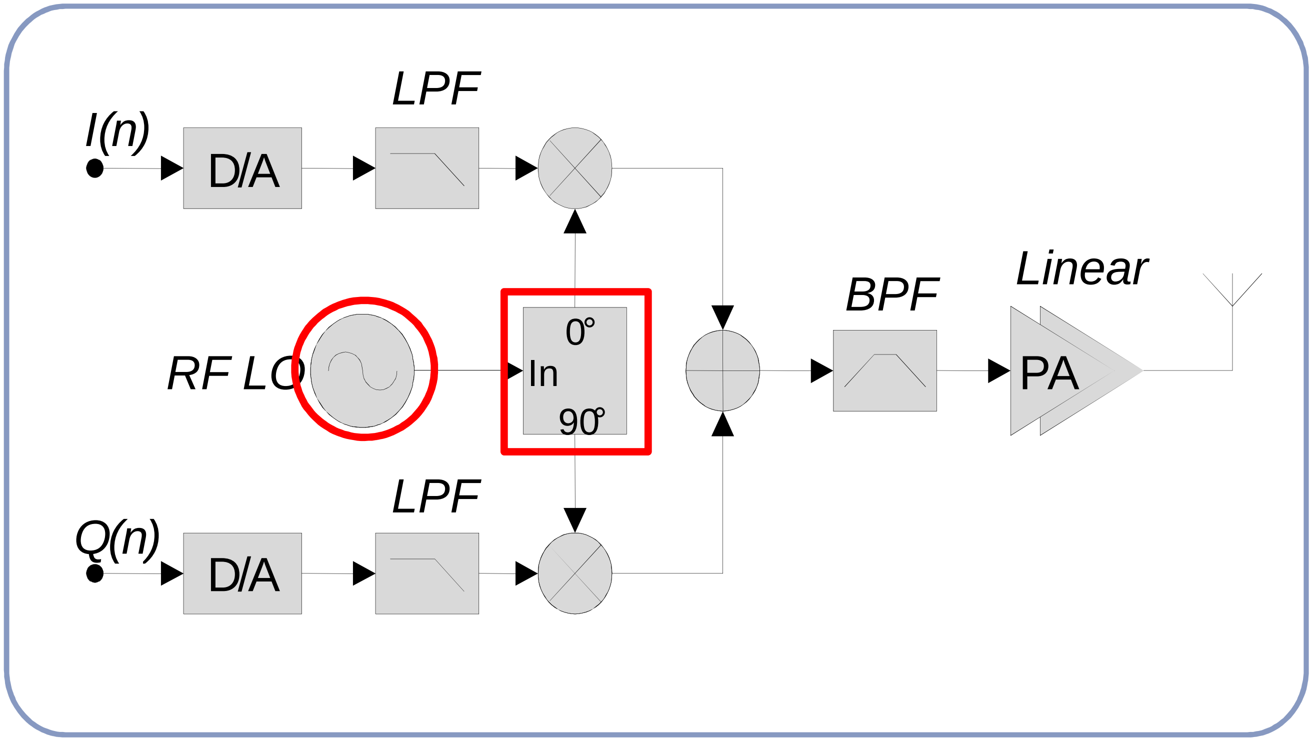
- DC at mixer input -> LO leakage
- Phase and amplitude mismatch ->degrades orthogonality: IQ leakage
- need feedback or calibration to counteract mismatches

Homodyne Transmitter(4)



DAC: - generates white noise over fs/2 bandwidth
- ΣΔ : quantization noise pushed towards fs/2
- output : NRZ like signal -> alias signal at each fs harmonics. (upsampling or precompensation)
- INL, DNL -> distortion

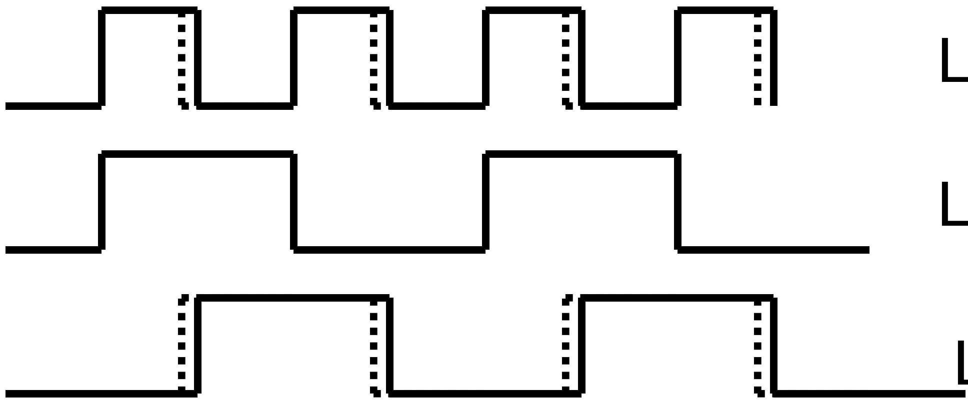
Homodyne Transmitter(5)



LO and quadrature:

- LO : twice RF frequency -> minimizing pulling
- quadrature obtained using both rising and falling edge of a divider by 2.

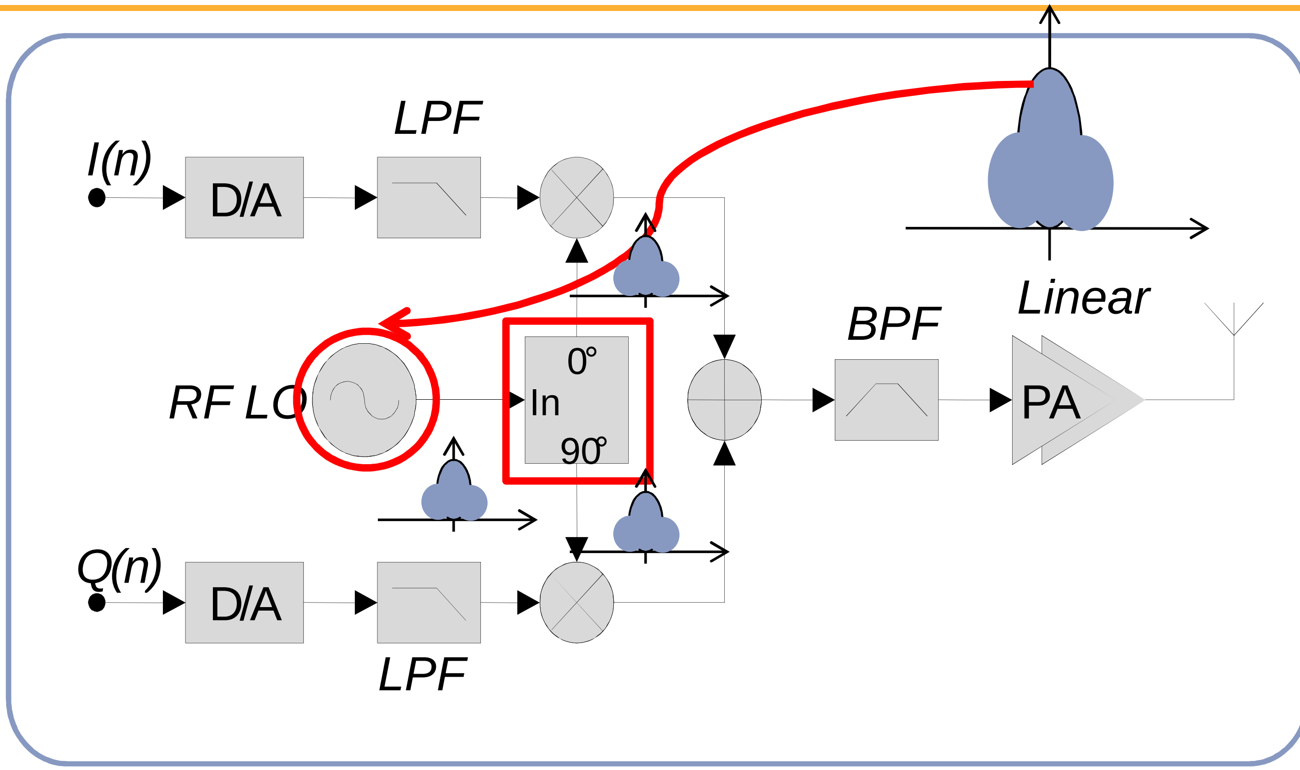
Homodyne Transmitter(6)



LO and quadrature:

- any imbalance in LO rising and falling edge timing degrades LO I&Q generations -> loss of orthogonality

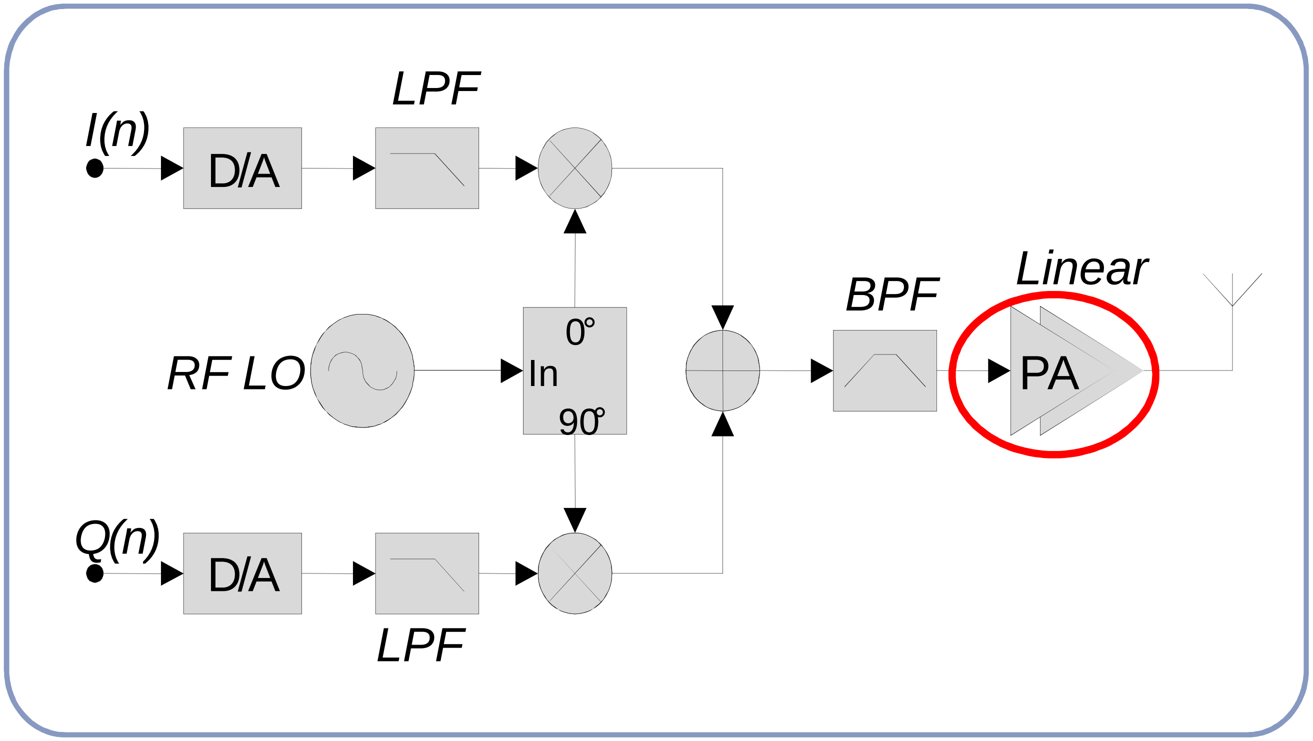
Homodyne Transmitter(7)



LO pulling:

- PA leakage could lock by injection the LO (substate noise, power supply, modulation of LO load impedance).
- LO tracks the PA modulation especially outside PLL badnwidth. -> corrupted signal at output

Homodyne Transmitter(8)



PA and all others drivers:

- must preserve enveloppe -> spectral regrowth
- should be linear -> PA inefficient (40% at peak output power)
- high DC power
- power control

Polar RF transmitter (1)

- RF transmission using a phase and an amplitude phase

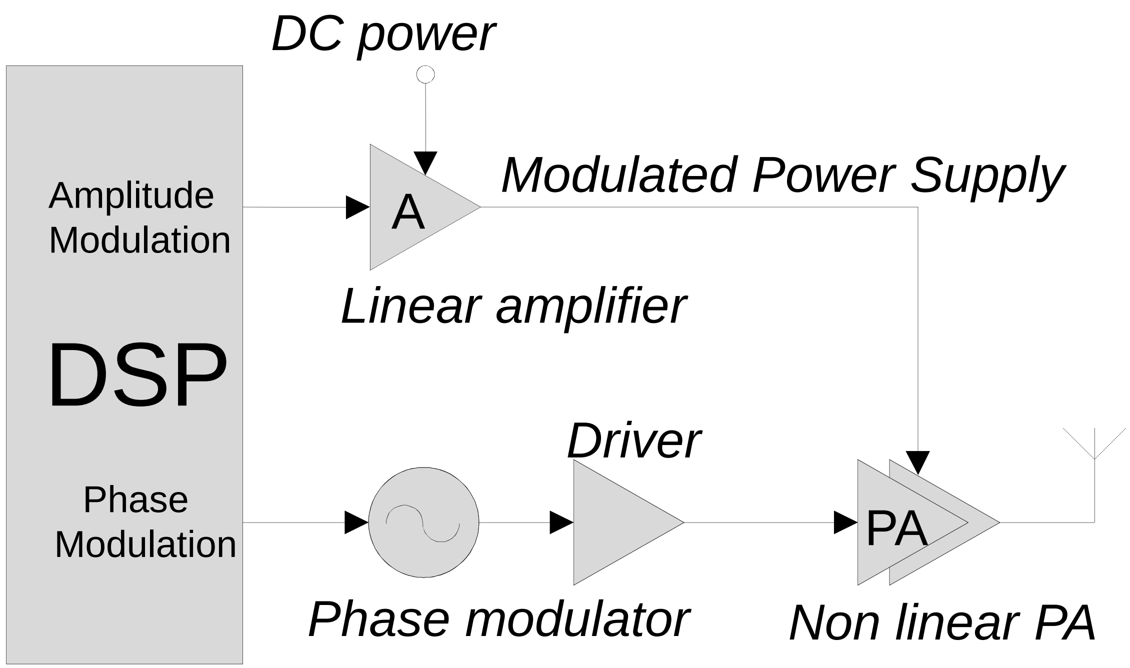
$$RF(t) = I(t)\cos(\omega_{RF}t) + Q(t).\sin(\omega_{RF}t)$$

$$RF(t) = A(t)\cos(\omega_{RF}t + \varphi(t))$$

$$A(t) = \sqrt{I(t)^2 + Q(t)^2}$$

$$\varphi(t) = \arctan(\frac{Q(t)}{I(t)})$$

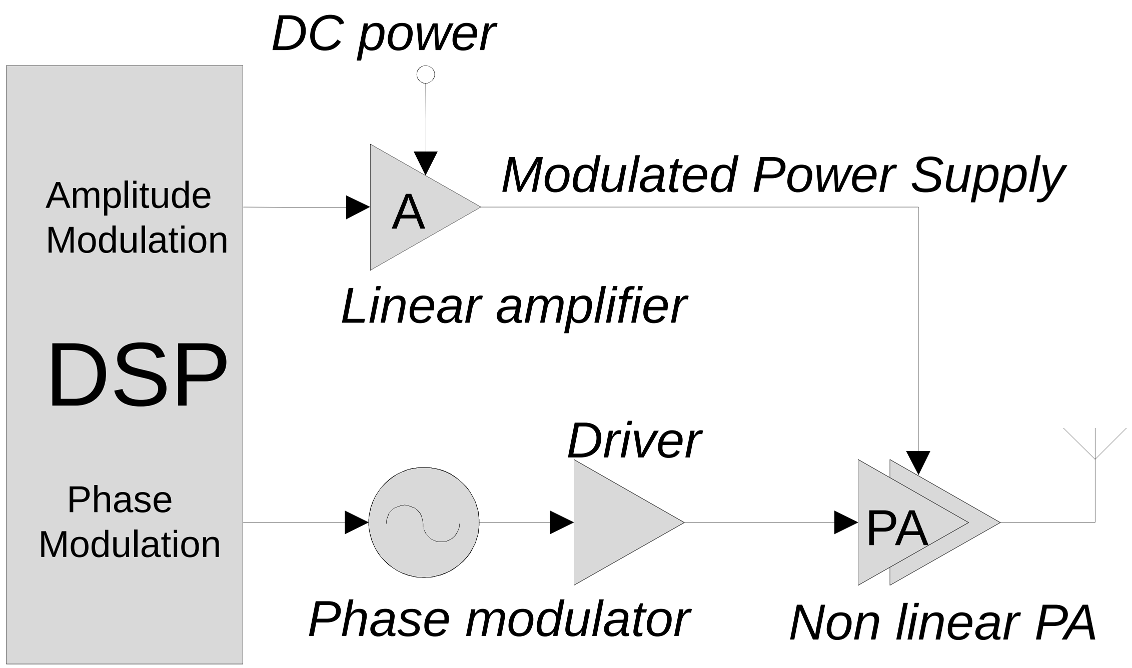
Polar Transmitter (2)



Principle :Is –I

- Generation of A and φ in baseband
- A modulate the power supply of a saturated PA (good efficiency
- Φ is provided at RF using PLL modulation

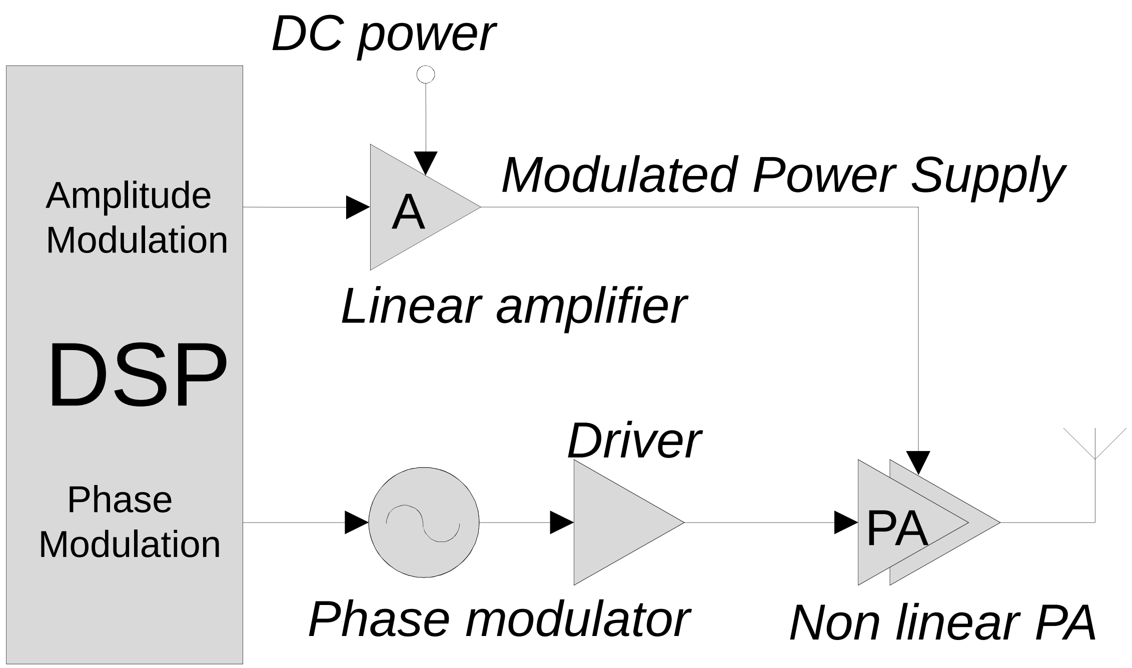
Polar Transmitter (3)



PA:

- Better efficiency obtained with saturated PA (> 60 %)
- Modulation through a DC/DC converter -> efficiency depends on switching frequency (noise, AM bandwidth)
-Distortion for low supply voltages
- needsof predistortion or feedback correction

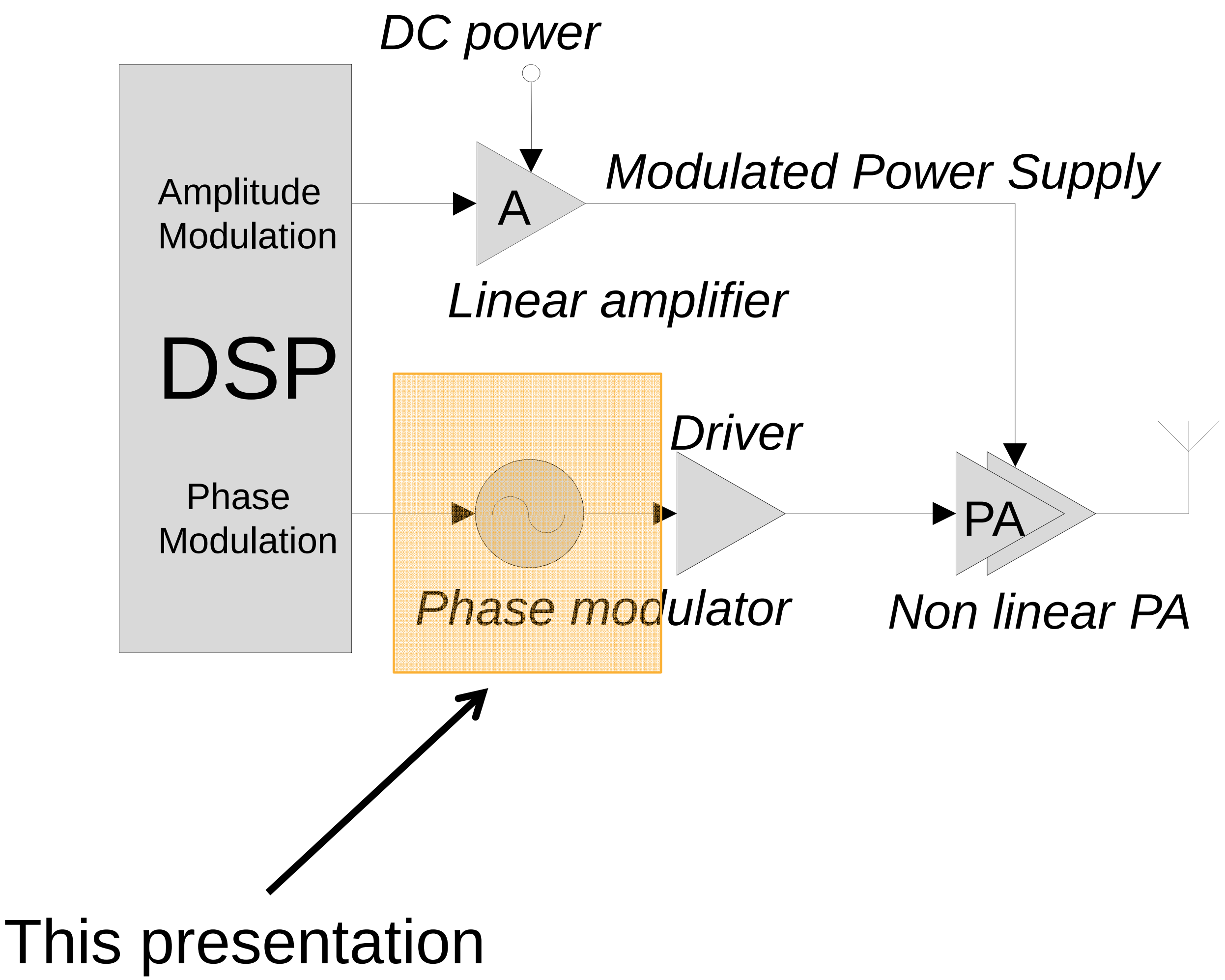
Polar Transmitter (4)



Phase and amplitude combination:

- To be effective, amplitude and phase modulations should arrive in the same time.
- The phase modulator using modulated PLL brings group delay -> to be compensated

Polar Transmitter (5)



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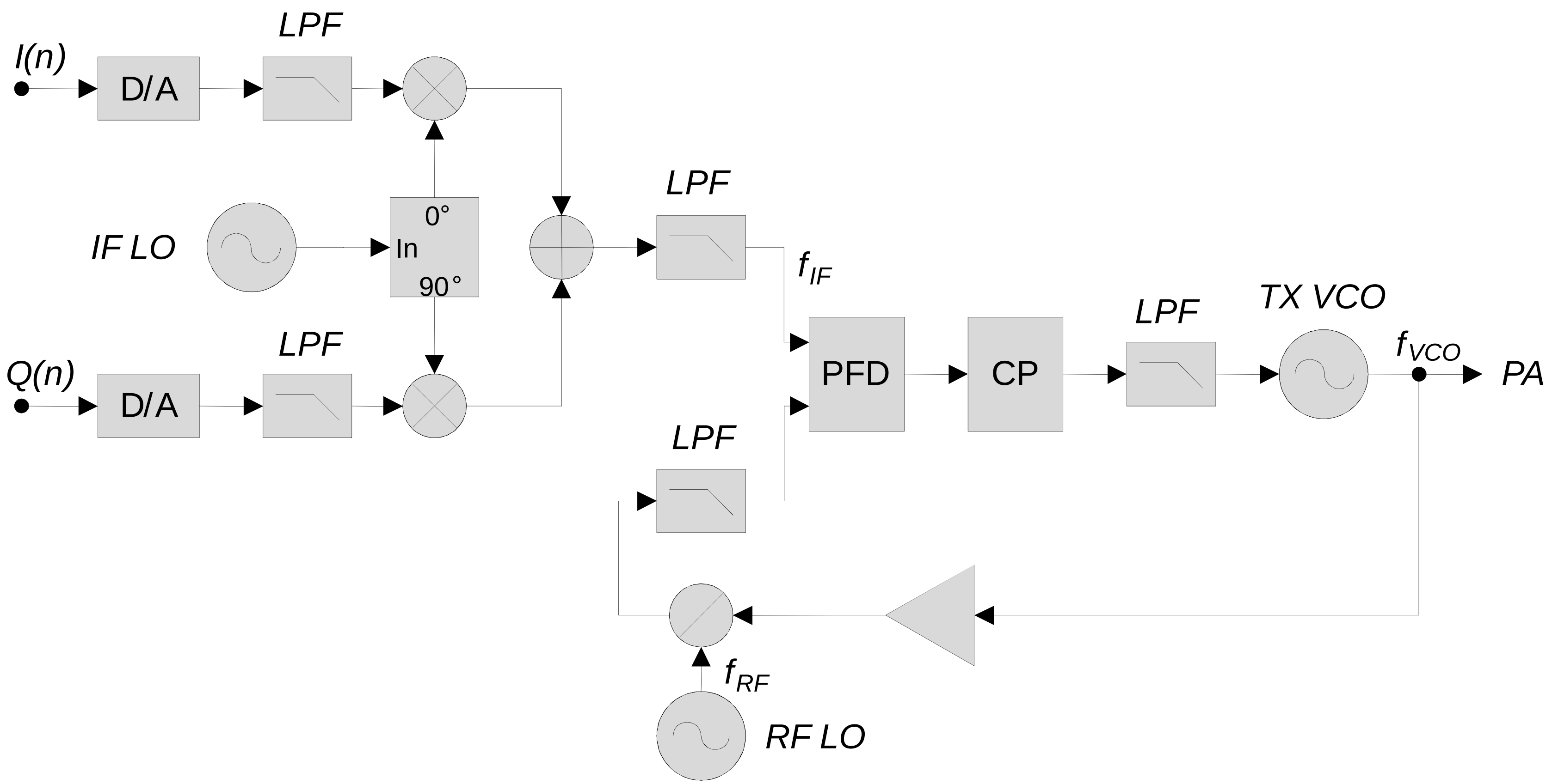
Offset PLL based Transmitter



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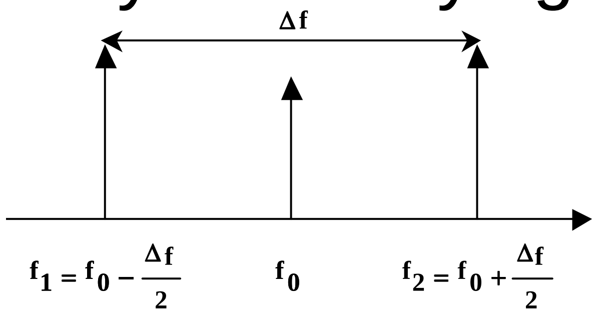
FSK modulation (1)

- FSK : Frequency Shift Keying



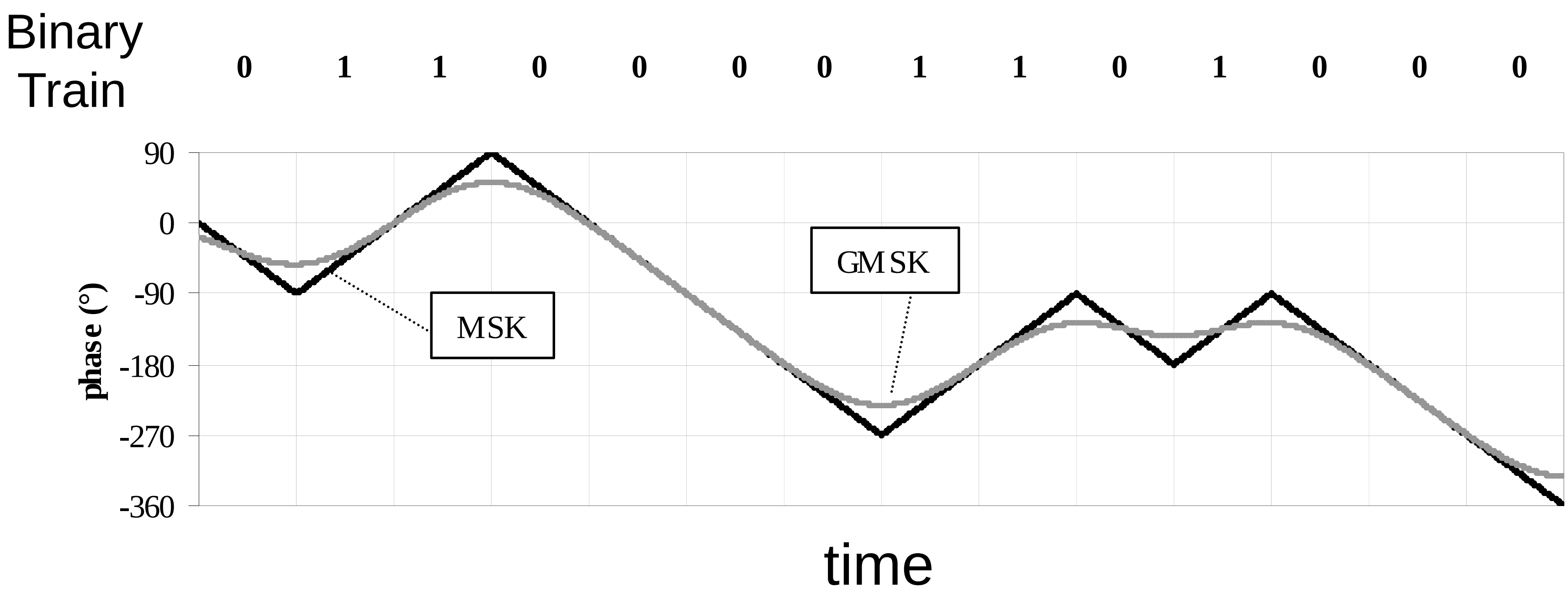
  - Bit duration = Tb
  - RF expression:

$$RF(t) = A\cos(\omega_0 t + \pi\Delta f \int_0^t s(u)du)$$

  - Modulation index : h = Δ f/fb
  - Phase deviation over one bit : π.Δf.Tbit

MSK modulation

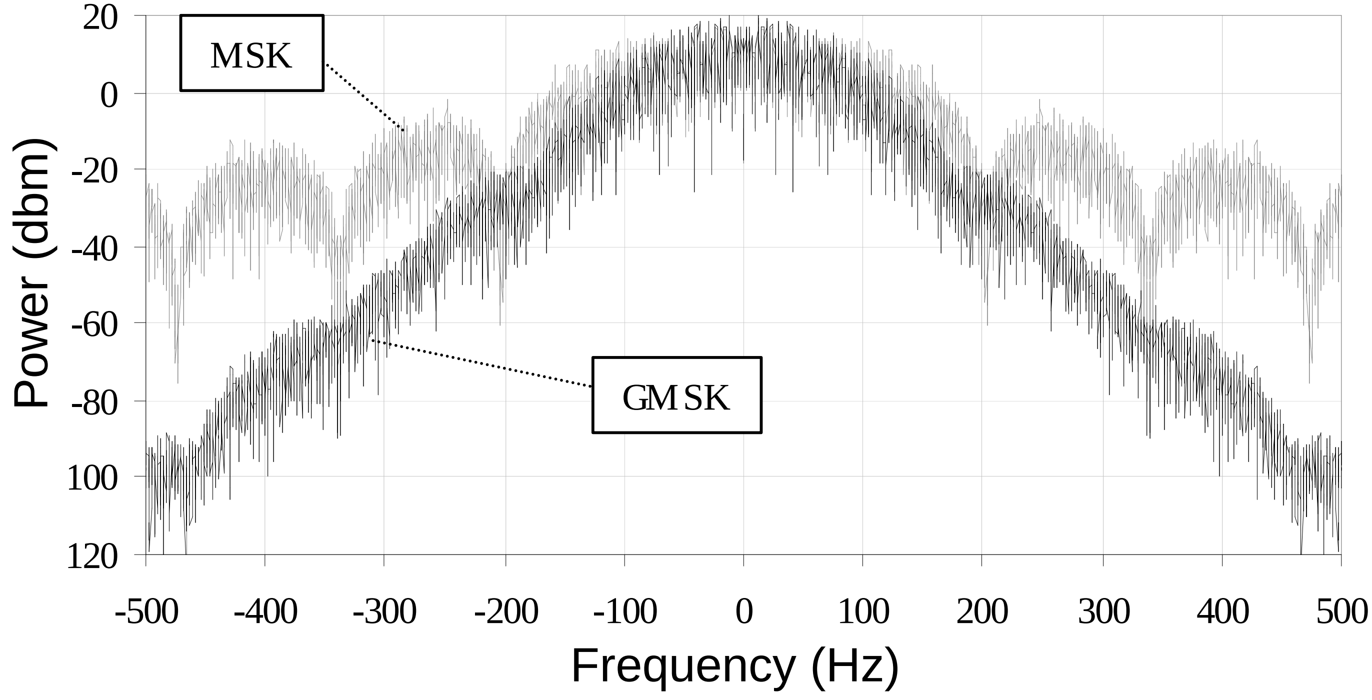
- When FSK modulation index = 0.5 -> MSK
- Phase deviation over one Tbit : 90º



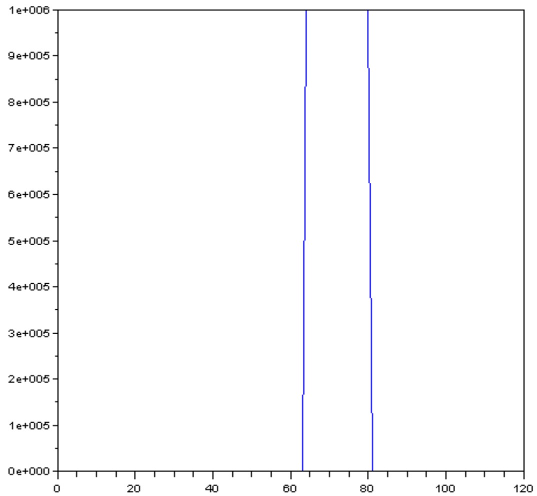
GMSK modulation(2)

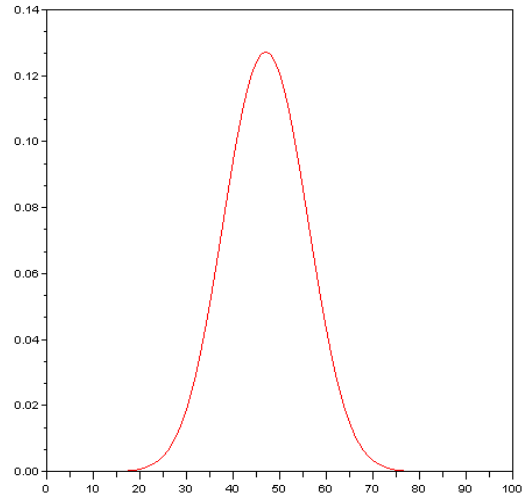
- FSK spectral occupation : $\frac{2}{T_b} + \Delta f$

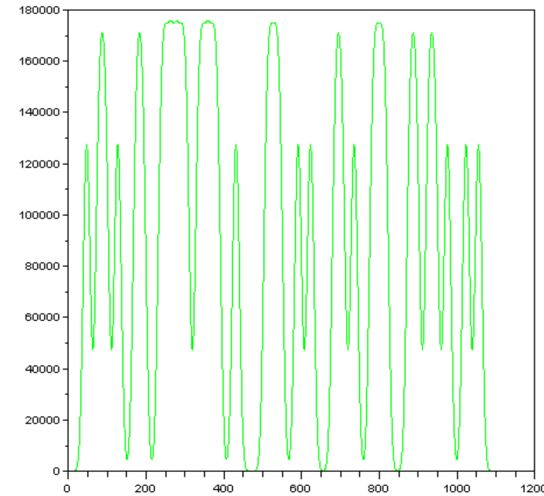
- GMSK : filtering data using a gaussain filter in order to lower the spectral occupation without information loss



GMSK modulation(3)



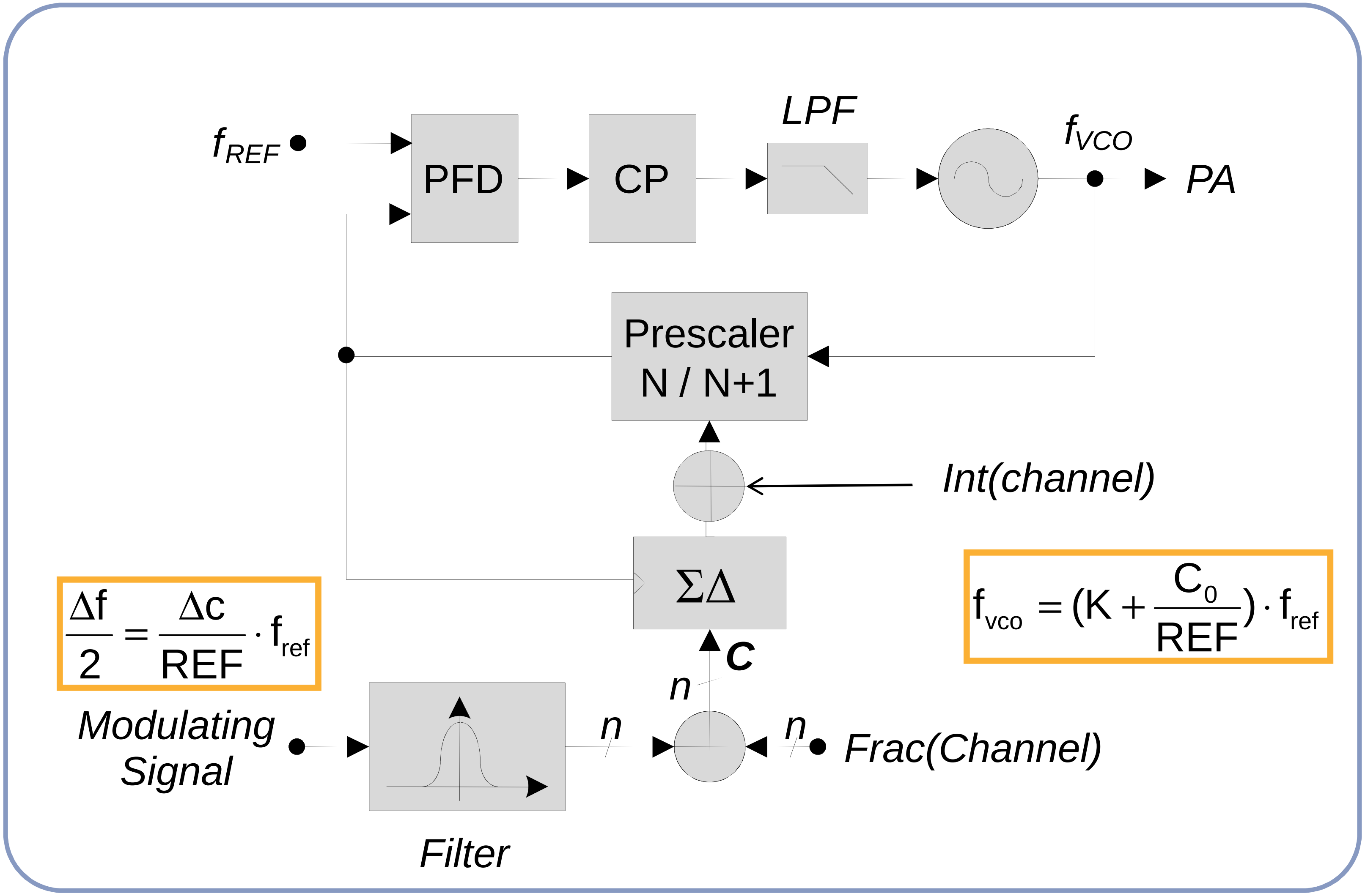




$$\mathrm{rect}\left(\frac{t}{\mathrm{Tbit}}\right) * \frac{\exp\left(\frac{-t^2}{2\cdot\sigma^2\cdot T_{BIT}{}^2}\right)}{\sqrt{2\pi}\cdot\sigma\cdot T_{bit}} = f(t)$$

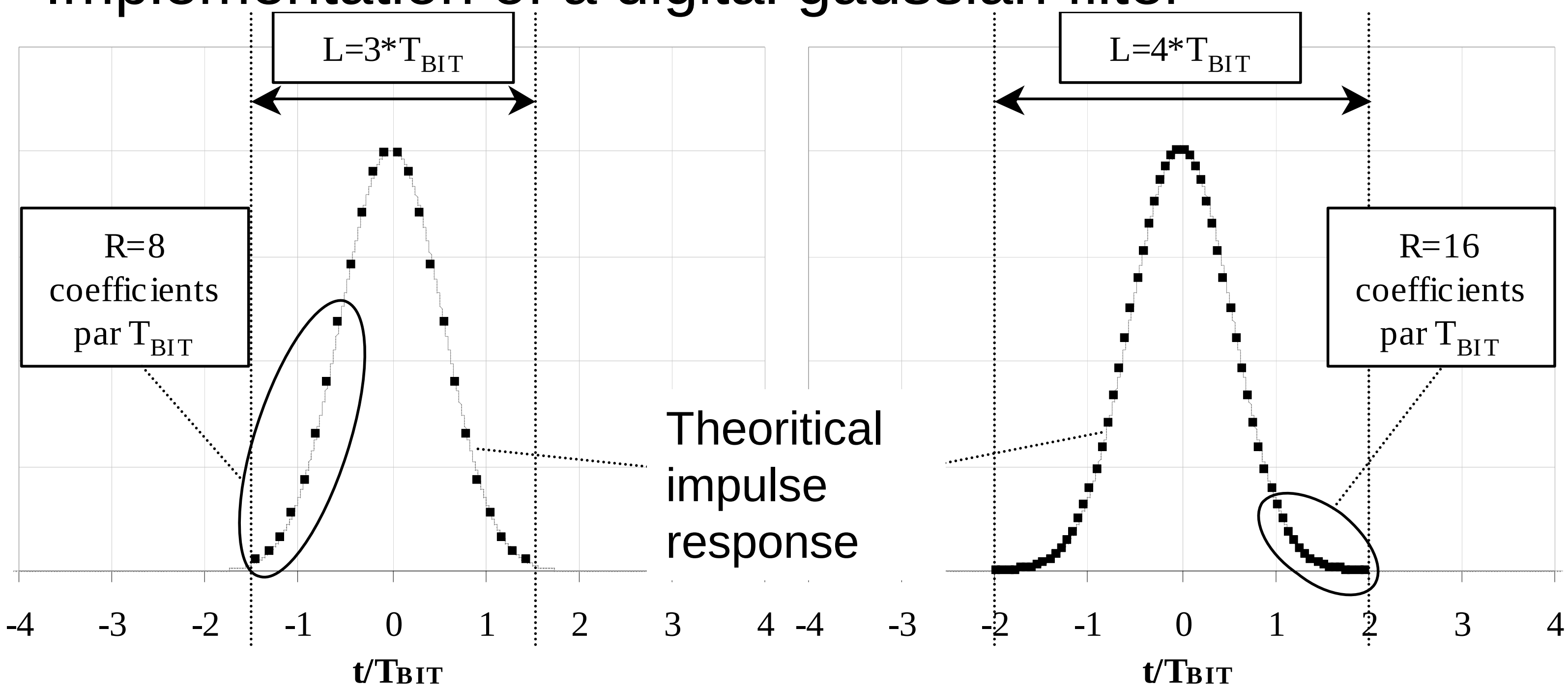
$$\sigma = \frac{\sqrt{\ln(2)}}{2\pi . B . T_{BIT}}$$

Fractional N PLL based Transmitter



Gaussian Filter optimisation(2)

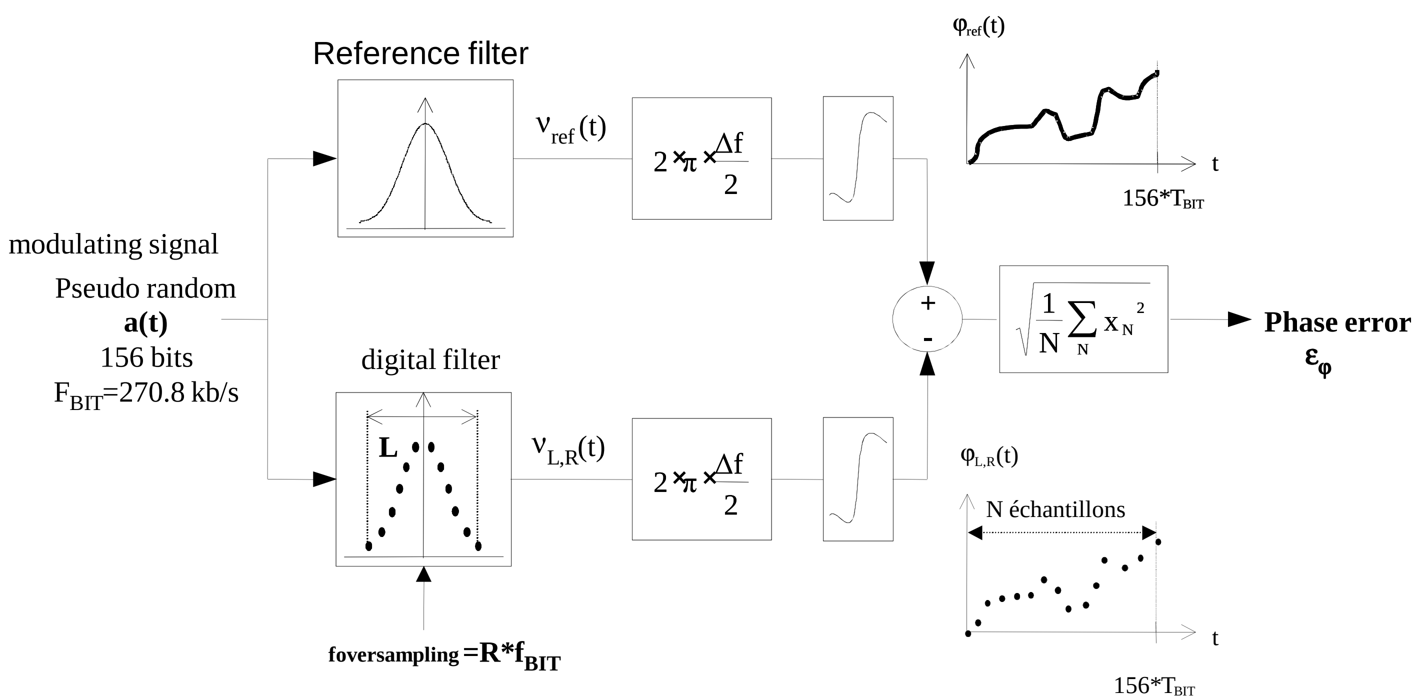
- Implementation of a digital gaussian filter



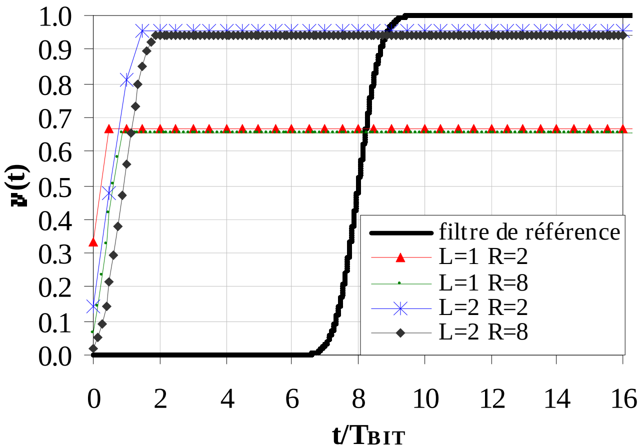
- Determination of optimal impulse response length L and oversampling coefficient R.
- Coefficient number: R*L

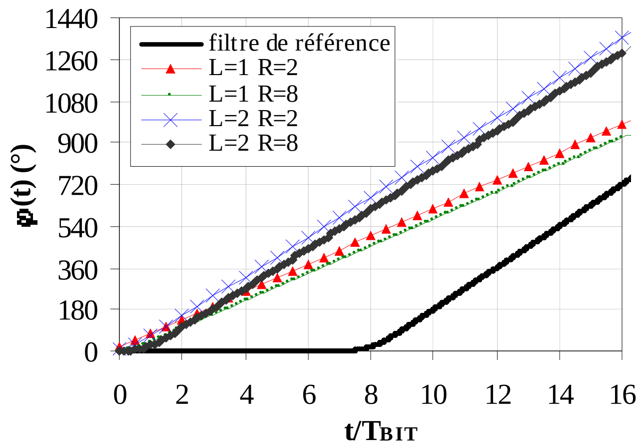
Gaussian Filter Optimisation(3)

- Constraints on L&R
  - $R_{max} = f_{ref} / f_{bit}$
  - Area occupied by digital filter
  - Phase error due to the pulse response sampling

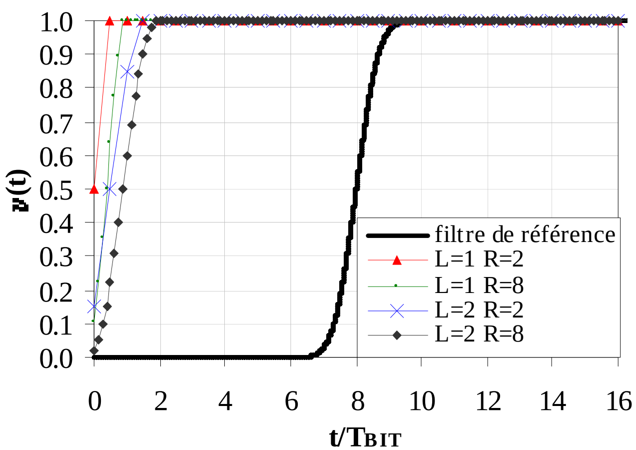


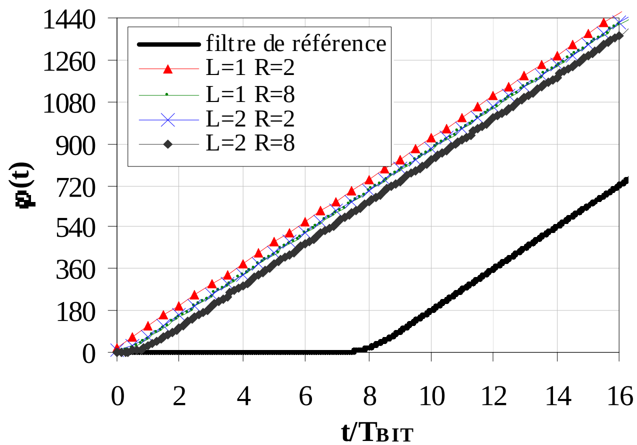
Gaussian Filter Compensation





- Before comparison, filters need to be compensated in gain and group delay





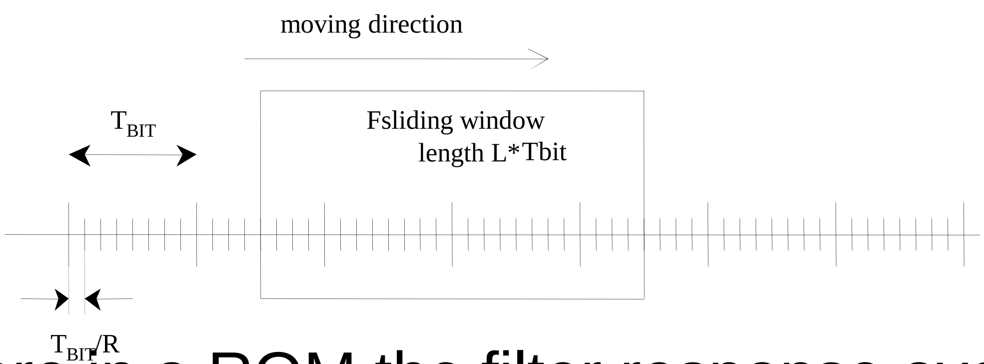
Gaussian Filter Optimization

L \ R	2	4	8	16	32
1	12.9	10.2	9.6	9.5	9.4
2	3.9	2.74	2.46	2.39	2.37
3	1.7	0.56	**0.29**	**0.23**	0.22
4	1.6	0.39	**0.10**	**0.04**	0.03
5	1.6	0.38	9.9E-2	3.8E-2	3.1E-2
6	1.6	0.38	9.9E-2	3.8E-2	3.1E-2

- Table gives the quadratic phase error in degrees
- L=3 R=8 has been chosen

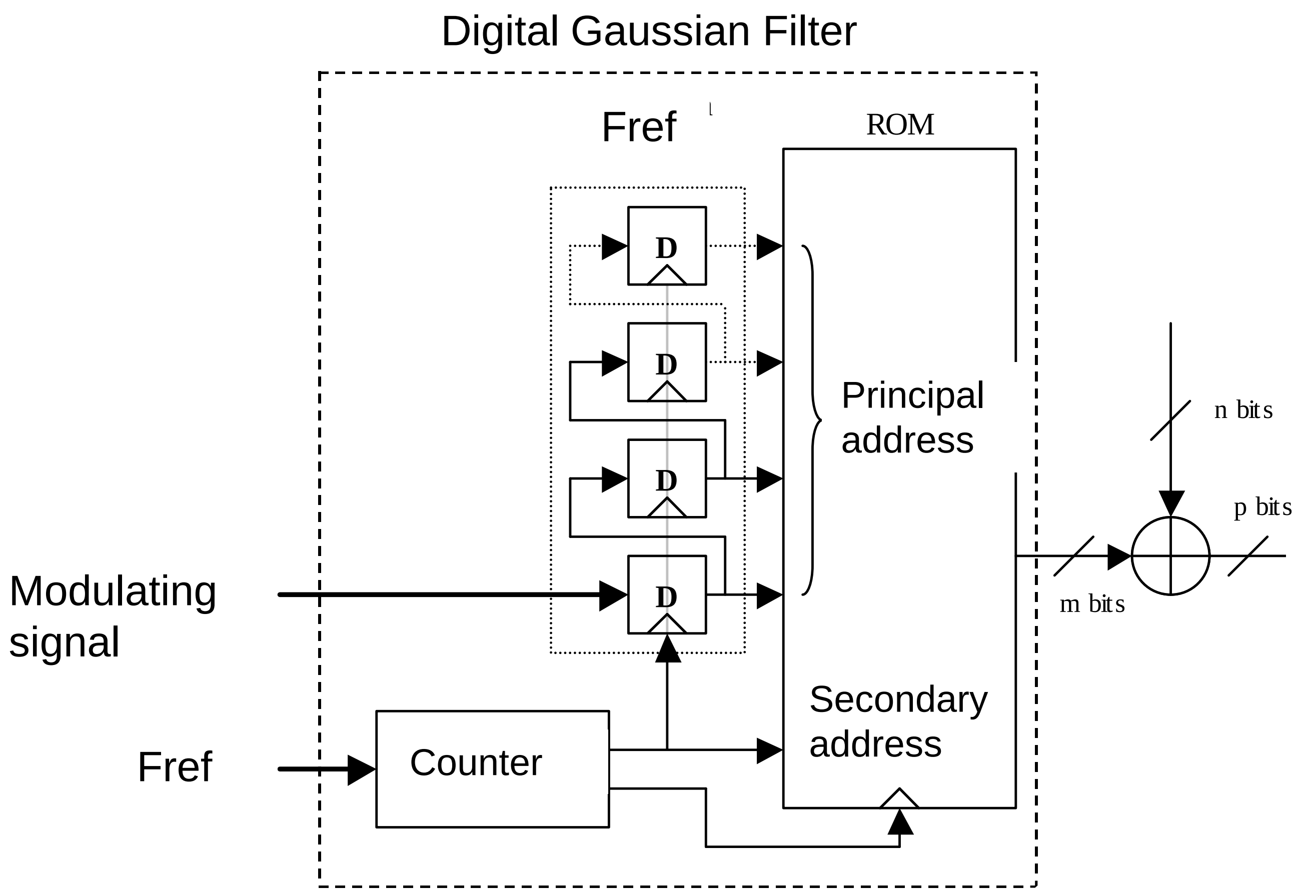
GMSK Modulator Implementation (1)

- Gaussian filter of 3-bit impulse response could be seen as a sliding window of 3 bits and that concerns 4 bit

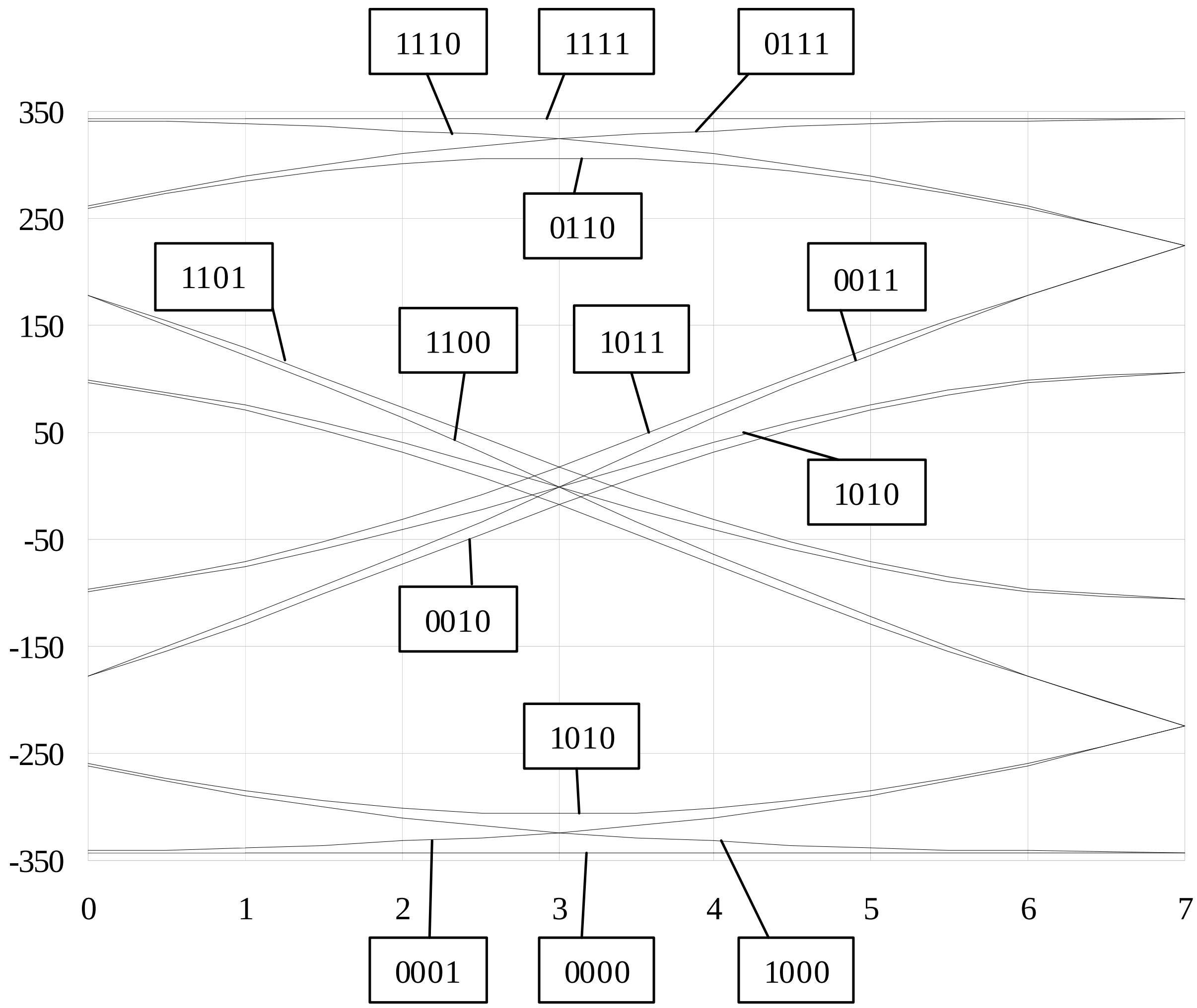


- Idea: store in a ROM the filter response over 4 bits sequences (16 possibilities)

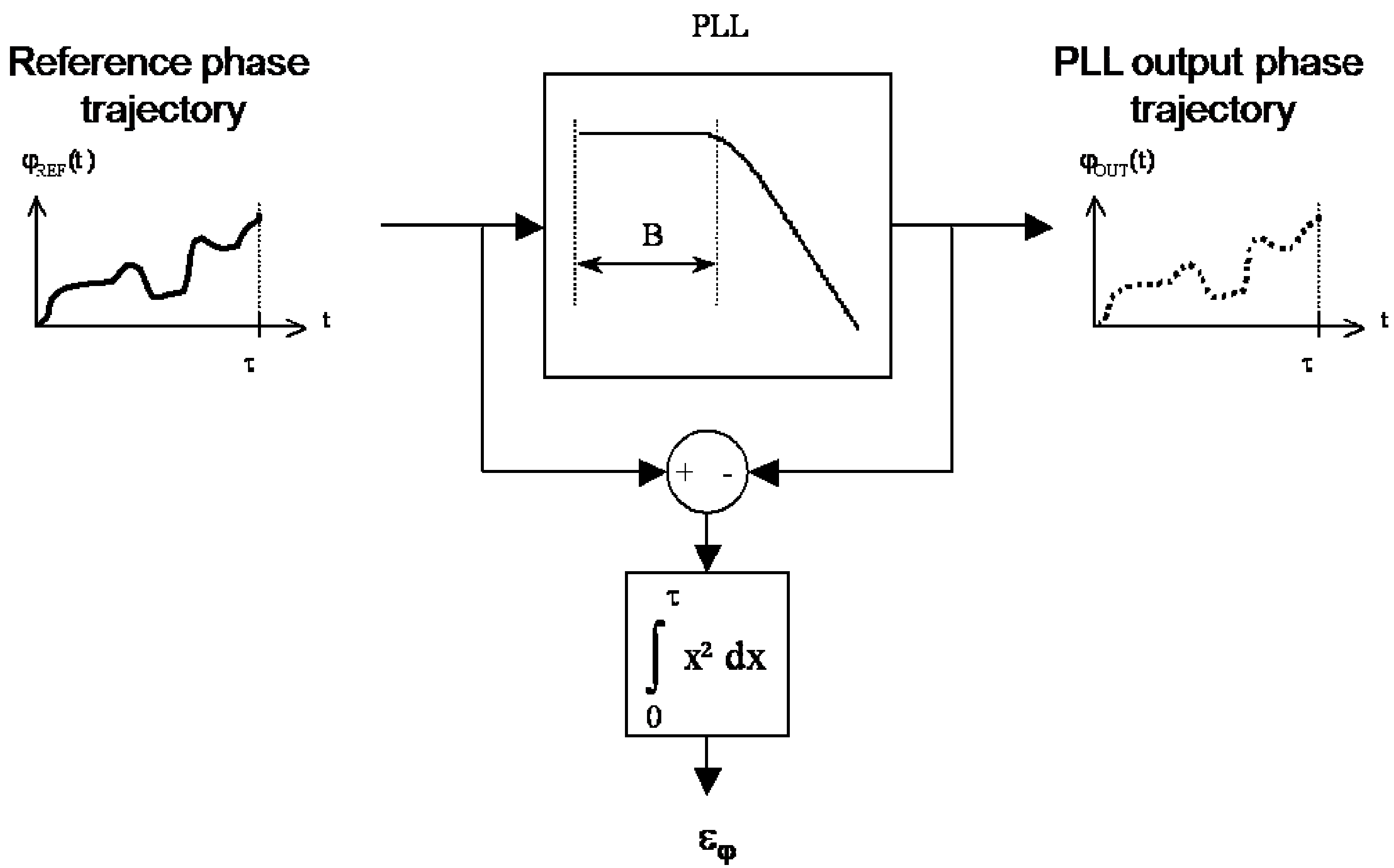
GMSK Modulator implementation (2)



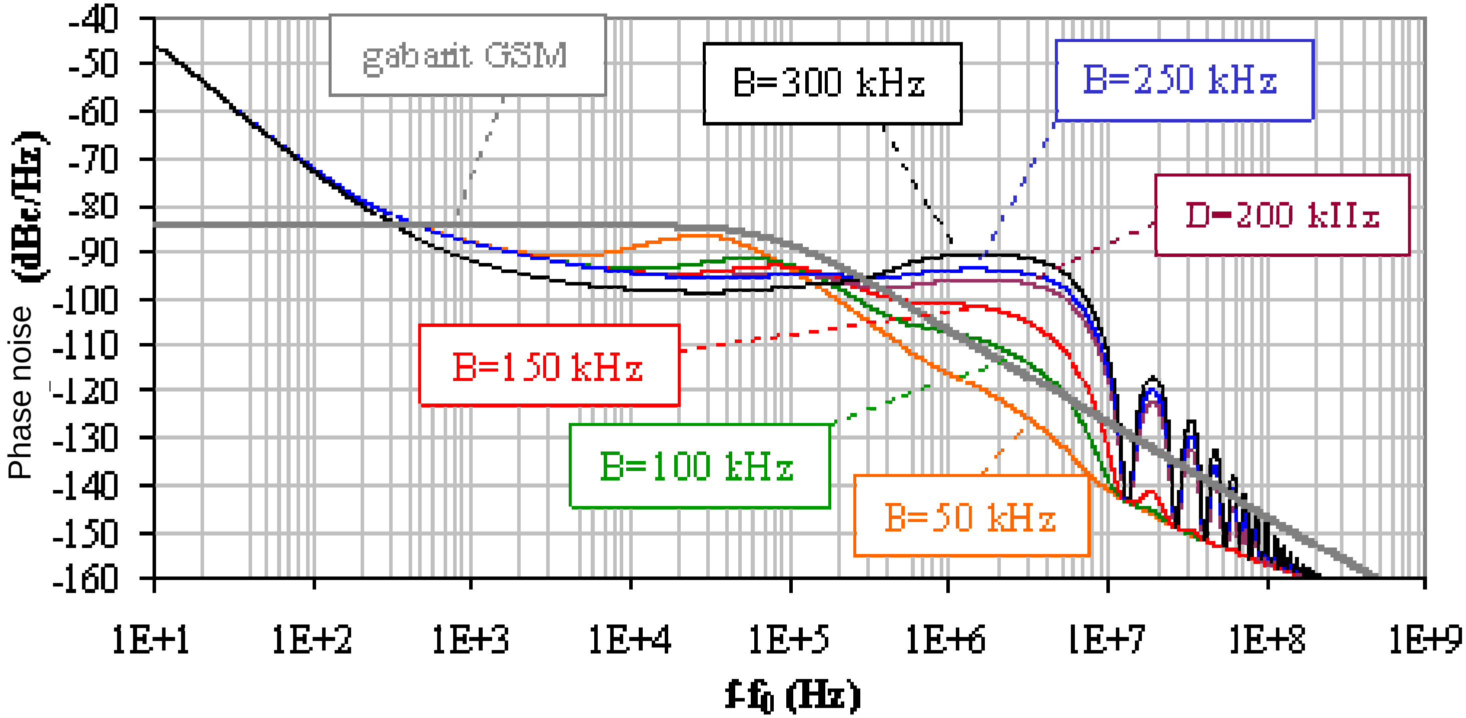
GMSK modulator implementation (3)



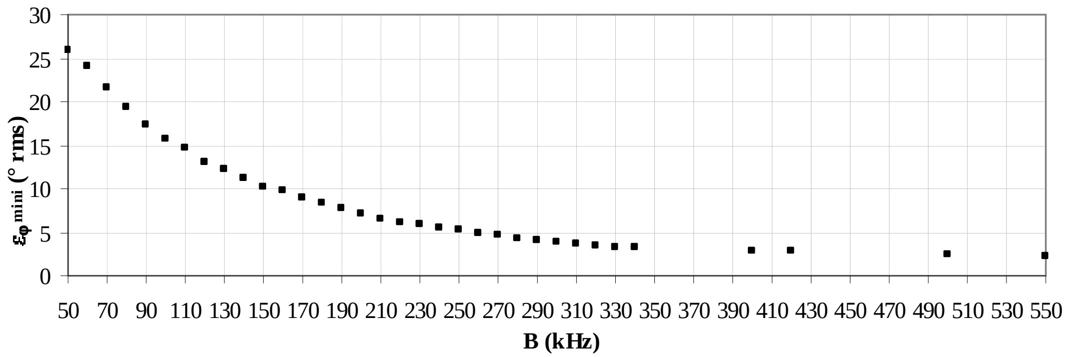
PLL bandwidth influence on modulation (1)



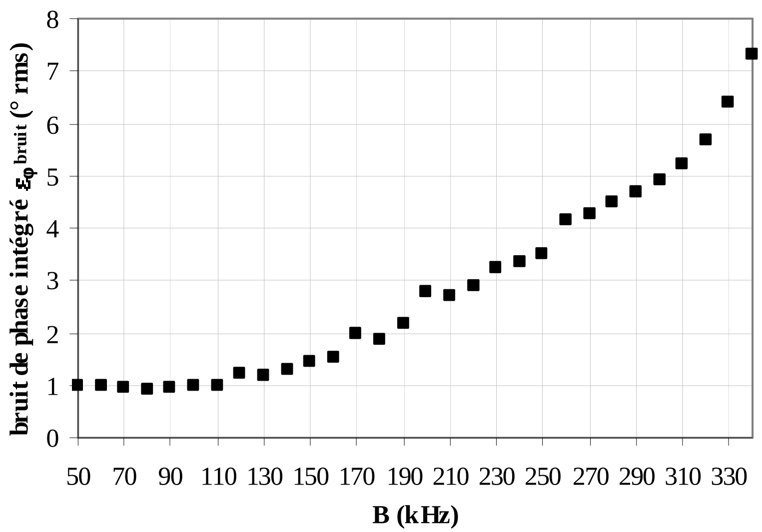
PLL bandwidth influence on phase noise



PLL bandwidth tradeoff

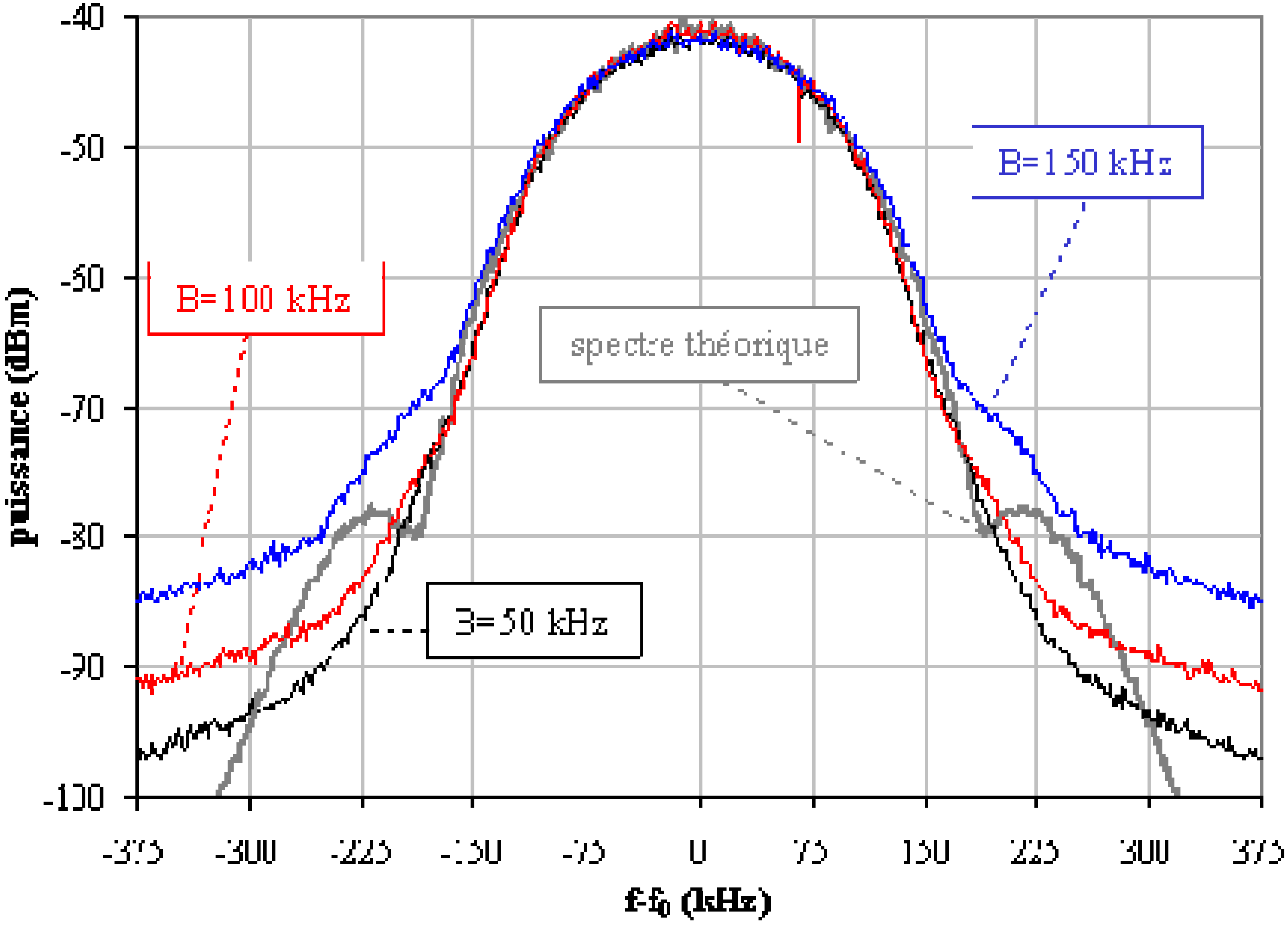


Integrated error decreases with PLL bandwidth

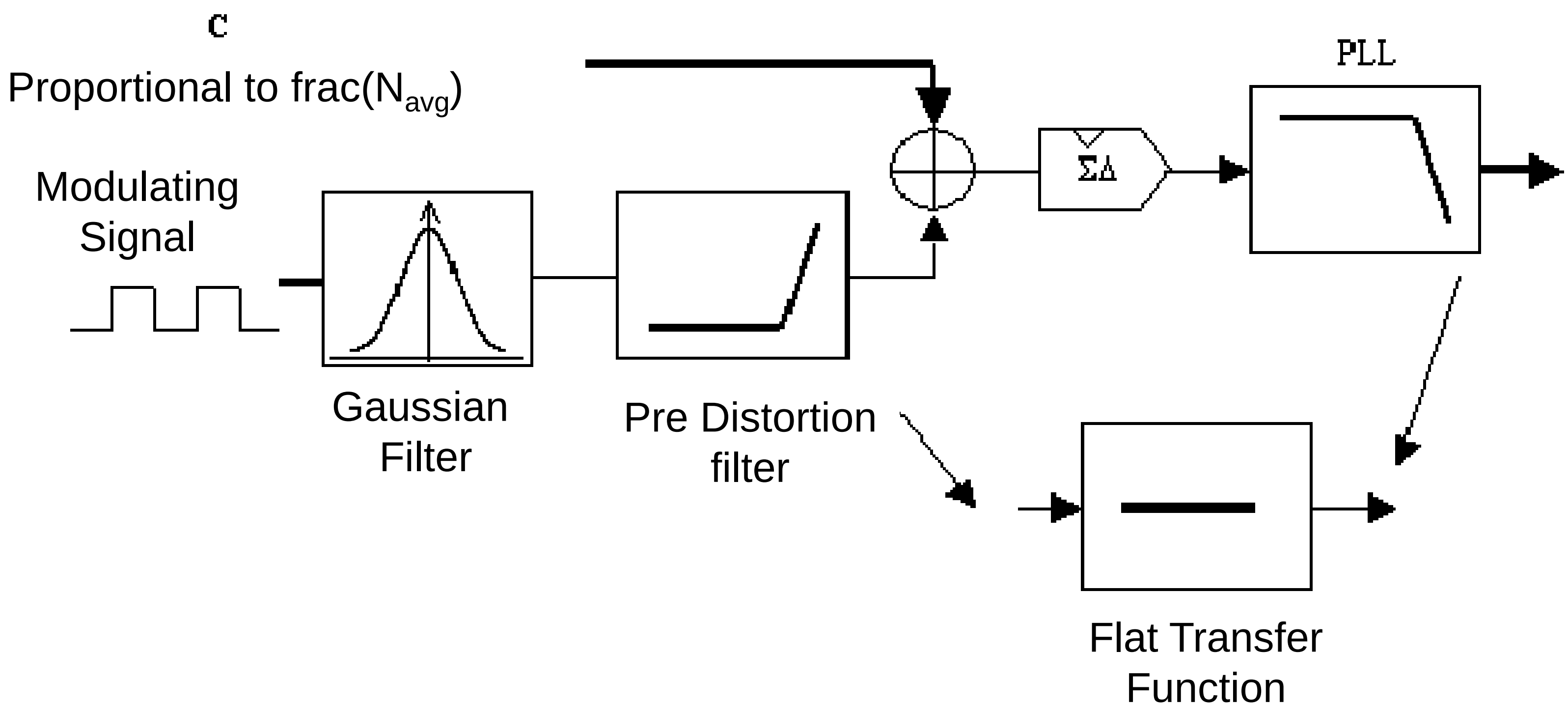


Phase noise increases with PLL bandwidth

PLL bandwidth effect on GSMK modulation



Modulation Bandwidth Extension



- Predistortion filter to counteract the PLL bandwidth effect
- Needs to know and control the PLL transfer bandwidth over PVT -> rather complicated

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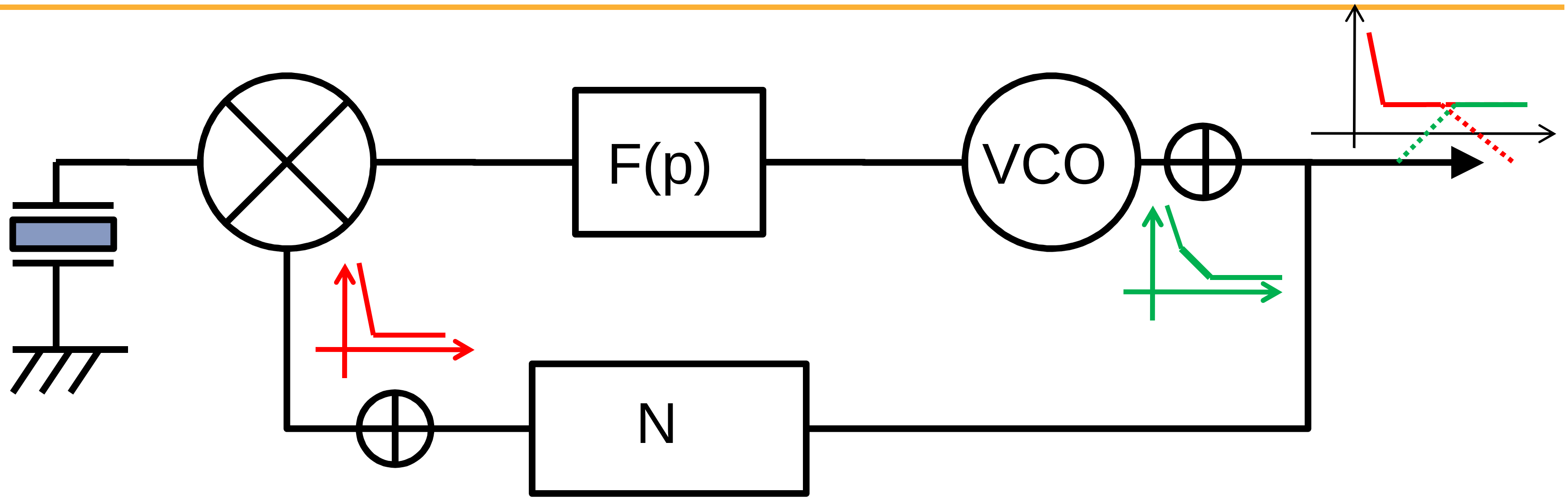
Two Point Modulation Architecture



- Principle : PLL is a high pass filter for VCO noise and a low pass filter for divider noise.
- Idea : apply modulation on both divider and VCO to enlarge the modulation bandwidth

Modulated Divider Small Signal Model

- Frequency step at divider output:

$$df = \frac{f_{VCO}}{N+1} - \frac{f_{VCO}}{N} \approx -\frac{f_{VCO}}{N_{avg}^{2}} \approx -\frac{f_{Ref}}{N_{avg}}$$

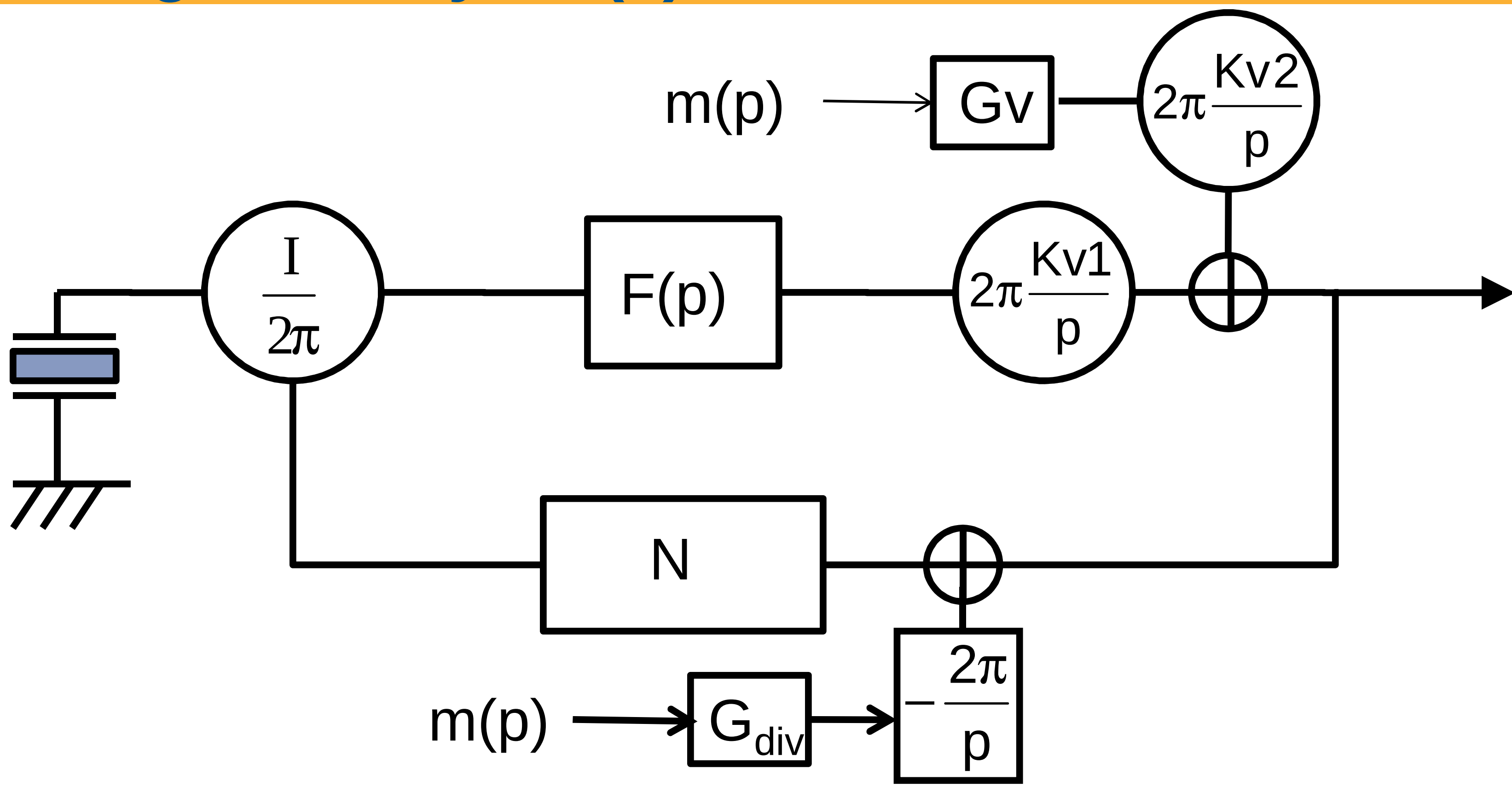
- Frequency modulation due to divider modulus deviation:

$$df_{ref}(t) = -n(t) * \frac{f_{ref}}{N_{avg}} \qquad m(t) = n(t) * fref$$

- Integration in z domain then in laplace domain leads to:

$$d\phi(p) = -2\pi \frac{m(p)}{p} * \frac{1}{N_{avg}}$$

Two Point Modulation : small signal analysis (1)



- Modulation applied on another VCO varactor
- Modulation applied on feed back loop divider: modulates the frequency need thus to be integrated in phase noise model

Two Point Modulation : small signal analysis (1)

- Output response for VCO modulation:

$$\phi_{out1} = 2\pi K_{v2} G_V \frac{m(p)}{p} \frac{1}{1+BO(p)}$$

- Output response for divider modulation

$$\phi_{out2} = G_{Div} \frac{m(p)}{p} \frac{BO(p)}{1+BO(p)}$$

- Output response for modulation applied on both inputs

$$\phi_{out} = \phi_{out2} + \phi_{out1} = 2\pi \frac{m(p)}{p} \left(\frac{G_v K_{V2} + G_{div} BO(p)}{1+BO(p)} \right)$$

Two Point Modulation : small signal analysis (2)

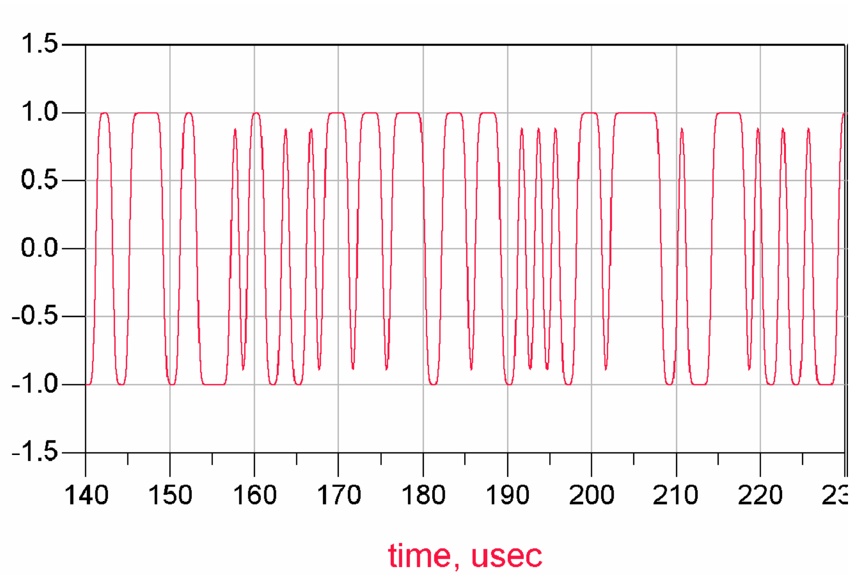
- If Gdiv = 1 and Gv = 1/Kv2:

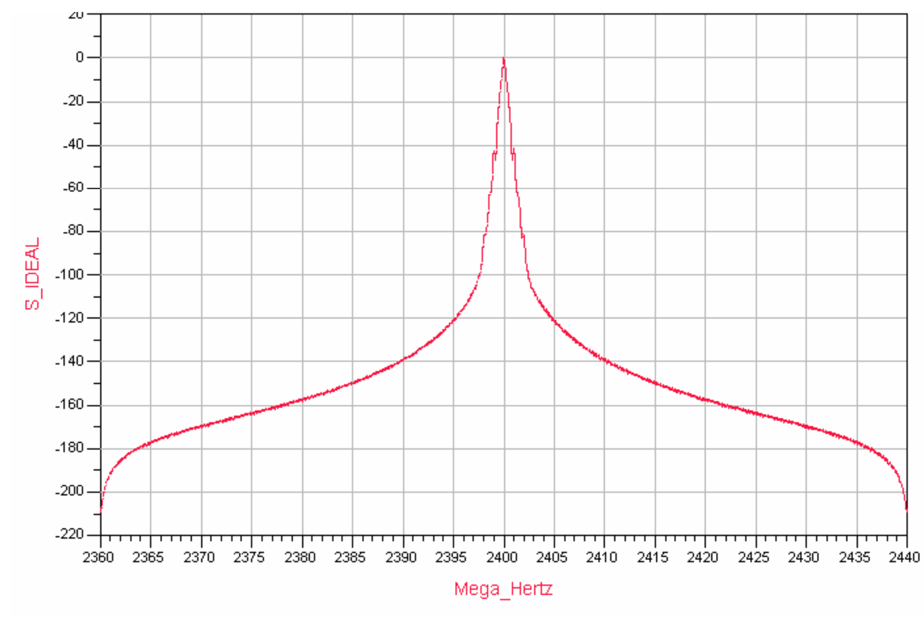
$$\phi_{out} = 2\pi \frac{m(p)}{p}$$

- It is thus possible to use a frequency synthesizer as a modulator even for bandwidth signal greater than the PLL bandwidth
- Accuracy of the method depends strongly on the accuracy of the gain Gv that should equal to the 1 over the VCO gain.

Example: GMSK modulation

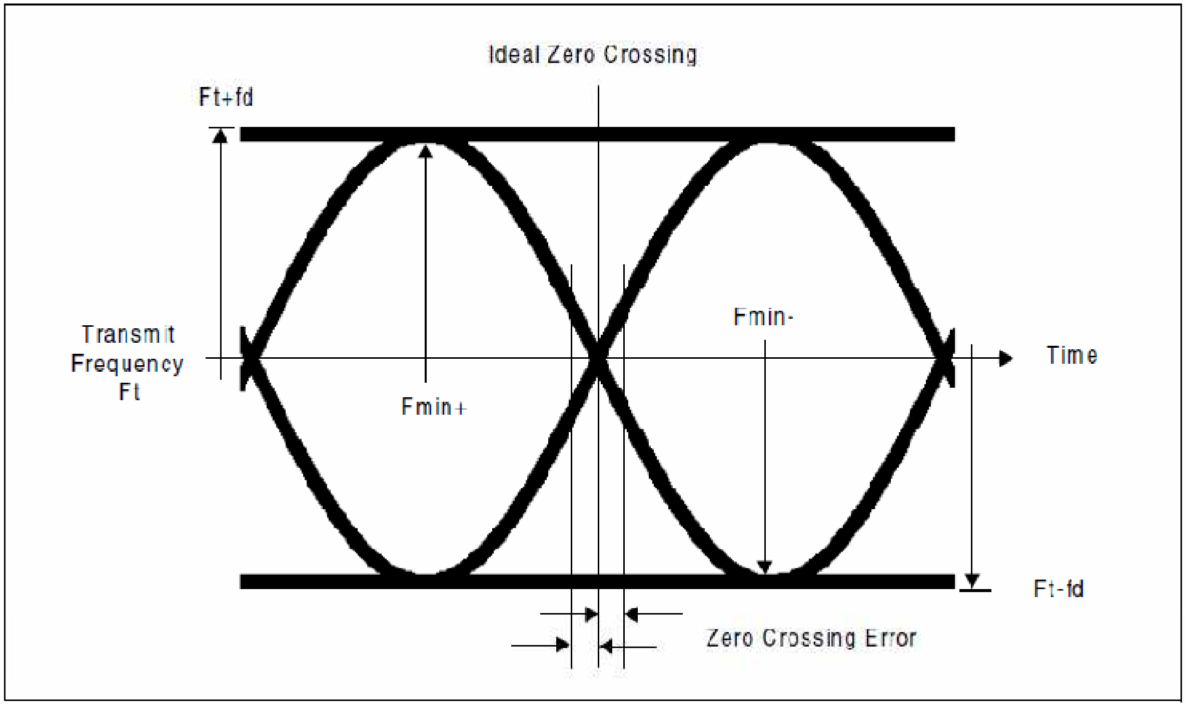
- GFSK 1Mb/s – modulation index 0.33
- Gaussian filtering index BT = 0.5



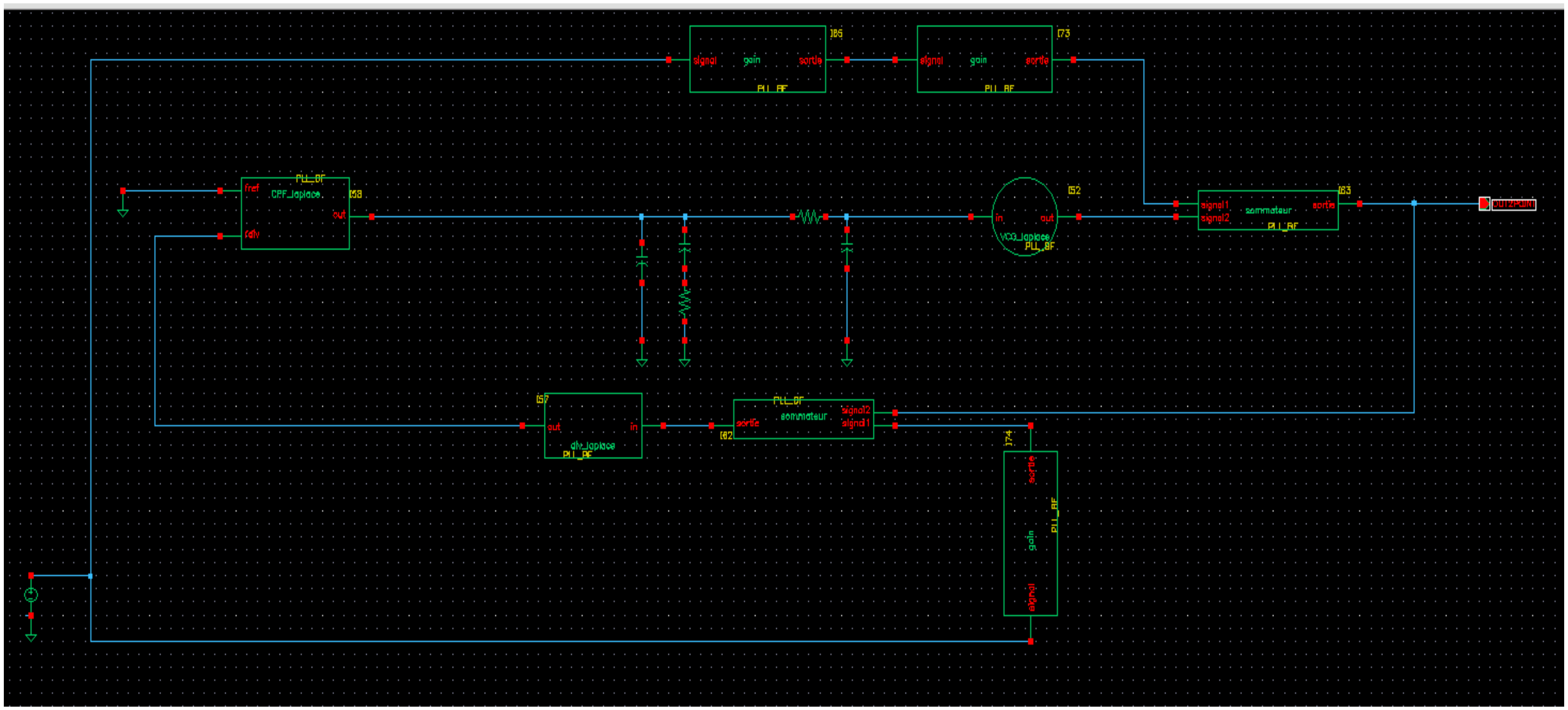


Bluettooth Eye Diagram

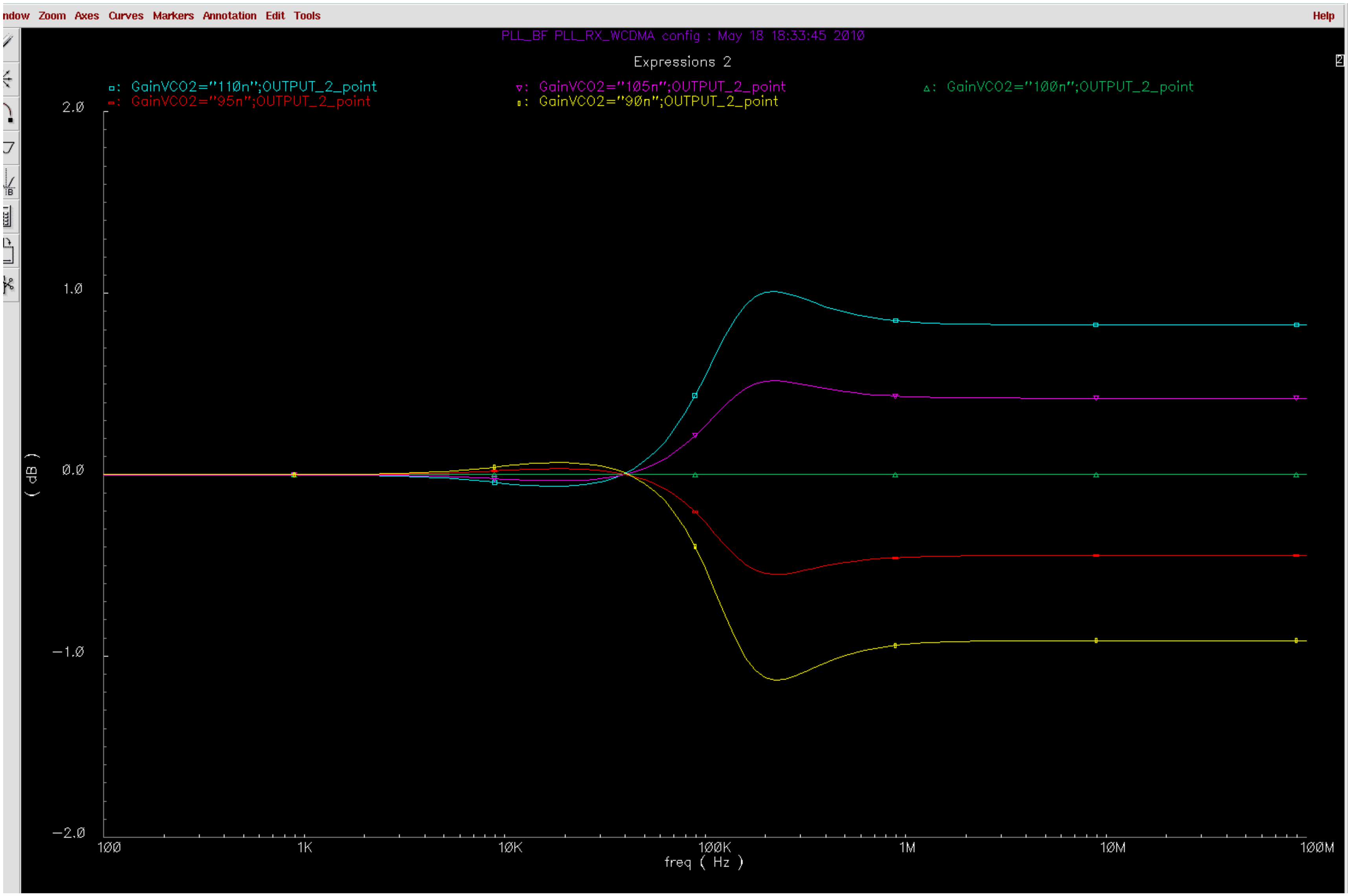
- Bluetooth specifies minimum openings of transmitted data eye diagram



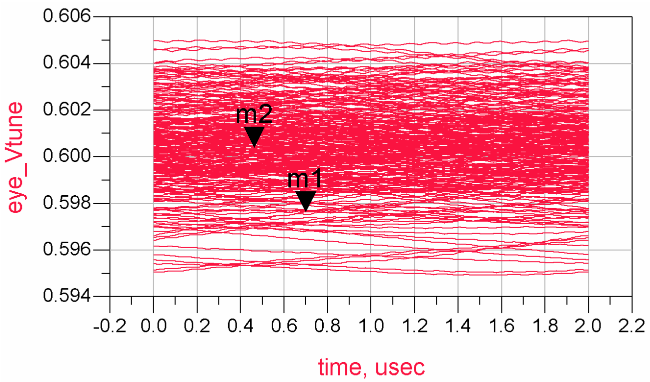
PLL test bench



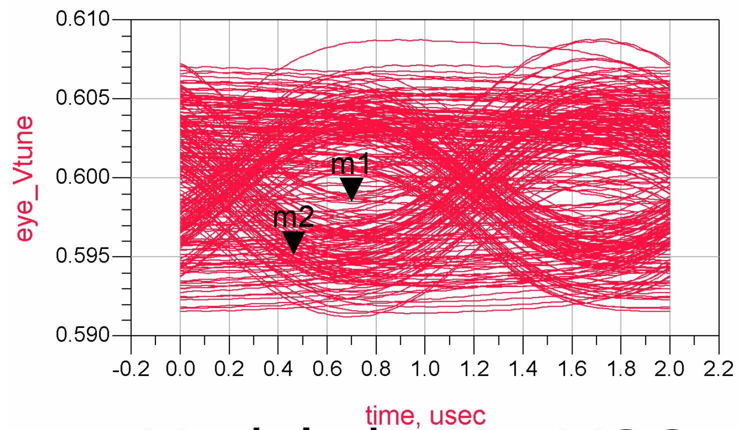
Modulation gain vs gain on VCO



Effect on eye Diagram

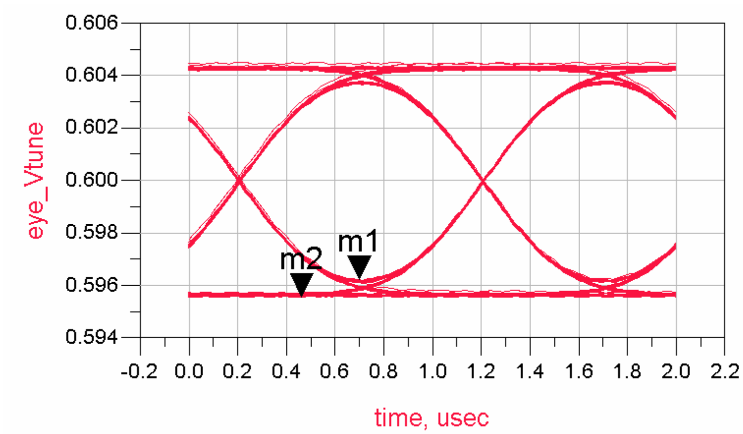


Modulation on divider only

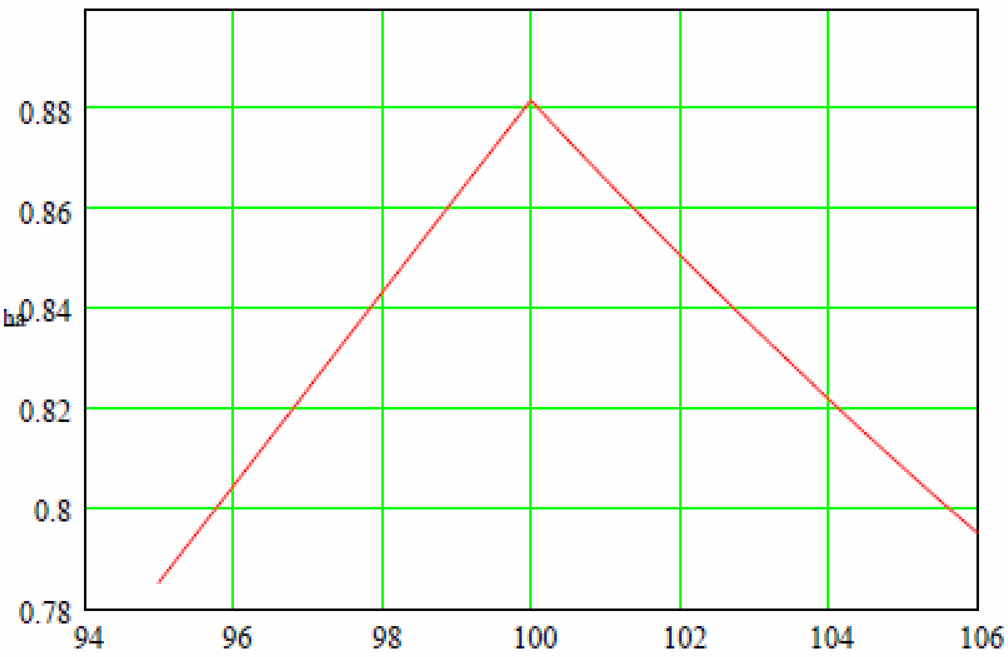


Modulation on VCO

Output PLL Modulation



Precision on VCO gain



- Precision on VCO gain degrades eye opening -> precision needed of 5 %
- Need to calibrate the VCO gain before each transmission in a new channel

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Research context

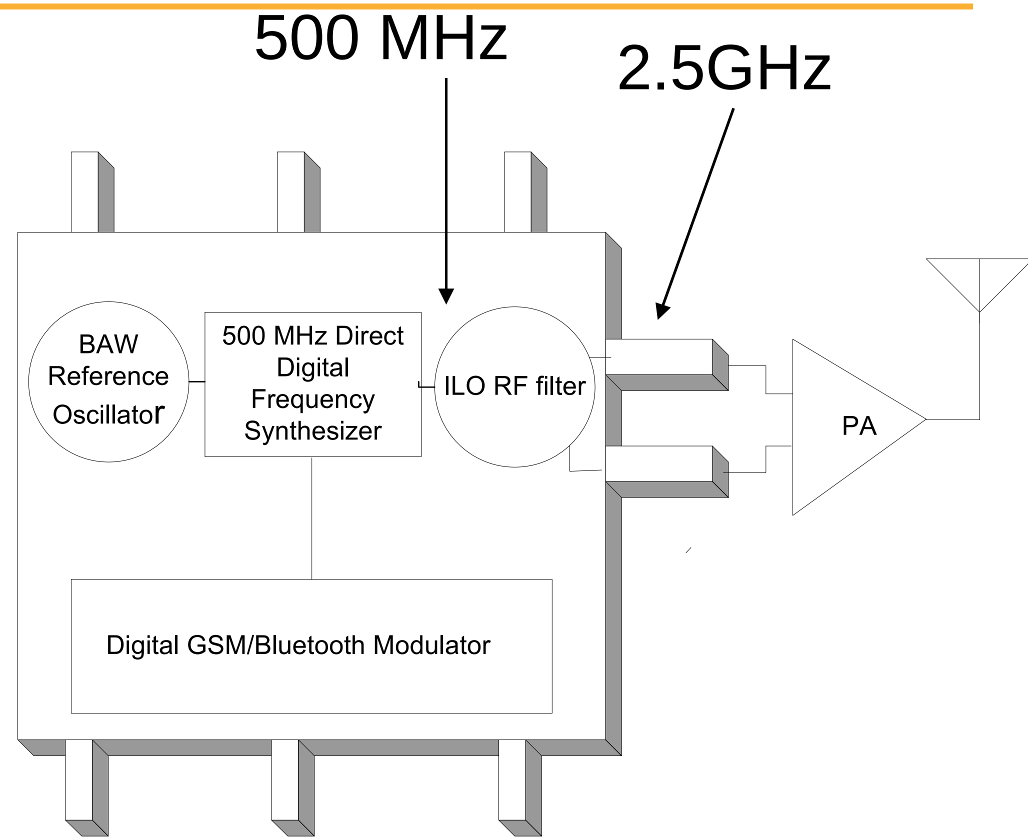
- Frequency synthesis and transmitter trend
  - All digital
  - Re-congirugability : going towards SDR: Software Defined Radio

- Try to be competitive with all digital PLL

- Applications: phase modulator to be able to be embedded in polar TX – Able to transmit constant phase envelop modulations (GSM, Bluetooth…)

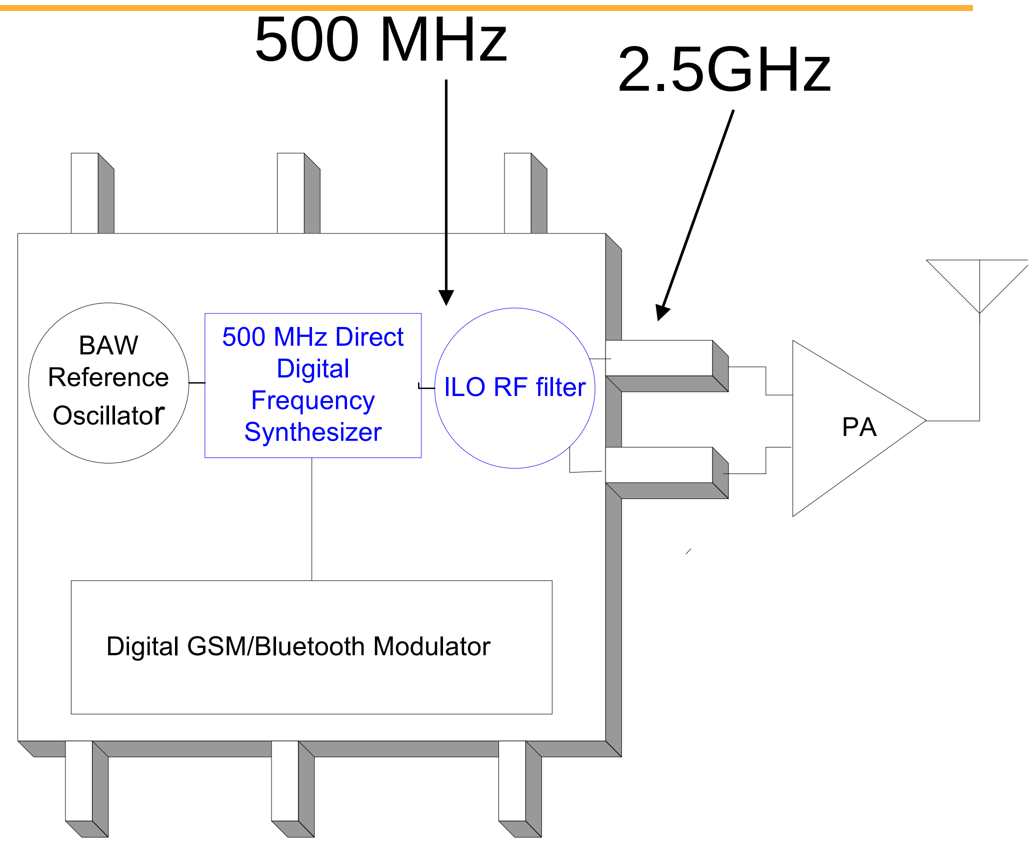
Proposed Architecture

- Fully Integrated Bluetooth transmitter:
  - Fully integrated Reference Oscillator (based on BAW oscillator for example)
  - RF – DDS generating 500 MHz signal
  - Injection Locked Oscillator as a frequency multiplier
- Advantages:
  - No feed Back Loop
  - Fully integrated
  - Could be quickly Powered on
  - Low phase group delay -> easy to handle within polar TX



Proposed Architecture

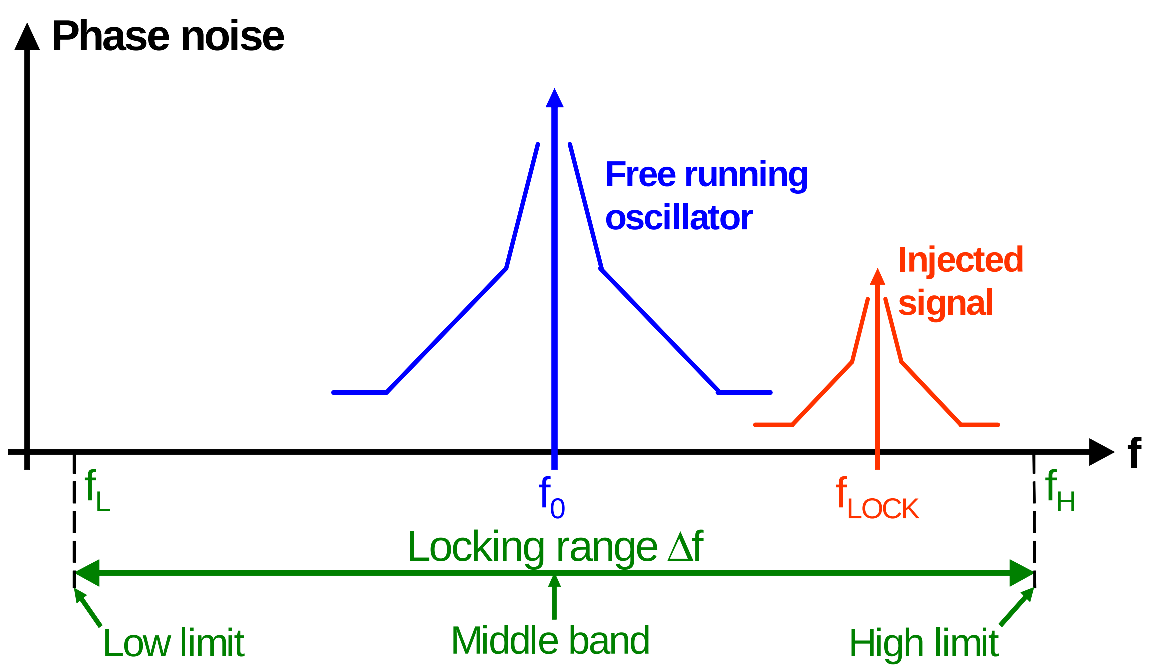
- Fully Integrated Bluetooth transmitter:
  - Fully integrated Reference Oscillator (based on BAW oscillator for example)
  - RF – DDS generating 500 MHz signal
  - Injection Locked Oscillator as a frequency multiplier
- Advantages:
  - No feed Back Loop
  - Fully integrated
  - Could be quickly Powered on
  - Low phase group delay -> easy to handle within polar TX

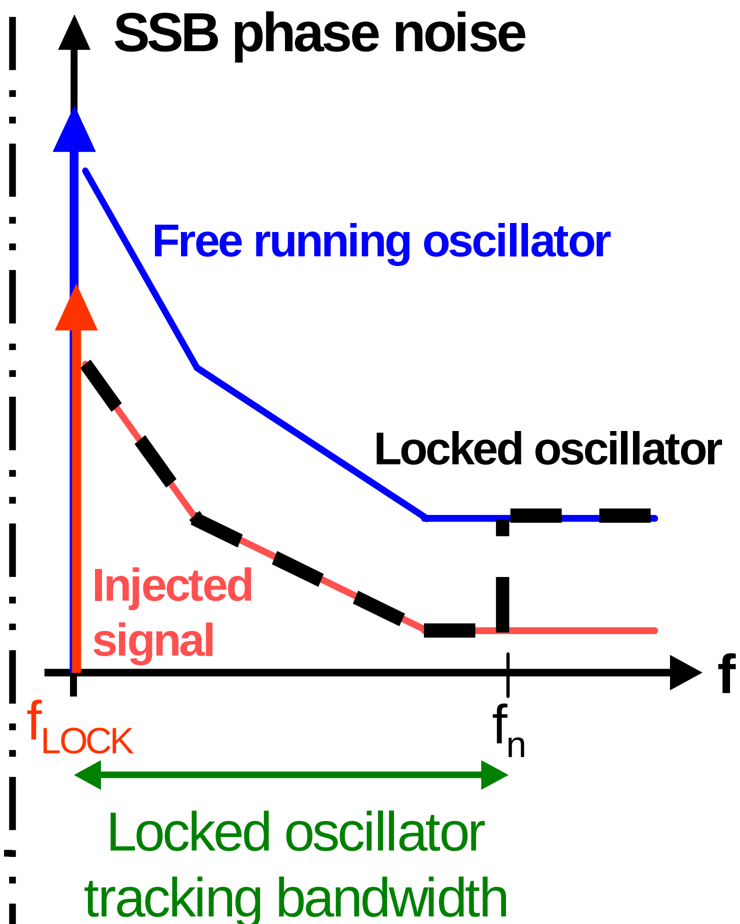


Outline

- Introduction
  - Transmitter integration challenges
- Frequency Synthesizer Modulation
  - Translationnal TX loop
  - Modulation of sigma delta frequency synthesizer
  - Two point modulation
- DDS and ILO based RF transmitter
  - Injection Locked Oscillator
  - 400 MHz DDS
  - Bluetooth DDS/ILO based transmitter

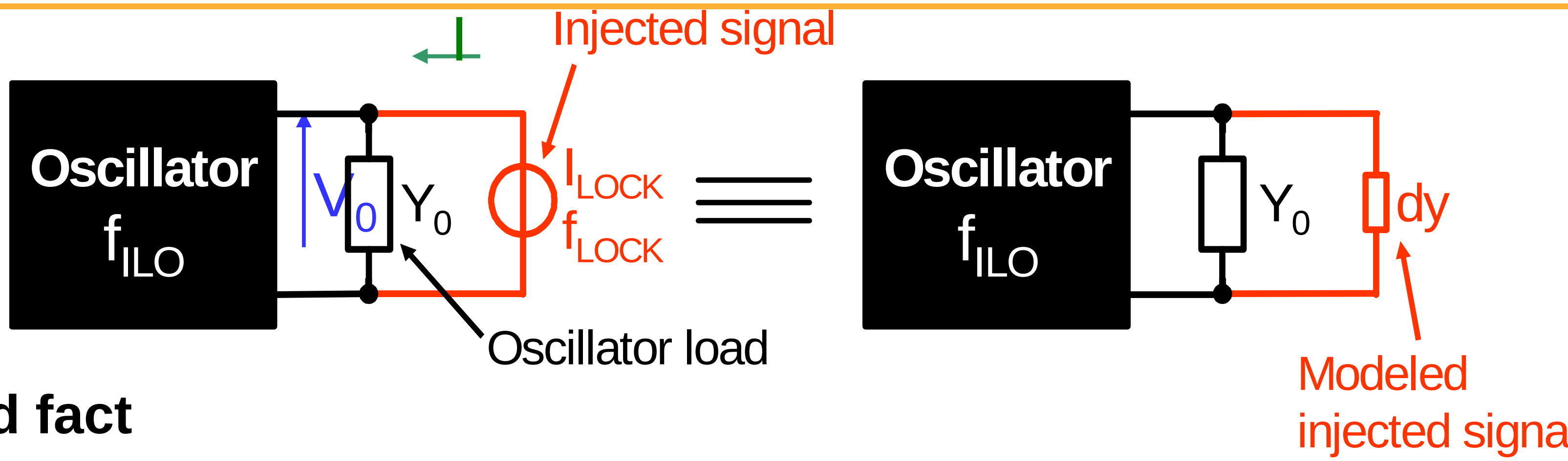
Injection Locking Phenomenon





Locked oscillator acts as a 1st order PLL

Injection Locking Theory (1) - Huntoon & Weiss (1947) (*)



Solid fact

- Oscillator frequency is function of admittance load Y_0 ➔ $f_{ILO} = fct(Y_0)$

$$E_F = \left.\frac{\partial f}{\partial Y}\right|_{Y=Y_0} = |E_F| \cdot e^{j.\beta}$$

Hypothesis

- Injected signal at f_{LOCK} in the vicinity of f_0
- I_{LOCK} magnitude small enough to not modify V_0 magnitude

Assumption

- Locking source modeled by a small load admittance variation dy

Injection Locking Theory (2) - Huntoon & Weiss (1947)

Huntoon & Weiss theory leads to:

ILO output phase

$$\frac{1}{2.\pi}\cdot\frac{d\phi}{dt}=(f_{LOCK}-f_0)-\frac{|E_F|.|I_{LOCK}|}{|V_0|}\cdot\cos(\phi+\beta)$$

$$\phi=\phi_{LOCK}-\phi_{ILO}$$

ILO locking range

$$\Delta f=2\cdot\frac{|E_F|\cdot|I_{LOCK}|}{|V_0|}$$

Constant depending on oscillator structure and locking process

ILO Modulation

- Modulated locking signal phase $\phi_{LOCK}(t) = 2.\pi.f_{LOCK}.t + m(t)$
- ILO output phase once locked $\phi_{ILO}(t) = 2.\pi.f_{LOCK}.t + n(t) - \phi_0$

$$\frac{1}{2.\pi}\cdot\frac{d\phi}{dt} = \left[\left(f_{LOCK} + \frac{1}{2\cdot\pi}\cdot\frac{dm(t)}{dt}\right) - f_0\right] - \frac{|E_F|.|I_{LOCK}|}{|V_0|}\cdot\cos(\phi+\beta)$$

$$\phi(t) = \phi_{SYNC}(t) - \phi_{ILO}(t) = m(t) - n(t) + \phi_0$$

- Assuming a small tracking phase error

$$\frac{1}{2\cdot\pi}\cdot\frac{dn(t)}{dt} = f_n\cdot[m(t) - n(t)]$$

Fourier Transform

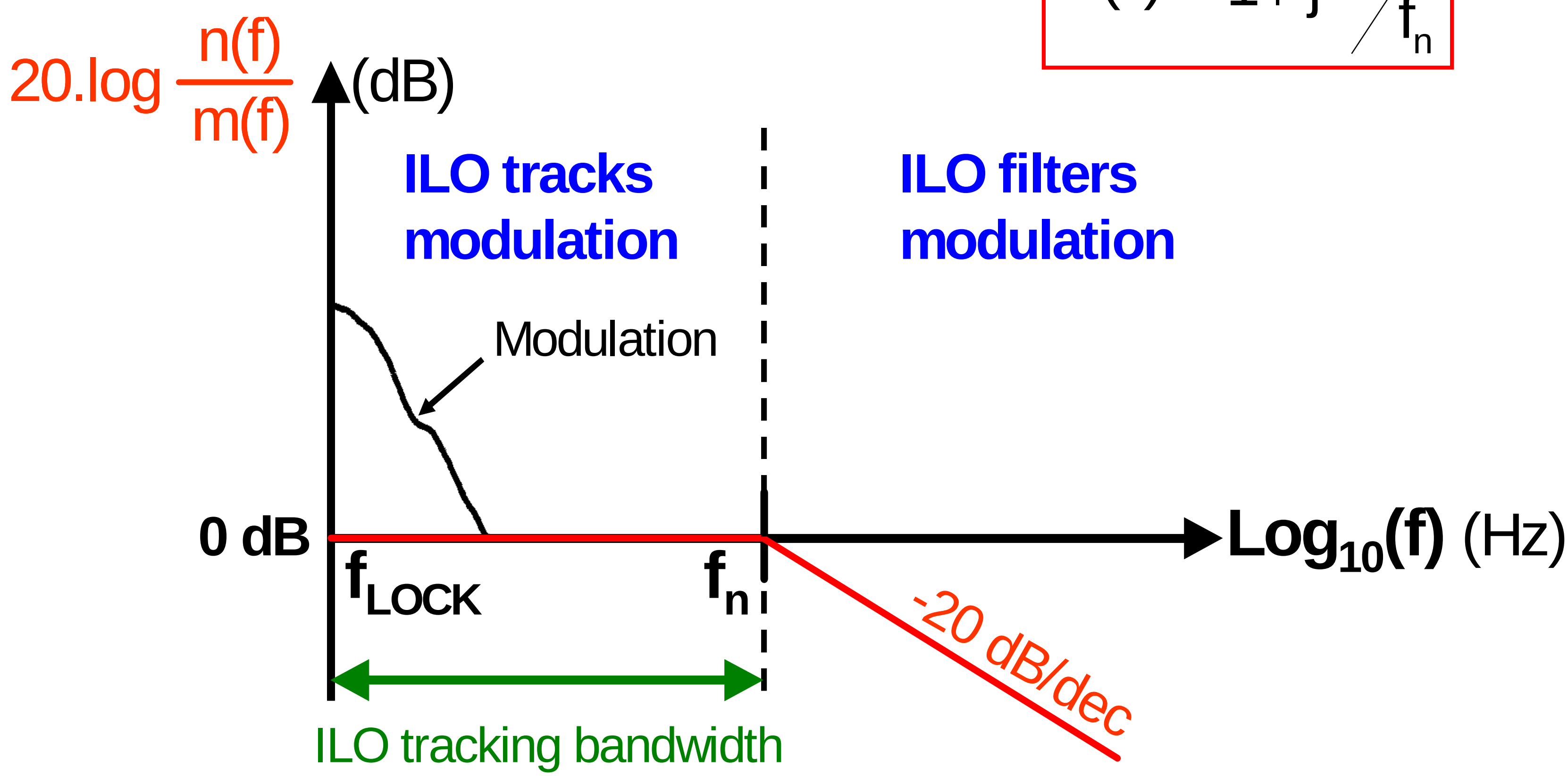
$$\frac{n(f)}{m(f)} = \frac{1}{1 + j\cdot {}^{f}\!/\!_{f_n}}$$

$$f_n = \sqrt{\frac{(\Delta f)^2}{4} - (f_{LOCK} - f_0)^2}$$

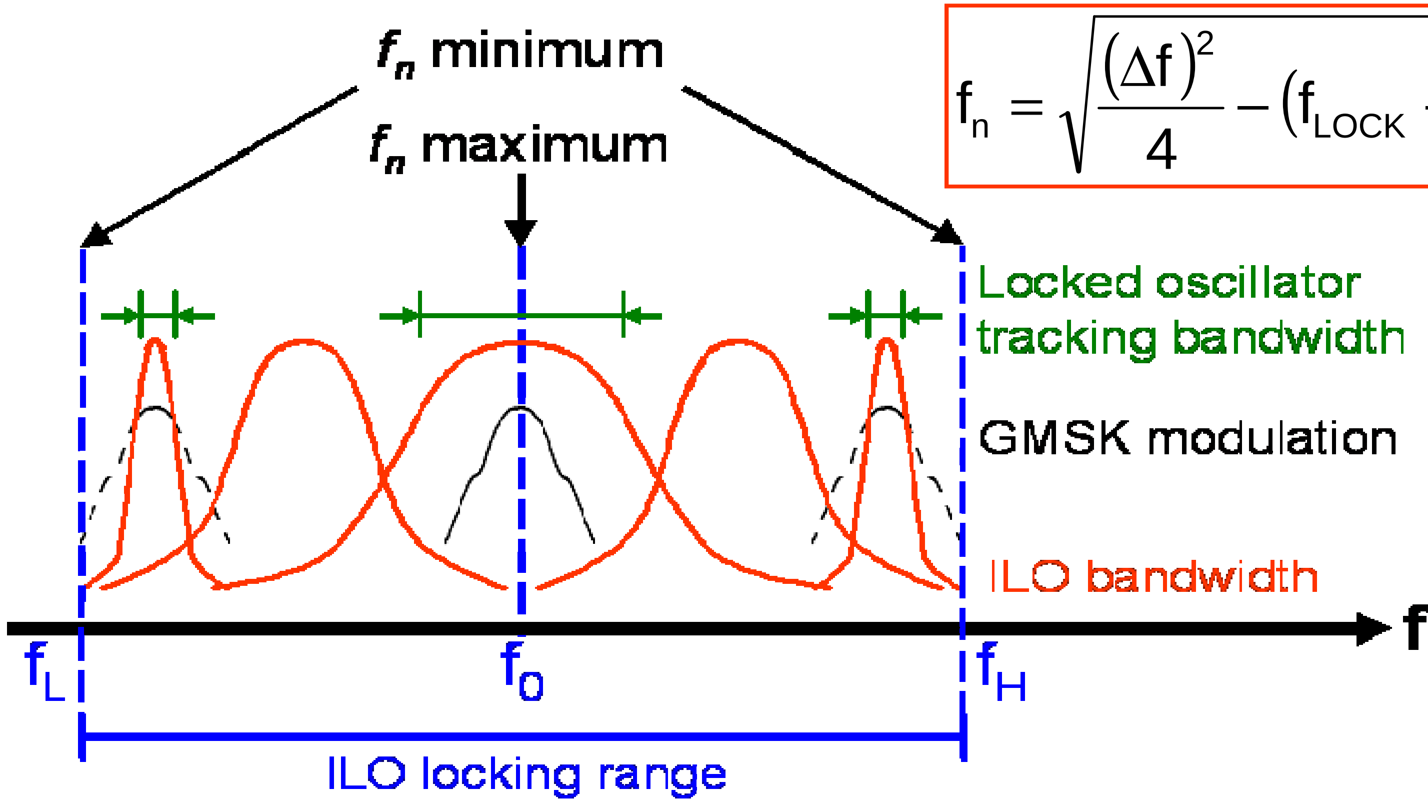
Tracking Phase Modulation

Ability to track phase modulation

$$\frac{n(f)}{m(f)} = \frac{1}{1 + j \cdot f/f_n}$$



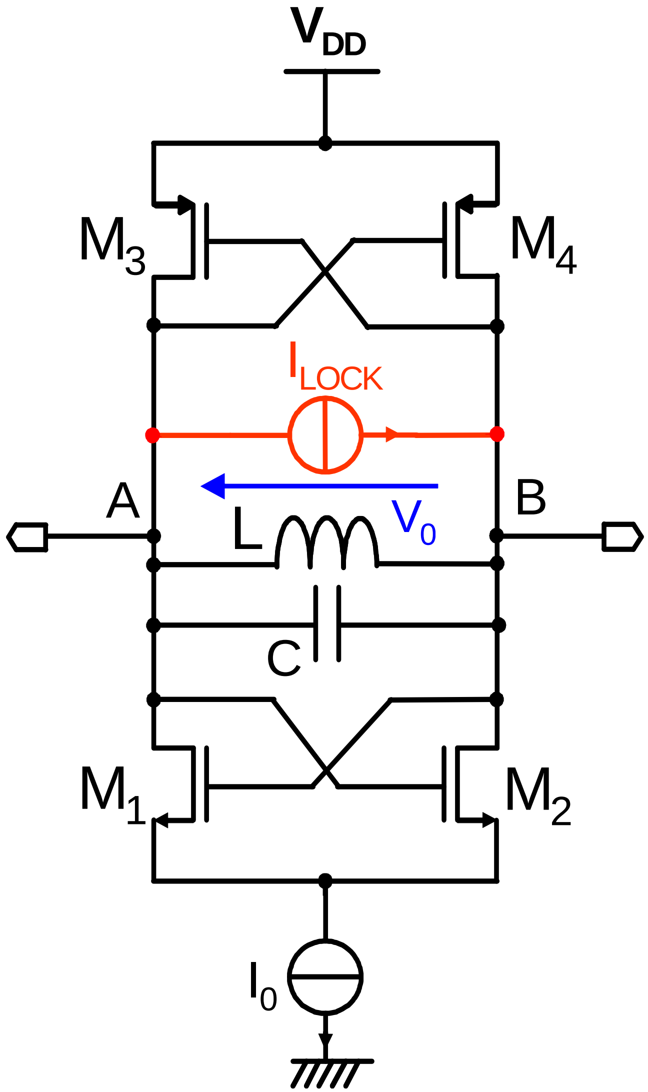
ILO Tracking Bandwidth



$$f_n = \sqrt{\frac{(\Delta f)^2}{4} - (f_{LOCK} - f_0)^2}$$

- Tracking bandwidth depends on the difference between the Injected signal frequency and the ILO free running frequency

2-GHz Injection Locked Oscillator Design



$$\Delta f = 2 \cdot \frac{I_{LOCK}}{V_0} \cdot \frac{1}{4 \cdot \pi \cdot C_{AB}}$$

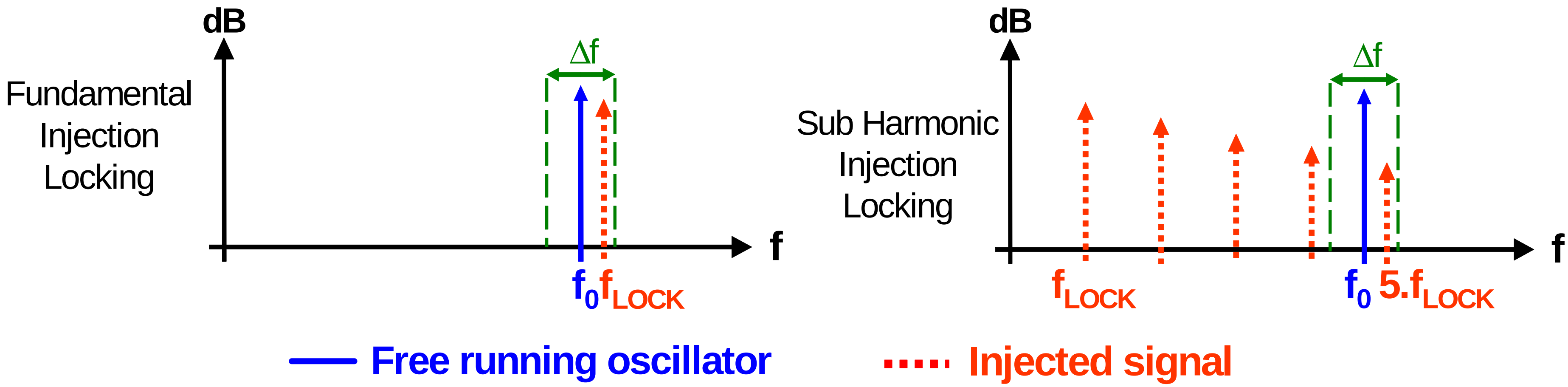
E_F

$C_{AB} = C + C_{M1} + C_{M2} + C_{PARASITIC}$

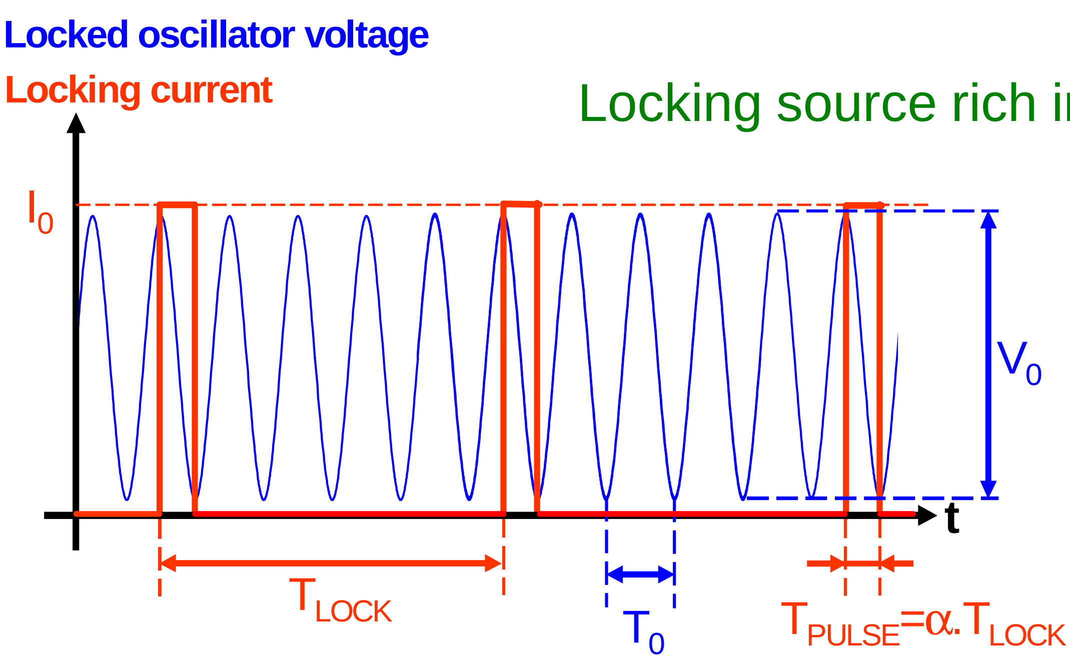
Δf parameters known

➔ **Optimized design possible**

Injection Locking by a Sub-harmonic

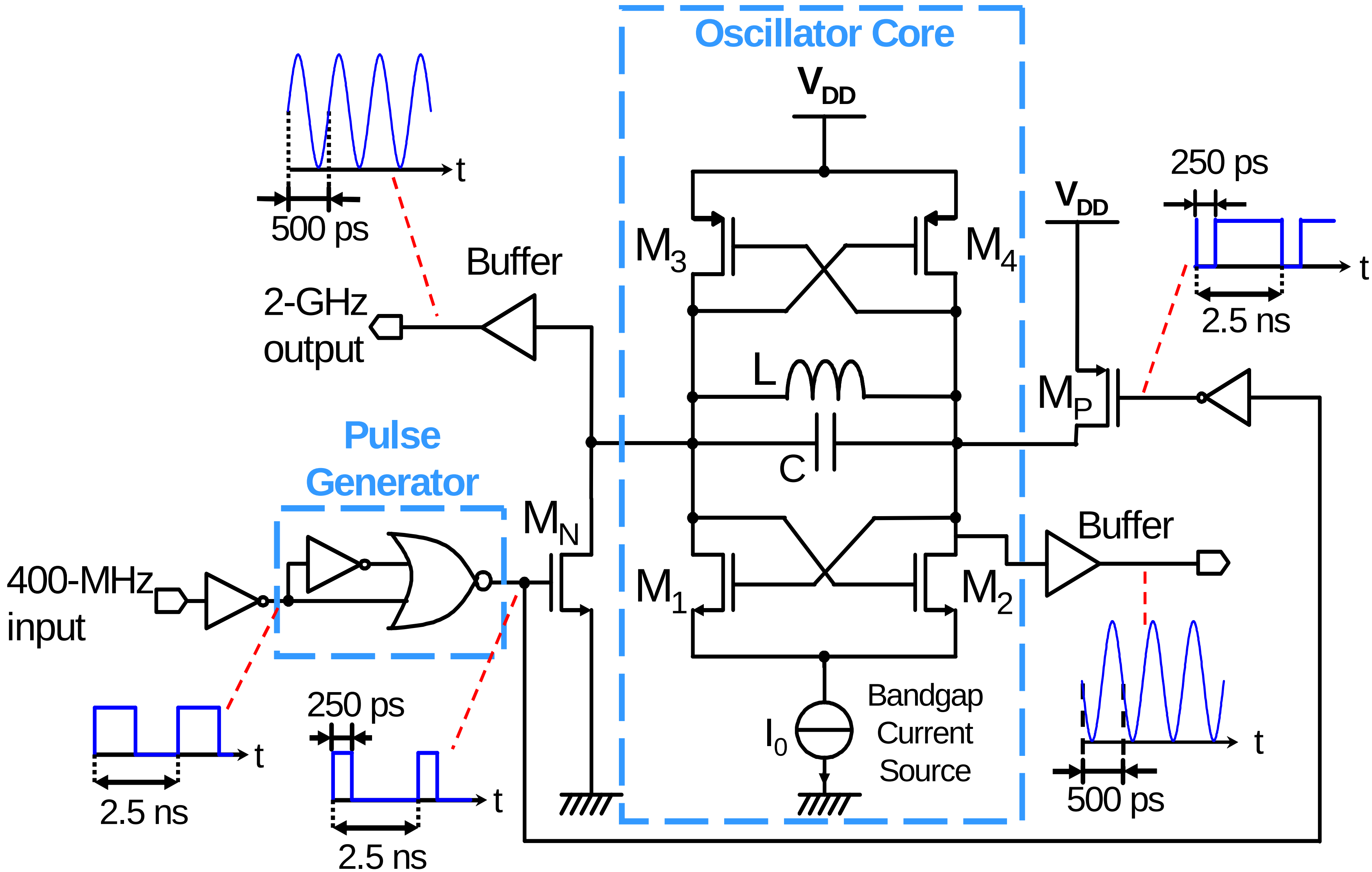


Locking source rich in n[th] harmonic

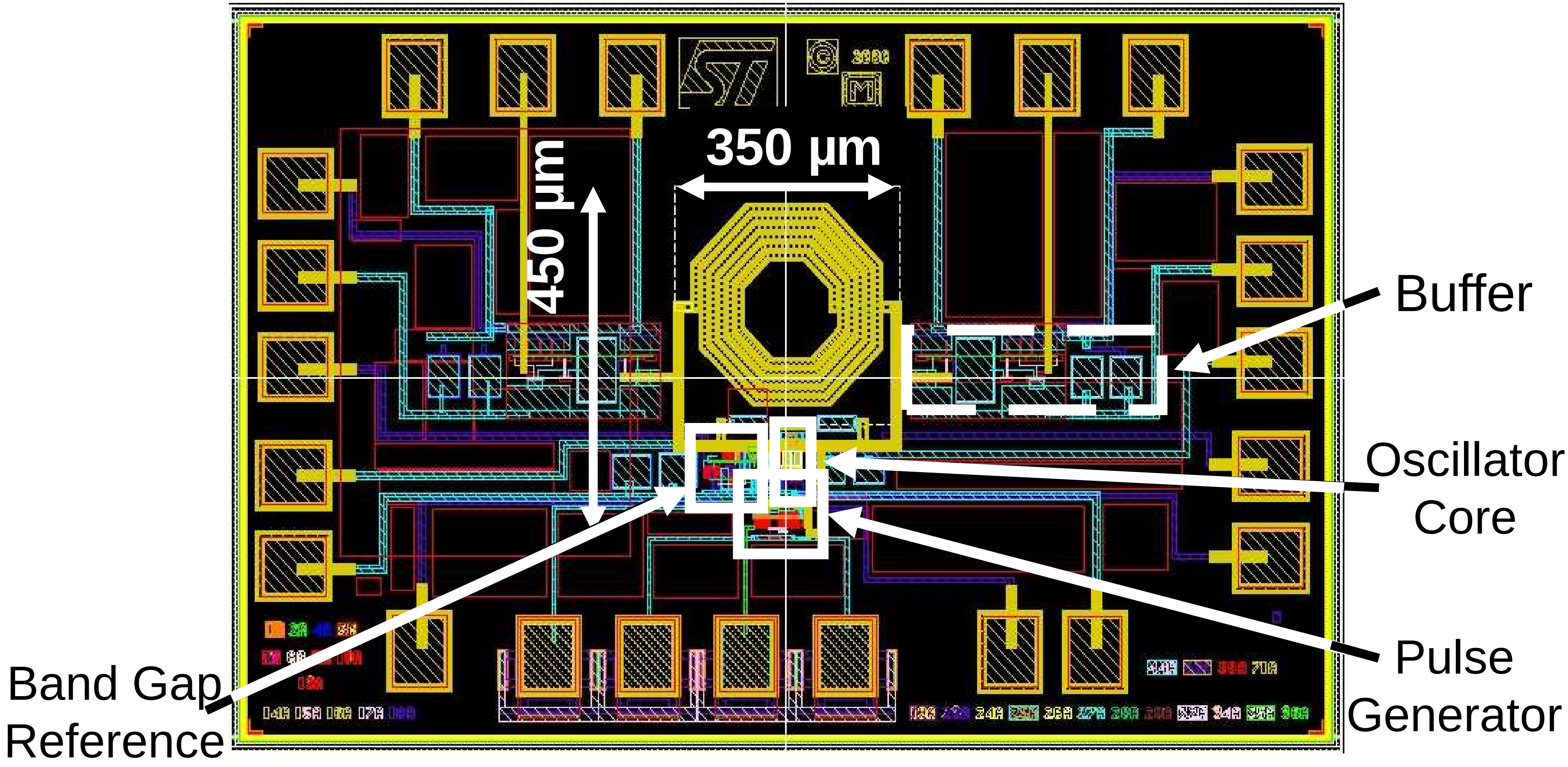


$$I_N = I_{LOCK} = \frac{2.I_0}{n.\pi}$$

2-GHz Fifth SbILO Schematic



2-GHz Fifth SbILO layout

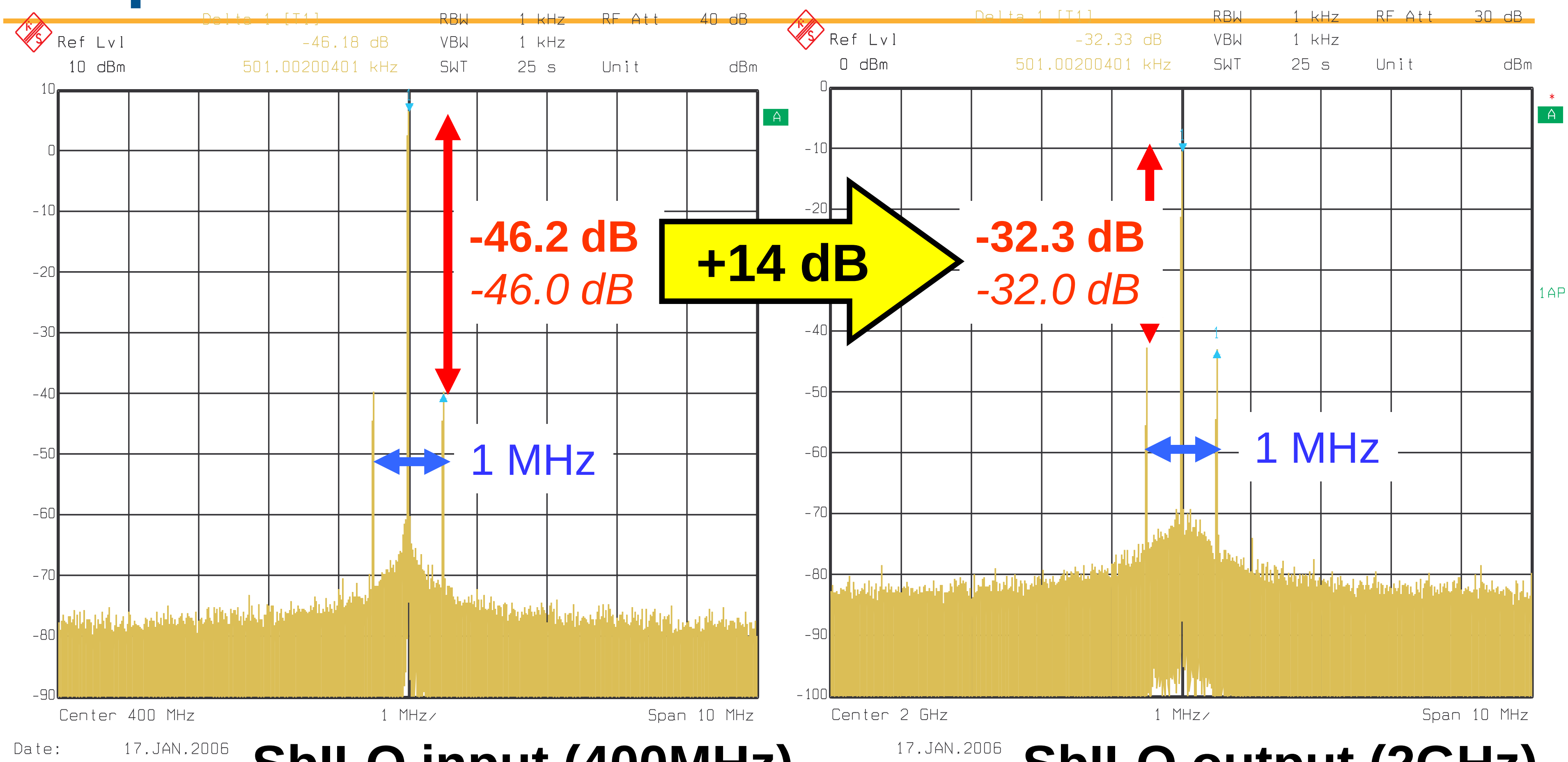


0.35-µm BiCMOS STMicroelectronics technology

Design Summary

<table>
<tr><th colspan="2">PARAMETER</th><th>VALUE</th></tr>
<tr><td colspan="2">Technology</td><td>0.35-µm BiCMOS STMicroelectronics</td></tr>
<tr><td colspan="2">Voltage Supply</td><td>2.5 V</td></tr>
<tr><td colspan="2">Current Consumption</td><td>16 mA</td></tr>
<tr><td rowspan="2">Current Consumption</td><td>Output Buffers</td><td>15 mA</td></tr>
<tr><td>ILO Core
+ Pulse Generator
+ Bandgap Current Source</td><td>1 mA</td></tr>
<tr><td colspan="2">Locking Range</td><td>400 MHz</td></tr>
<tr><td colspan="2">Center Frequency</td><td>2 GHz</td></tr>
<tr><td colspan="2">Chip Area (w/o pads and buffers)</td><td>0.160 mm^2</td></tr>
</table>

Spectrum Measurements



SbILO input (400MHz) — *10-mrad phase deviation*

SbILO output (2GHz) — *50-mrad phase deviatio*

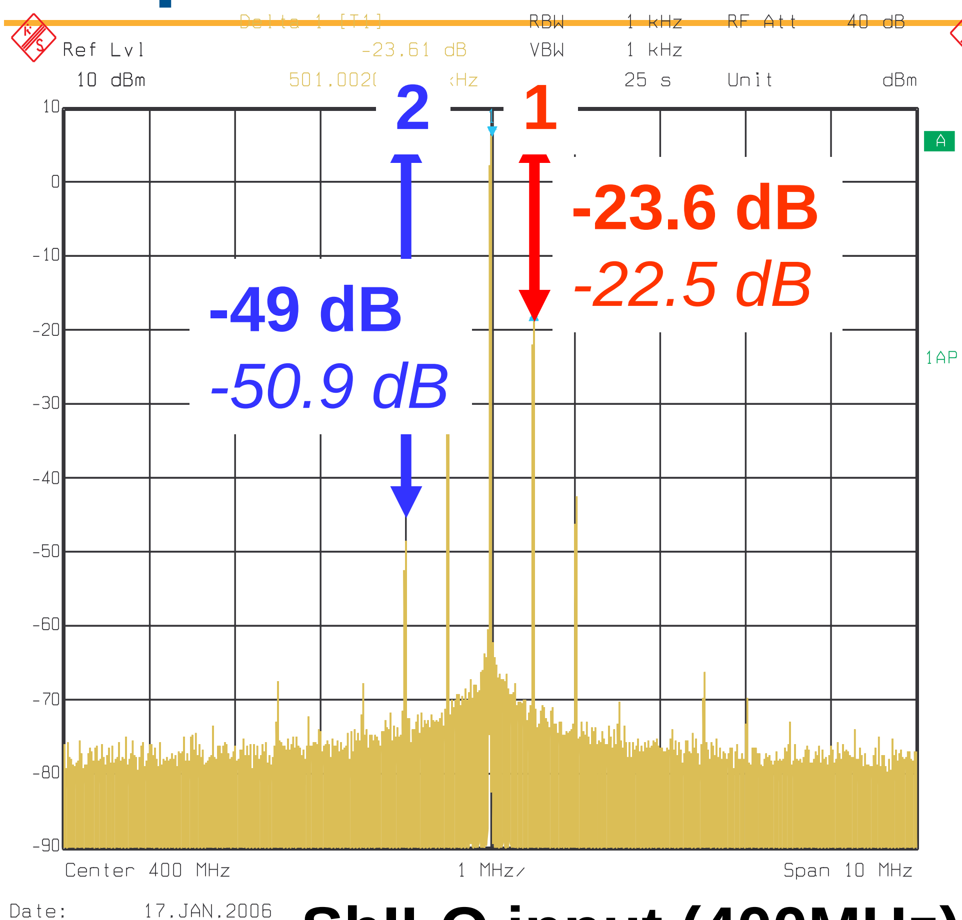
-46.2 dB Measurement result

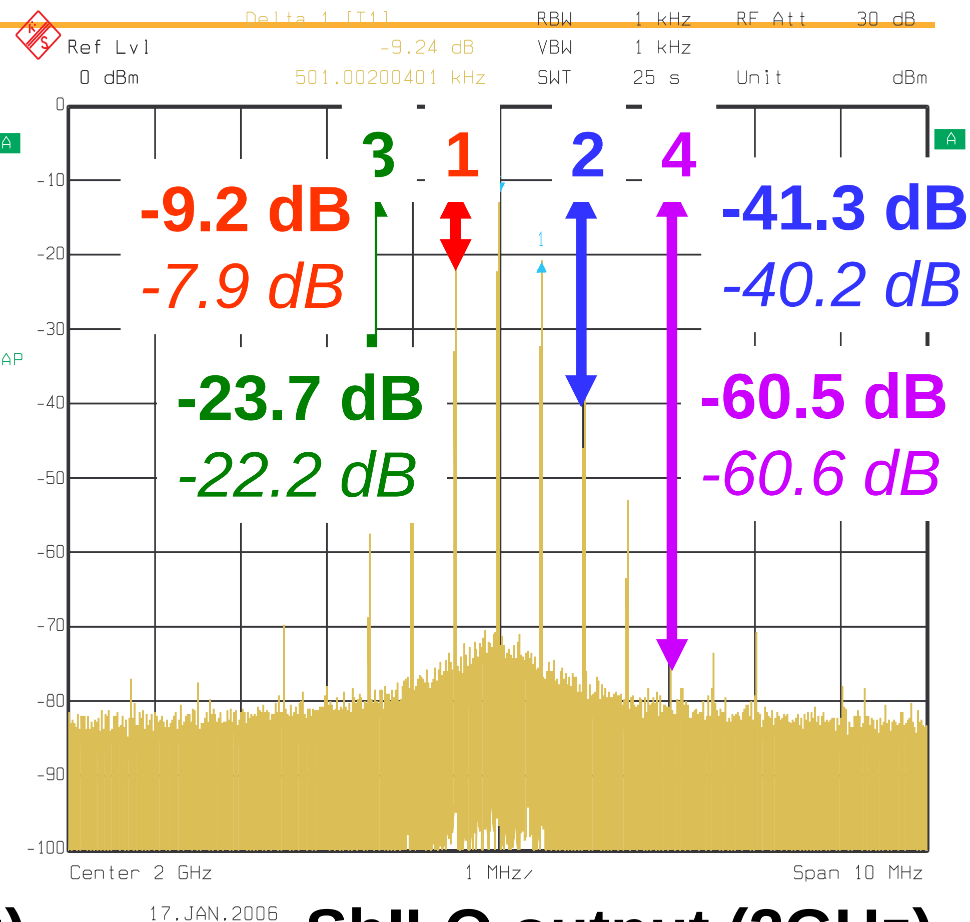
-46.0 dB Bessel function of the first kind

$S(t)=A.\cos[n.\omega_C.t+n.\Phi(t)] \approx A.\cos(n.\omega_C.t) - A.n.\Phi(t).\sin(n.\omega_C.t)$

Phase multiplied by 5 ➔ **$20.\log_{10}(5)$ = 14 dB**

Spectrum Measurements





SbILO input (400MHz) — *150-mrad phase deviation*

SbILO output (2GHz) — *750-mrad phase deviati*

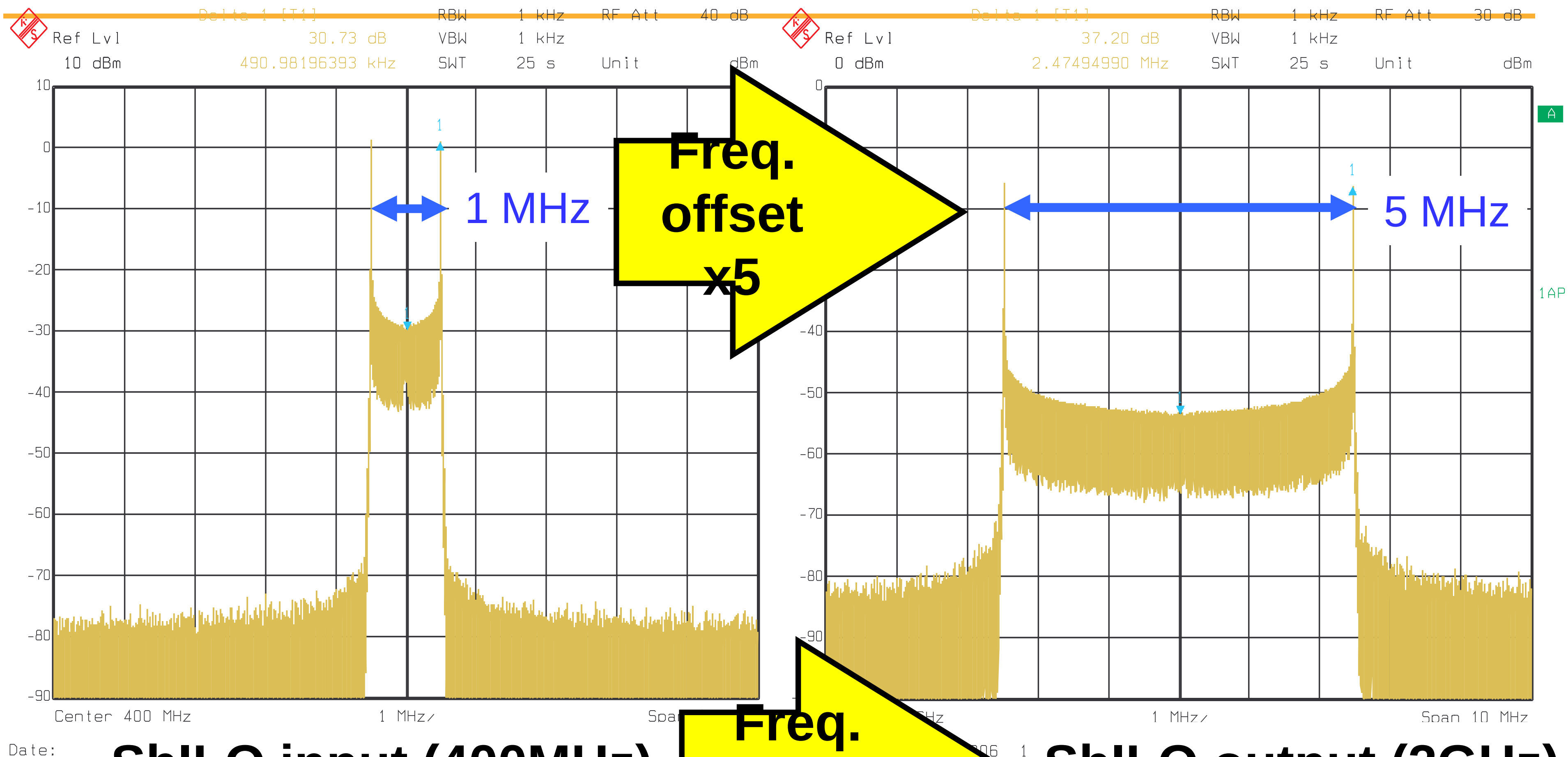
-46.2 dB Measurement result

-46.0 dB Bessel function of he first kind

Large phase deviation requires Bessel functions

Phase deviation has to be multiplied by

Spectrum Measurements



SbILO input (400MHz)

500-kHz frequency deviation

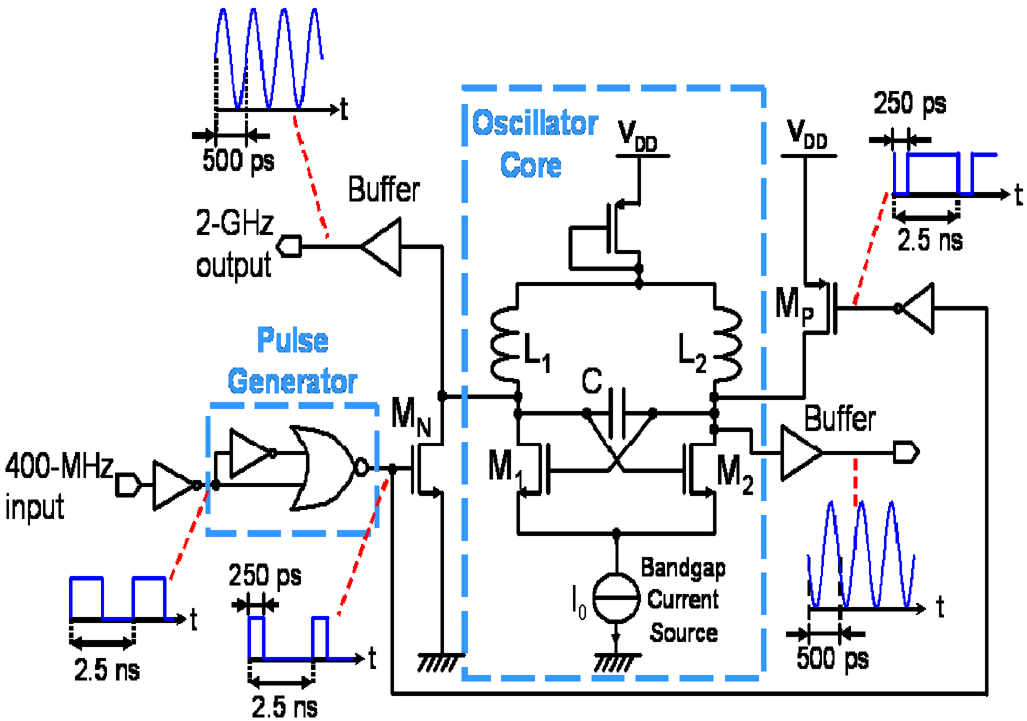
SbILO output (2GHz)

2.5-MHz frequency deviation

Frequency deviation widen spectrum by a ratio 5

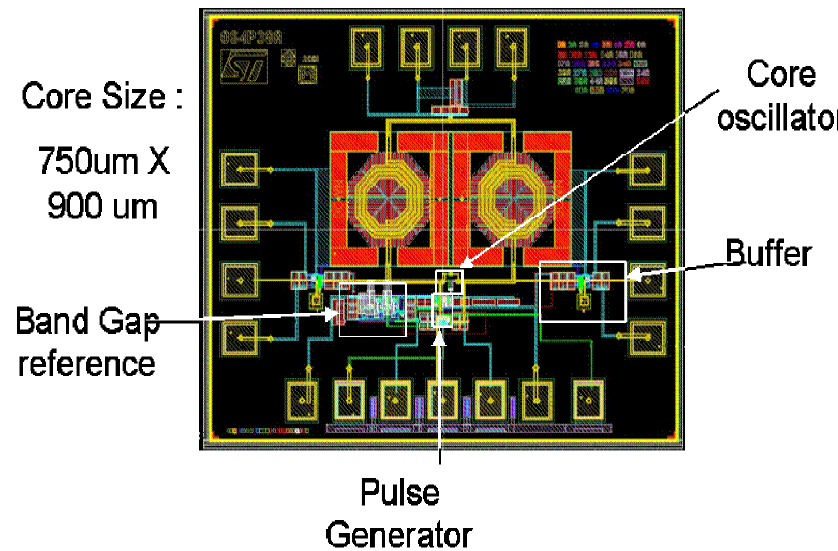
Carrier and offset between carrier and spurious are multiplied by 5 at ILO output

ILO : Proof of Concept (1)



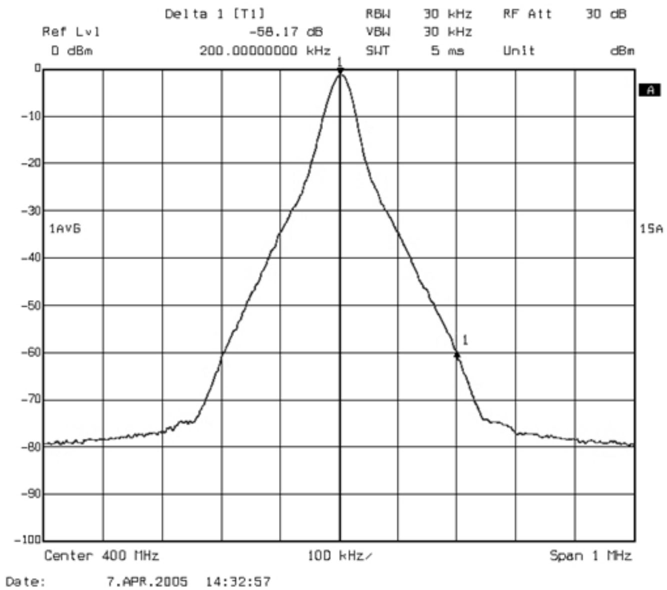
Core Size :

750um X 900 um

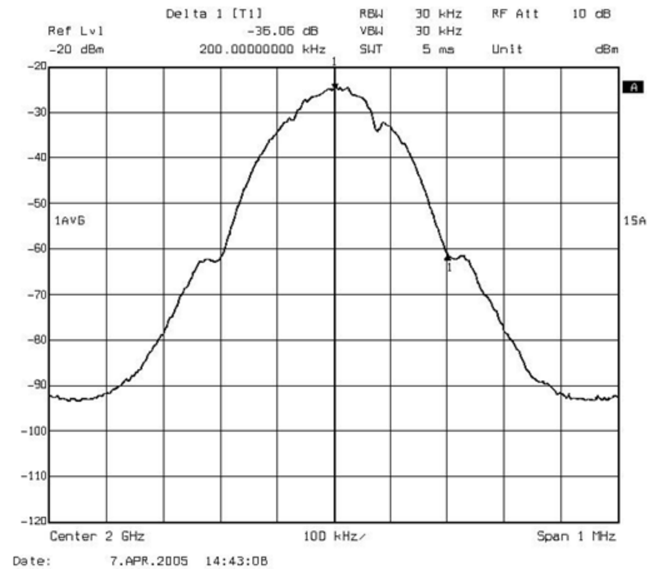


- ILO designed in BiCMOS6 as a multiplier by 5

ILO : Proof of Concept (2)



ILO input



ILO output

TEST	**MAXIMUM VALUES REQUIRED**	**SBILO INPUT**	**SBILO OUTPUT**
Phase Error (° rms)	5	0.22	0.26
Phase Error (° Peak)	20	0.83	0.85

Conclusion ILO

- A theory on ILO modulation has been proposed
- A fifth sub-harmonic injection locked oscillator designed
  - Wide locking range: **400 MHz**
  - Center frequency: **2 GHz**
- Spectrum at SbILO output can be predicted for
  - Low phase deviation with Bessel function or Taylor development
  - Large phase deviation with Bessel function of the first kind
  - Frequency deviation thanks to the ILO multiplication ratio
- Phase error introduced by ILO once modulated negligeable

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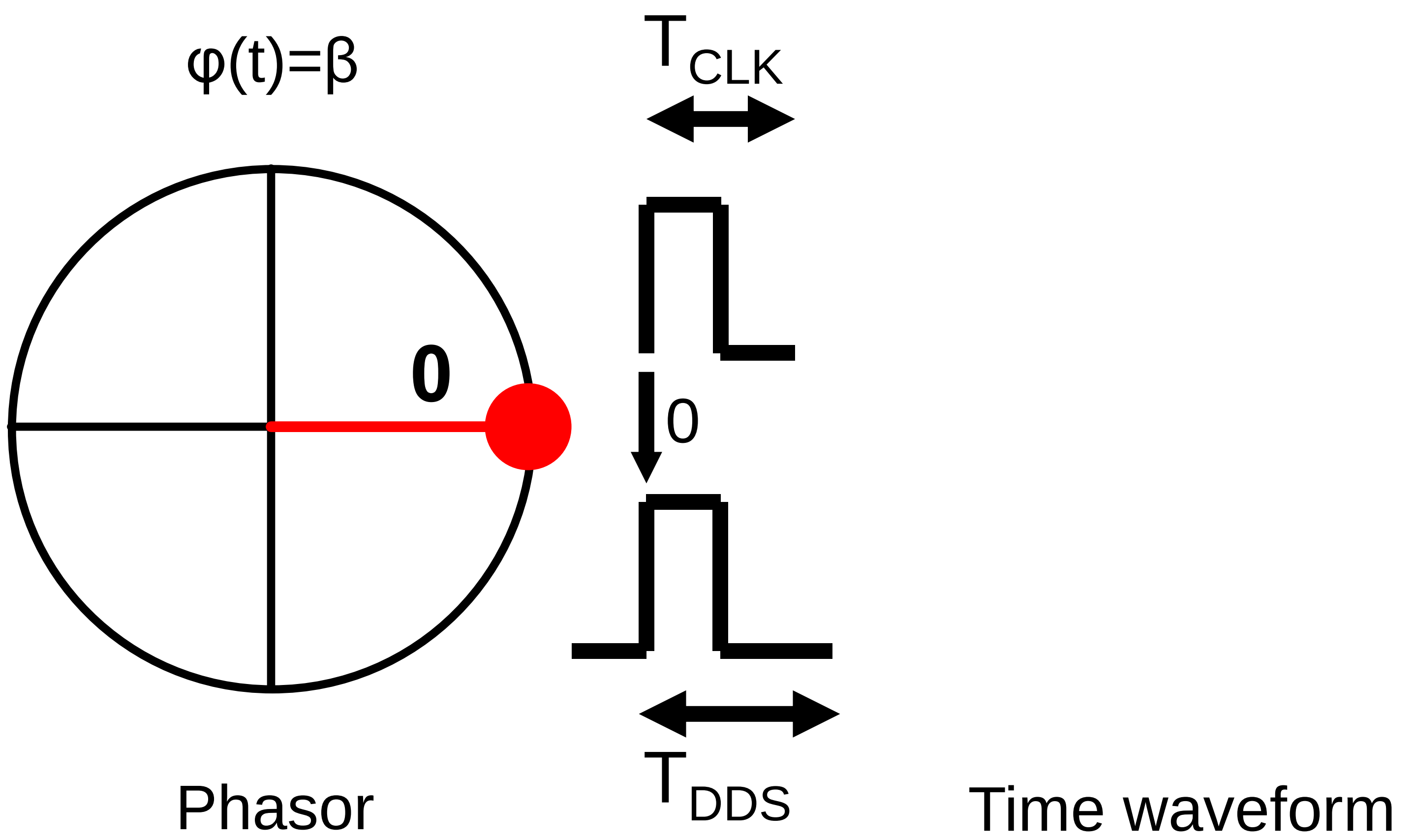
400 MHz DDS Principle (1)

$$V_{RF}(t) = A\cos(\omega_1 t) = A\cos(\omega_0 t + \omega_1 t) = A\cos(\omega_0 t + \varphi(t))$$

$$\varphi(t) = 2\pi f_1 t$$

- Frequency synthesis could be seen as a phase modulation, where the modulated phase is a ramp.
- The slope of the ramp is related to the frequency step
- Frequency synthesizer composed of
  - An RF clock
  - A phase shifter that increments a value at each rising edge of the clock

400 MHz DDS Principle (2)



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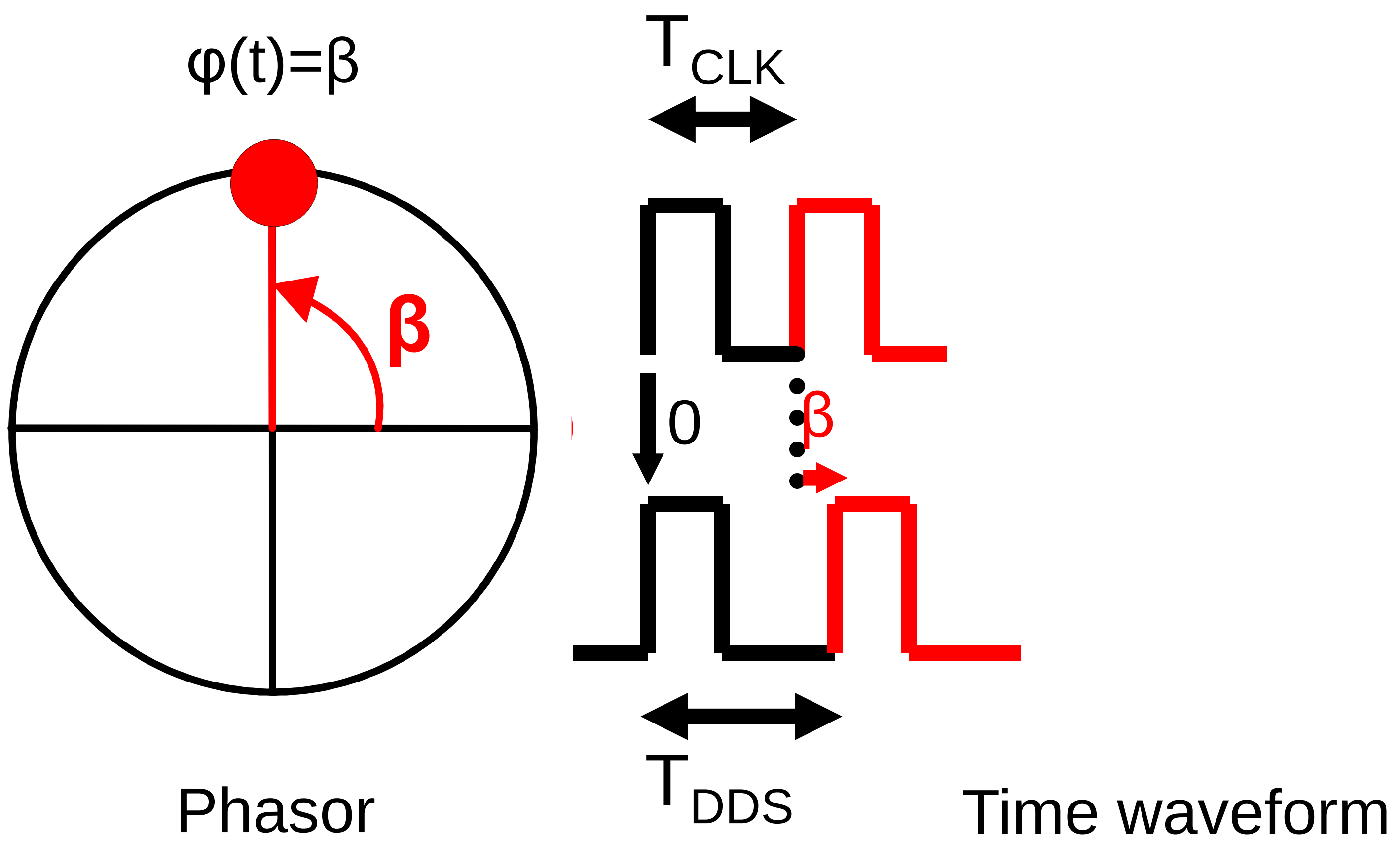
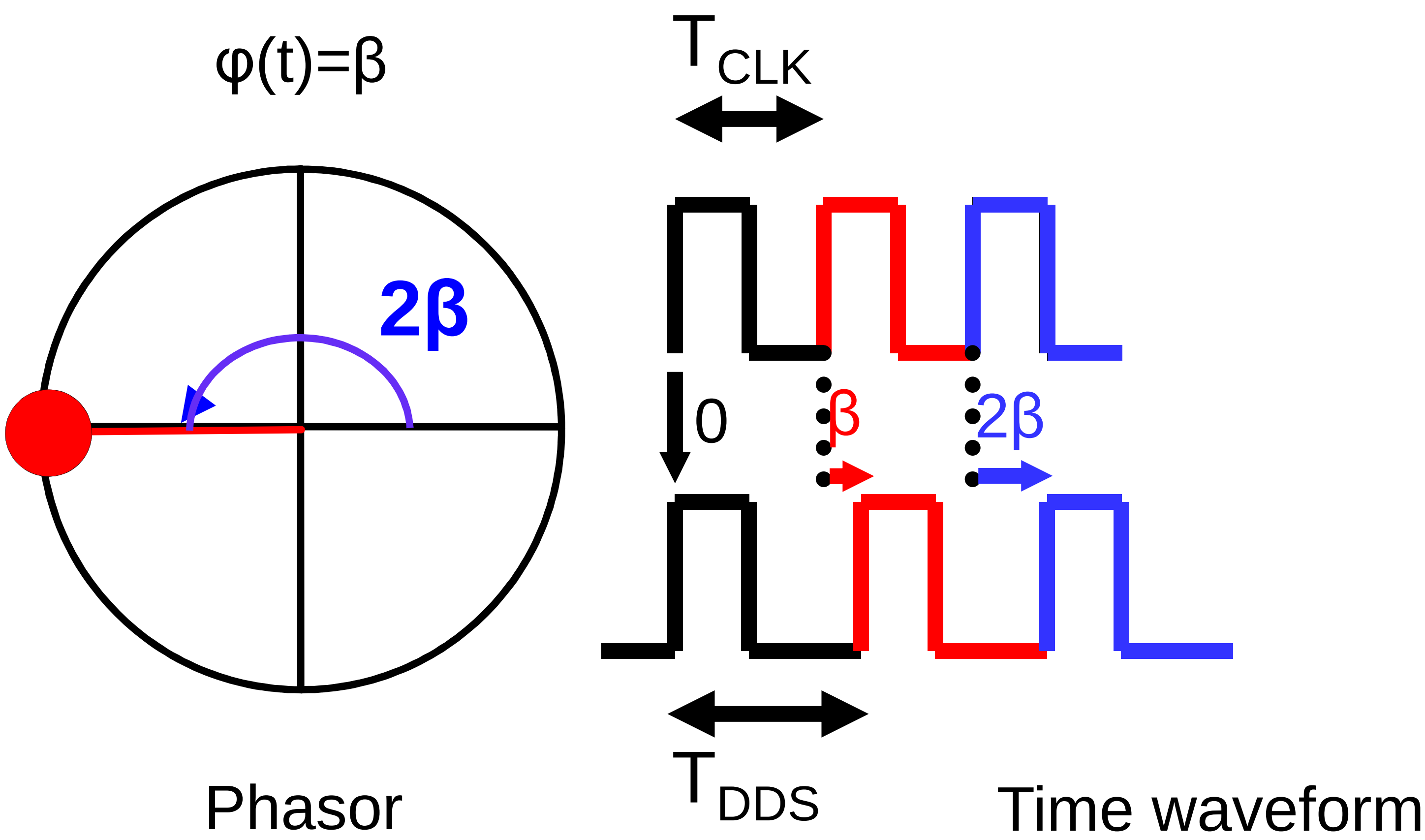
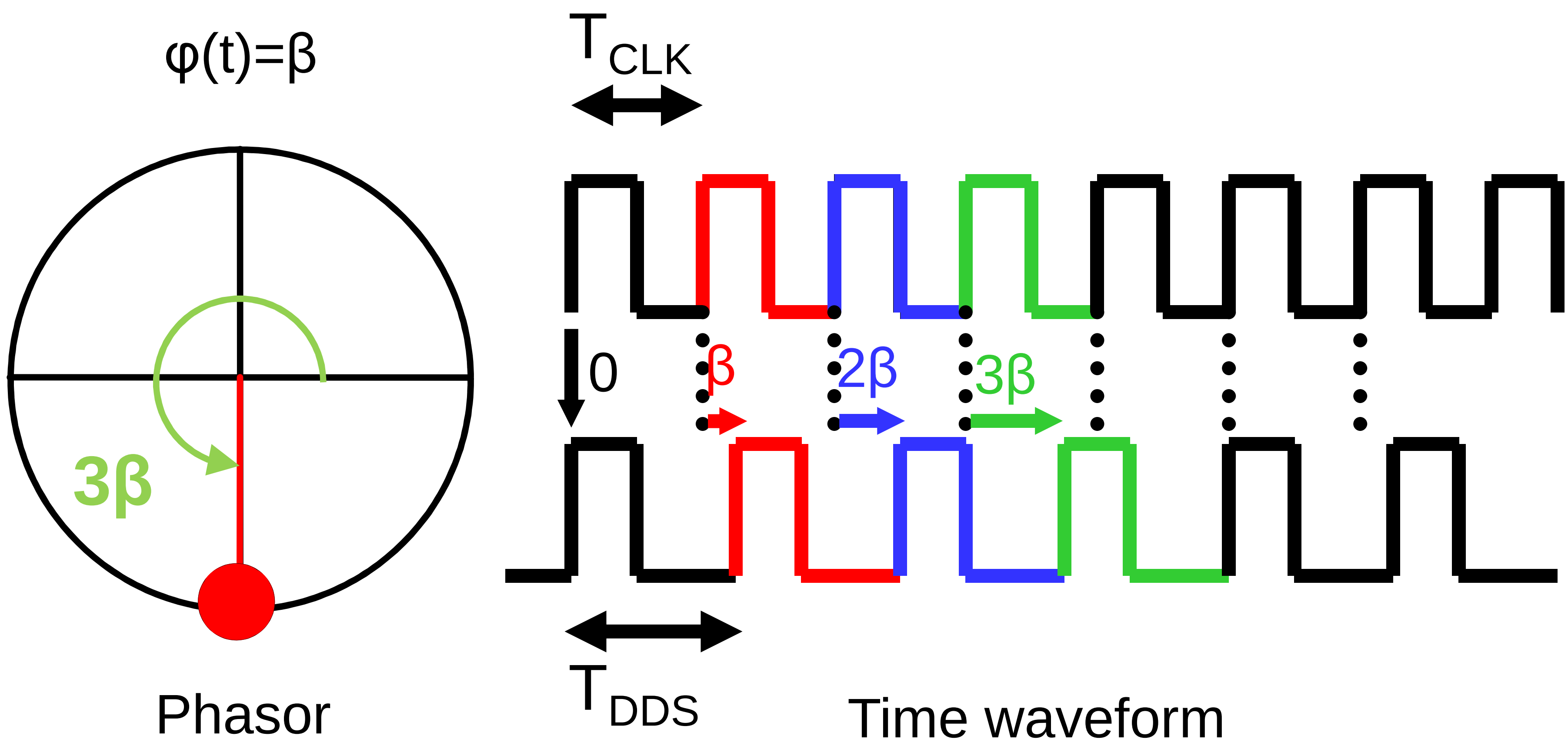


400 MHz DDS Principle (2)



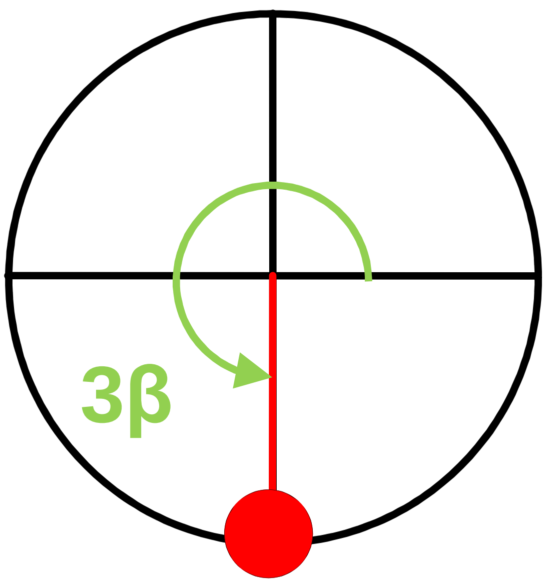
400 MHz DDS Principle (2)



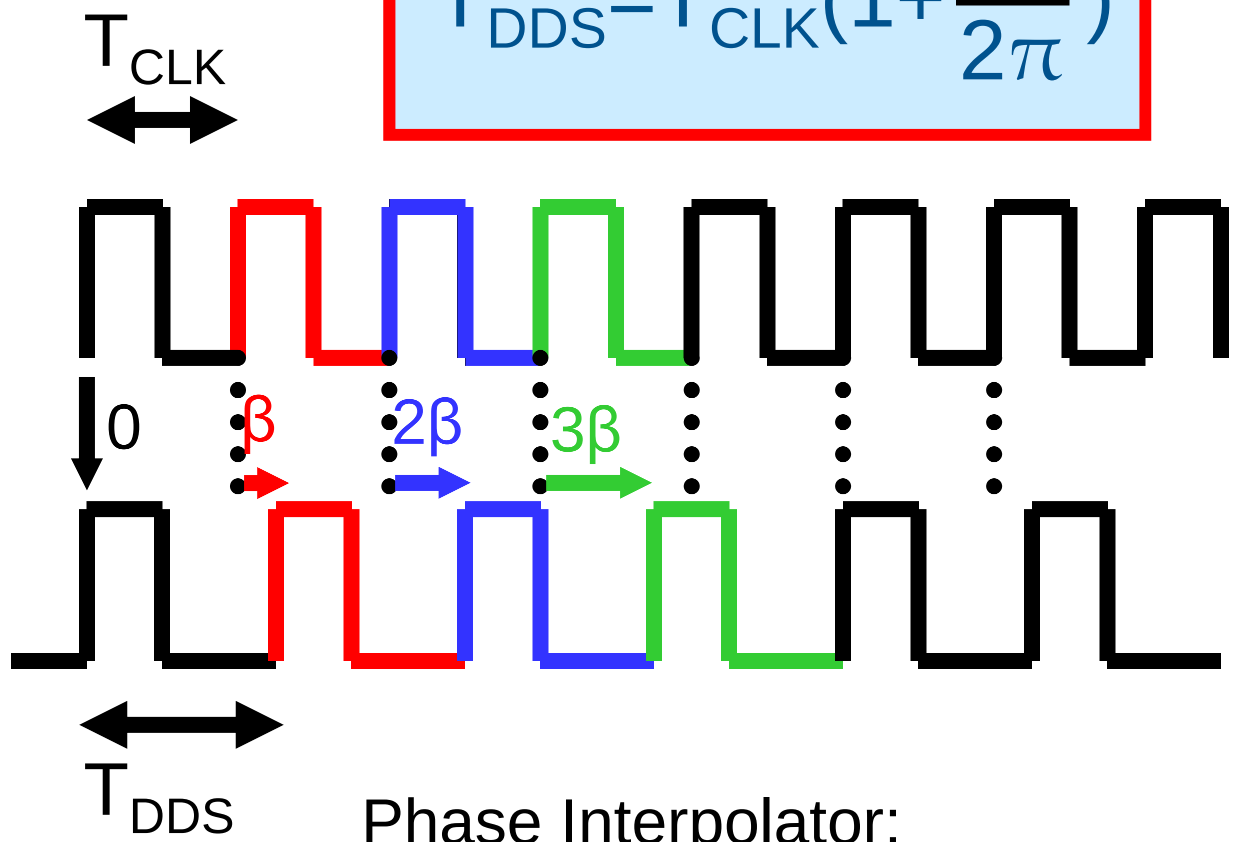
400 MHz DDS Principle (2)

$$T_{DDS}=T_{CLK}\left(1+\frac{\beta}{2\pi}\right)$$

$\varphi(t)=\beta$

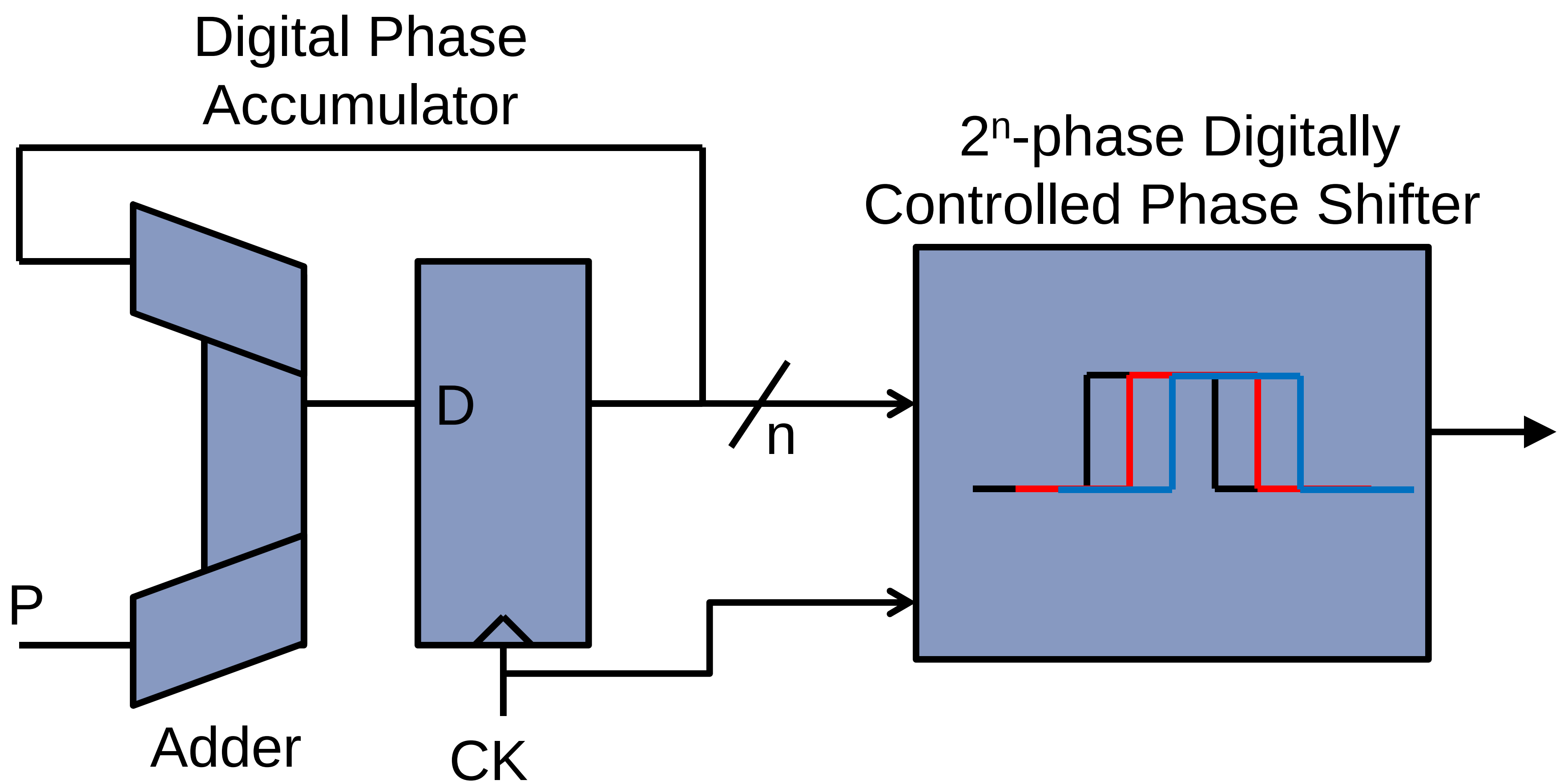


Phase Accumulator:
Digital context



Phase Interpolator:
Analog Context

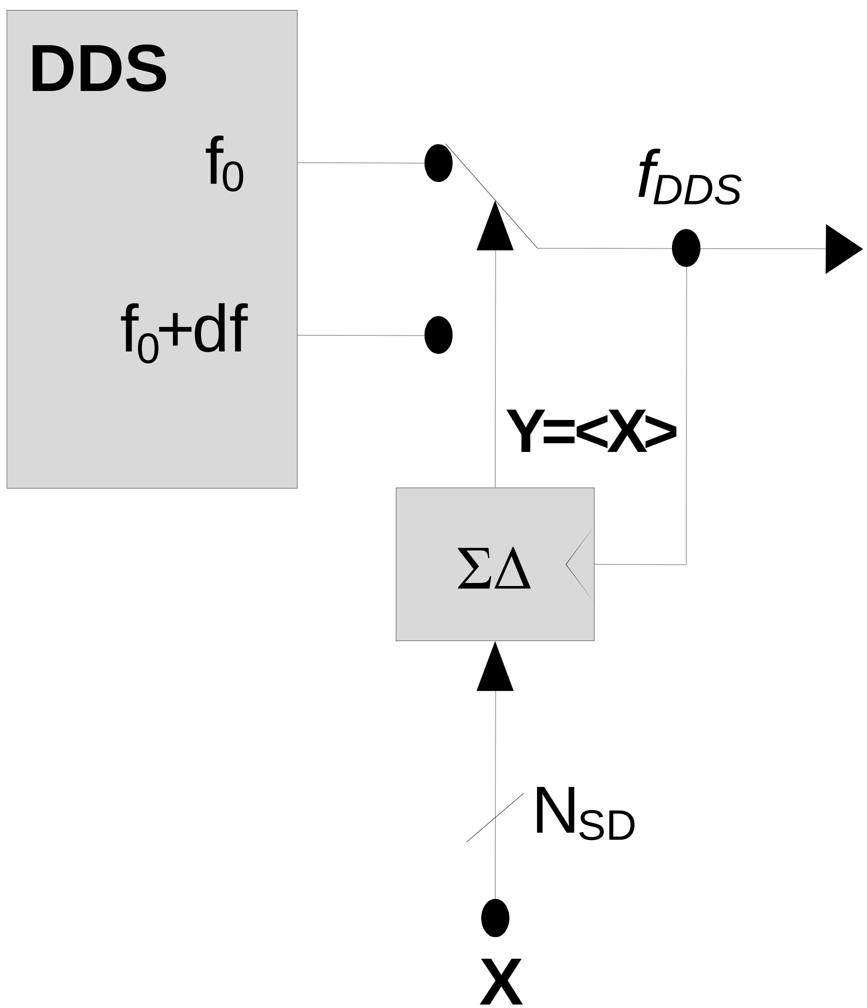
400 MHz DDS architecture (1)



400 MHz DDS architecture (2)

- Advantages
  - ROM less
  - High frequency (classical implementation output frequency restricted to Fclock/2 at least)
- Drawbacks
  - Step frequency limited by the resolution of the digitally controlled phase shifter
  - Spurious response depends on the phase accuracy

Decreasing Step Frequency



- ΣΔ modulator is used to decrease the step of the DDS by switching ramdomly between two coarse frequencies

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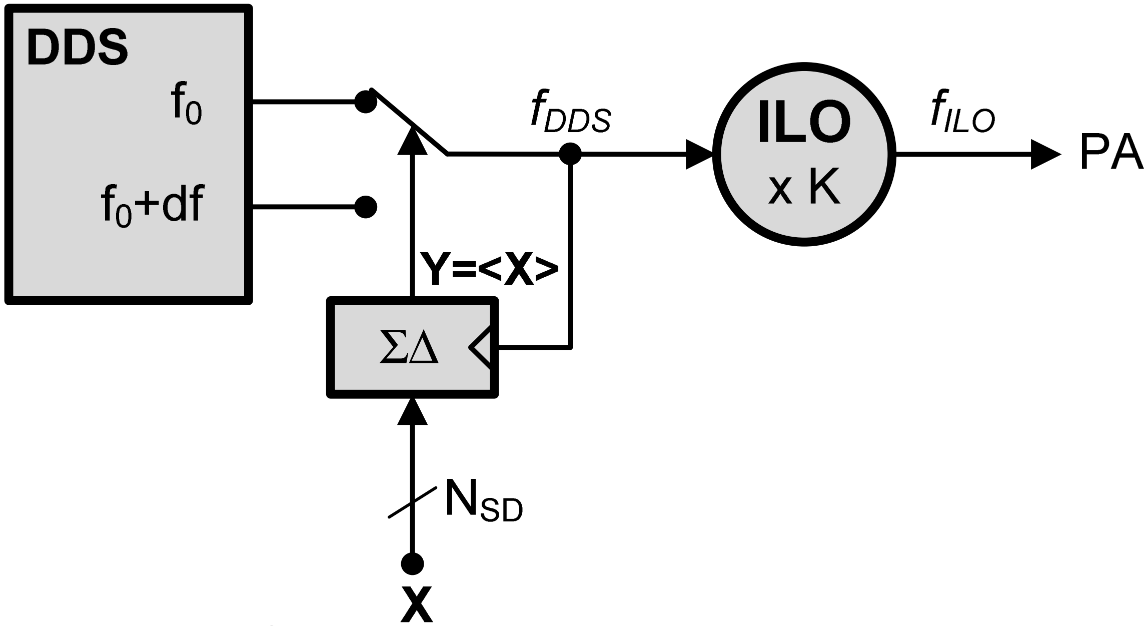
DDS based RF transmitter principle

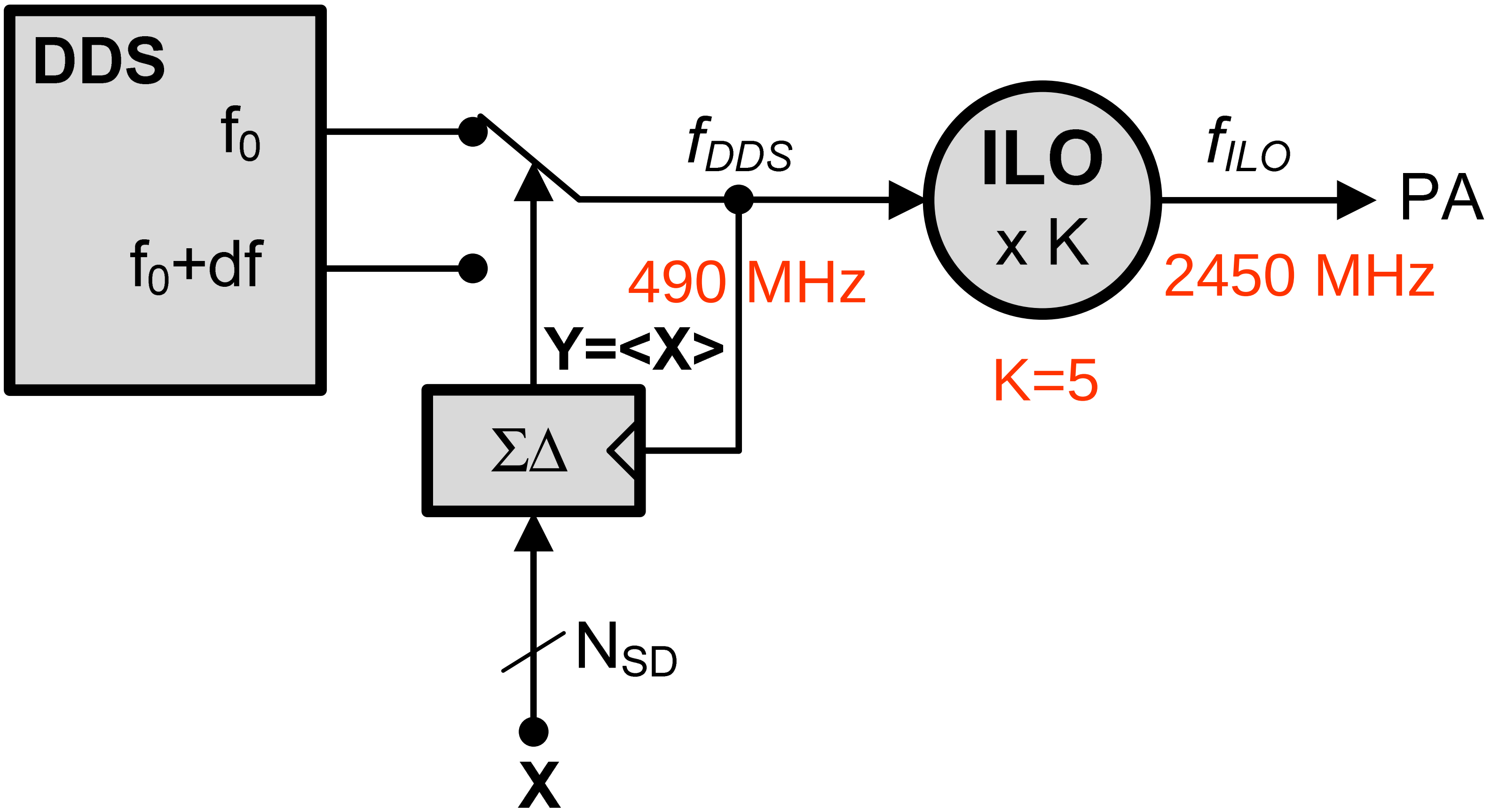


- f_{DDS} : DDS output frequency
- df : frequency step
- ΣΔ modulator synthesizes carrier frequency and shapes quantification noise.
- An ILO will act as a frequency multiplier to get the RF signal

Frequency plan

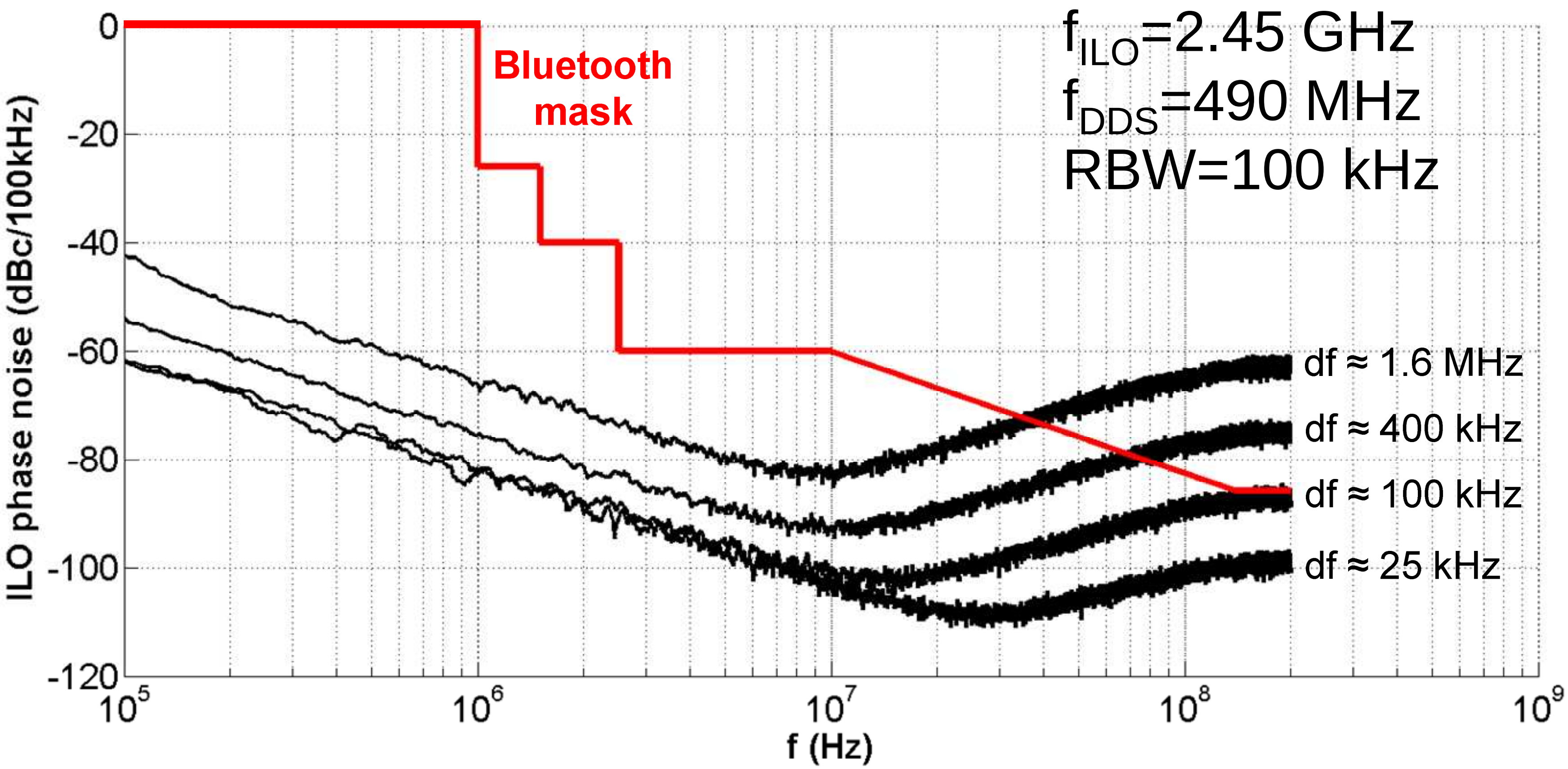
- GSM (x2) – DCS
  - Frequency range: 1710 – 1830 MHz
  - Frequency step: 0.1 ppm (170 Hz)
  - ILO multiplication factor: 4
  - DDS frequency range 427.5 – 457.5 MHz
  - DDS Frequency step: 42.5 Hz
- Bluetooth
  - Frequency range: 2402 – 2480 MHz
  - Frequency step: 1 ppm (2400 Hz)
  - ILO multiplication factor: 5
  - DDS frequency range: 480.4 – 496 MHz
  - DDS frequency step: 480 Hz

Bluetooth schematic



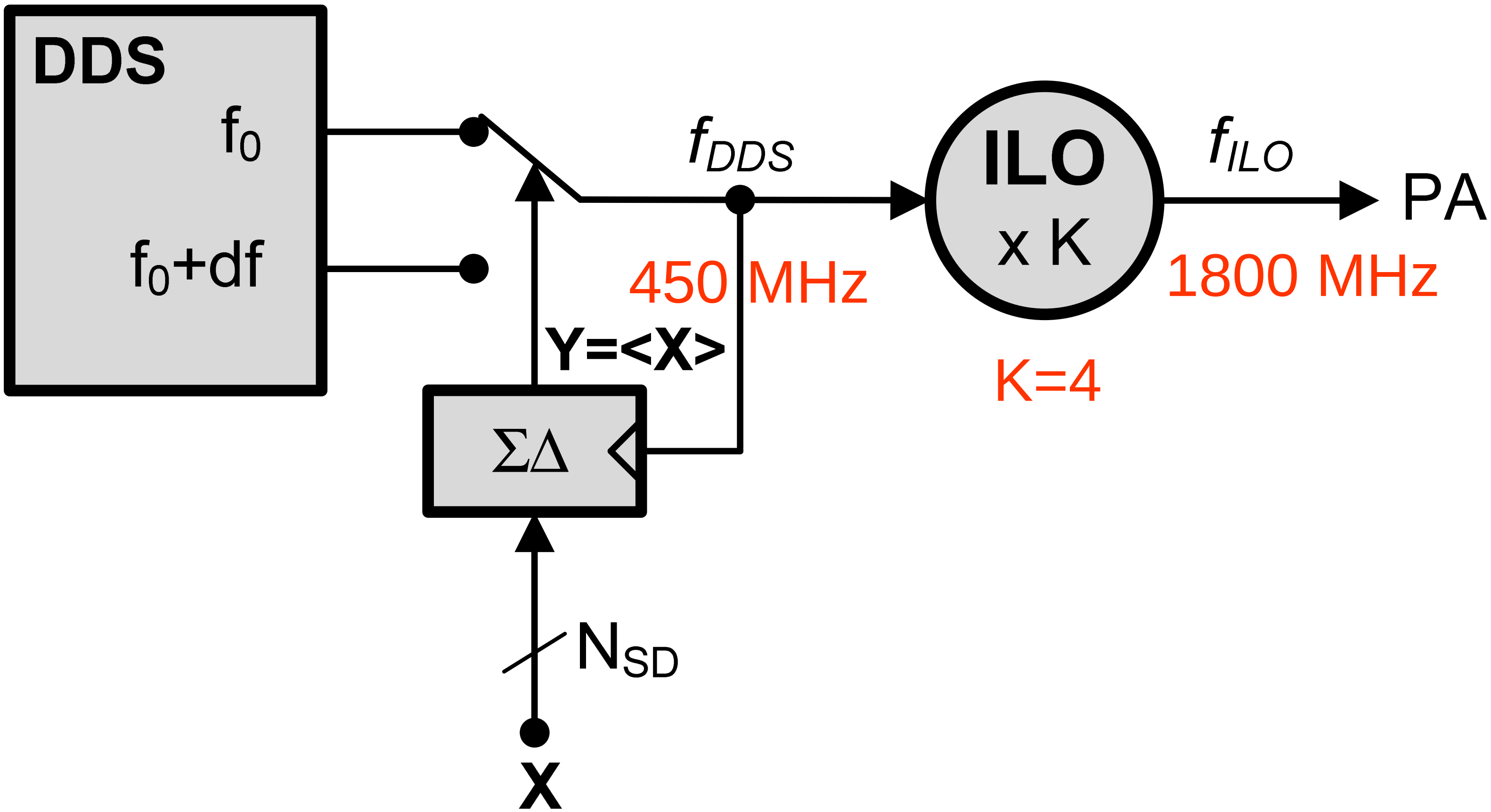
ΣΔ generates $2^{N_{SD}}$ frequencies between f_0 and f_0+df

Transmitter modelization- Bluetooth



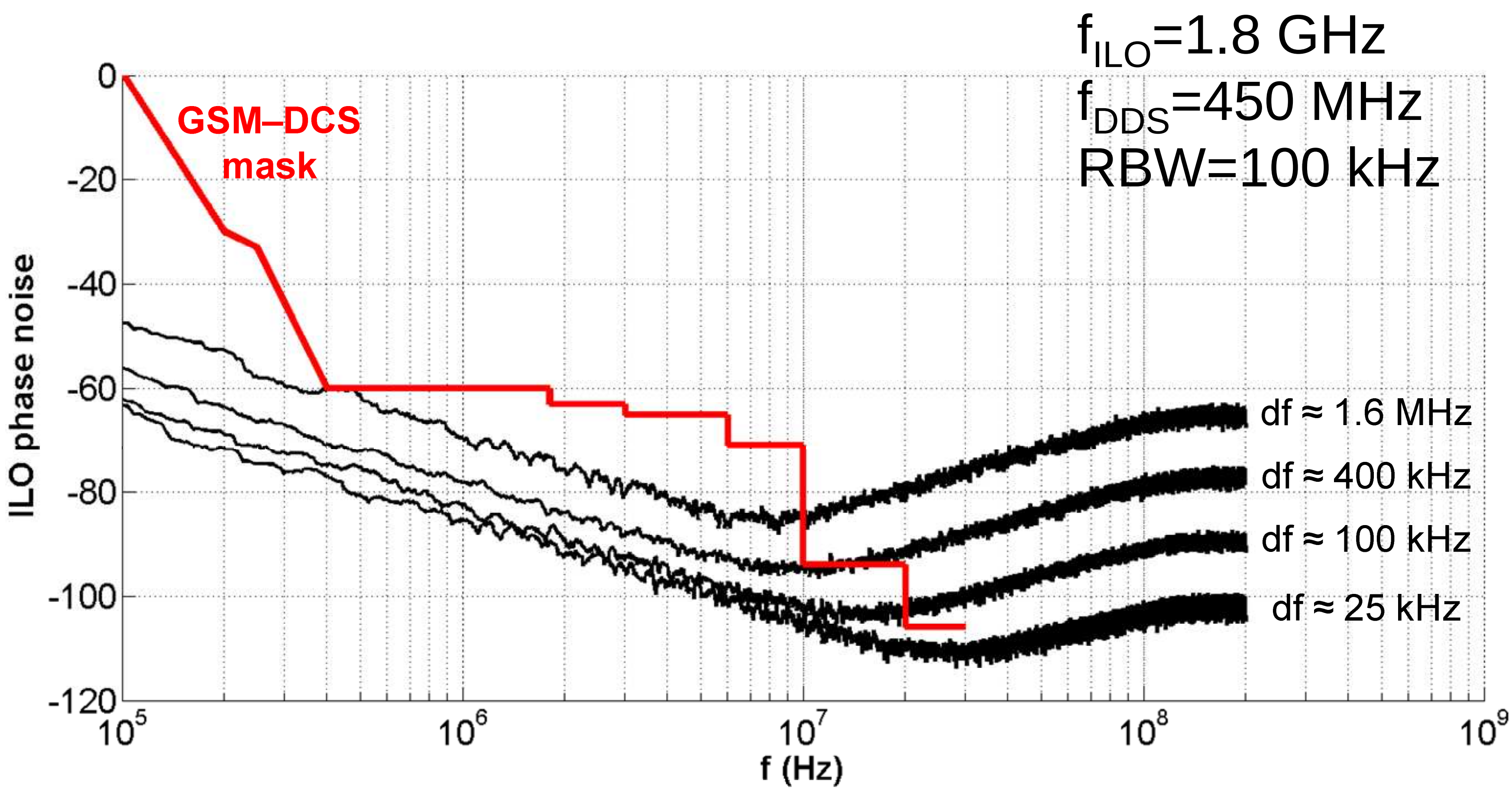
Lowering df lowers the phase noise

GSM/DCS schematics

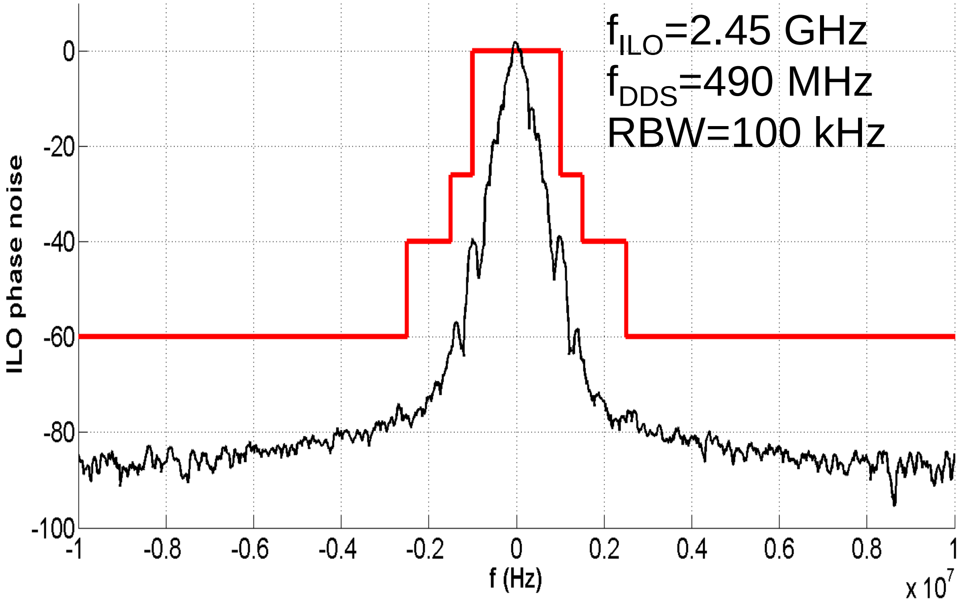


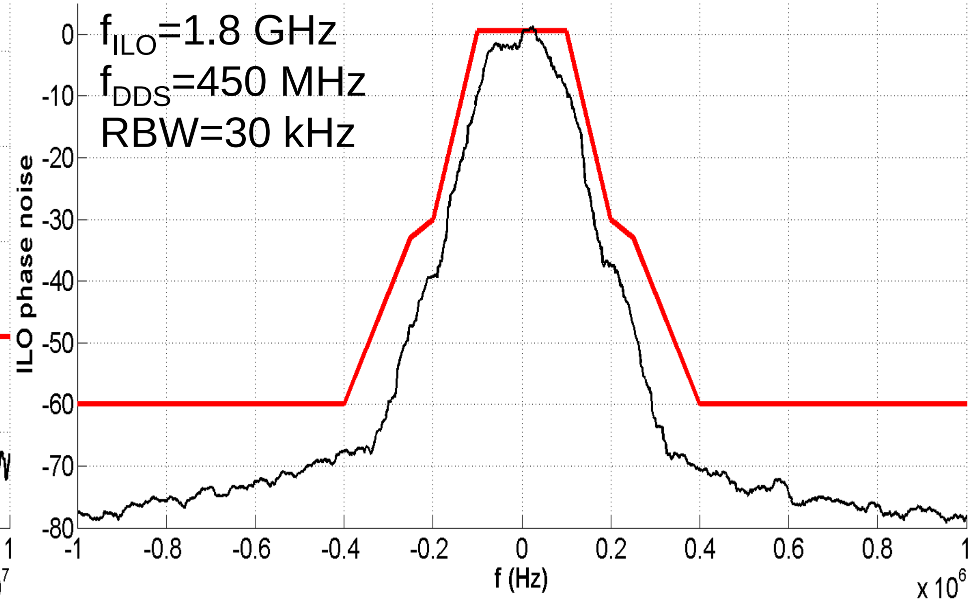
ΣΔ modulator generates $2^{N_{SD}}$ frequencies between f_0 and f_0+df

Transmitter modelisation– GSM/DCS



Modulations





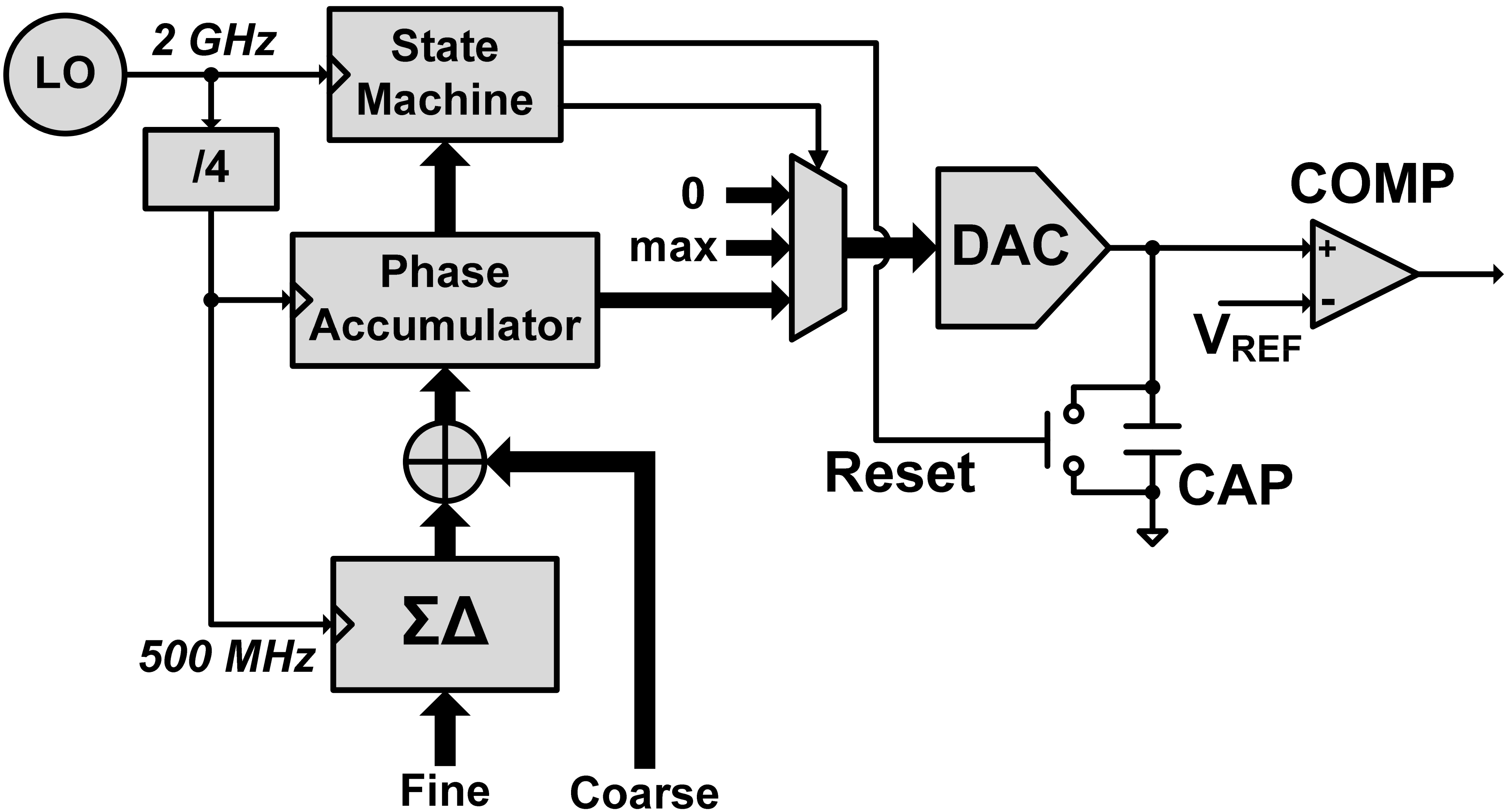
Bluetooth

- f_{BIT}: 1 MHz
- Modulator ovesampling: 32
- Symbols number: 50
- df: 400 kHz

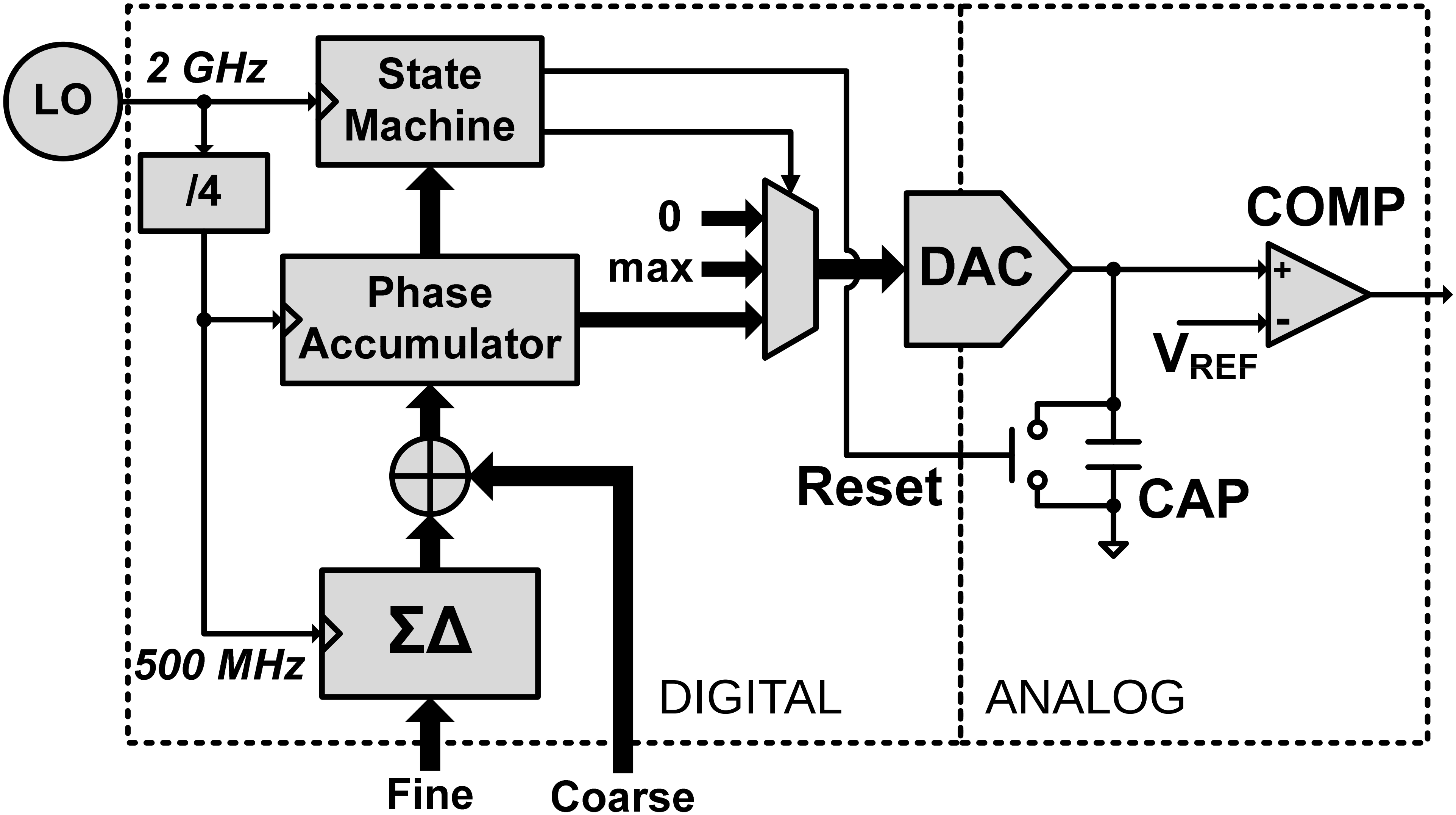
GSM

- f_{BIT}: 270.833 kb/s
- Modulator oversampling: 64
- Symbols number: 148
- df: 400 kHz

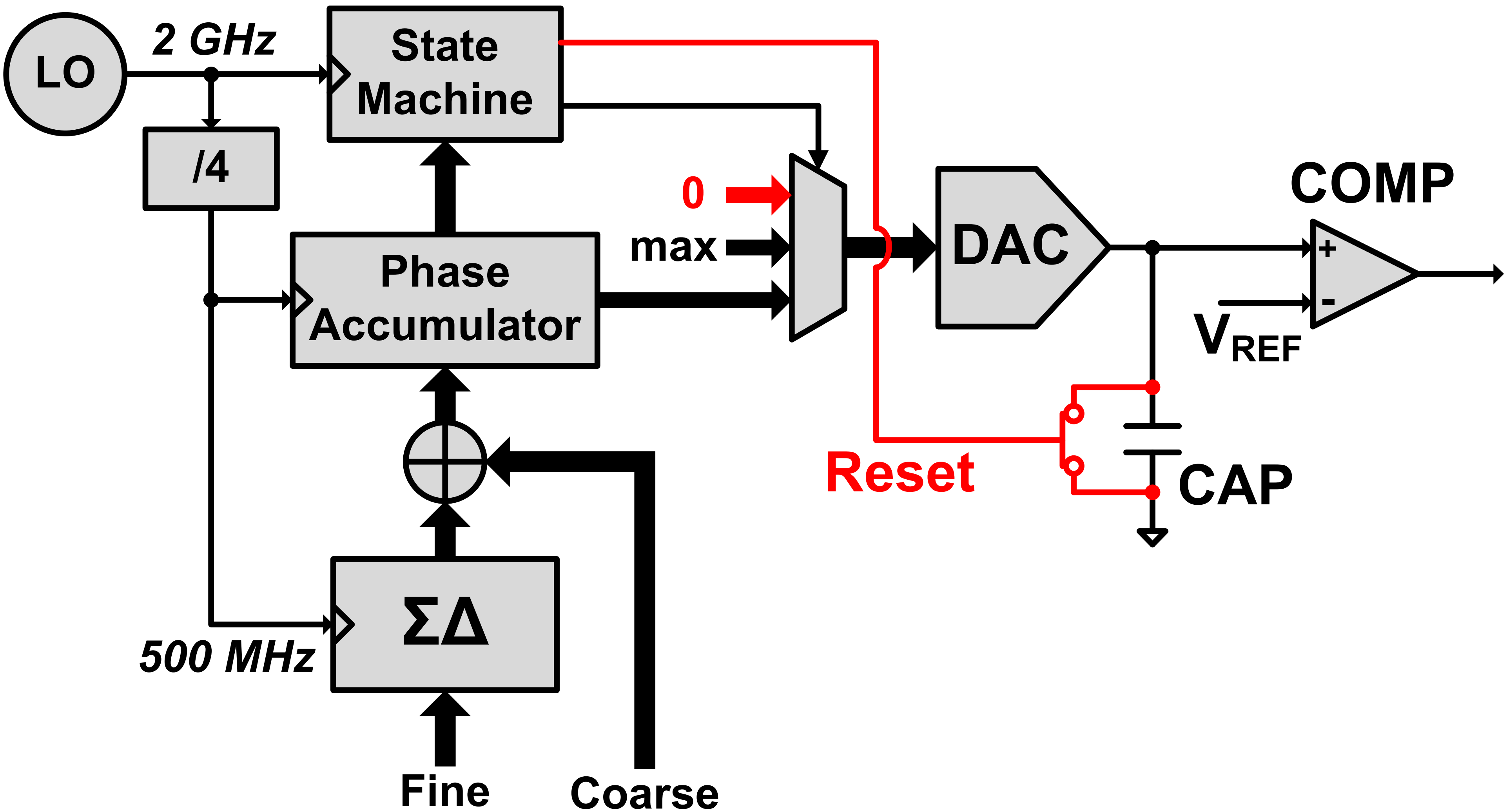
ΣΔ and phase interpolation based DDS



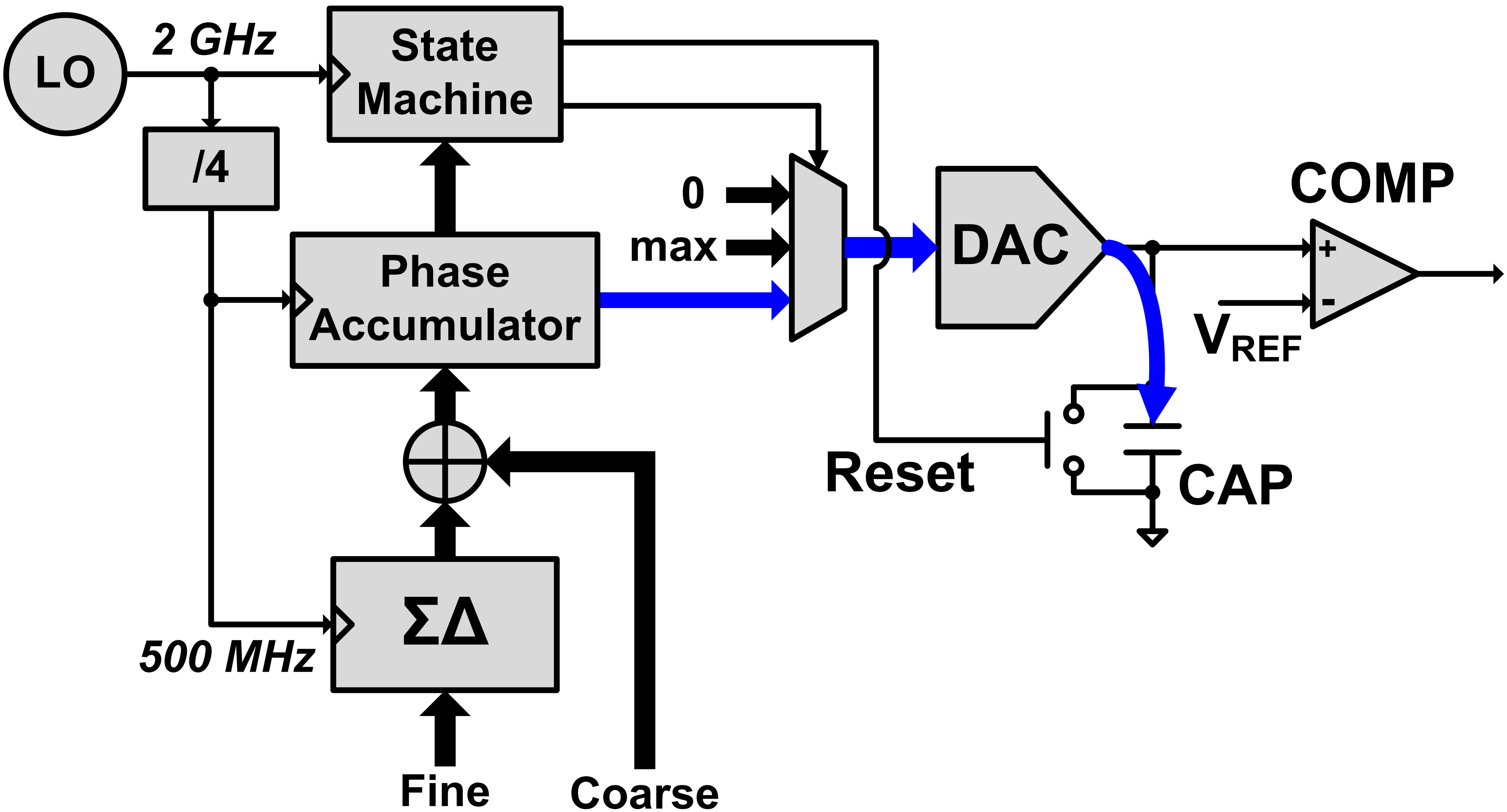
ΣΔ and phase interpolation based DDS



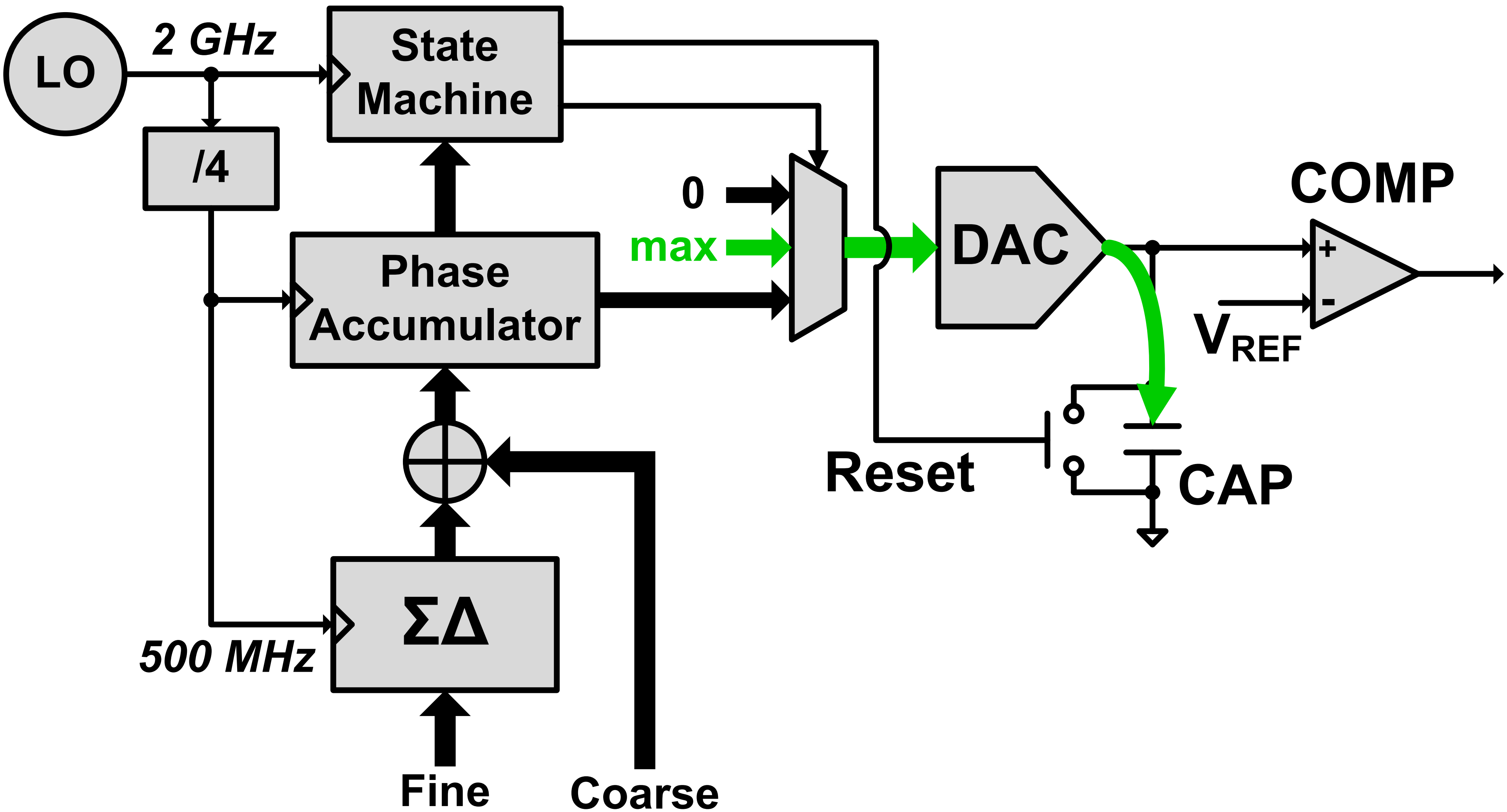
RAZ


LO
2 GHz
State Machine
/4
Phase Accumulator
0
max
DAC
COMP
+
-
V_{REF}
Reset
CAP
ΣΔ
500 MHz
Fine
Coarse

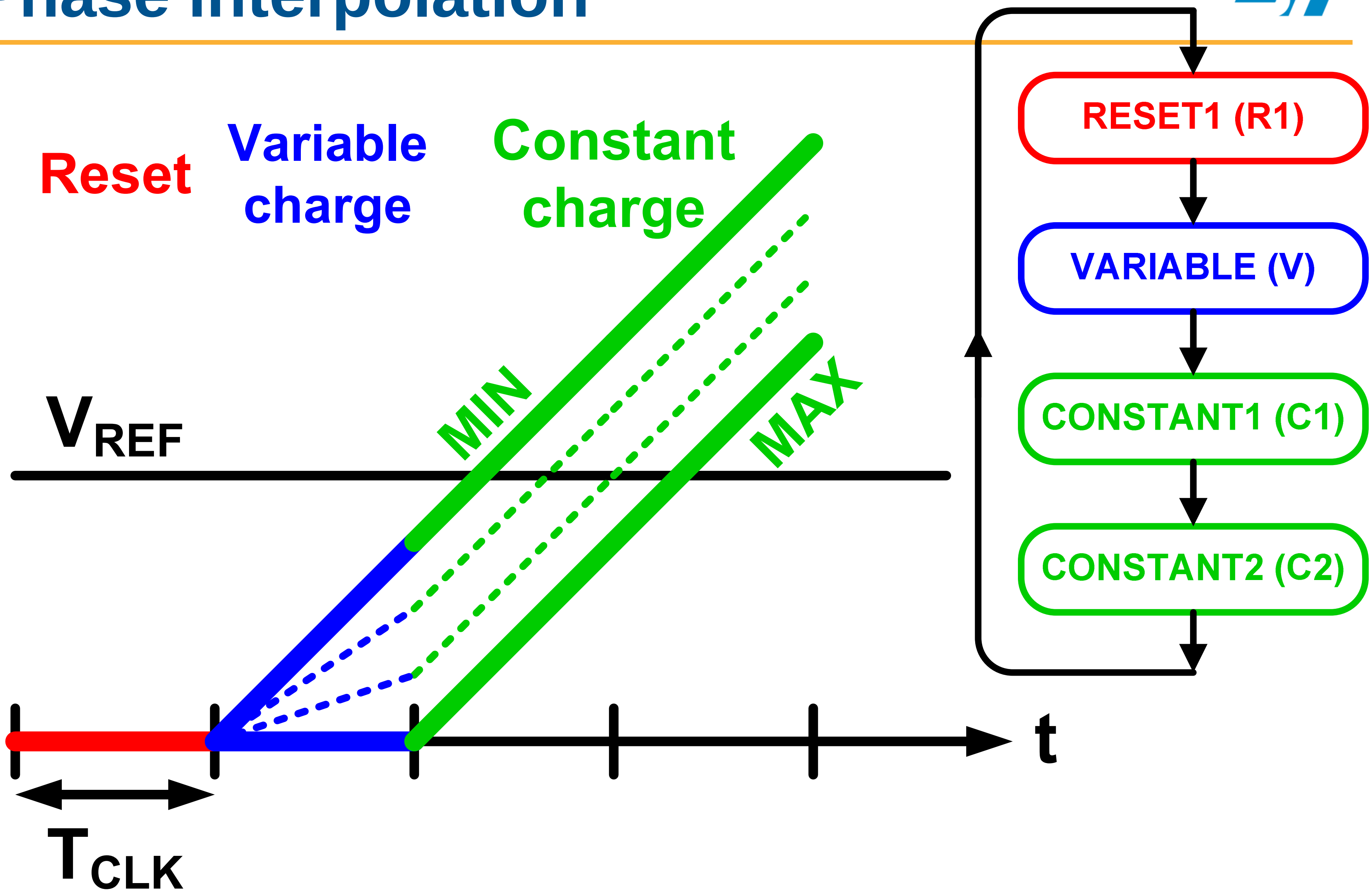
Capacitor charge with variable current



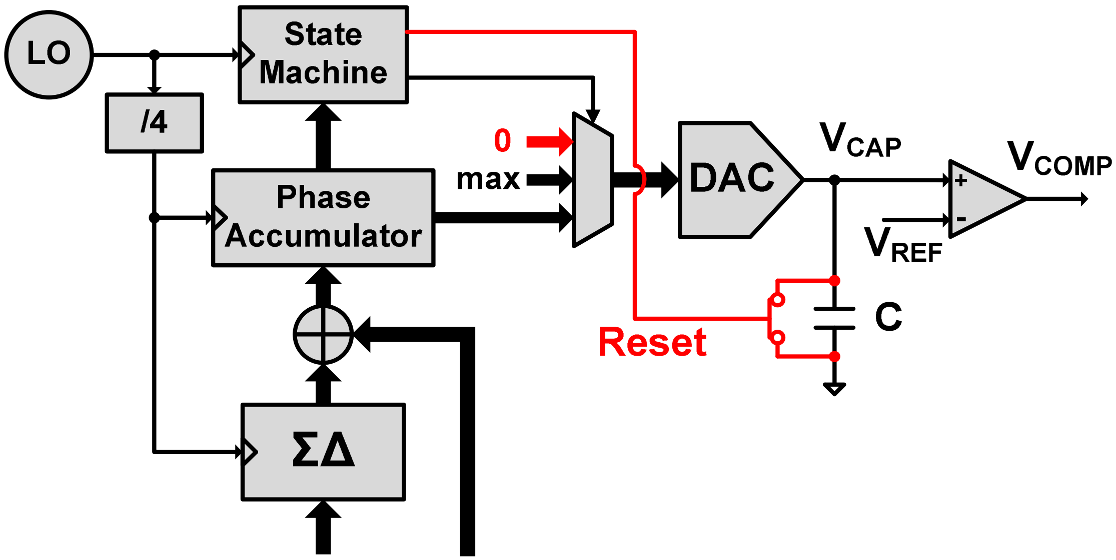
Capacitor charge with Imax

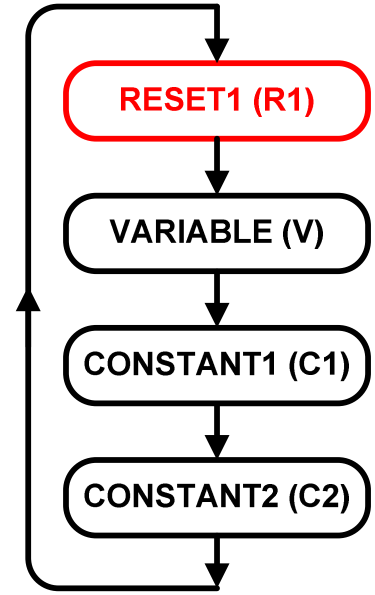


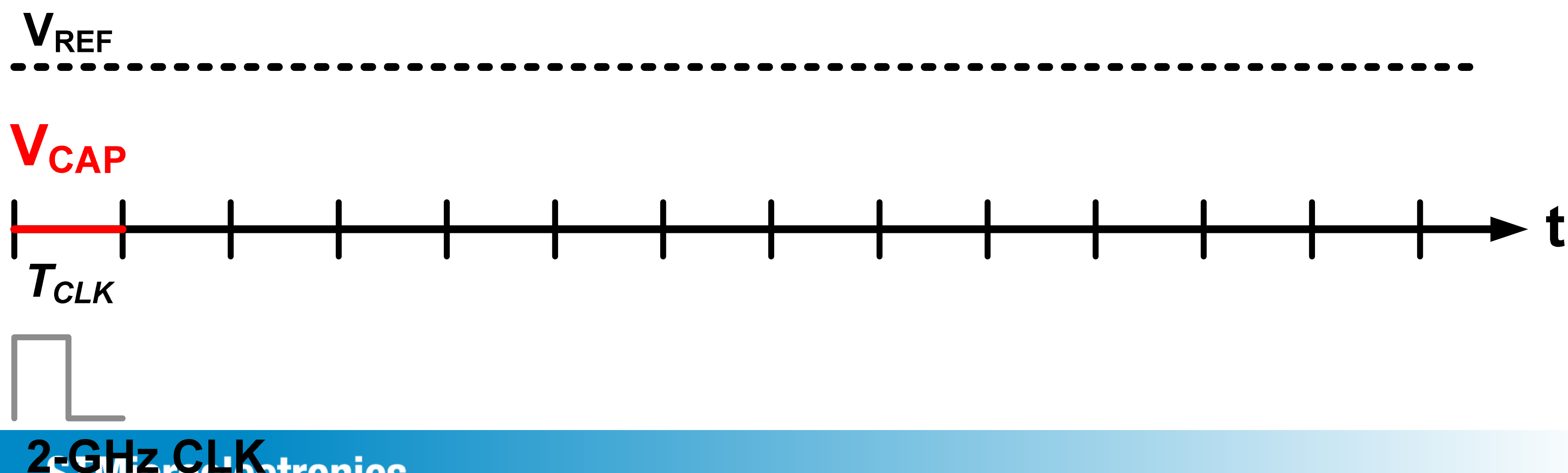
Phase interpolation



Synthesizer working process







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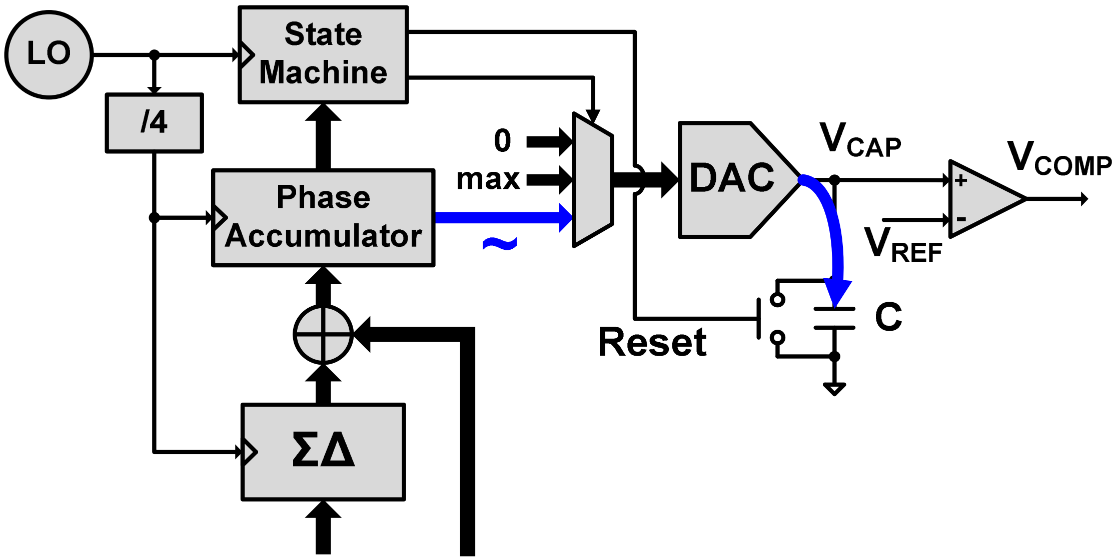

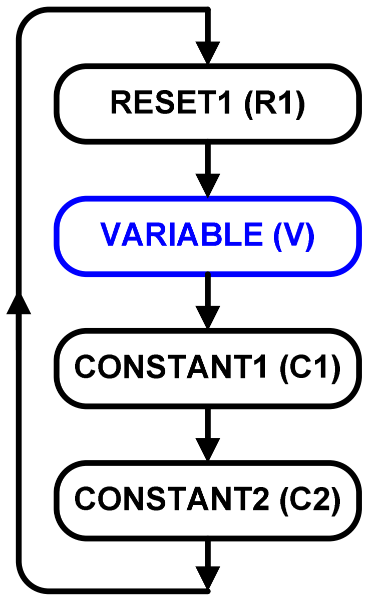

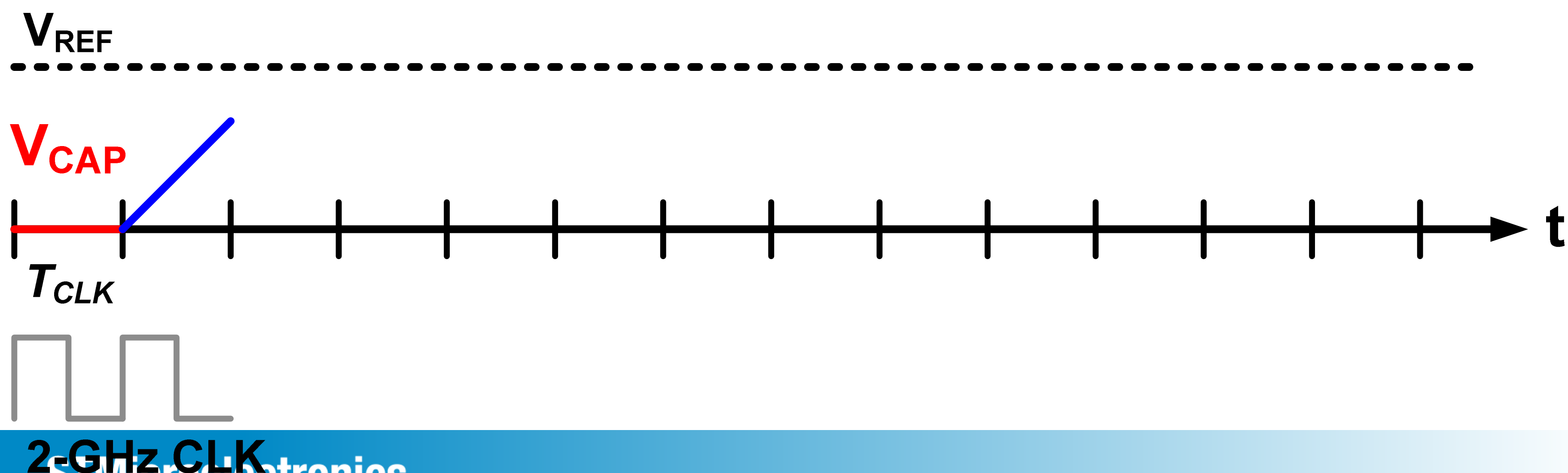

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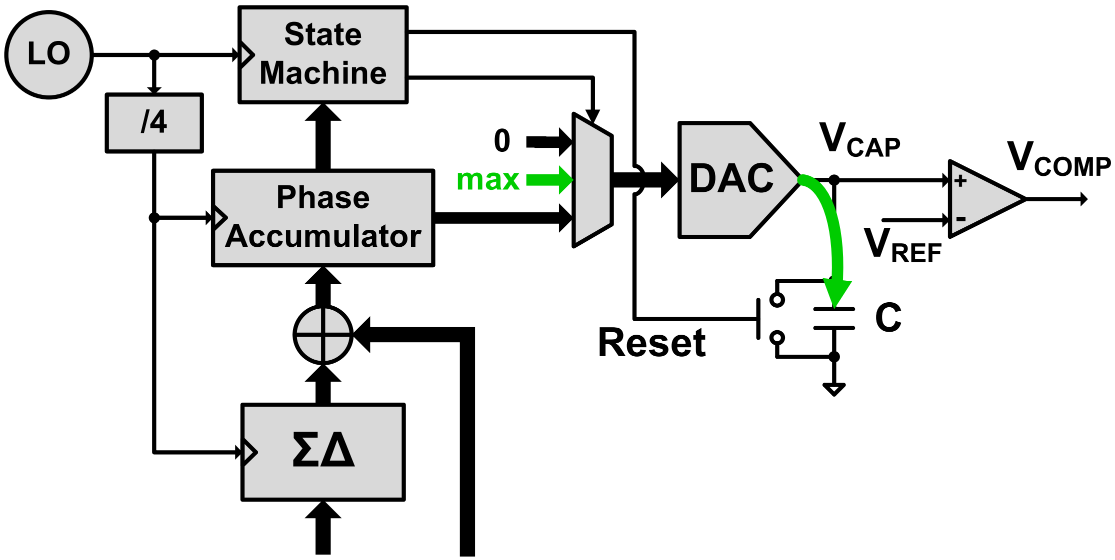
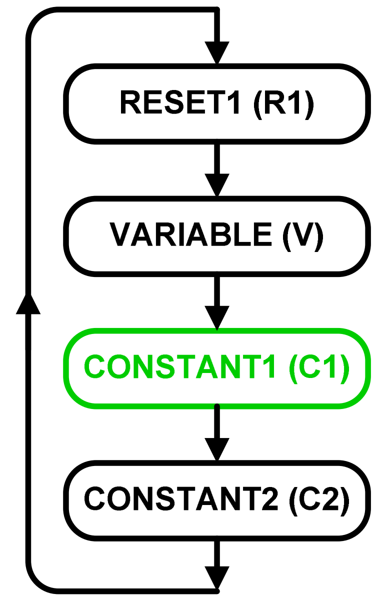
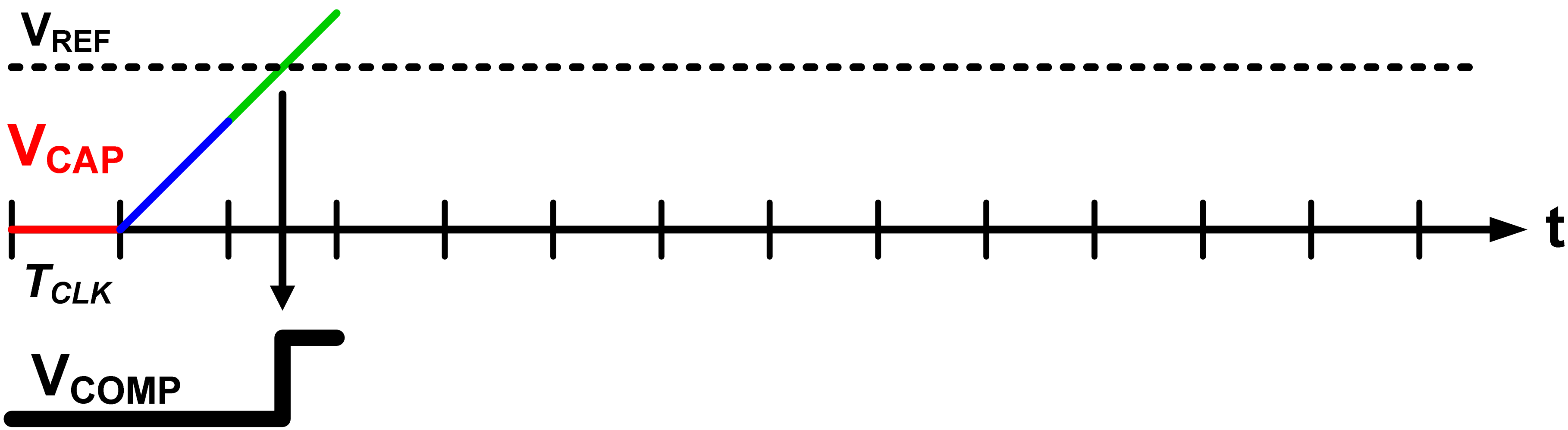
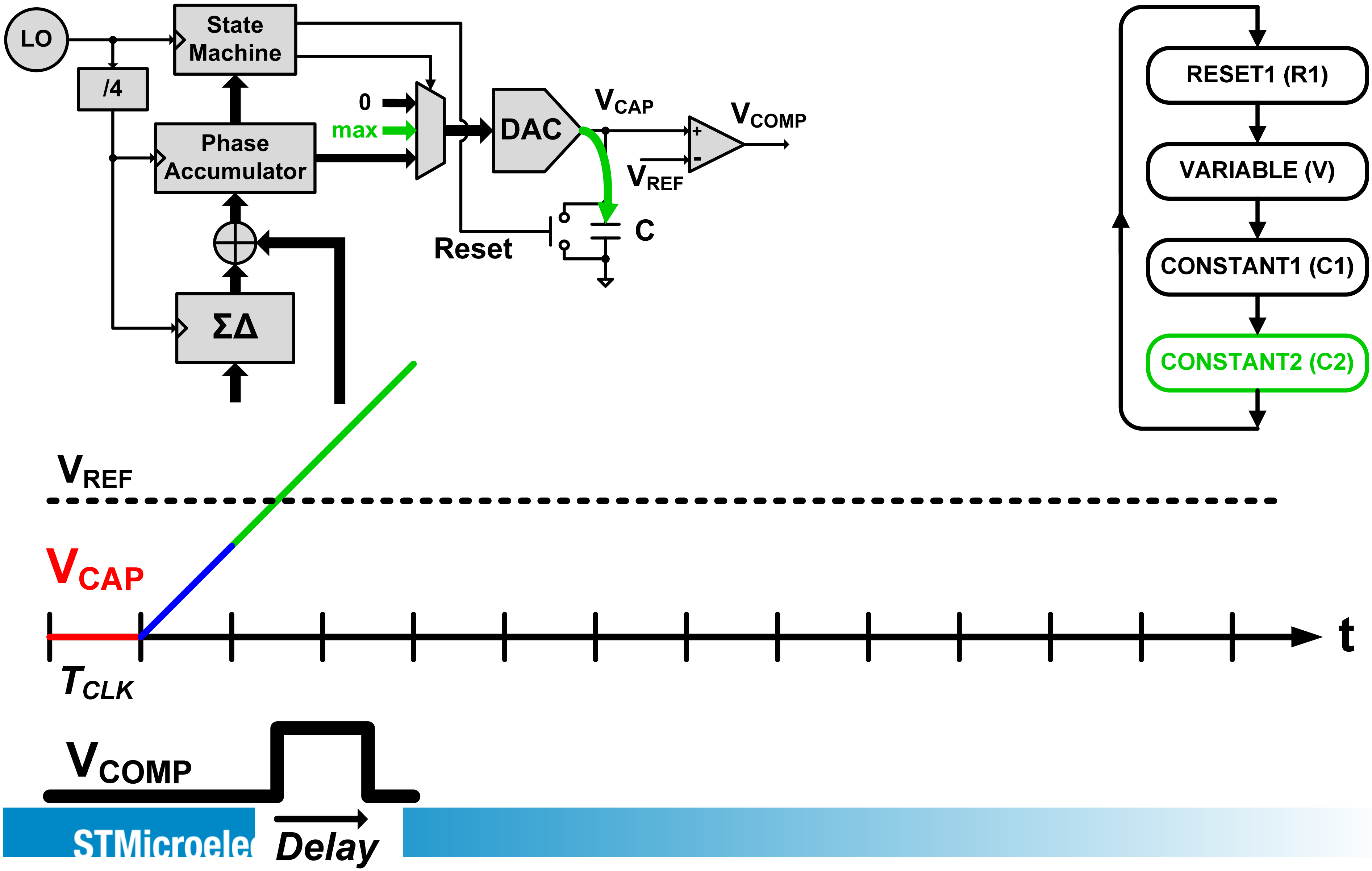


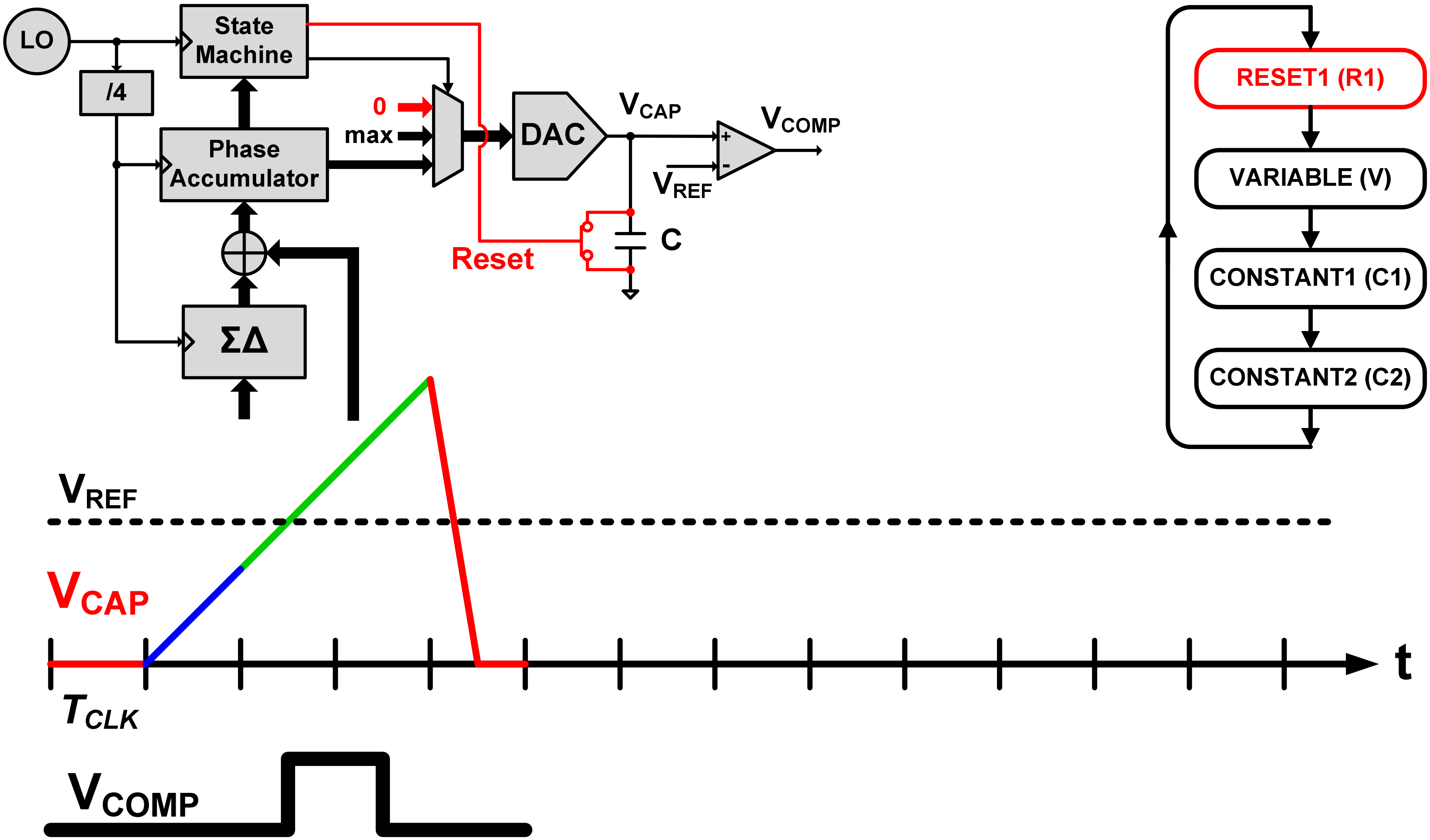




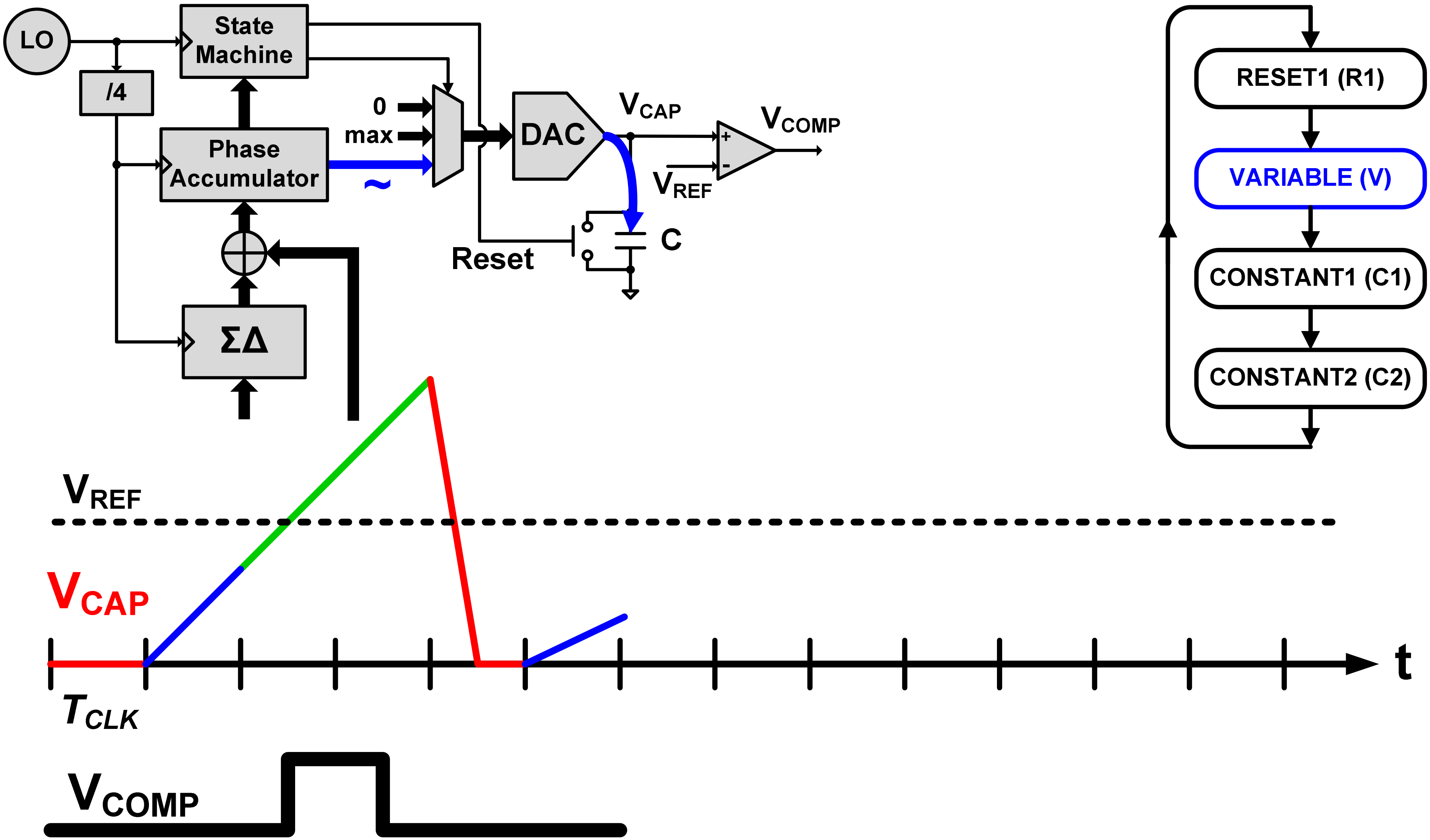
Synthesizer working process



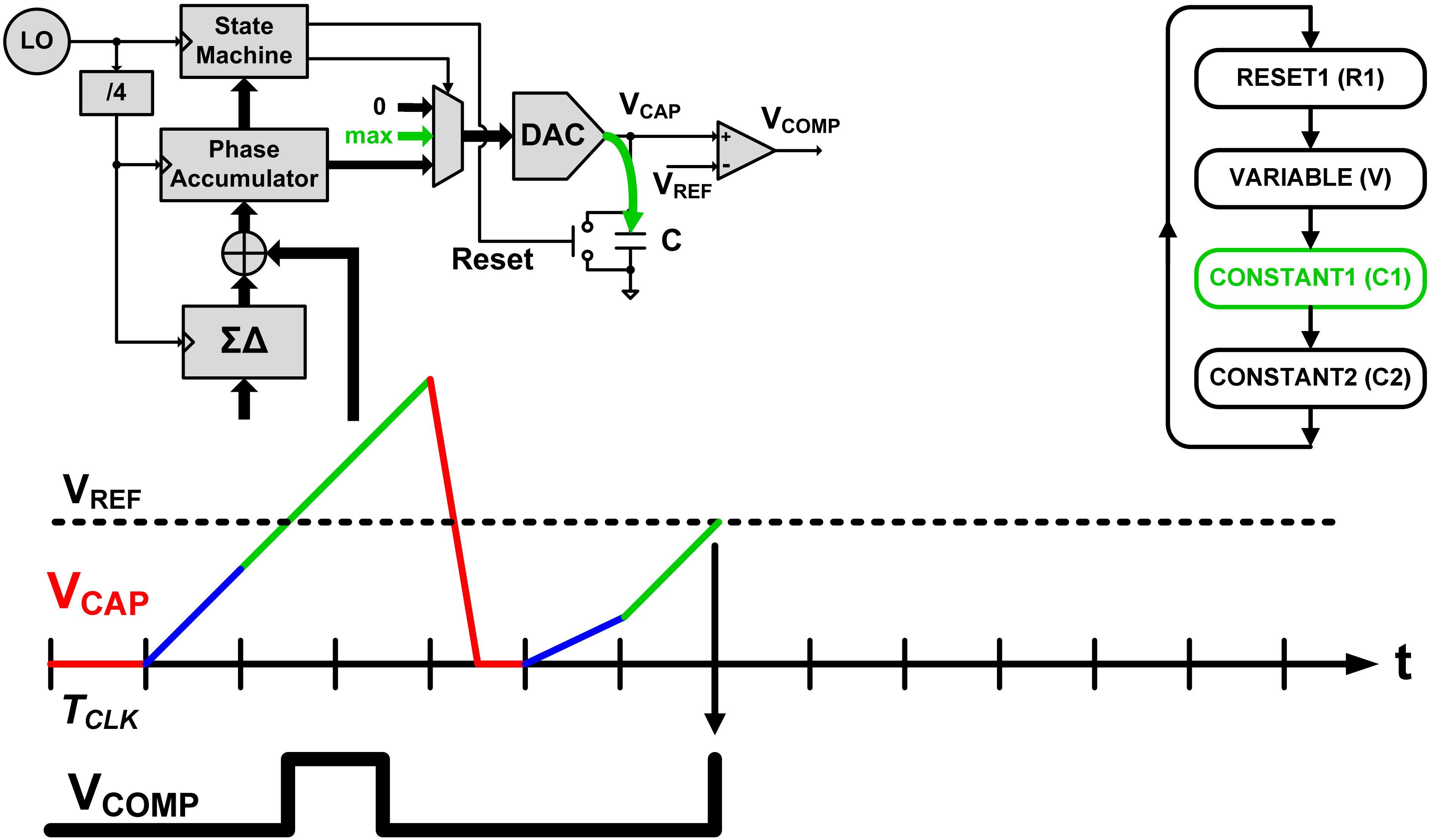
Synthesizer working process



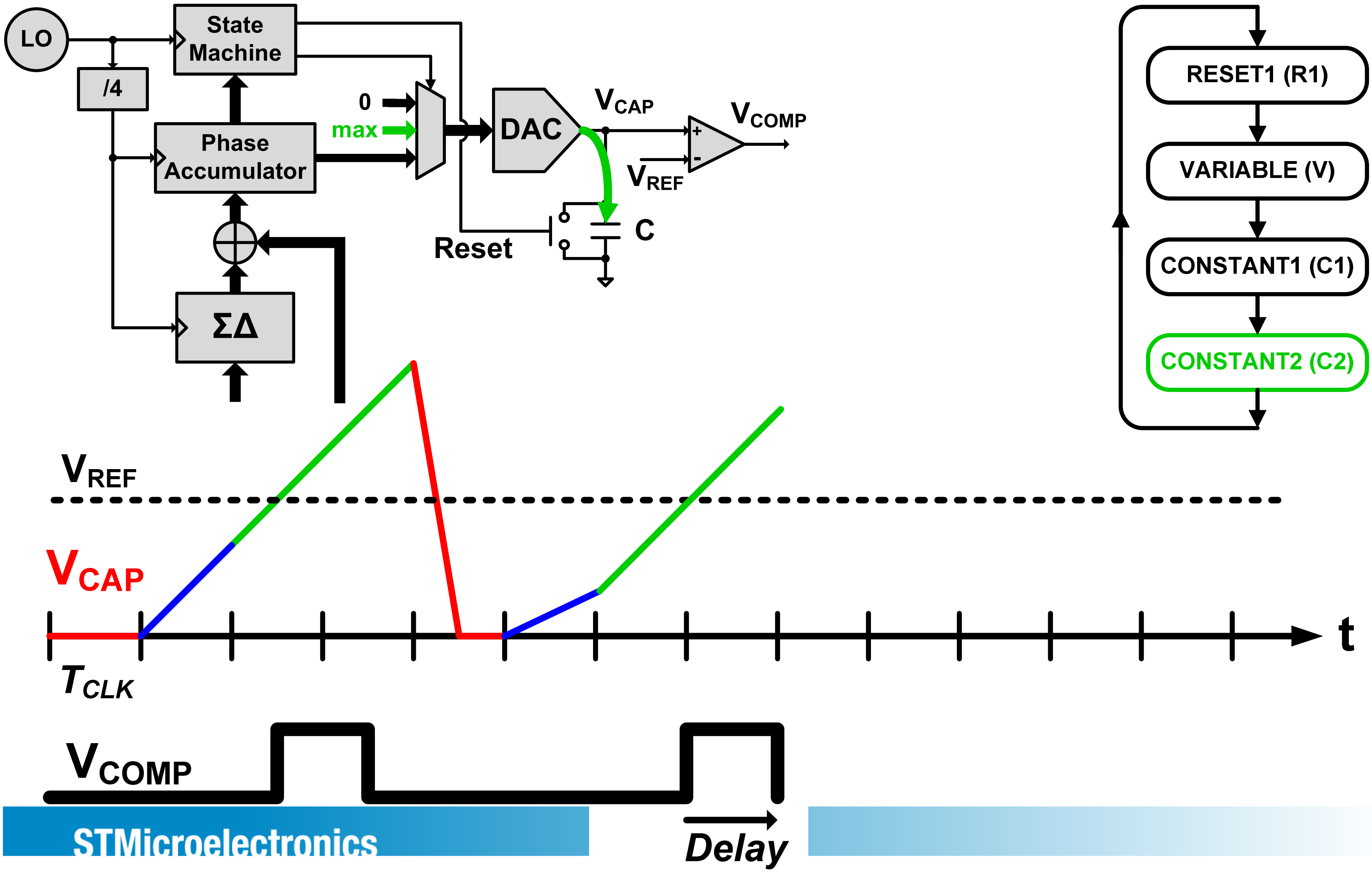
Synthesizer working process



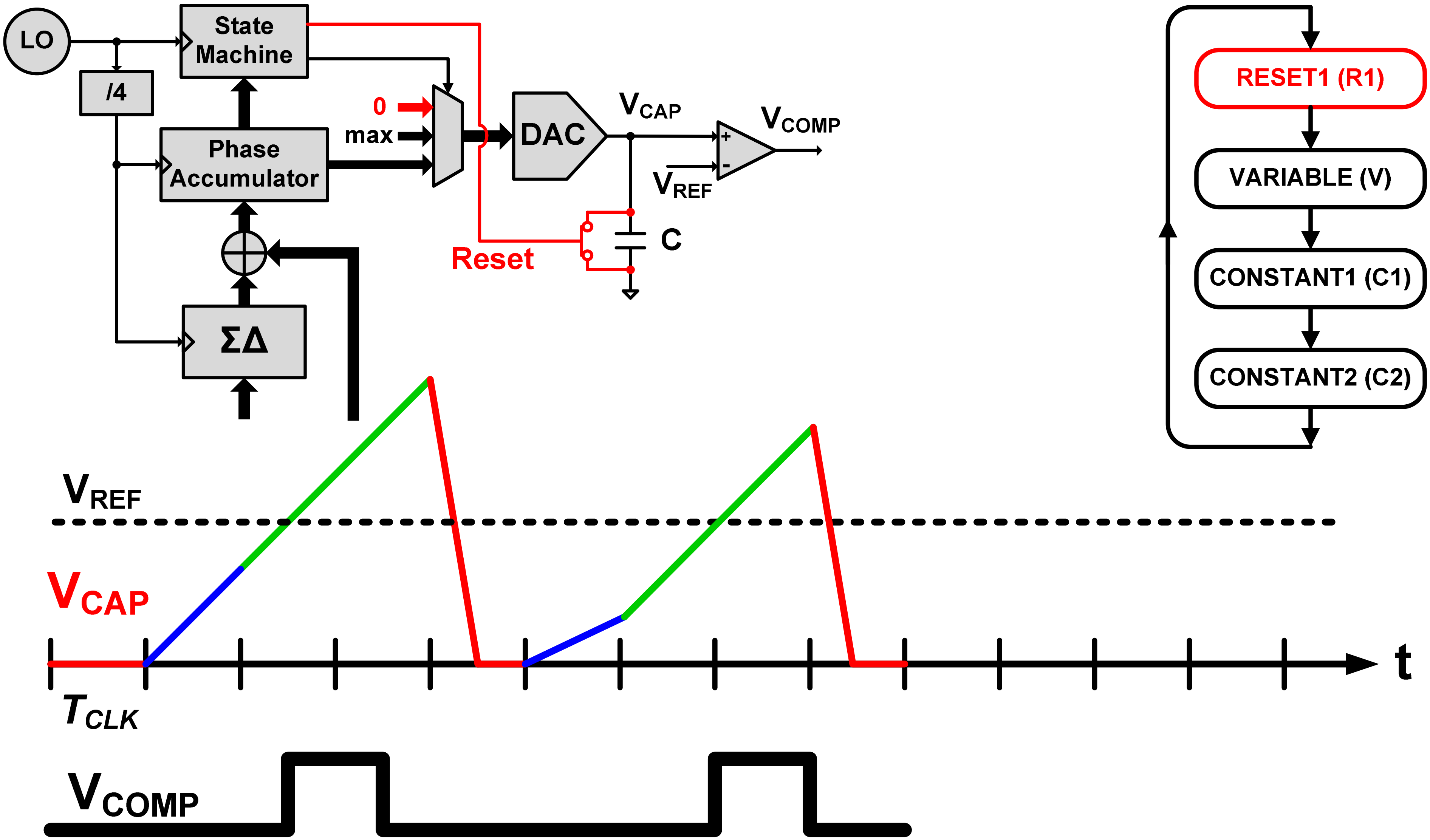
Synthesizer working process



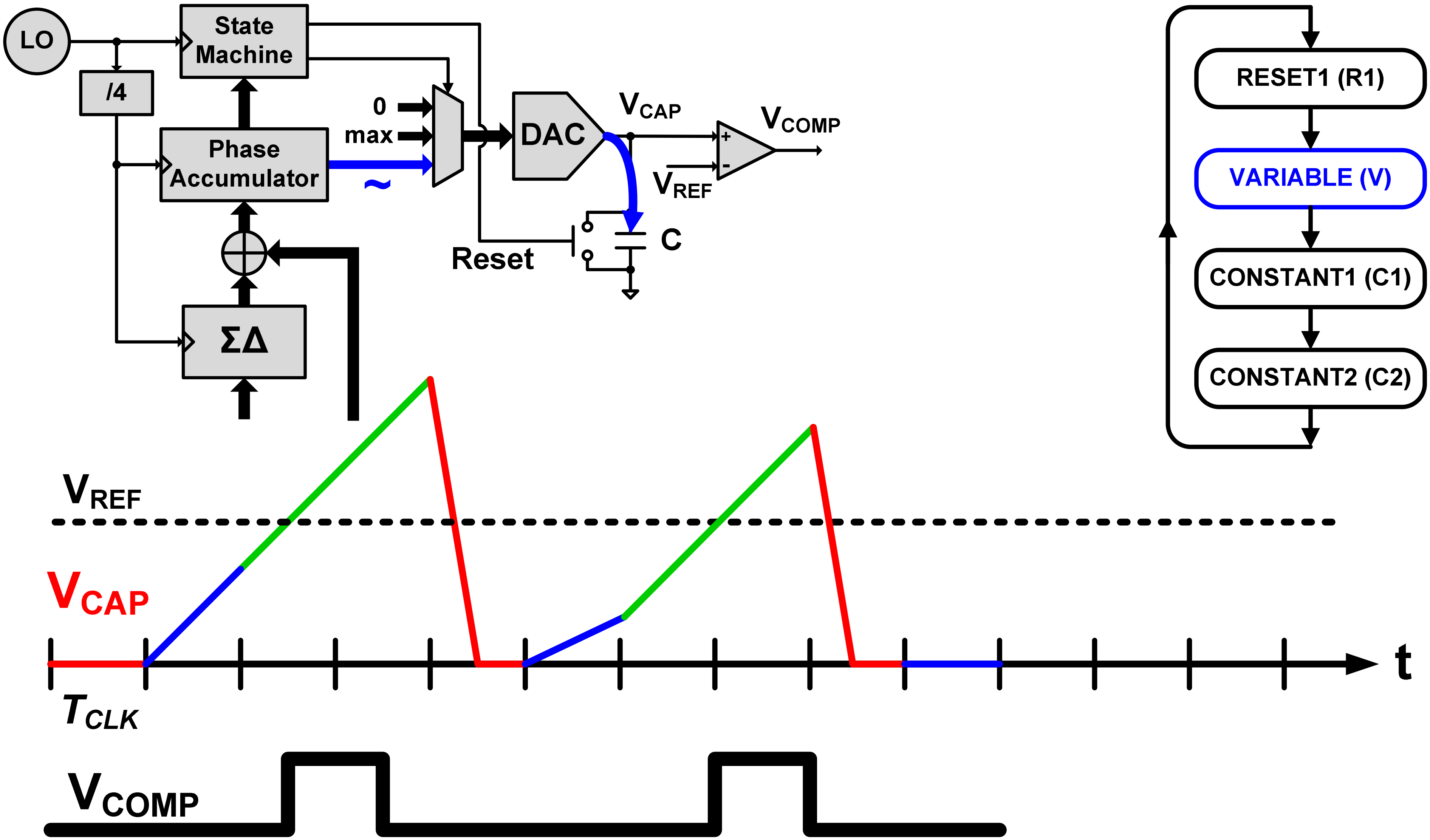
Synthesizer working process



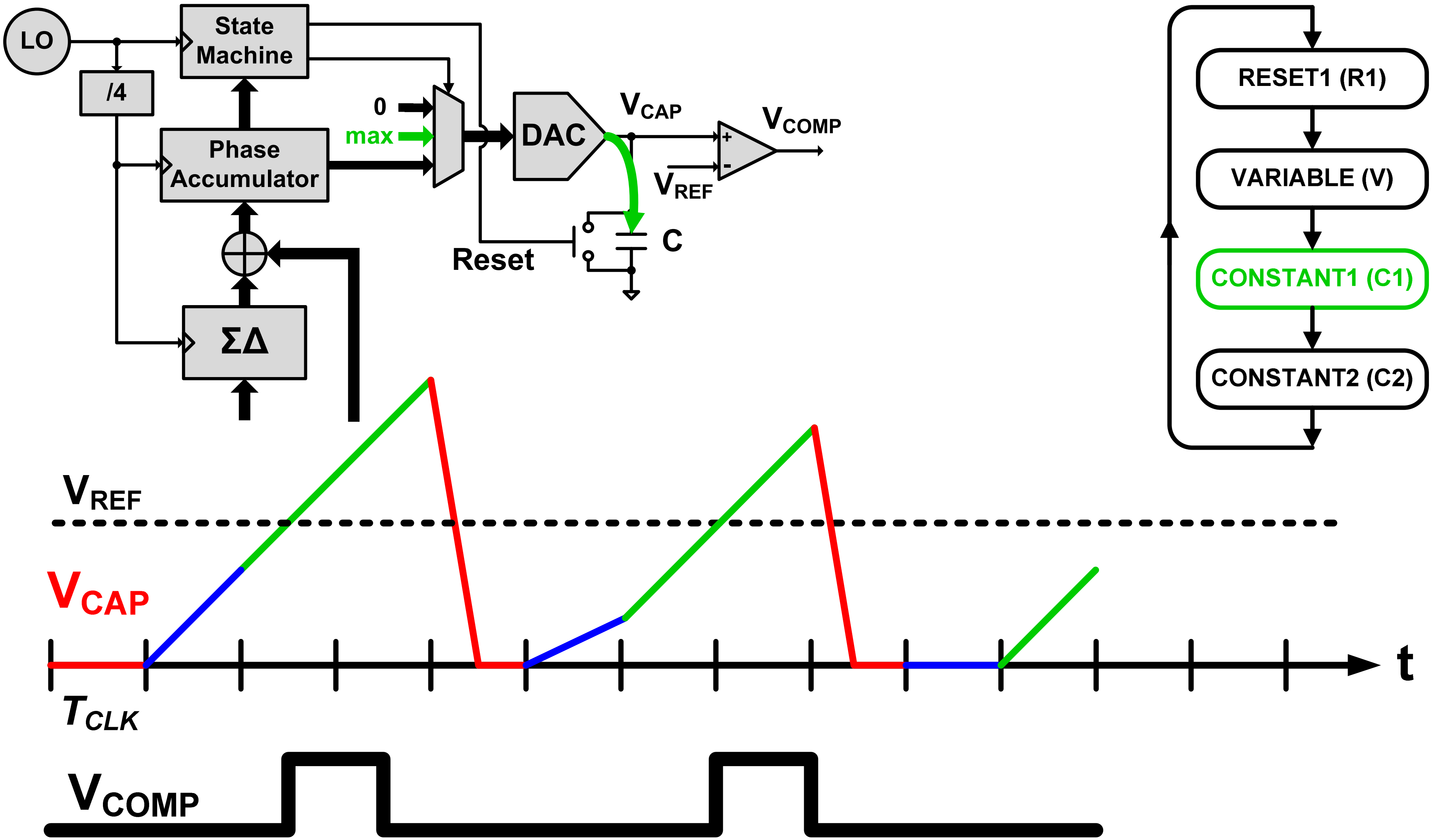
Synthesizer working process



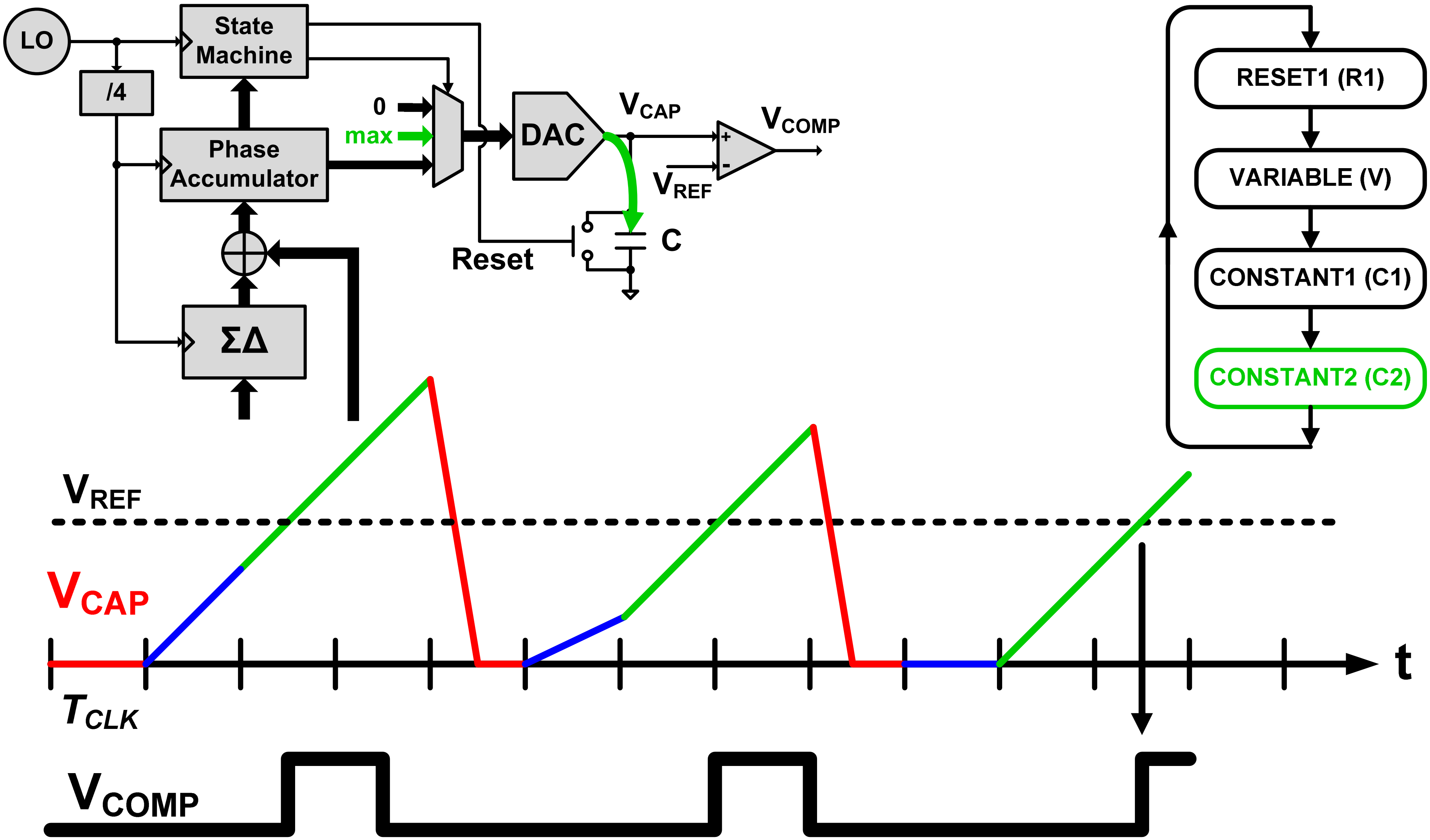
Synthesizer working process



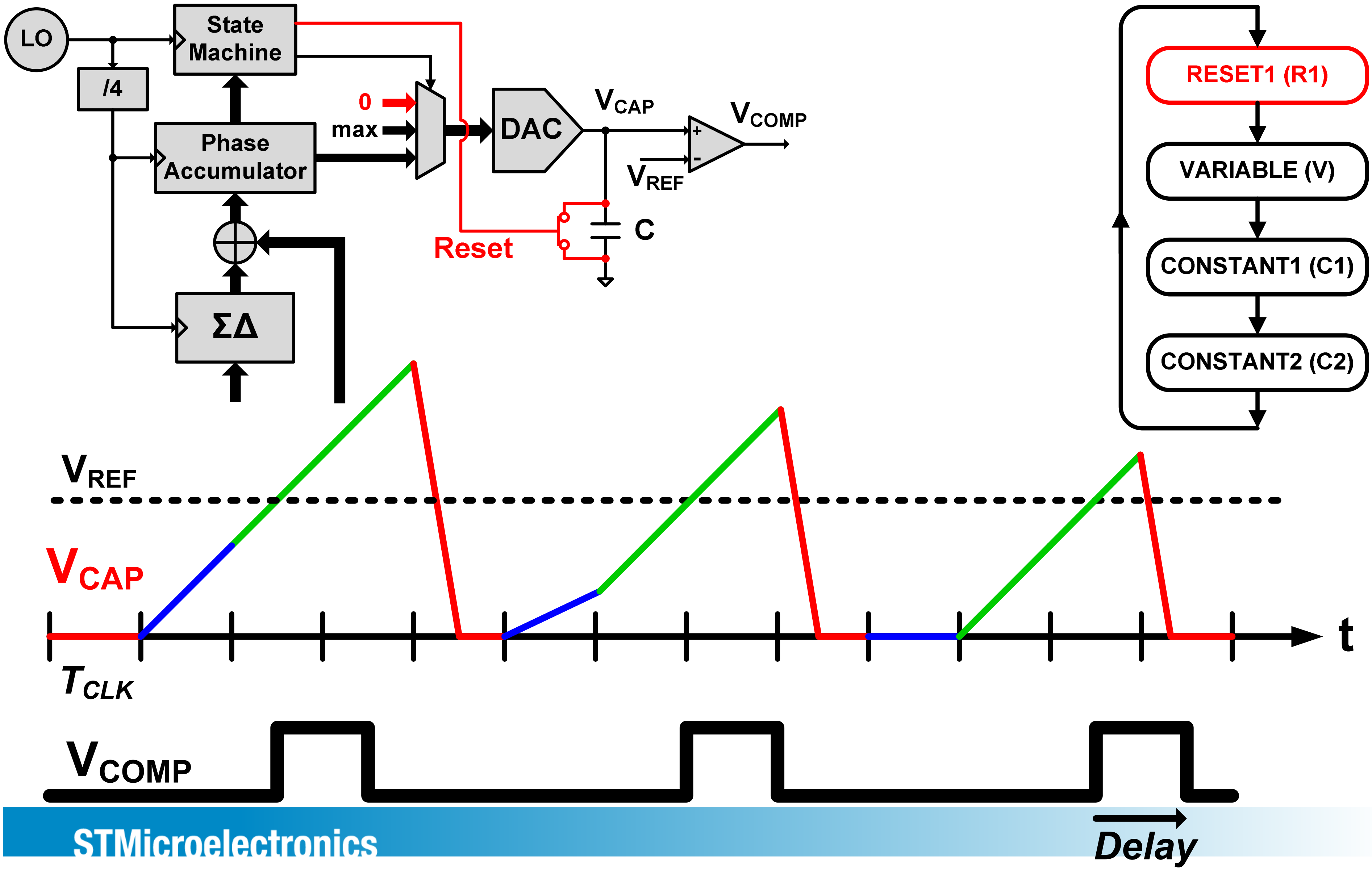
Synthesizer working process



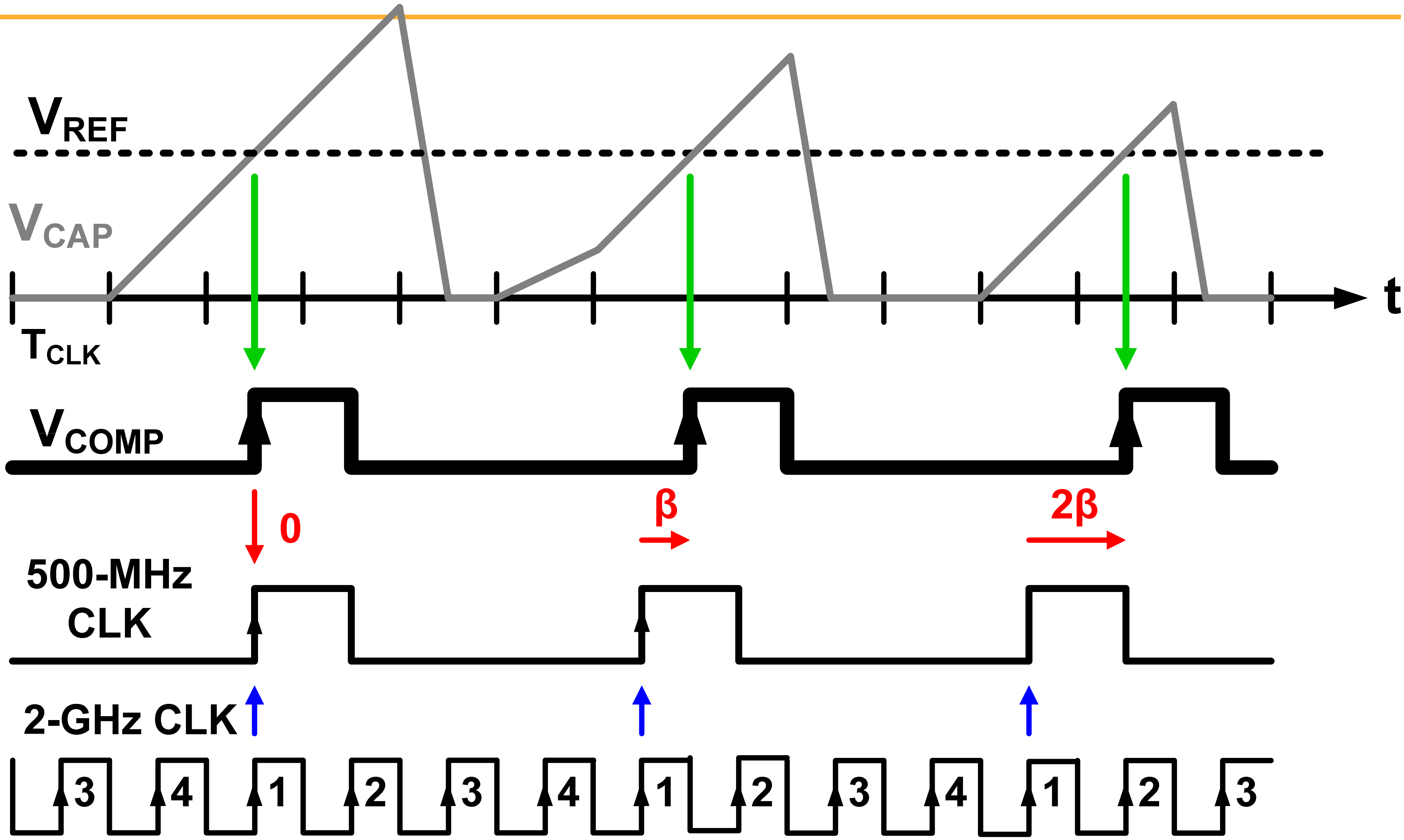
Synthesizer working process



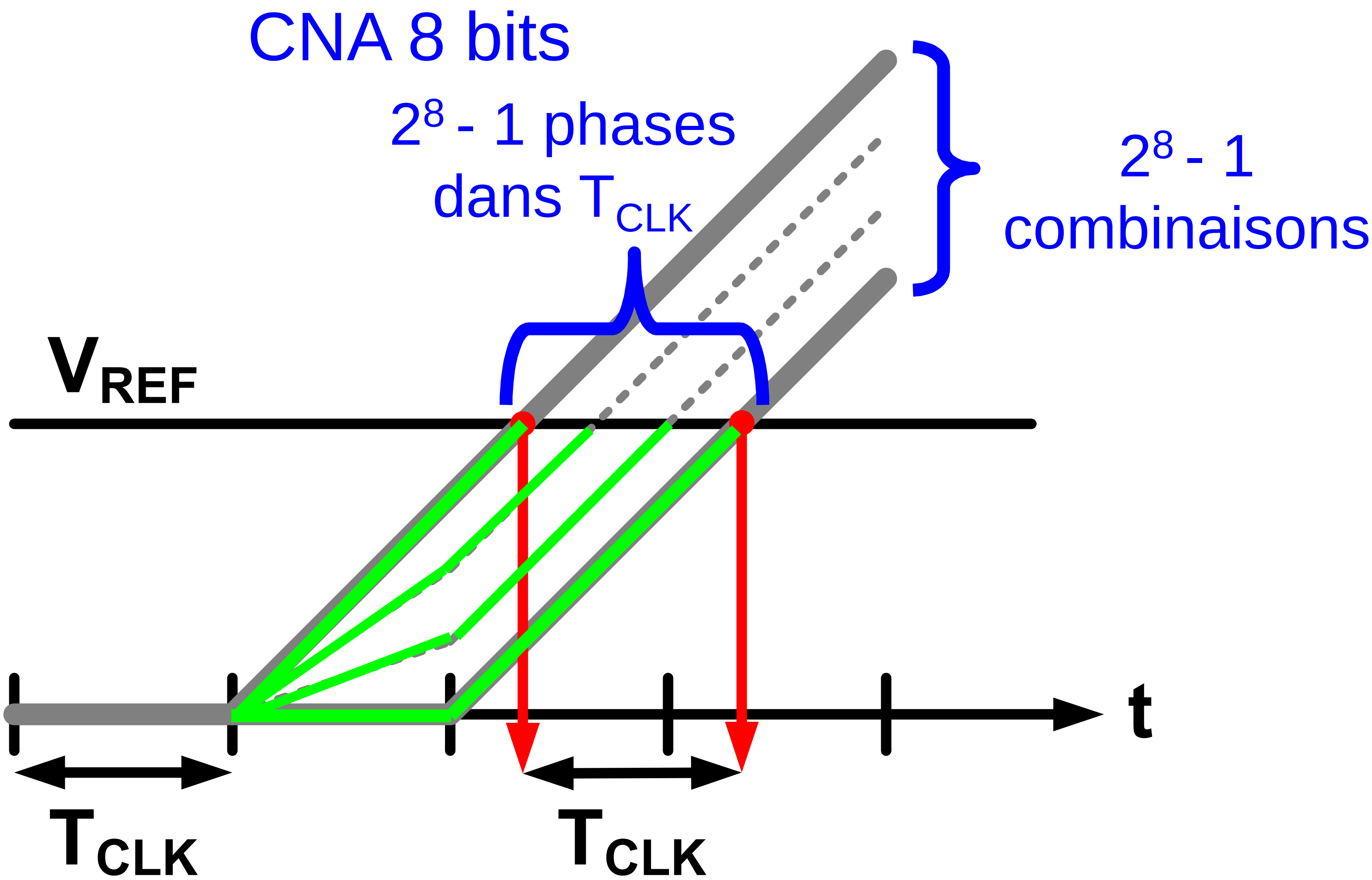
Synthesizer working process



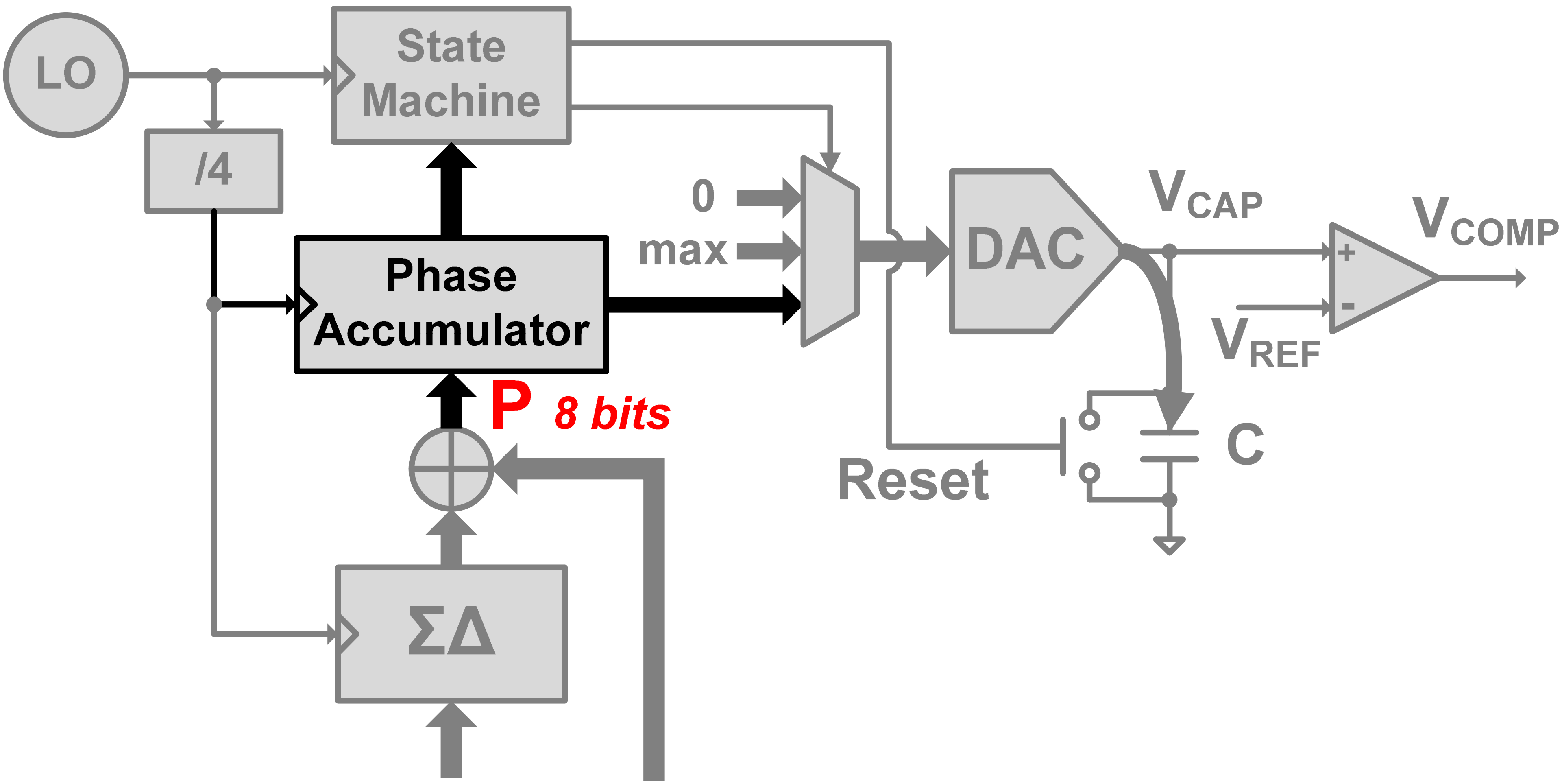
Time waveform



Combinaisons de l'interpolation de phase



Detailed DDS bloc Diagramm



DDS frequencies calculation

- 1 phase interpolation each $4T_{CLK}$
- $(2^8 - 1)$ phases in T_{CLK}

$$f_{DDS} = \frac{\frac{f_{CLK}}{4}}{\left(1 + \frac{P}{4(2^8-1)}\right)}$$

$f_{CLK} = 2$ GHz

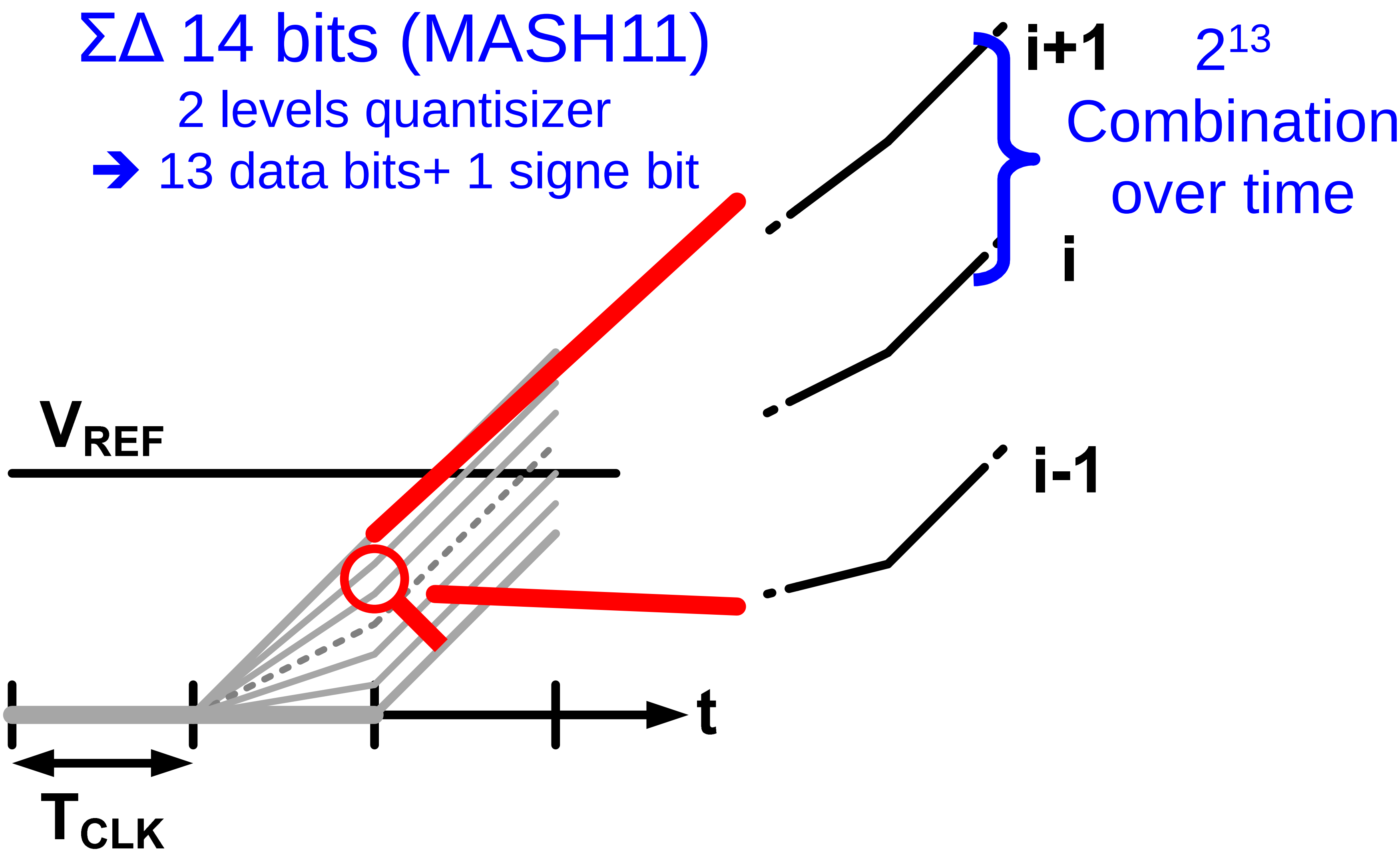
$f_{CLK}/4 = 500$ MHz

$P = 0 \rightarrow f_{DDS\_MAX} = 500$ MHz

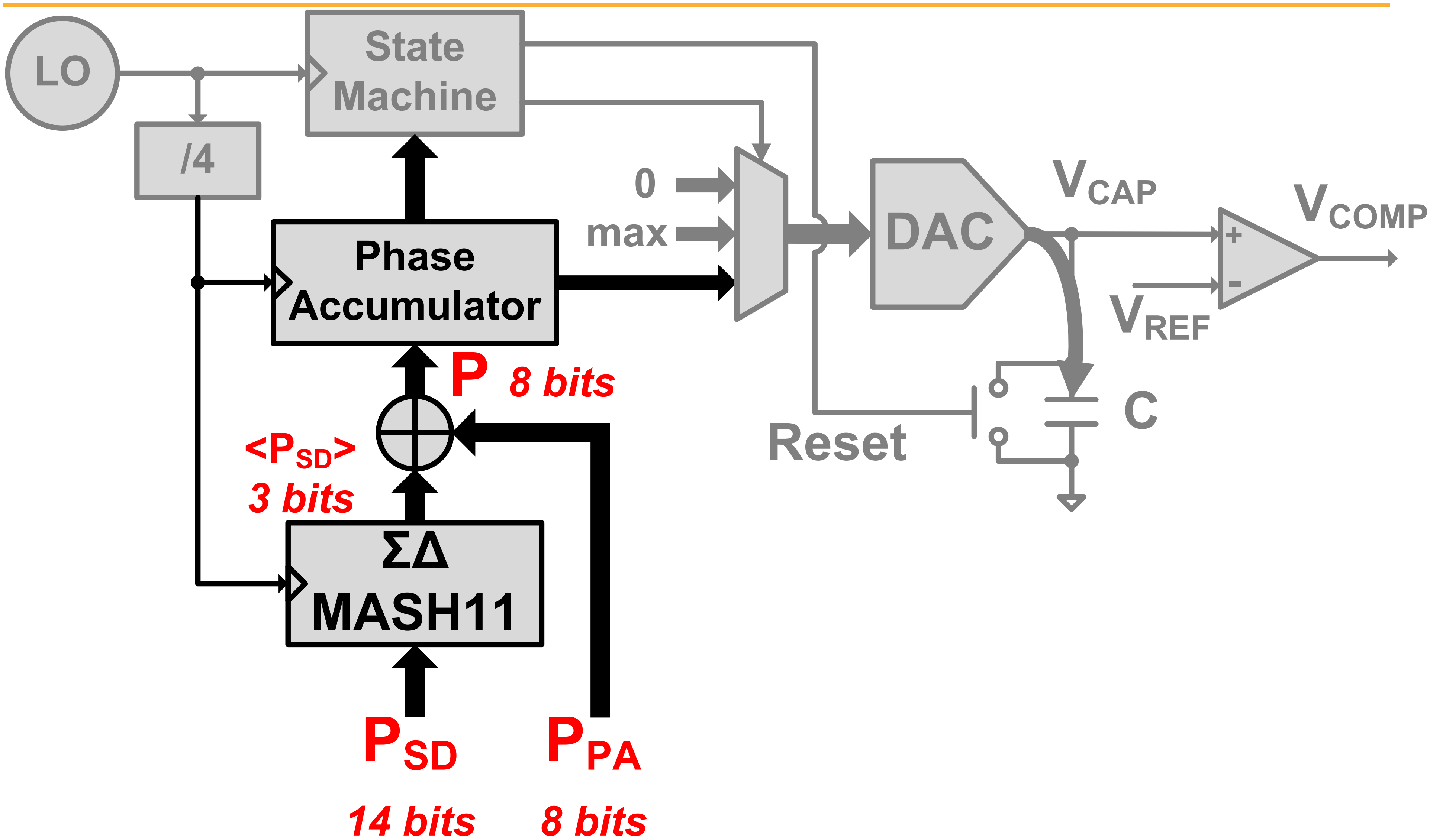
$P = 2^8-1 \rightarrow f_{DDS\_MIN} = 400$ MHz

$\Delta f \approx 500$ kHz

ΣΔ Combinations



Detailed DDS bloc Diagramm



ΣΔ advantages

- P is composed of an integer part P_{PA} and a fractional one P_{SD}

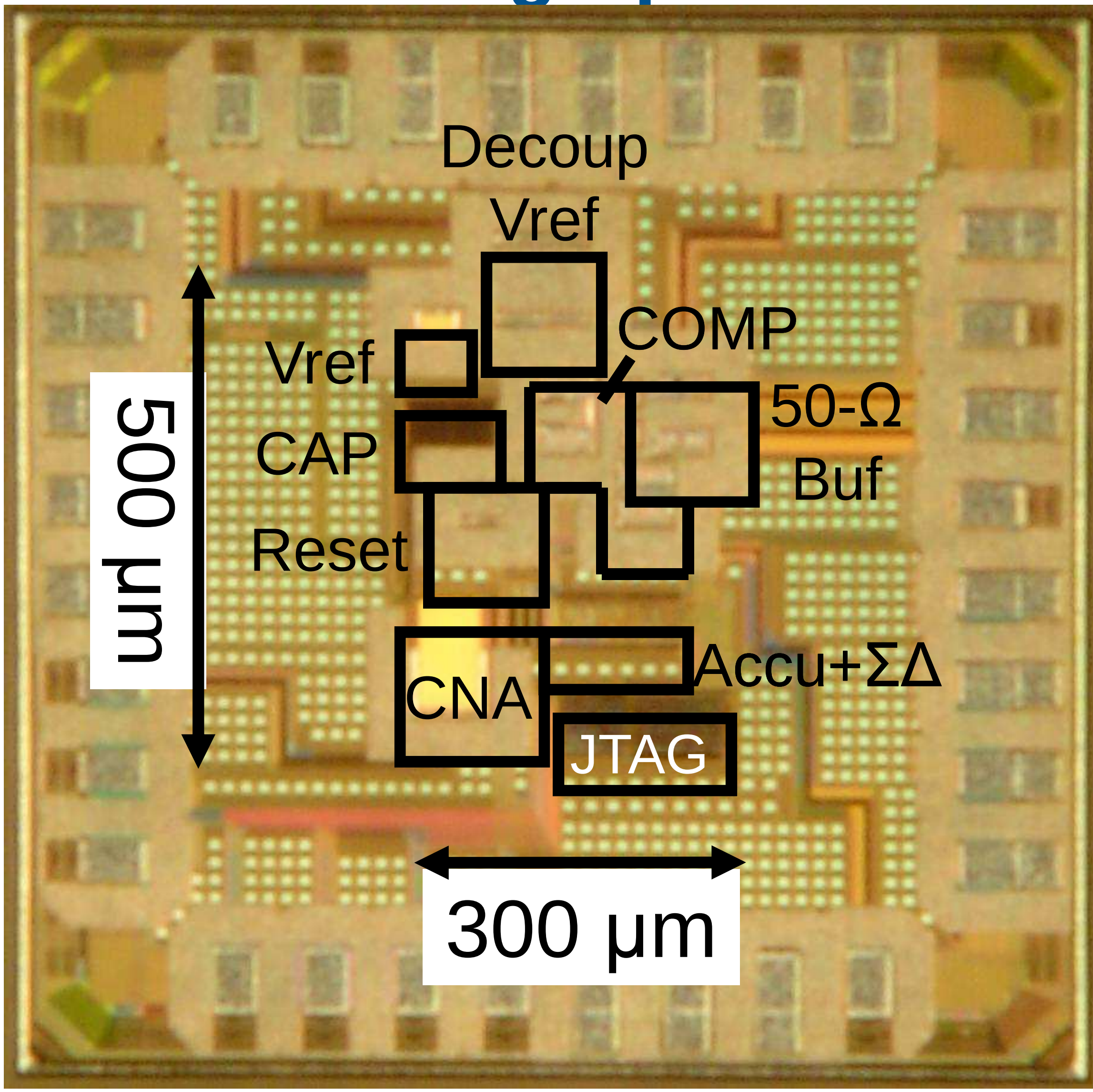
$$f_{DDS} = \frac{\frac{f_{CLK}}{4}}{\left(1 + \frac{P_{PA} + \frac{P_{SD}}{2^{13}}}{4(2^8-1)}\right)}$$

$\Delta f_{COARSE} \approx 500$ kHz

$\Delta f_{ACCURATE} \approx \Delta f_{COARSE}/2\text{\textasciicircum}13$
≈ 60 Hz

- Diminution of frequency resolution
- Quantisizer noise shaping

DDS micrograph



CMOS 65-nm STMicroelectronics

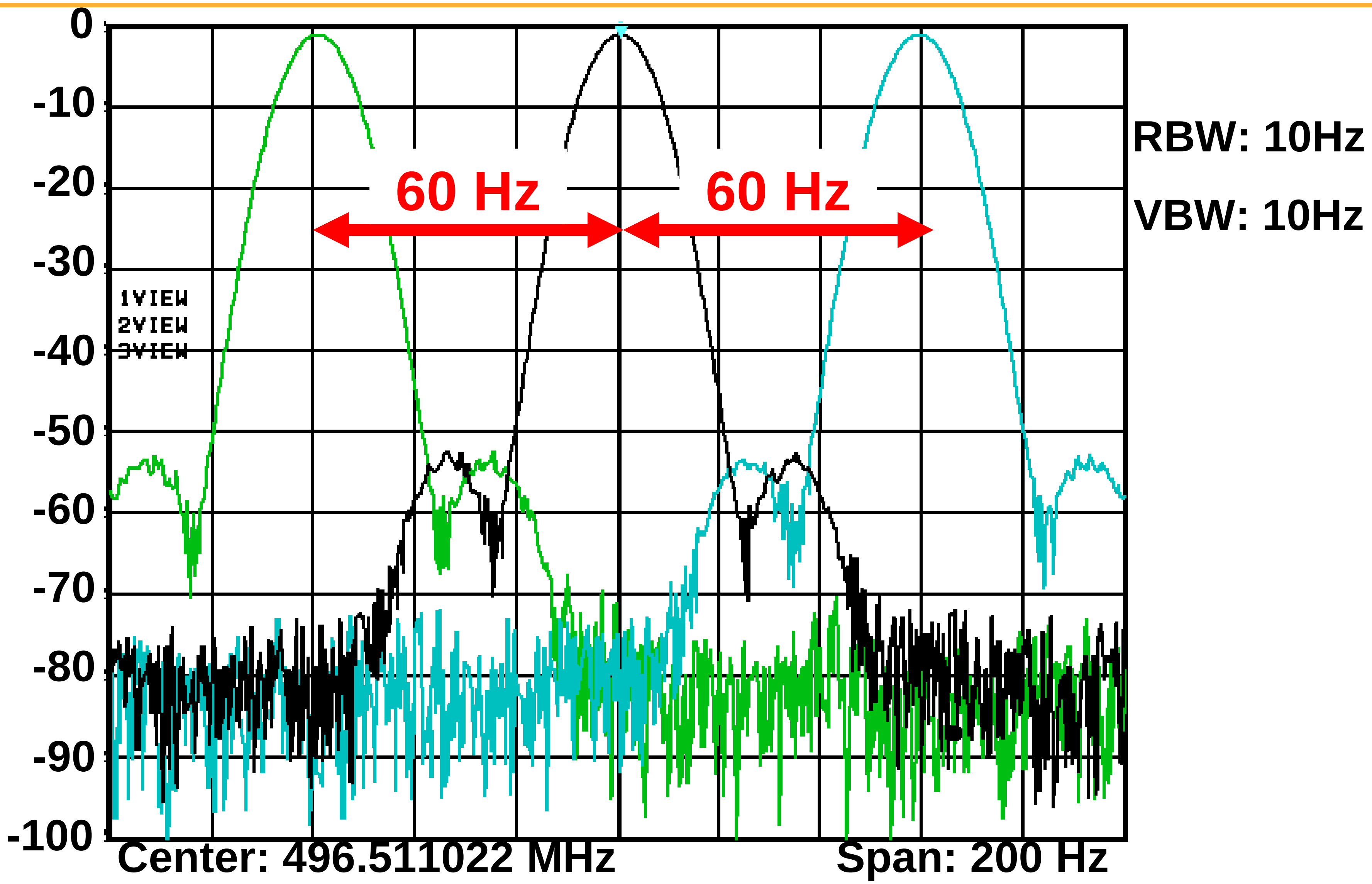
Active ara: 0.1 mm^2
Power supply: 1.2 V
Power consumption:
29 mW (without buffers)

State machine, ΣΔ,
And phase accumulator
P&R with standard cells

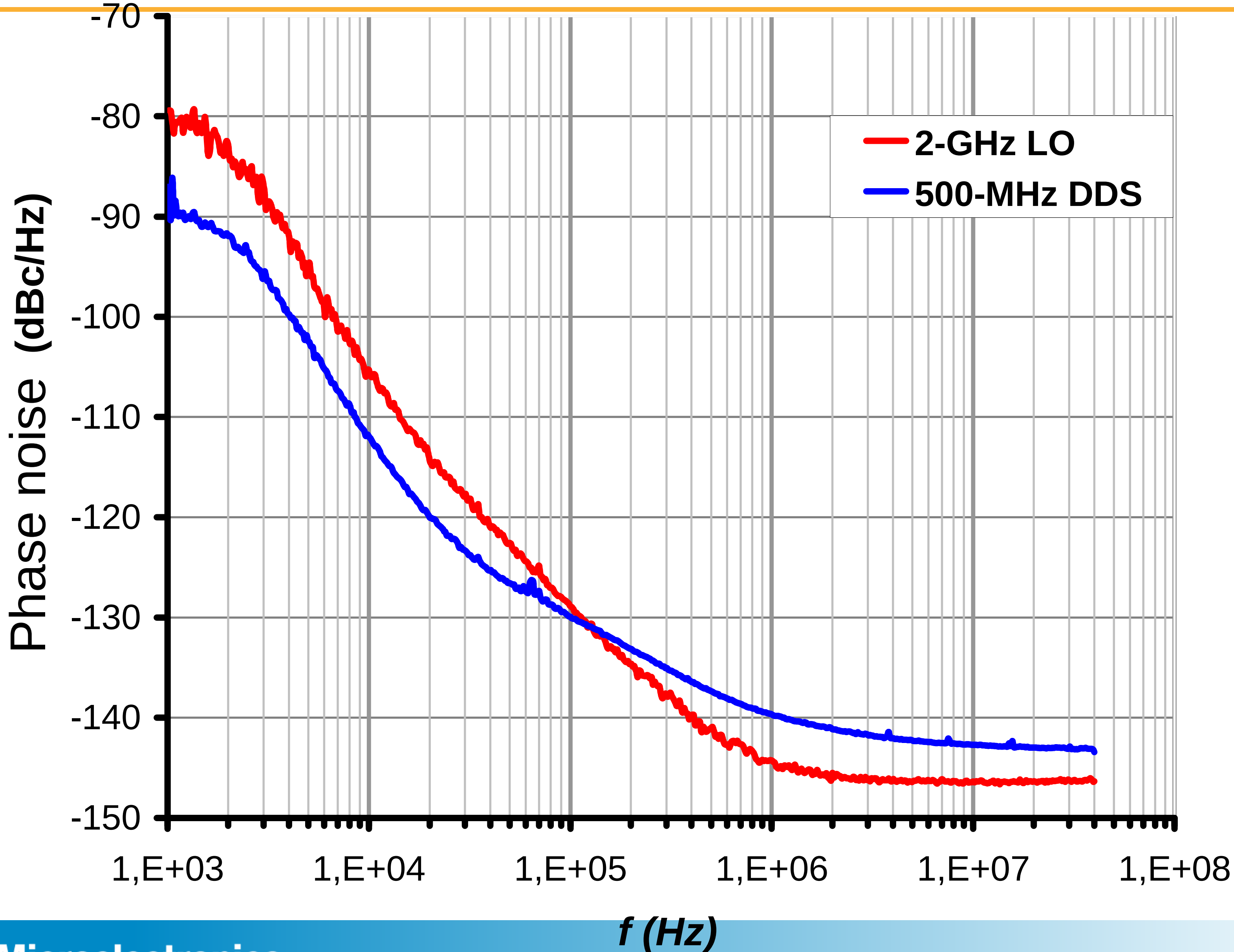
Clock
Typcal: 2 GHz
worst case: 2.8 GHz

package: TQFP 32

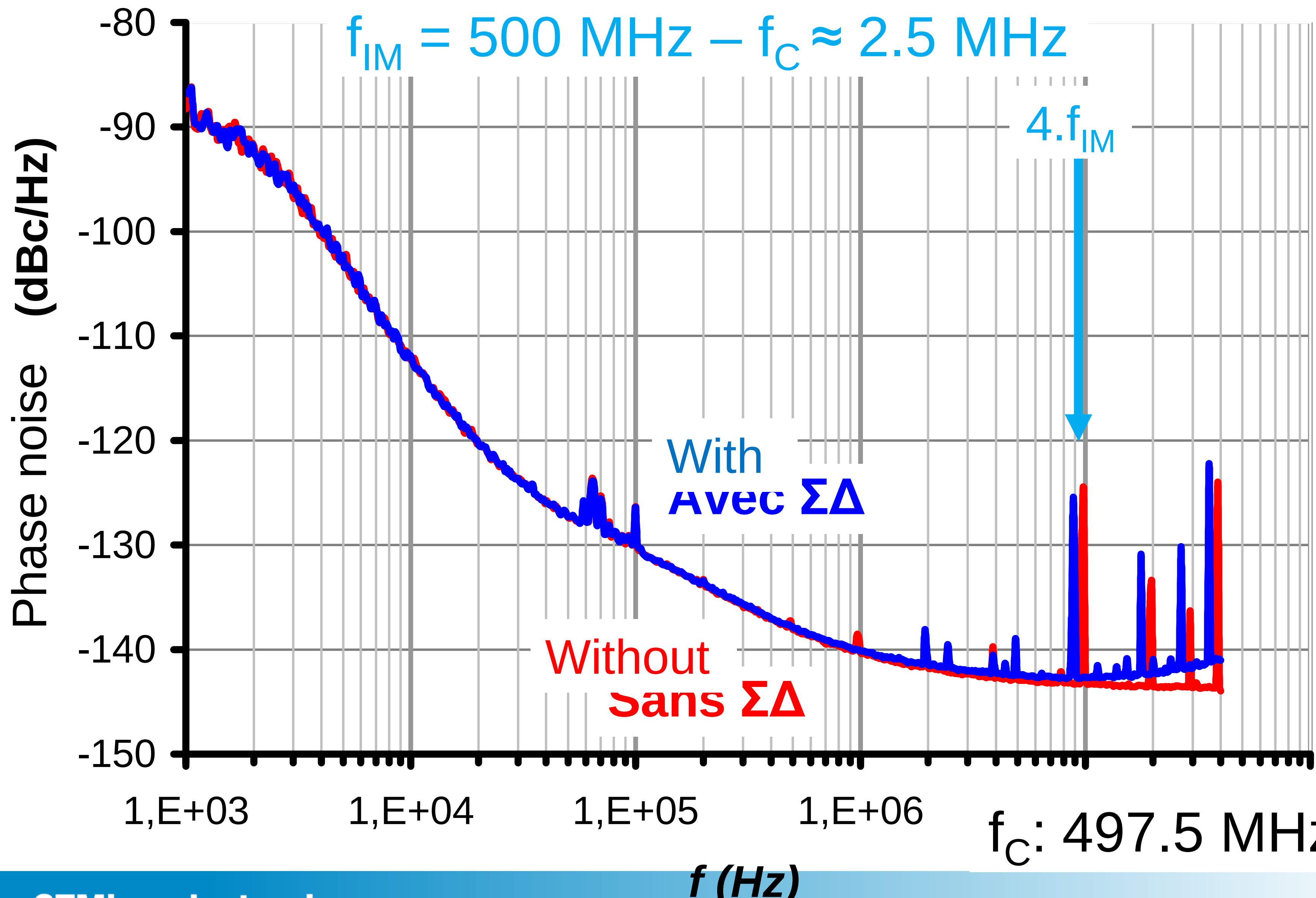
Frequency resolution



Phase Noise – LO / DDS

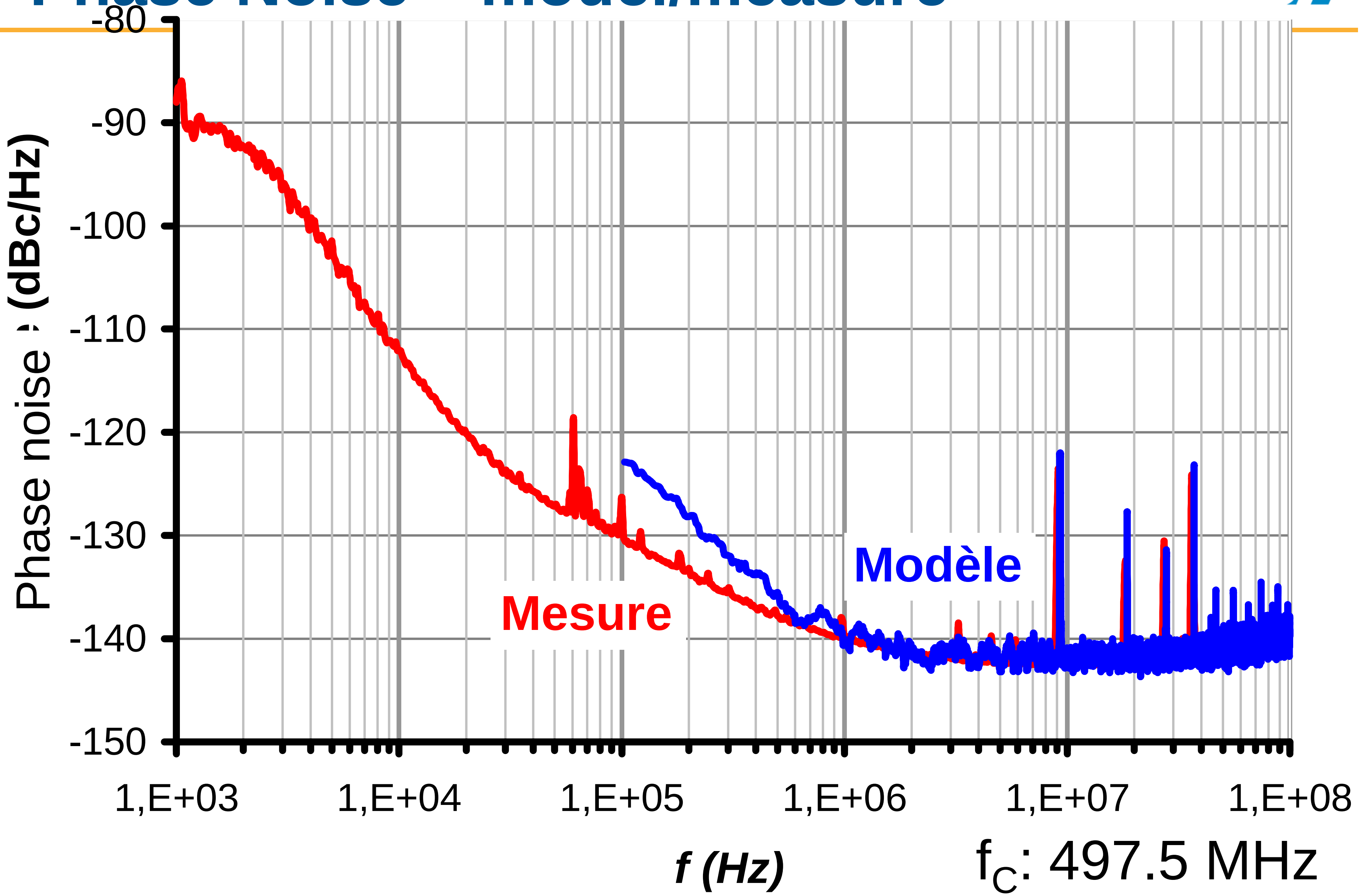


Phase noise – with/ ΣΔ



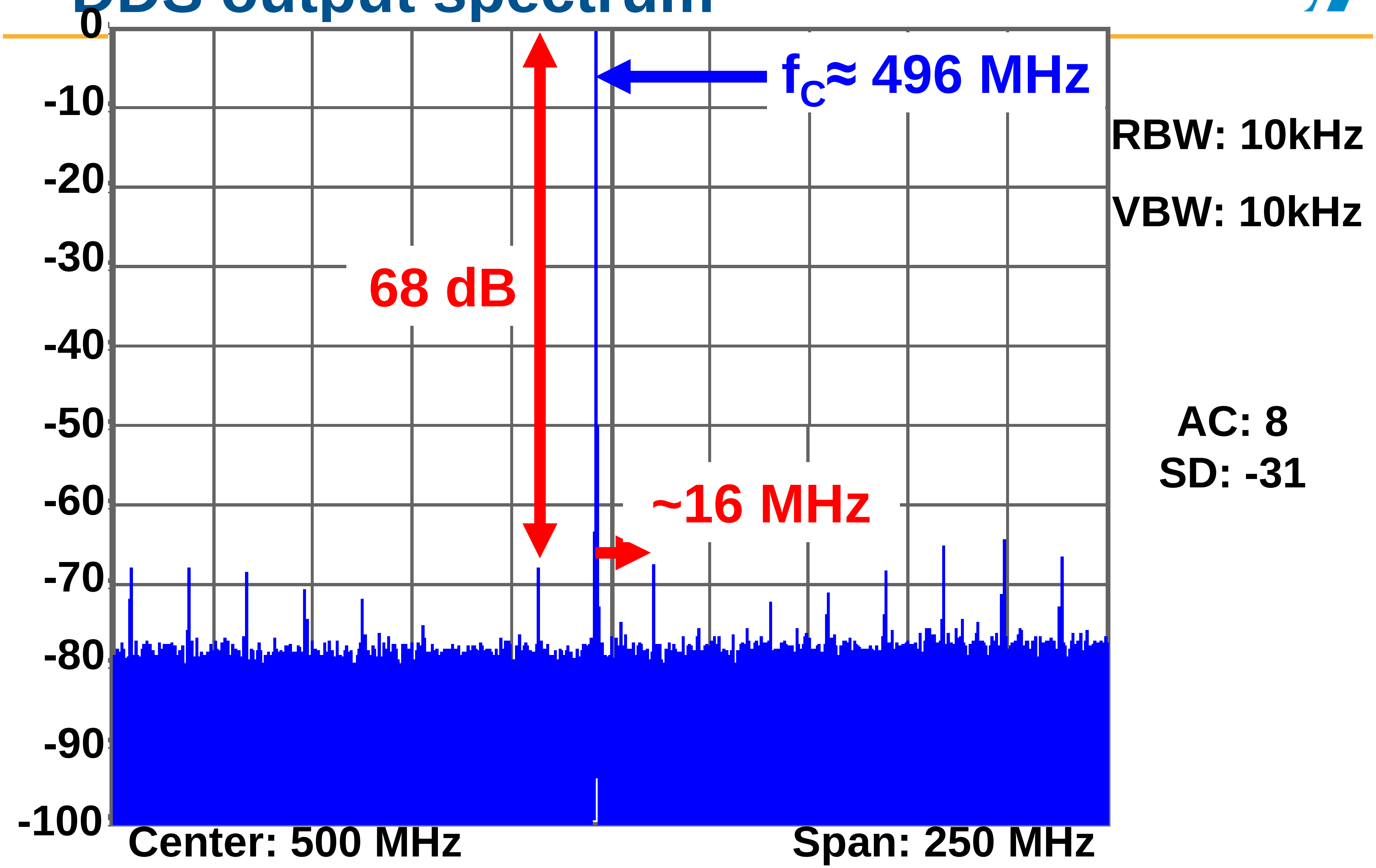
f_C: 497.5 MHz

Phase Noise – model/measure



f_C: 497.5 MHz

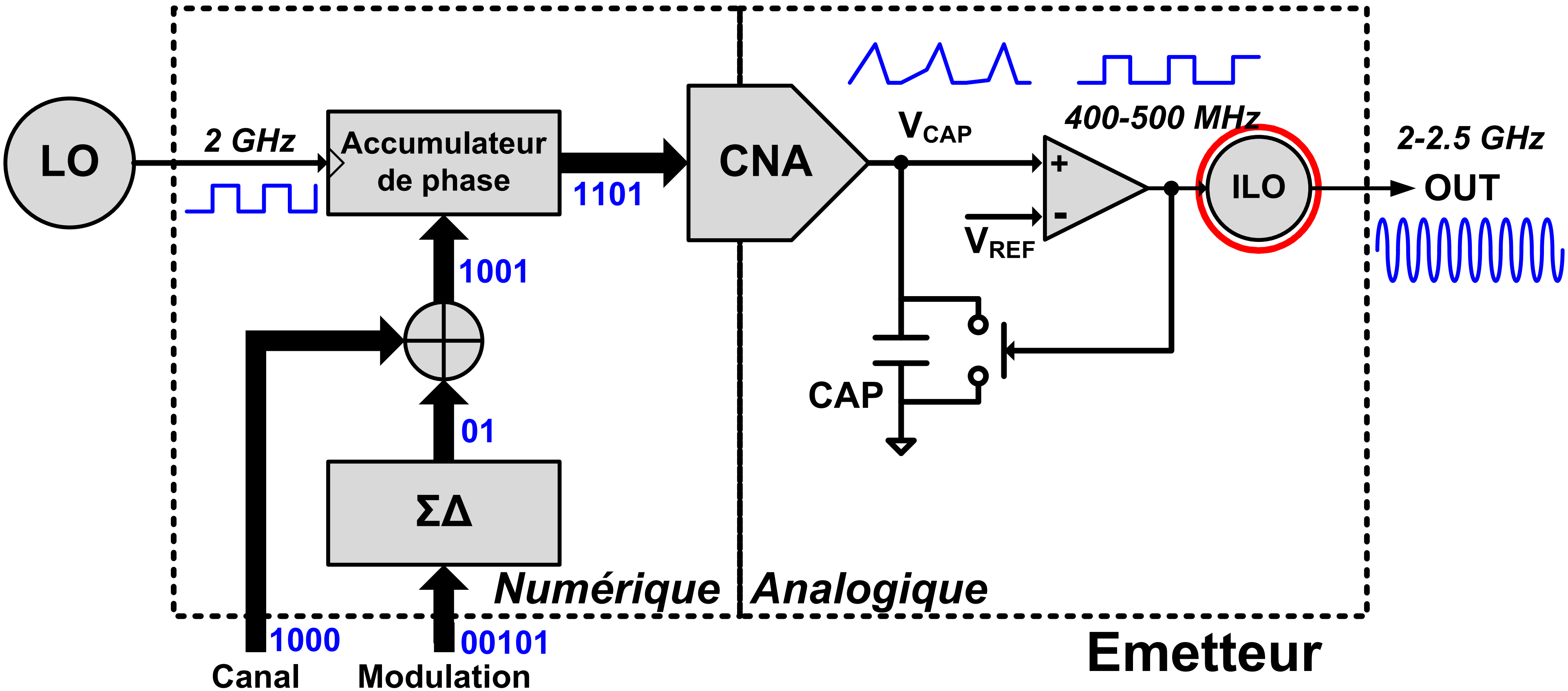
DDS output spectrum



DDS state of the art

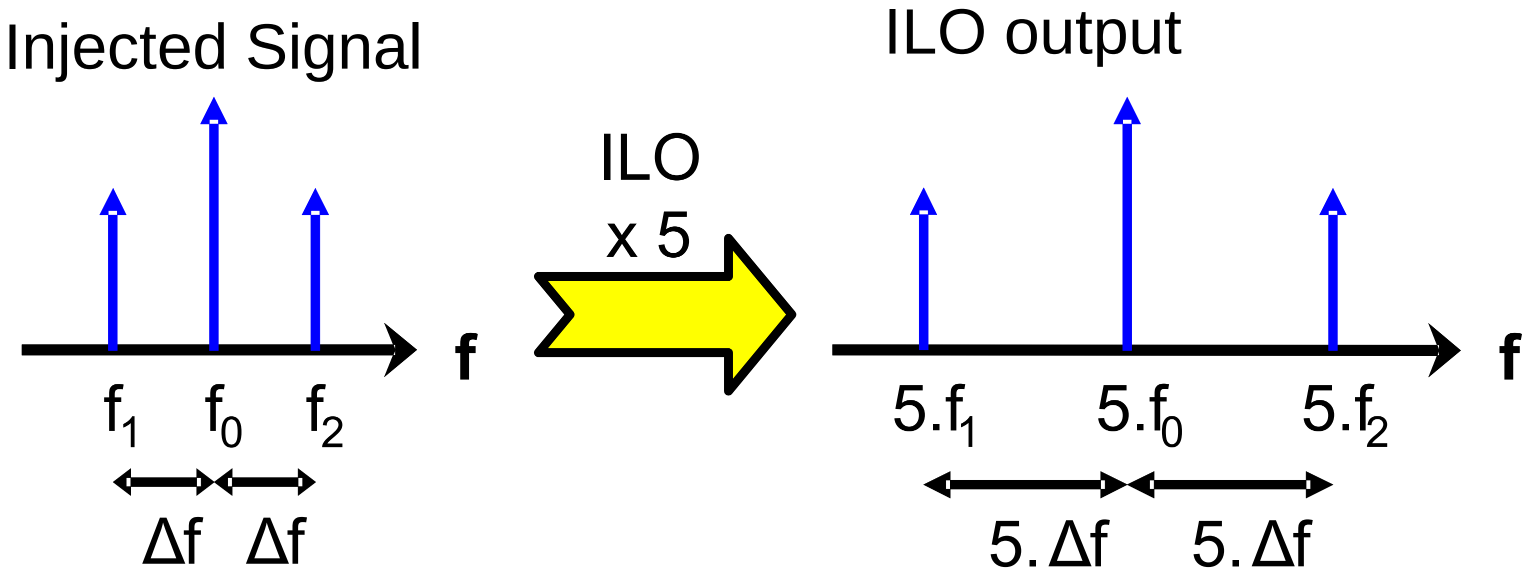
		Lindeberg *JSSC 2005*	Daï *JSSC 2006*	Strollo *JSSC 2007*	Ce travail *ASSCC 2007*
Fréquence de sortie (MHz)	Min	0	0	0	400
	Max	100	150	315	500
Fréquence d'horloge (MHz)		200	300	630	2000
Sortie		1 bit *CAN 1 bit*	1 bit *CNA 12 bits*	13 bits *quadrature*	1 bit *CNA 8 bits*
Tension d'alimentation (V)		1.5	3.3	2.5	1.2
Puissance consommée (mW)		138	200	76	29
Technologie (µm)		0.13	0.35	0.25	0.065
Surface (mm^2)		2,02	1.11	0.063	0.1
Figure de mérite (mW/MHz)		690	666	121	29

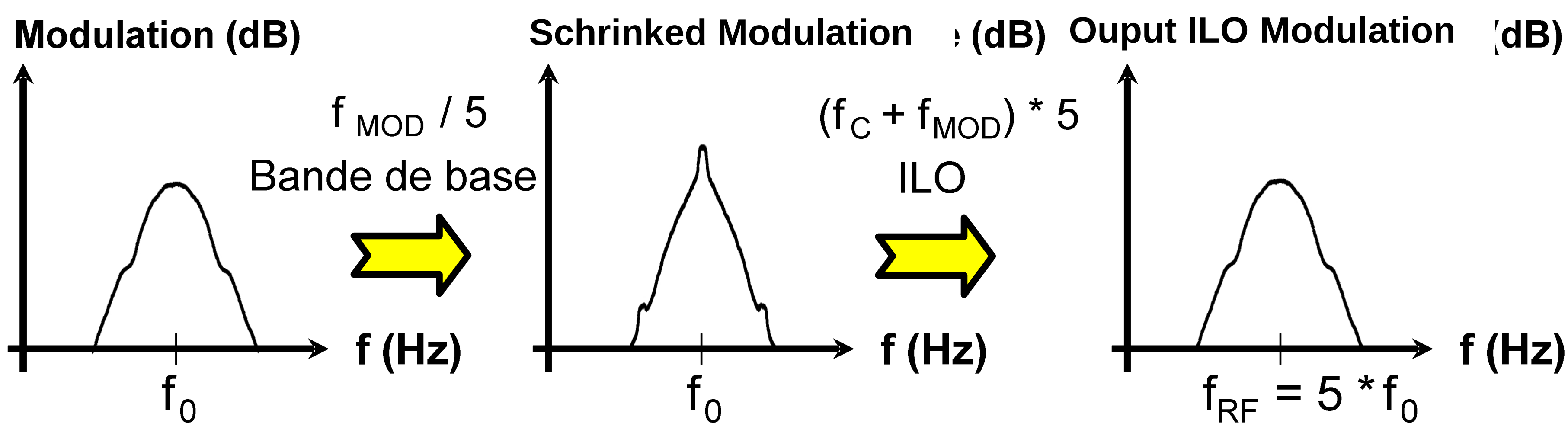
Transmitter Block Diagramm



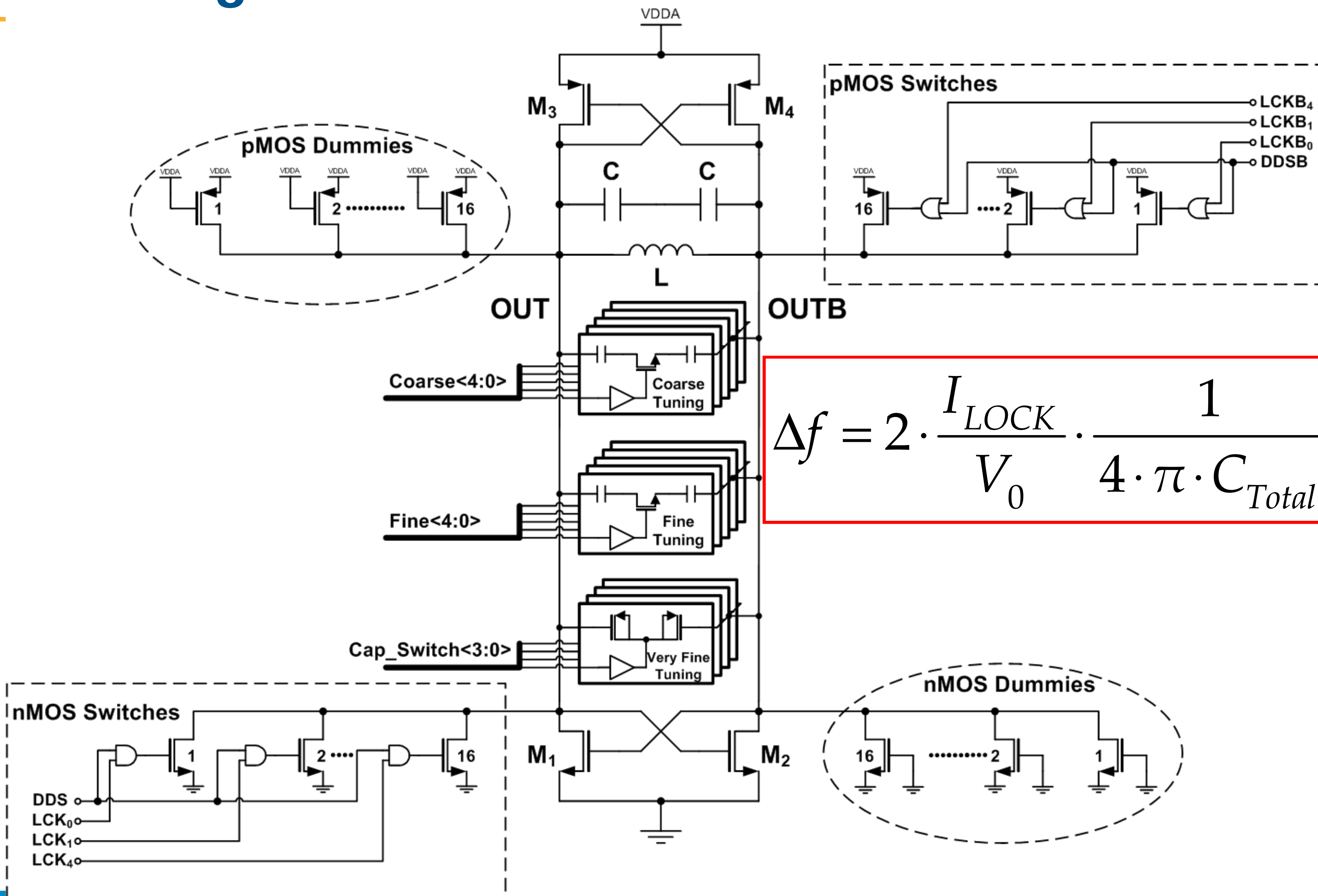
- Output Frequency Range: 2 to 2.5 GHz
- Frequency step : 300 Hz
- RF filtering provided by ILO

ILO frequency multiplication



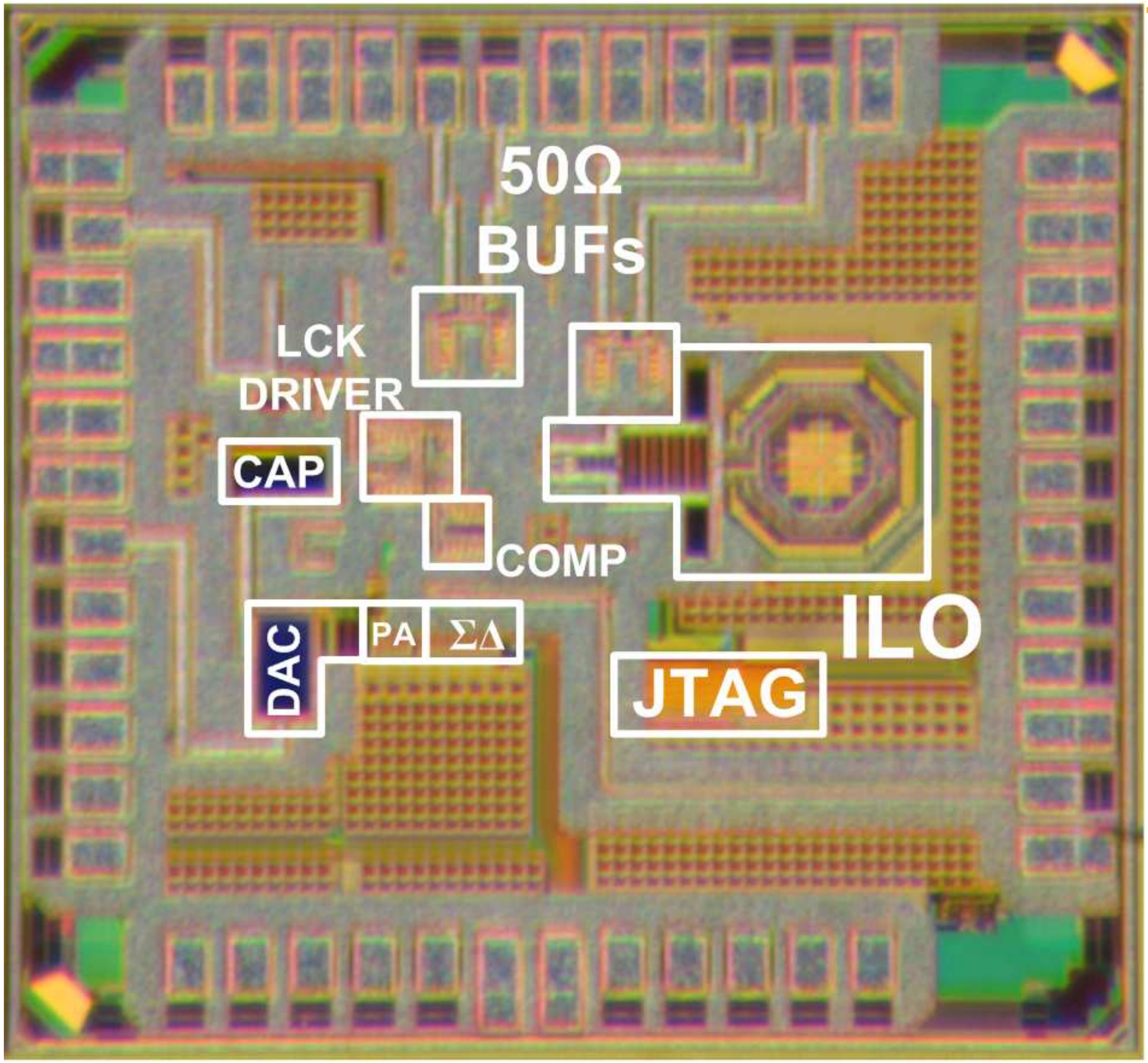


ILO Design



$$\Delta f = 2 \cdot \frac{I_{LOCK}}{V_0} \cdot \frac{1}{4 \cdot \pi \cdot C_{Total}}$$

Transmitter Micrograph



CMOS 65-nm STMicroelectronics

Active area: 0.25 mm^2

Power Supply: 1.2 V

Dissipated Power:

37 mW (without output buffers)

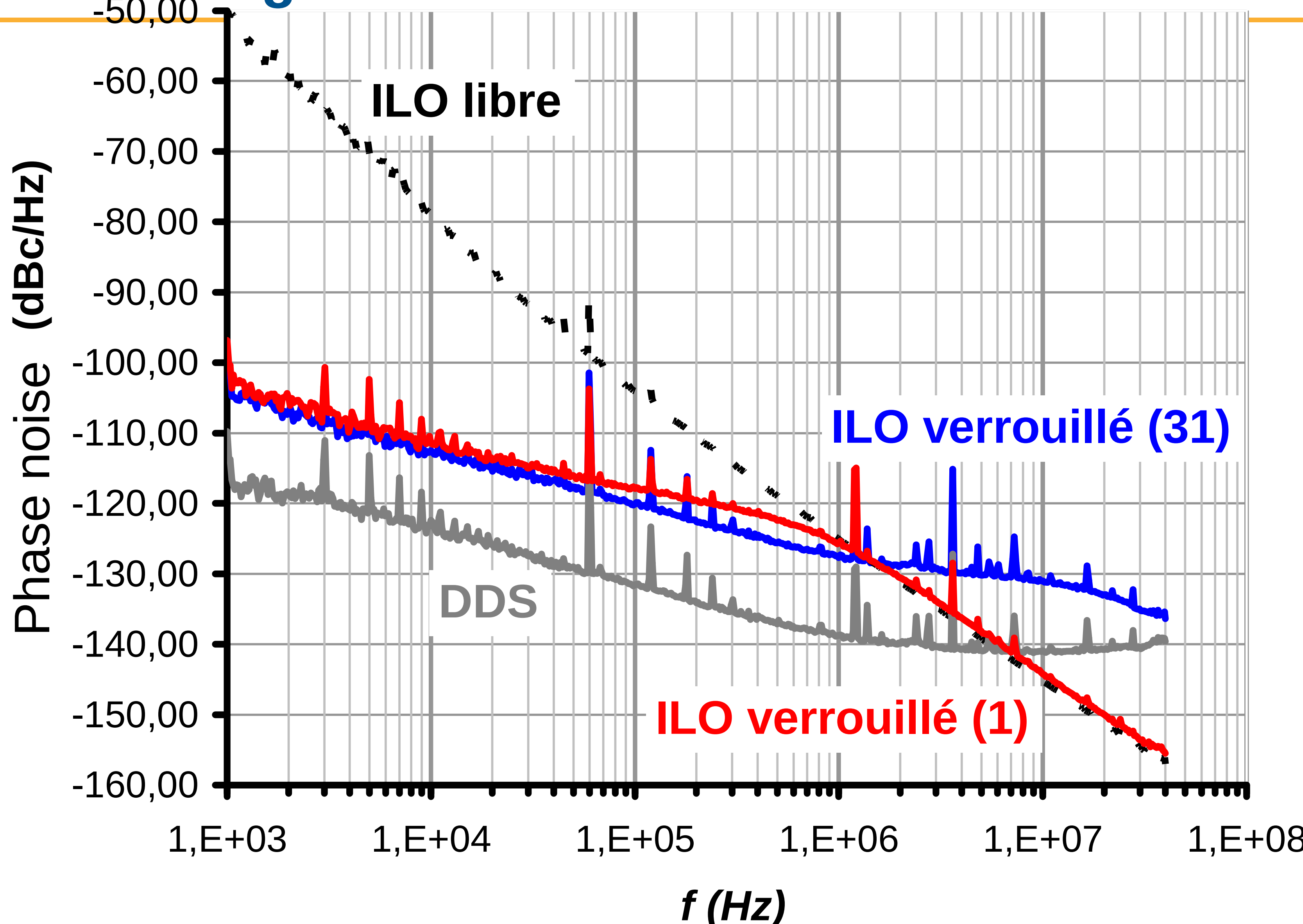
DDS + ILO

ILO locking range programmable

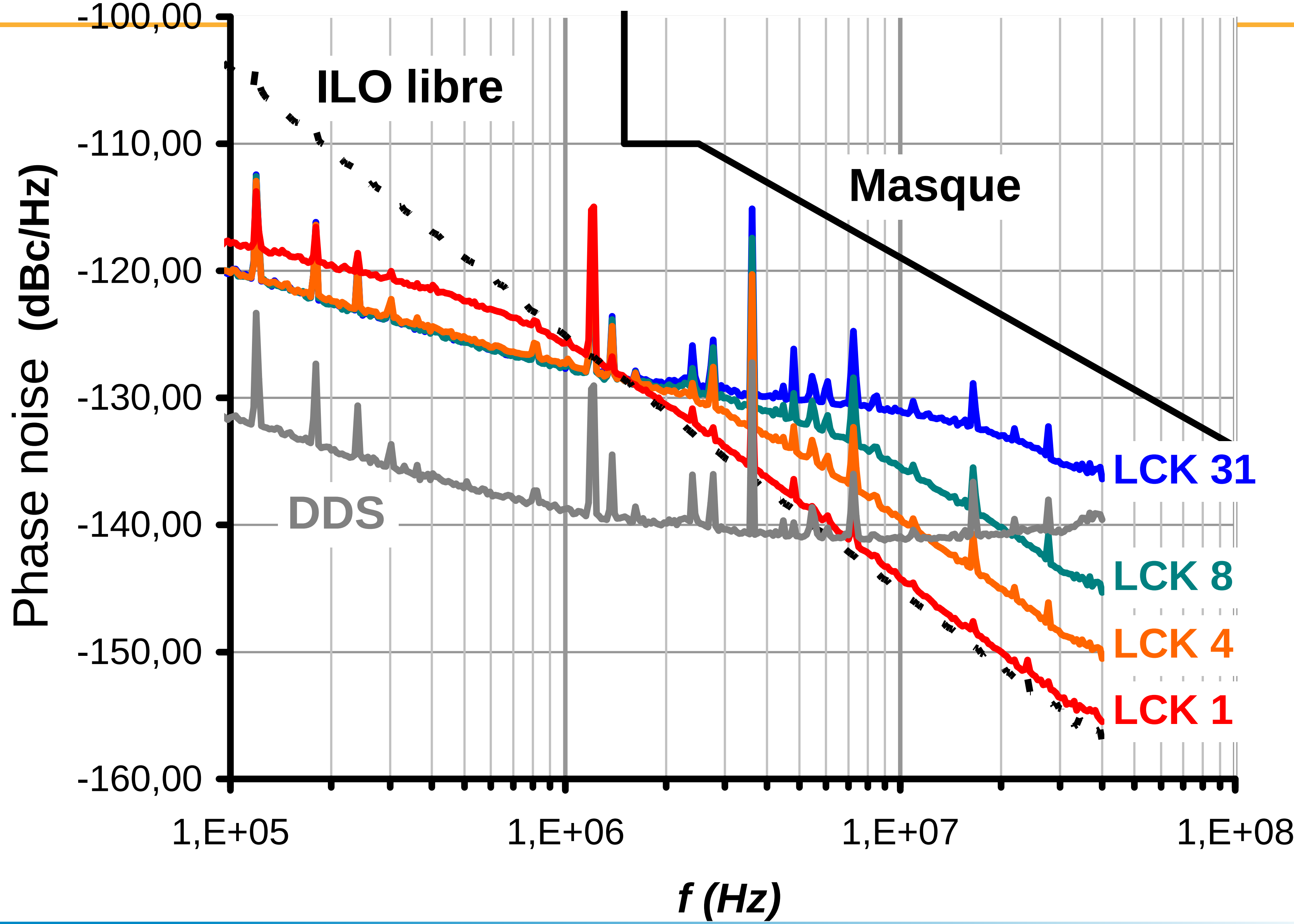
From 1 to 31 MHz

TQFP 48 package

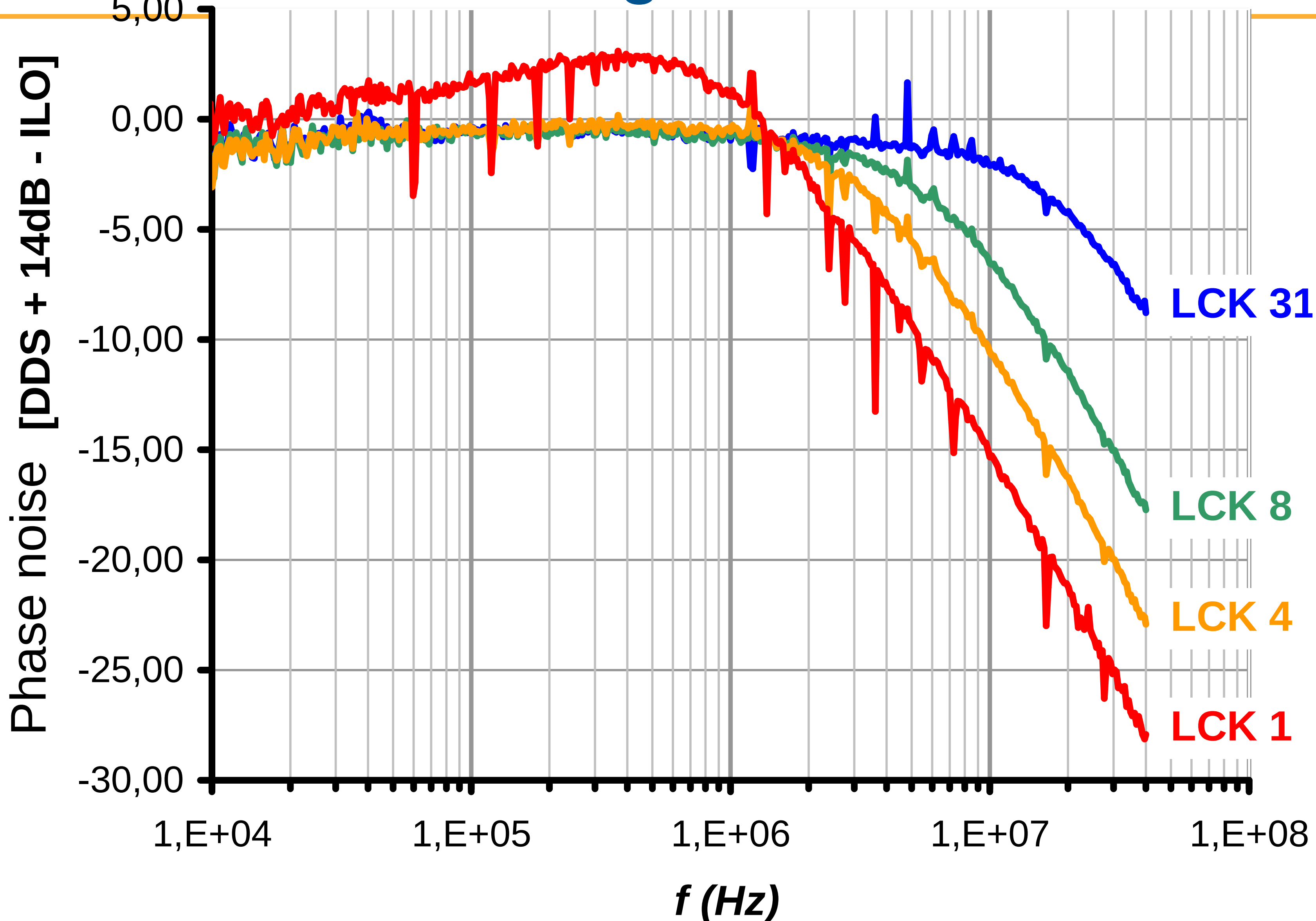
Free Running and Locked – ILO Phase Noise



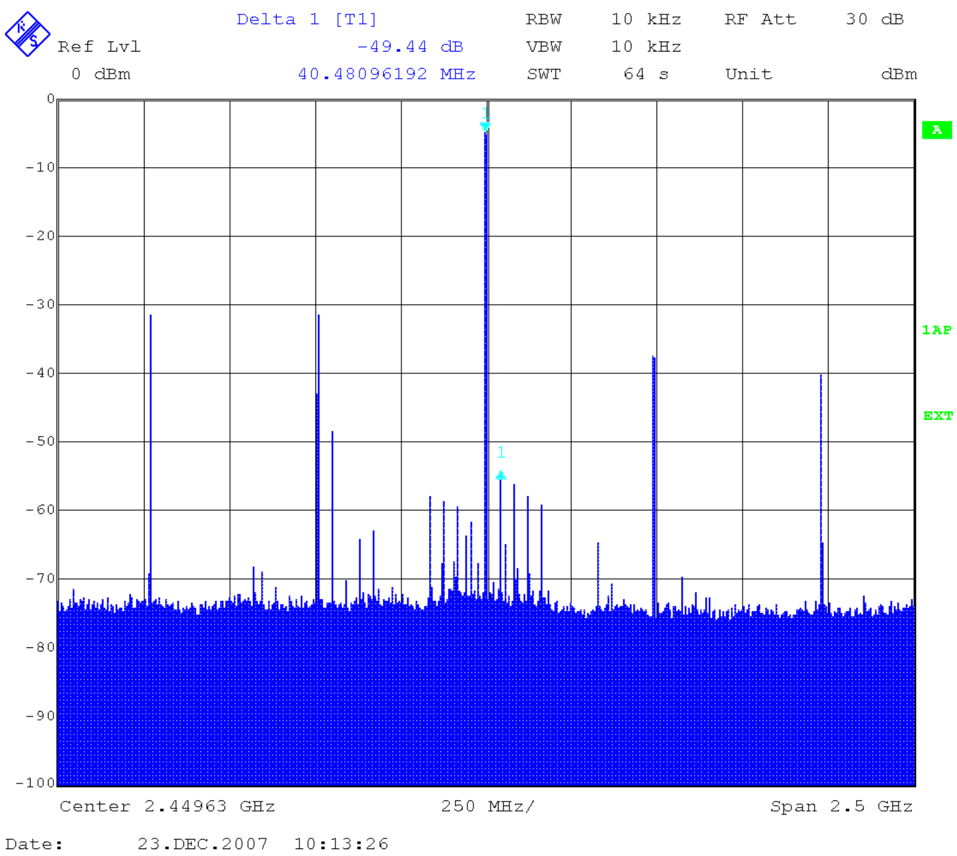
Phase Noise for different ILO locking range



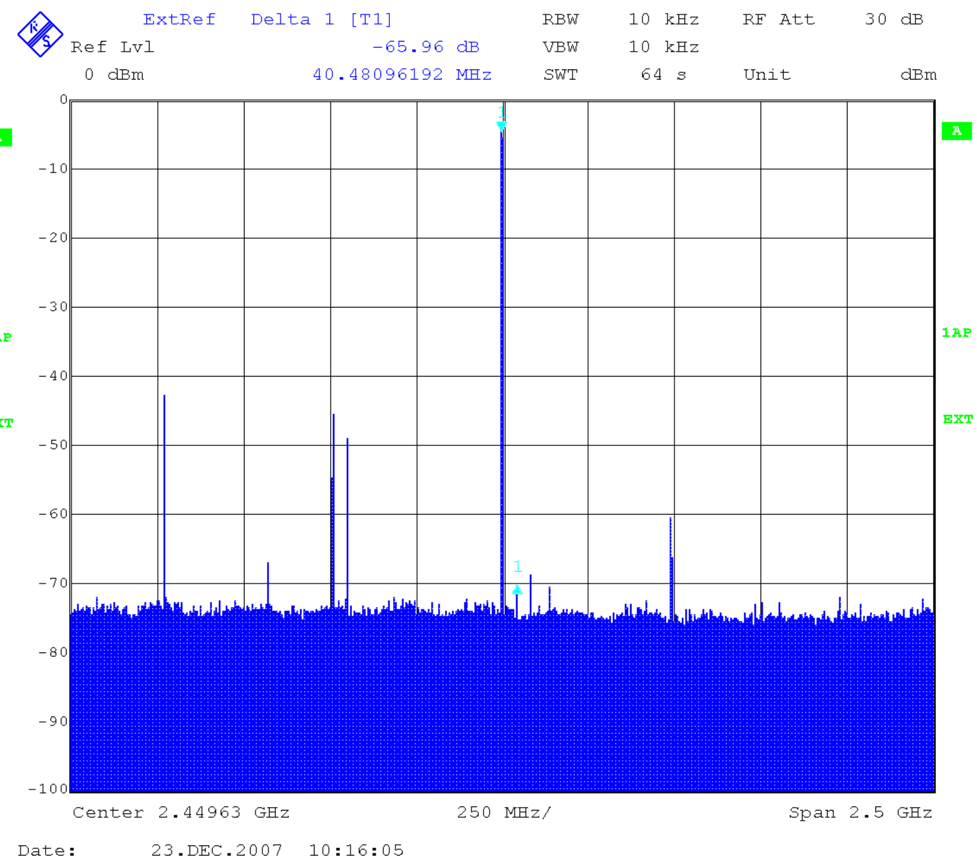
Phase Noise Filtering – ILO/DDS



Transmitter output spectrum

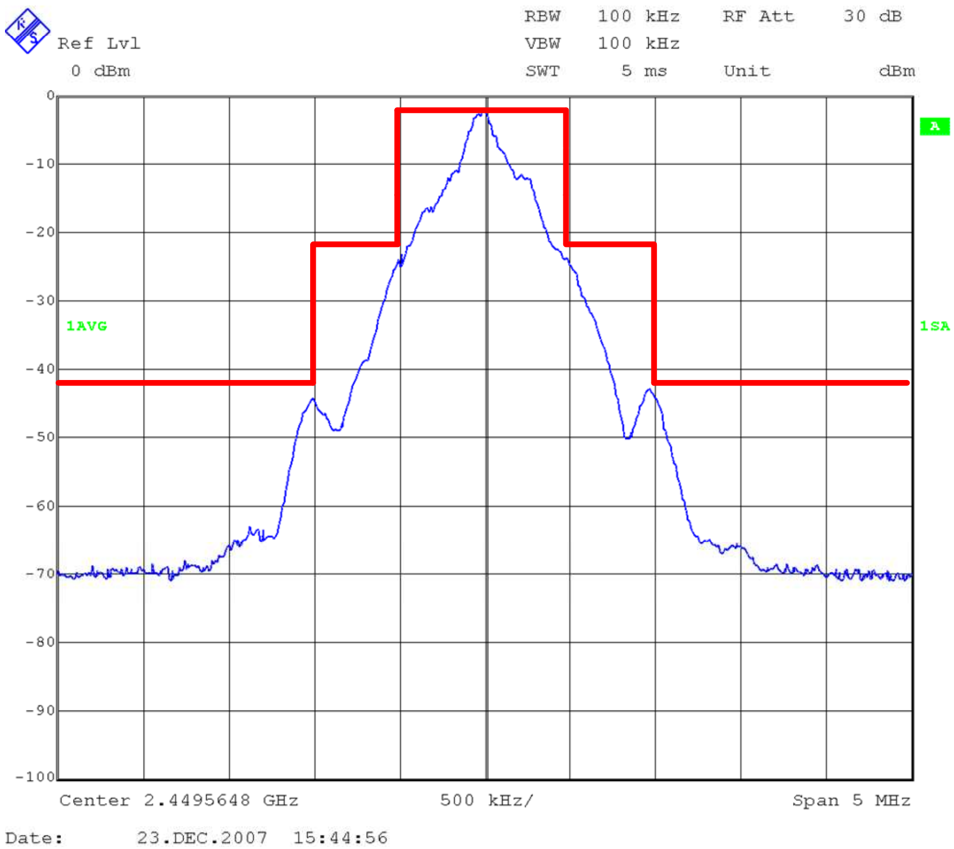


Locking Range
= 31 MHz

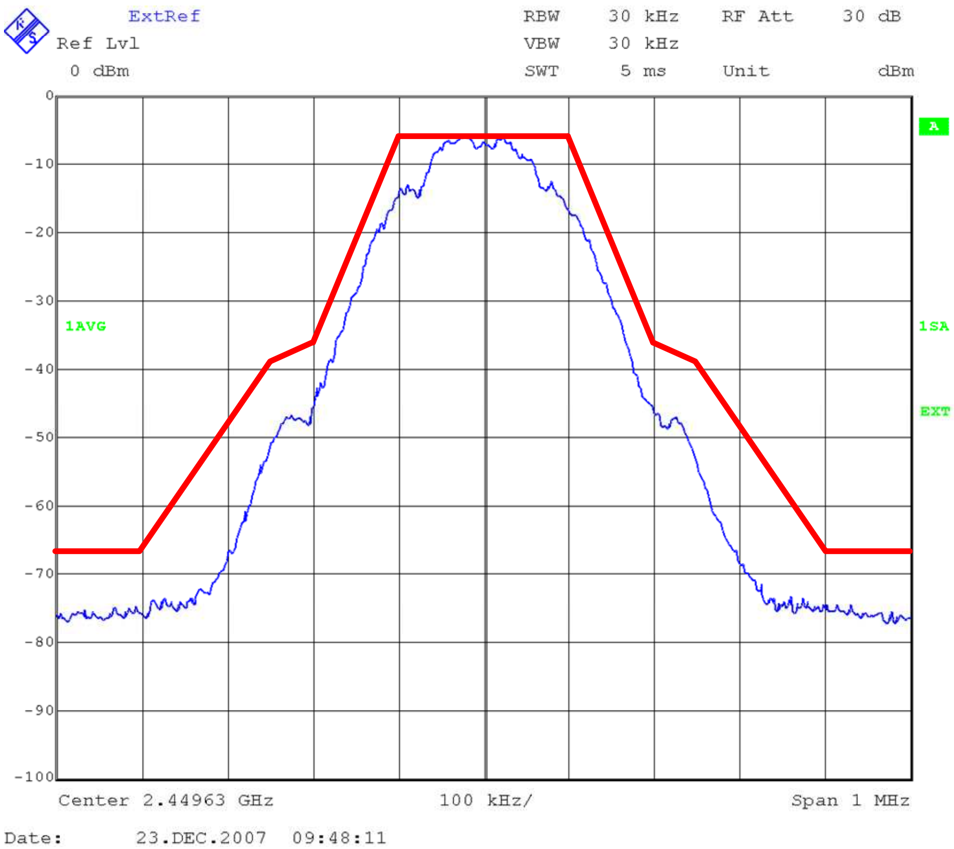


Locking Range
= 1 MHz

GSM 1 Bluetooth Modulation Plots



Bluetooth Modulation



GSM Modulation

Conclusion

- Innovative tansmitter based on Phase Shifter based pulse output DDS
- Demonstrated feasabilitty from system to silicon
  - Matlab modelization including mismatches
  - DDS measurement
    - DDS output frequency from 400 MHz to 500 MHz
    - 60 Hz frequency resolution
    - 29 mW
  - Transmitter Measurement
    - Frequency band from 2 GHz à 2.5 GHz
    - 300 Hz frequency resolution
    - 37 mw

Acknowledgements

- This presentation is based on Ph D work of L.Camino (modulation of $\Sigma\Delta$ fractional PLL) and T. Finateu (DDS –ILO based transmitter)