RF Transmitter based on Frequency Synthesizer

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Outline

- Introduction
  - Transmitter integration challenges
- Frequency Synthesizer Modulation
  - Translationnal TX loop
  - Modulation of sigma delta frequency synthesizer
  - Two point modulation
- DDS and ILO based RF transmitter
  - Injection Locked Oscillator
  - 400 MHz DDS
  - Bluetooth DDS/ILO based transmitter
I Q based RF transmitter

- General expression of signal to be transmitted

\[ RF(t) = A(t) \cos(\omega t + \varphi(t)) = A(t) \cos(\varphi(t)) \cos(\omega t) - A(t) \sin(\varphi(t)) \sin(\omega t) \]

\[ RF(t) = I(t) \cos(\omega t) - Q(t) \sin(\omega t) \]

- Principle:
  - Generation of I and Q in baseband
  - Generation of RF signal using in phase and quadrature Local Oscillator
Heterodyne Transmitter Architecture

Drawbacks:
- needs one external high Q RF filter
- Precision needed on IF image rejection mixer
- 2 LOs : 2 PLLs
- Linear PA : Power hungry
Homodyne Transmitter(1)

Architecture:
- Zero IF -> eliminates a filter
- IQ modulator shifts the spectrum of baseband signal directly to the Rf carrier frequency
Mixers:
- act as switches (lower noise)
- work better when quickly switched
- → responsible for generation of odd harmonics
- non linearity → intermodulation products
Mismatches:
- DC at mixer input -> LO leakage
- Phase and amplitude mismatch -> degrades orthogonality: IQ leakage
- need feedback or calibration to counteract mismatches
Homodyne Transmitter(4)

DAC:  - generates white noise over fs/2 bandwidth
      - ΣΔ : quantization noise pushed towards fs/2
      - output : NRZ like signal -> alias signal at each fs harmonics. (upsampling or precompensation)
      - INL, DNL -> distortion
LO and quadrature:
- LO : twice RF frequency -> minimizing pulling
- quadrature obtained using both rising and falling edge of a divider by 2.
LO and quadrature:
- any imbalance in LO rising and falling edge timing degrades LO I&Q generations -> loss of orthogonality
LO pulling:
- PA leakage could lock by injection the LO (substrate noise, power supply, modulation of LO load impedance).
- LO tracks the PA modulation especially outside PLL bandwidth. -> corrupted signal at output
Homodyne Transmitter(8)

PA and all others drivers:
- must preserve envelope -> spectral regrowth
- should be linear -> PA inefficient (40% at peak output power)
- high DC power
- power control
RF transmission using a phase and an amplitude phase

RF(t) = I(t)\cos(\omega_{RF}t) + Q(t)\sin(\omega_{RF}t)

RF(t) = A(t)\cos(\omega_{RF}t + \varphi(t))

A(t) = \sqrt{I(t)^2 + Q(t)^2}

\varphi(t) = \arctan\left(\frac{Q(t)}{I(t)}\right)
Polar Transmitter (2)

Principle :  \( |s| \leq 1 \)

- Generation of \( A \) and \( \varphi \) in baseband
- \( A \) modulate the power supply of a saturated PA (good efficiency
- \( \varphi \) is provided at RF using PLL modulation
Polar Transmitter (3)

PA:
- Better efficiency obtained with saturated PA (> 60 %)
- Modulation through a DC/DC converter -> efficiency depends on switching frequency (noise, AM bandwidth)
- Distortion for low supply voltages
- Needs of predistortion or feedback correction
Phase and amplitude combination:
- To be effective, amplitude and phase modulations should arrive in the same time.
- The phase modulator using modulated PLL brings group delay -> to be compensated
Polar Transmitter (5)

This presentation
Introduction
  - Transmitter integration challenges

Frequency Synthesizer Modulation
  - Translationnal TX loop
  - Modulation of sigma delta frequency synthesizer
  - Two point modulation

DDS and ILO based RF transmitter
  - Injection Locked Oscillator
  - 400 MHz DDS
  - Bluetooth DDS/ILO based transmitter
Offset PLL based Transmitter

- $I(n)$
- $Q(n)$
- $\text{D/A}$
- $\text{LPF}$
- $\text{IF LO}$
- $\text{PFD}$
- $\text{CP}$
- $\text{LPF}$
- $\text{RF LO}$
- $f_{RF}$
- $f_{IF}$
- $f_{VCO}$
- $PA$
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FSK modulation (1)

- FSK: Frequency Shift Keying

- Bit duration = Tb

- RF expression:

\[
RF(t) = A \cos(\omega_0 t + \pi \Delta f \int_0^t s(u) du)
\]

- Modulation index: \( h = \Delta f / fb \)

- Phase deviation over one bit: \( \pi.\Delta f. T_{bit} \)
MSK modulation

- When FSK modulation index = 0.5 -> MSK
- Phase deviation over one Tbit : 90°
GMSK modulation (2)

- FSK spectral occupation: \( \frac{2}{T_b} + \Delta f \)

- GMSK: filtering data using a Gaussian filter in order to lower the spectral occupation without information loss.
GMSK modulation (3)

\[ \text{rect} \left( \frac{t}{T_{\text{bit}}} \right) \ast \exp \left( \frac{-t^2}{2 \cdot \sigma^2 \cdot T_{\text{BIT}}^2} \right) \frac{\sqrt{2 \pi \cdot \sigma \cdot T_{\text{bit}}}}{\sqrt{2 \pi \cdot \sigma}} = f(t) \]

\[ \sigma = \frac{\sqrt{\ln(2)}}{2 \pi B T_{\text{BIT}}} \]
Fractional N PLL based Transmitter

\[ \frac{\Delta f}{2} = \frac{\Delta c}{f_{\text{REF}}} \cdot f_{\text{ref}} \]

\[ f_{\text{vco}} = (K + \frac{C_0}{f_{\text{REF}}}) \cdot f_{\text{ref}} \]
Gaussian Filter optimisation(2)

- Implementation of a digital gaussian filter

- Determination of optimal impulse response length \( L \) and oversampling coefficient \( R \).

- Coefficient number: \( R \times L \)
Gaussian Filter Optimisation(3)

- Constraints on L&R
  - $R_{\text{max}} = \frac{f_{\text{ref}}}{f_{\text{bit}}}$
  - Area occupied by digital filter
  - Phase error due to the pulse response sampling

\[ \phi_{\text{ref}}(t) \]
\[ \phi_{L,R}(t) \]
\[ f_{\text{oversampling}} = R \cdot f_{\text{BIT}} \]

modulating signal
Pseudo random
\[ a(t) \]
156 bits
\[ F_{\text{BIT}} = 270.8 \text{ kb/s} \]
Gaussian Filter Compensation

- Before comparison, filters need to be compensated in gain and group delay.
### Gaussian Filter Optimization

Table gives the quadratic phase error in degrees

<table>
<thead>
<tr>
<th>L</th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>16</th>
<th>32</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>12.9</td>
<td>10.2</td>
<td>9.6</td>
<td>9.5</td>
<td>9.4</td>
</tr>
<tr>
<td>2</td>
<td>3.9</td>
<td>2.74</td>
<td>2.46</td>
<td>2.39</td>
<td>2.37</td>
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<tr>
<td>3</td>
<td>1.7</td>
<td>0.56</td>
<td>0.29</td>
<td>0.23</td>
<td>0.22</td>
</tr>
<tr>
<td>4</td>
<td>1.6</td>
<td>0.39</td>
<td>0.10</td>
<td>0.04</td>
<td>0.03</td>
</tr>
<tr>
<td>5</td>
<td>1.6</td>
<td>0.38</td>
<td>9.9E-2</td>
<td>3.8E-2</td>
<td>3.1E-2</td>
</tr>
<tr>
<td>6</td>
<td>1.6</td>
<td>0.38</td>
<td>9.9E-2</td>
<td>3.8E-2</td>
<td>3.1E-2</td>
</tr>
</tbody>
</table>

- L=3 R=8 has been chosen
GMSK Modulator Implementation (1)

- Gaussian filter of 3-bit impulse response could be seen as a sliding window of 3 bits and that concerns 4 bit

- Idea: store in a ROM the filter response over 4 bits sequences (16 possibilities)
GMSK Modulator implementation (2)

Digital Gaussian Filter

Modulating signal

Counter

Fref

ROM

Principal address

Secondary address

n bits

p bits

Fref

m bits

D

D

D

D
GMSK modulator implementation (3)
PLL bandwidth influence on modulation

Reference phase trajectory

PLL

PLL output phase trajectory

\[ \int_{0}^{\tau} x^2 \, dx \]

\[ \epsilon_{\theta p} \]
PLL bandwidth influence on phase noise

Graph showing the phase noise in dBc/Hz as a function of frequency (f/f₀ in Hz) for different bandwidths (B) and GSM parameters (D). The graph includes curves for bandwidths of 50 kHz, 100 kHz, 150 kHz, 200 kHz, 250 kHz, and 300 kHz.
PLL bandwidth tradeoff

Integrated error decreases with PLL bandwidth

Phase noise increases with PLL bandwidth
PLL bandwidth effect on GSMK modulation
Predistortion filter to counteract the PLL bandwidth effect

- Needs to know and control the PLL transfer bandwidth over PVT -> rather complicated
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Two Point Modulation Architecture

- Principle: PLL is a high pass filter for VCO noise and a low pass filter for divider noise.
- Idea: apply modulation on both divider and VCO to enlarge the modulation bandwidth
Modulated Divider Small Signal Model

- Frequency step at divider output:
  \[ df = \frac{f_{VCO}}{N+1} - \frac{f_{VCO}}{N} \approx -\frac{f_{VCO}}{N_{avg}} \approx -\frac{f_{Ref}}{N_{avg}} \]

- Frequency modulation due to divider modulus deviation:
  \[ df_{ref}(t) = -n(t) \cdot \frac{f_{ref}}{N_{avg}} \quad m(t) = n(t) \cdot f_{ref} \]

- Integration in z domain then in laplace domain leads to:
  \[ d\phi(p) = -2\pi \frac{m(p)}{p} \cdot \frac{1}{N_{avg}} \]
- Modulation applied on another VCO varactor
- Modulation applied on feedback loop divider: modulates the frequency, need thus to be integrated in phase noise model
Two Point Modulation: small signal analysis (1)

- Output response for VCO modulation:
  \[ \phi_{out1} = 2\pi K_v v_2 G_v \frac{m(p)}{p} \frac{1}{1 + BO(p)} \]

- Output response for divider modulation
  \[ \phi_{out2} = G_{Div} \frac{m(p)}{p} \frac{BO(p)}{1 + BO(p)} \]

- Output response for modulation applied on both inputs
  \[ \phi_{out} = \phi_{out2} + \phi_{out1} = 2\pi \frac{m(p)}{p} \left( \frac{G_v K_v v_2 + G_{div} BO(p)}{1 + BO(p)} \right) \]
Two Point Modulation: small signal analysis (2)

- If $G_{\text{div}} = 1$ and $G_{v} = 1/K_{v^2}$:

  $\phi_{out} = 2\pi \frac{m(p)}{p}$

- It is thus possible to use a frequency synthesizer as a modulator even for bandwidth signal greater than the PLL bandwidth.

- Accuracy of the method depends strongly on the accuracy of the gain $G_{v}$ that should equal to the $1$ over the VCO gain.
Example: GMSK modulation

- GFSK 1Mb/s – modulation index 0.33
- Gaussian filtering index $BT = 0.5$
Bluetooth specifies minimum openings of transmitted data eye diagram.

- Bluetooth specifies minimum openings of transmitted data eye diagram.
PLL test bench
Modulation gain vs gain on VCO
Effect on eye Diagram

Modulation on divider only

Modulation on VCO

Output PLL Modulation
Precision on VCO gain

- Precision on VCO gain degrades eye opening -> precision needed of 5%
- Need to calibrate the VCO gain before each transmission in a new channel
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Research context

- Frequency synthesis and transmitter trend
  - All digital
  - Re-configurability: going towards SDR: Software Defined Radio

- Try to be competitive with all digital PLL

- Applications: phase modulator to be able to be embedded in polar TX – Able to transmit constant phase envelope modulations (GSM, Bluetooth...)

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Proposed Architecture

- Fully Integrated Bluetooth transmitter:
  - Fully integrated Reference Oscillator (based on BAW oscillator for example)
  - RF – DDS generating 500 MHz signal
  - Injection Locked Oscillator as a frequency multiplier

- Advantages:
  - No feedback loop
  - Fully integrated
  - Could be quickly powered on
  - Low phase group delay -> easy to handle within polar TX
### Proposed Architecture

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![Proposed Architecture Diagram]
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Injection Locking Phenomenon

 Locked oscillator acts as a 1\textsuperscript{st} order PLL

Phase noise

- Free running oscillator
- Injected signal
- Locked oscillator

SSB phase noise

Free running oscillator

Locked oscillator

Injected signal

Locked oscillator tracking bandwidth

Locking range $\Delta f$

Low limit

Middle band

High limit

$f_L$, $f_0$, $f_{LOCK}$, $f_H$, $f_{n}$
Solid fact

- Oscillator frequency is function of admittance load $Y_0 \Rightarrow f_{\text{ILO}} = \text{fct}(Y_0)$

\[
E_F = \left. \frac{\partial f}{\partial Y} \right|_{Y=Y_0} = |E_F| \cdot e^{i\beta}
\]

Hypothesis

- Injected signal at $f_{\text{LOCK}}$ in the vicinity of $f_0$
- $I_{\text{LOCK}}$ magnitude small enough to not modify $V_0$ magnitude

Assumption

- Locking source modeled by a small load admittance variation $dy$
Hunton & Weiss theory leads to:

**ILO output phase**

\[
\frac{1}{2\pi} \cdot \frac{d\phi}{dt} = (f_{\text{LOCK}} - f_0) - \frac{|E_F| \cdot |I_{\text{LOCK}}|}{|V_0|} \cdot \cos(\phi + \beta)
\]

\[\phi = \phi_{\text{LOCK}} - \phi_{\text{ILO}}\]

**ILO locking range**

\[
\Delta f = 2 \cdot \frac{|E_F| \cdot |I_{\text{LOCK}}|}{|V_0|}
\]

Constant depending on oscillator structure and locking process.
ILO Modulation

Modulated locking signal phase
\[ \phi_{\text{LOCK}}(t) = 2\pi f_{\text{LOCK}} t + m(t) \]

ILO output phase once locked
\[ \phi_{\text{ILO}}(t) = 2\pi f_{\text{LOCK}} t + n(t) - \phi_0 \]

\[
\frac{1}{2\pi} \frac{d\phi}{dt} = \left[ f_{\text{LOCK}} + \frac{1}{2\pi} \frac{dm(t)}{dt} \right] - f_0 - \frac{|E_F| |I_{\text{LOCK}}|}{|V_0|} \cdot \cos(\phi + \beta)
\]

\[ \phi(t) = \phi_{\text{SYNC}}(t) - \phi_{\text{ILO}}(t) = m(t) - n(t) + \phi_0 \]

Assuming a small tracking phase error
\[
\frac{1}{2\pi} \frac{dn(t)}{dt} = f_n \cdot [m(t) - n(t)]
\]

**Fourier Transform**
\[
n(f) = \frac{1}{m(f)} \cdot \frac{1}{1 + j \cdot \frac{f}{f_n}}
\]

\[ f_n = \sqrt{\frac{(\Delta f)^2}{4} - (f_{\text{LOCK}} - f_0)^2} \]
Tracking Phase Modulation

Ability to track phase modulation

\[
\frac{n(f)}{m(f)} = \frac{1}{1 + j \cdot \frac{f}{f_n}}
\]

ILO tracks modulation

ILO filters modulation

20.\log \frac{n(f)}{m(f)}

0 dB

\(f_{\text{LOCK}}\)

\(f_n\)

-20 dB/dec

ILO tracking bandwidth

\(\log_{10}(f)\) (Hz)
Tracking bandwidth depends on the difference between the Injected signal frequency and the ILO free running frequency.

\[ f_n = \sqrt{\frac{(\Delta f)^2}{4}} - (f_{\text{LOCK}} - f_0)^2 \]

- **ILO Tracking Bandwidth**
- **Locked oscillator tracking bandwidth**
- **GMSK modulation**
- **ILO bandwidth**

**ILO locking range**
2-GHz Injection Locked Oscillator Design

\[ \Delta f = 2 \cdot \frac{I_{\text{LOCK}}}{V_0} \cdot \frac{1}{4 \cdot \pi \cdot C_{AB}} \]

\[ C_{AB} = C + C_{M1} + C_{M2} + C_{\text{PARASITIC}} \]

\( \Delta f \) parameters known

\( \Rightarrow \) Optimized design possible
Injection Locking by a Sub-harmonic

- **Fundamental Injection Locking**: dB vs. f
- **Sub Harmonic Injection Locking**: dB vs. f

- **Free running oscillator**
- **Injected signal**

Locked oscillator voltage

Locking current

- Locking source rich in \( n^{th} \) harmonic

\[
I_N = I_{LOCK} = \frac{2I_0}{n\pi}
\]

- \( I_0 \)
- \( V_0 \)
- \( T_{LOCK} \)
- \( T_0 \)
- \( T_{PULSE} = \alpha T_{LOCK} \)

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2-GHz Fifth SbILO layout

Buffer
Oscillator Core
Pulse Generator

Band Gap Reference

0.35-µm BiCMOS STMicroelectronics technology
# Design Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.35-µm BiCMOS STMicroelectronics</td>
</tr>
<tr>
<td>Voltage Supply</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>16 mA</td>
</tr>
<tr>
<td>Current Consumption</td>
<td></td>
</tr>
<tr>
<td>- Output Buffers</td>
<td>15 mA</td>
</tr>
<tr>
<td>- ILO Core + Pulse Generator + Bandgap Current Source</td>
<td>1 mA</td>
</tr>
<tr>
<td>Locking Range</td>
<td>400 MHz</td>
</tr>
<tr>
<td>Center Frequency</td>
<td>2 GHz</td>
</tr>
<tr>
<td>Chip Area (w/o pads and buffers)</td>
<td>0.160 mm²</td>
</tr>
</tbody>
</table>
Spectrum Measurements

SbILO input (400MHz)  
10-mrad phase deviation

-46.2 dB  -46.0 dB

SbILO output (2GHz)  
50-mrad phase deviation

-32.3 dB  -32.0 dB

-46.2 dB  Measurement result  
-46.0 dB  Bessel function of the first kind

S(t) = A.cos[n.ωC.t+n.Φ(t)] ≈ A.cos(n.ωC.t) - A.n.Φ(t).sin(n.ωC.t)

Phase multiplied by 5  \( \Rightarrow 20.\log_{10}(5) = 14 \text{ dB} \)
Spectrum Measurements

Large phase deviation requires Bessel functions. Phase deviation has to be multiplied by

**SbILO input (400MHz)**

-150-mrad phase deviation
-46.2 dB Measurement result

**SbILO output (2GHz)**

-750-mrad phase deviation
-46.0 dB Bessel function of the first kind

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Spectrum Measurements

Freq. offset x5

Frequency deviation widens spectrum by a ratio 5
Carrier and offset between carrier and spurious are multiplied by 5 at ILO output

SbILO input (400MHz)
500-kHz frequency deviation

SbILO output (2GHz)
2.5-MHz frequency deviation
ILO designed in BiCMOS6 as a multiplier by 5
## ILO: Proof of Concept (2)

**Table:**

<table>
<thead>
<tr>
<th>TEST</th>
<th>MAXIMUM VALUES REQUIRED</th>
<th>SBILO INPUT</th>
<th>SBILO OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Error (° rms)</td>
<td>5</td>
<td>0.22</td>
<td>0.26</td>
</tr>
<tr>
<td>Phase Error (° Peak)</td>
<td>20</td>
<td>0.83</td>
<td>0.85</td>
</tr>
</tbody>
</table>

**Graphs:**

- **ILO input**
- **ILO output**
Conclusion ILO

- A theory on ILO modulation has been proposed

- A fifth sub-harmonic injection locked oscillator designed
  - Wide locking range: 400 MHz
  - Center frequency: 2 GHz

- Spectrum at SbILO output can be predicted for
  - Low phase deviation with Bessel function or Taylor development
  - Large phase deviation with Bessel function of the first kind
  - Frequency deviation thanks to the ILO multiplication ratio

- Phase error introduced by ILO once modulated negligible
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400 MHz DDS Principle (1)

\[ V_{RF}(t) = A \cos(\omega_1 t) = A \cos(\omega_0 t + \omega_1 t) = A \cos(\omega_0 t + \varphi(t)) \]
\[ \varphi(t) = 2\pi f_1 t \]

- Frequency synthesis could be seen as a phase modulation, where the modulated phase is a ramp.
- The slope of the ramp is related to the frequency step
- Frequency synthesizer composed of
  - An RF clock
  - A phase shifter that increments a value at each rising edge of the clock
\[ \varphi(t) = \beta \]

Phasor

Time waveform

\[ T_{CLK} \quad T_{DDS} \]
$\varphi(t) = \beta$

Phasor

$T_{CLK}$

$T_{DDS}$

Time waveform
$\varphi(t) = \beta$

Phasor

$T_{CLK}$

$T_{DDS}$

Time waveform

$2\beta$

$\beta$
$\varphi(t) = \beta$

Phasor

$T_{CLK}$

$T_{DDS}$

Time waveform

$3\beta$

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400 MHz DDS Principle (2)

\[ \varphi(t) = \beta \]

\[ T_{DDS} = T_{CLK}(1 + \frac{\beta}{2\pi}) \]

Phase Accumulator: Digital context

Phase Interpolator: Analog Context
400 MHz DDS architecture (1)
400 MHz DDS architecture (2)

- **Advantages**
  - ROM less
  - High frequency (classical implementation output frequency restricted to Fclock/2 at least)

- **Drawbacks**
  - Step frequency limited by the resolution of the digitally controlled phase shifter
  - Spurious response depends on the phase accuracy
Decreasing Step Frequency

- ΣΔ modulator is used to decrease the step of the DDS by switching randomly between two coarse frequencies.

![Diagram showing DDS with f_0 and f_0+df inputs, ΣΔ modulator, and DDS output f_{DDS} with Y=<X> and N_{SD} connected to X.]
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DDS based RF transmitter principle

- \( f_{DDS} \): DDS output frequency
- \( df \): frequency step
- \( \Sigma\Delta \) modulator synthesizes carrier frequency and shapes quantification noise.
- An ILO will act as a frequency multiplier to get the RF signal
Frequency plan

- **GSM (x2) – DCS**
  - Frequency range: 1710 – 1830 MHz
  - Frequency step: 0.1 ppm (170 Hz)
  - ILO multiplication factor: 4
  - DDS frequency range: 427.5 – 457.5 MHz
  - DDS Frequency step: 42.5 Hz

- **Bluetooth**
  - Frequency range: 2402 – 2480 MHz
  - Frequency step: 1 ppm (2400 Hz)
  - ILO multiplication factor: 5
  - DDS frequency range: 480.4 – 496 MHz
  - DDS frequency step: 480 Hz
Bluetooth schematic

ΣΔ generates $2^{N_{SD}}$ frequencies between $f_0$ and $f_0+df$
Transmitter modelization - Bluetooth

- LO frequency: \( f_{\text{LO}} = 2.45 \text{ GHz} \)
- DDS frequency: \( f_{\text{DDS}} = 490 \text{ MHz} \)
- RBW: 100 kHz

Lowering \( df \) lowers the phase noise.
$\Sigma\Delta$ modulator generates $2^{N_{SD}}$ frequencies between $f_0$ and $f_0+df$
Transmitter modelisation– GSM/DCS

\[ f_{\text{ILO}} = 1.8 \text{ GHz} \]
\[ f_{\text{DDS}} = 450 \text{ MHz} \]
\[ \text{RBW} = 100 \text{ kHz} \]
Modulations

Bluetooth
- $f_{\text{BIT}}$: 1 MHz
- Modulator oversampling: 32
- Symbols number: 50
- $df$: 400 kHz

GSM
- $f_{\text{BIT}}$: 270.833 kb/s
- Modulator oversampling: 64
- Symbols number: 148
- $df$: 400 kHz
ΣΔ and phase interpolation based DDS

Diagram:
- LO input at 2 GHz
- State Machine
- Phase Accumulator
- ΣΔ modulator
- DAC
- Comparator (COMP)
- Reference voltage (V_{REF})
- Capacitor (CAP)
- Reset signal

Connections:
- 2 GHz input
- 500 MHz input from ΣΔ modulator
- Coarse and Fine outputs from Phase Accumulator
- 0 max output to DAC
- DAC output to Comparator
- Comparator inputs + and -
ΣΔ and phase interpolation based DDS

LO 2 GHz

State Machine

I/4

Phase Accumulator

0 max

DAC

COMP

DIGITAL

ANALOG

ΣΔ

500 MHz

Fine Coarse

Reset

VREF

CAP

STMicroelectronics
Capacitor charge with variable current

LO 2 GHz
/4

State Machine

Phase Accumulator

ΣΔ

Fine
Coarse

0 max

DAC

V_{REF}

COMP

Reset

CAP

500 MHz

STMicroelectronics
Capacitor charge with $I_{\text{max}}$
Phase interpolation

- **Reset**
- Variable charge
- Constant charge

Variables:
- $V_{REF}$
- $T_{CLK}$
- $t$

Outputs:
- **RESET1 (R1)**
- **VARIABLE (V)**
- **CONSTANT1 (C1)**
- **CONSTANT2 (C2)**
Synthesizer working process

LO

/4

State Machine

Phase Accumulator

ΣΔ

DAC

V_{CAP}

V_{COMP}

V_{REF}

Reset

C

T_{CLK}

2 GHz CLK

t

RESET1 (R1)

VARIABLE (V)

CONSTANT1 (C1)

CONSTANT2 (C2)
Synthesizer working process

V_{REF}

\( V_{CAP} \)

T_{CLK}

2-GHz CLK

RESET1 (R1)

VARIABLE (V)

CONSTANT1 (C1)

CONSTANT2 (C2)
Synthesizer working process

State Machine
Phase Accumulator
ΣΔ
DAC
V<sub>REF</sub>
V<sub>CAP</sub>
V<sub>COMP</sub>

RESET1 (R1)
VARIABLE (V)
CONSTANT1 (C1)
CONSTANT2 (C2)

V<sub>REF</sub>
V<sub>CAP</sub>
V<sub>COMP</sub>

T<sub>CLK</sub>
t
Synthesizer working process

LO

/4

State Machine

Phase Accumulator

ΣΔ

DAC

V_

REF

VCAP

VCOMP

Reset

C

VREF

VCOMP

VCOMP

STMicroelet

Delay

RESET1 (R1)

VARIABLE (V)

CONSTANT1 (C1)

CONSTANT2 (C2)

VCAP

VCOMP

TCLK

t
Synthesizer working process

LO

\( i4 \)

State Machine

Phase Accumulator

\( \Sigma \Delta \)

DAC

\( V_{\text{CAP}} \)

\( V_{\text{COMP}} \)

\( V_{\text{REF}} \)

C

Reset

\( T_{\text{CLK}} \)

\( V_{\text{COMP}} \)

\( V_{\text{REF}} \)

\( t \)

RESET1 (R1)

VARIABLE (V)

CONSTANT1 (C1)

CONSTANT2 (C2)
Synthesizer working process

State Machine

Phase Accumulator

ΣΔ

DAC

\( V_{\text{REF}} \)

\( V_{\text{COMP}} \)

\( V_{\text{CAP}} \)

\( T_{\text{CLK}} \)

\( V_{\text{COMP}} \)

\( 0_{\text{max}} \)

Reset

\( \text{RESET1 (R1)} \)

\( \text{VARIABLE (V)} \)

\( \text{CONSTANT1 (C1)} \)

\( \text{CONSTANT2 (C2)} \)
Synthesizer working process

LO

ΣΔ

Phase Accumulator

State Machine

DAC

VREF

VCOMP

VREF

VCAP

VCOMP

TCLK

Delay

STMicroelectronics

RESET1 (R1)

VARIABLE (V)

CONSTANT1 (C1)

CONSTANT2 (C2)
Synthesizer working process

LO

1/4

State Machine

Phase Accumulator

ΣΔ

VREF

VCAP

VCOMP

Reset

DAC

VREF

C

TCLK

VCOMP

RESET1 (R1)

VARIABLE (V)

CONSTANT1 (C1)

CONSTANT2 (C2)
Synthesizer working process
Synthesizer working process

- **LO**
- **State Machine**
- **Phase Accumulator**
- **ΣΔ**
- **DAC**
- **V<sub>REF</sub>**
- **V<sub>COMP</sub>**
- **V<sub>CAP</sub>**
- **T<sub>CLK</sub>**
- **V<sub>COMP</sub>**

Diagram:

- Reset
- \( V_{\text{CAP}} \)
- \( V_{\text{COMP}} \)
- \( V_{\text{REF}} \)
- \( 0_{\text{max}} \)

Flowchart:

- RESET1 (R1)
- VARIABLE (V)
- CONSTANT1 (C1)
- CONSTANT2 (C2)
Synthesizer working process

LO

Phase Accumulator

ΣΔ

State Machine

DAC

VREF

VCAP

VCOMP

RESET1 (R1)

VARIABLE (V)

CONSTANT1 (C1)

CONSTANT2 (C2)

Delay

STMicroelectronics
Combinaisons de l’interpolation de phase

CNA 8 bits
$2^8 - 1$ phases dans $T_{CLK}$

$V_{REF}$

$T_{CLK}$ $T_{CLK}$
**DDS frequencies calculation**

- 1 phase interpolation each $4T_{CLK}$
- $(2^8 - 1)$ phases in $T_{CLK}$

\[
f_{DDS} = \frac{\frac{f_{CLK}}{4}}{1 + \frac{P}{4(2^8 - 1)}}
\]

- $f_{CLK} = 2$ GHz
- $f_{CLK}/4 = 500$ MHz

\[
P = 0 \quad \Rightarrow \quad f_{DDS_{MAX}} = 500$ MHz
\[
P = 2^8 - 1 \quad \Rightarrow \quad f_{DDS_{MIN}} = 400$ MHz

$\Delta f \approx 500$ kHz
ΣΔ 14 bits (MASH11)
2 levels quantisizer
⇒ 13 data bits + 1 sign bit

$2^{13}$ Combination over time
Detailed DDS bloc Diagramm

LO

/4

State Machine

Phase Accumulator

ΣΔ MASH11

DAC

VCAP

VCOMP

VREF

C

Reset

ΣDAC

P8 bits

<PS> 3 bits

PSD

PPA

14 bits

8 bits

0 max
**ΣΔ advantages**

- P is composed of an integer part $P_{PA}$ and a fractional one $P_{SD}$

\[
f_{DDS} = \frac{f_{CLK}}{4} \frac{P_{PA} + \frac{P_{SD}}{2^{13}}}{(1 + \frac{4(2^8-1)}{2^{13}})}
\]

- Diminution of frequency resolution
- Quantisizer noise shaping

$\Delta f_{COARSE} \approx 500 \text{ kHz}$

$\Delta f_{ACCURATE} \approx \frac{\Delta f_{COARSE}}{2^{13}} \approx 60 \text{ Hz}$
DDS micrograph

CMOS 65-nm STMicroelectronics

Active area: 0.1 mm²
Power supply: 1.2 V
Power consumption:
29 mW (without buffers)

State machine, $\Sigma\Delta$, and phase accumulator
P&R with standard cells

Clock
Typical: 2 GHz
Worst case: 2.8 GHz

Package: TQFP 32
Frequency resolution

RBW: 10Hz
VBW: 10Hz

Center: 496.511022 MHz
Span: 200 Hz

60 Hz
60 Hz
Phase Noise – LO / DDS

Phase noise (dBc/Hz)

2-GHz LO
500-MHz DDS

$f (Hz)$
Phase noise – with/ $\Sigma\Delta$

$\text{f}_{\text{IM}} = 500 \text{ MHz} - \text{f}_c \approx 2.5 \text{ MHz}$

With $\Sigma\Delta$

Without $\Sigma\Delta$

$\text{f}_c: 497.5 \text{ MHz}^8$
Phase Noise – model/measure

Bruit de phase (dBc/Hz)

\[ f_C : 497.5 \text{ MHz} \]

-150 -140 -130 -120 -110 -100 -90 -80

1,\text{E}+03 1,\text{E}+04 1,\text{E}+05 1,\text{E}+06 1,\text{E}+07 1,\text{E}+08

\[ f (\text{Hz}) \]

Mesure

Modèle

STMicroelectronics
DDS output spectrum

Center: 500 MHz
Span: 250 MHz

f_C ≈ 496 MHz
68 dB
~16 MHz

RBW: 10 kHz
VBW: 10 kHz
AC: 8
SD: -31
## DDS state of the art

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>Fréquence de sortie (MHz)</td>
<td>Min</td>
<td>Max</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>100</td>
<td>0</td>
<td>400</td>
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<tr>
<td></td>
<td>0</td>
<td>150</td>
<td>0</td>
<td>500</td>
</tr>
<tr>
<td>Fréquence d’horloge (MHz)</td>
<td>200</td>
<td>300</td>
<td>630</td>
<td>2000</td>
</tr>
<tr>
<td>Sortie</td>
<td>1 bit CAN 1 bit</td>
<td>1 bit CNA 12 bits</td>
<td>13 bits quadrature</td>
<td>1 bit CNA 8 bits</td>
</tr>
<tr>
<td>Tension d’alimentation (V)</td>
<td>1.5</td>
<td>3.3</td>
<td>2.5</td>
<td>1.2</td>
</tr>
<tr>
<td>Puissance consommée (mW)</td>
<td>138</td>
<td>200</td>
<td>76</td>
<td>29</td>
</tr>
<tr>
<td>Technologie (µm)</td>
<td>0.13</td>
<td>0.35</td>
<td>0.25</td>
<td>0.065</td>
</tr>
<tr>
<td>Surface (mm²)</td>
<td>2.02</td>
<td>1.11</td>
<td>0.063</td>
<td>0.1</td>
</tr>
<tr>
<td>Figure de mérite (mW/MHz)</td>
<td>690</td>
<td>666</td>
<td>121</td>
<td>29</td>
</tr>
</tbody>
</table>
Transmitter Block Diagramm

- Output Frequency Range: 2 to 2.5 GHz
- Frequency step: 300 Hz
- RF filtering provided by ILO
ILO frequency multiplication

Injected Signal

\[ f_1 \quad f_0 \quad f_2 \]

\[ \Delta f \quad \Delta f \]

ILO output

\[ 5.f_1 \quad 5.f_0 \quad 5.f_2 \]

\[ 5.\Delta f \quad 5.\Delta f \]

Modulation (dB)

\[ f_{\text{MOD}} / 5 \]

Bande de base

\[ f_0 \]

\[ f (\text{Hz}) \]

Schrinked Modulation (dB)

\[ (f_C + f_{\text{MOD}}) \times 5 \]

ILO

\[ f_0 \]

\[ f (\text{Hz}) \]

Output ILO Modulation (dB)

\[ f_{\text{RF}} = 5 \times f_0 \]

\[ f (\text{Hz}) \]
\[ \Delta f = 2 \cdot \frac{I_{\text{LOCK}}}{V_0} \cdot \frac{1}{4 \cdot \pi \cdot C_{\text{Total}}} \]
Transmitter Micrograph

CMOS 65-nm STMicroelectronics
Active area: 0.25 mm²
Power Supply: 1.2 V
Dissipated Power:
37 mW (without output buffers)

DDS + ILO
ILO locking range programmable
From 1 to 31 MHz
TQFP 48 package

STMicroelectronics
Free Running and Locked – ILO Phase Noise

Phase noise (dBc/Hz) vs. frequency (Hz)

- ILO libre
- ILO verrouillé (31)
- DDS
- ILO verrouillé (1)
Phase Noise for different ILO locking range

-160,00
-150,00
-140,00
-130,00
-120,00
-110,00
-100,00
-90,00

Bruit de phase (dBc/Hz)

f (Hz)

1,0E+05 1,0E+06 1,0E+07 1,0E+08

ILO libre
Masque
DDS
LCK 31
LCK 8
LCK 4
LCK 1

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Phase Noise Filtering – ILO/DDS

-15,00
-10,00
-5,00
0,00
5,00

Bruit de phase [DDS + 14dB - ILO]

LCK 31
LCK 1
LCK 4
LCK 8

Phase noise [DDS + 14dB - ILO] vs. f (Hz)

LCK 31
LCK 8
LCK 4
LCK 1

STMicroelectronics
Transmitter output spectrum

Locking Range  
= 31 MHz

Locking Range  
= 1 MHz
Conclusion

- Innovative transmitter based on Phase Shifter based pulse output DDS
- Demonstrated feasibility from system to silicon
  - Matlab modelization including mismatches
  - DDS measurement
    - DDS output frequency from 400 MHz to 500 MHz
    - 60 Hz frequency resolution
    - 29 mW
- Transmitter Measurement
  - Frequency band from 2 GHz to 2.5 GHz
  - 300 Hz frequency resolution
  - 37 mw
Acknowledgements

- This presentation is based on Ph D work of L. Camino (modulation of $\Sigma\Delta$ fractional PLL) and T. Finateu (DDS –ILO based transmitter)