CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Angel Rodríguez-Vázquez

angel@imse.cnm.es

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH

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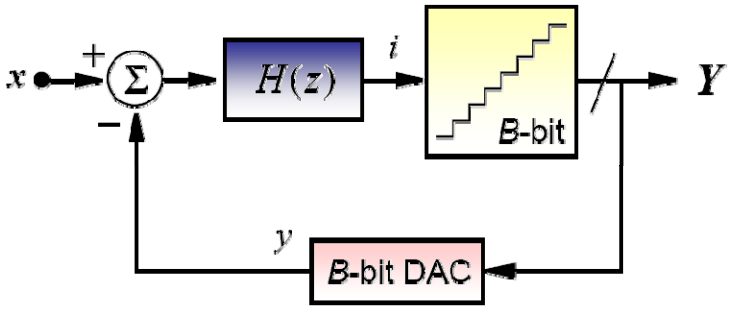
Materials in this course have been contributed by Fernando Medeiro, José M. de la Rosa, Rocío del Río, Belén Pérez-Verdú and Angel Rodríguez-Vázquez

DT-ΣΔMs: Overview of non-idealities



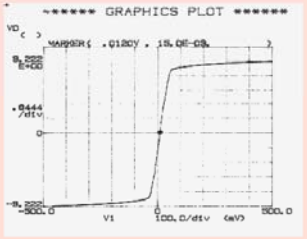
- **Ideal In-Band Error Power:**

$$P_Q = \frac{1}{12}\left(\frac{\Delta}{2^B - 1}\right)^2 \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}$$

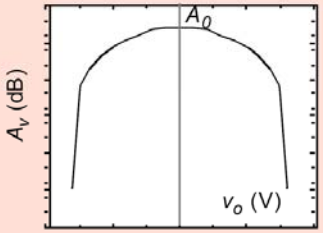
- **Actual In-Band Error Power:**

$$P_T = P_Q + \Delta P_Q + P_{TH} + P_J + P_{HD} + \ldots$$

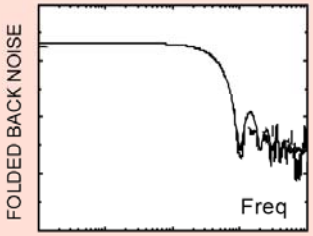
Finite Amplifier Gain



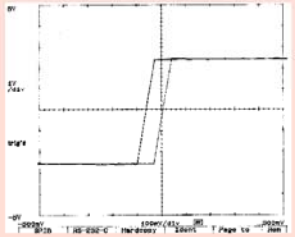
Non-Linearities



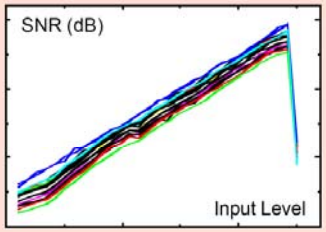
Thermal Noise



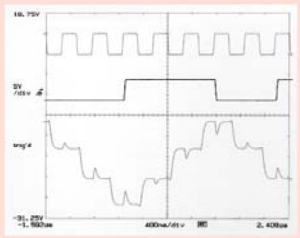
Comparator Hysteresis



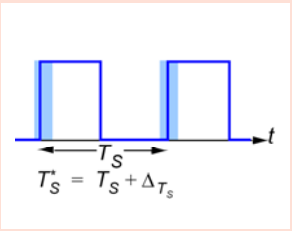
Capacitor Mismatch



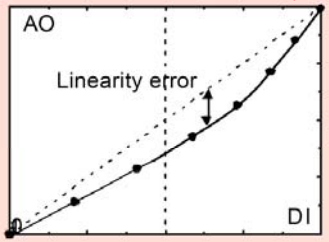
Settling Errors



Clock Jitter



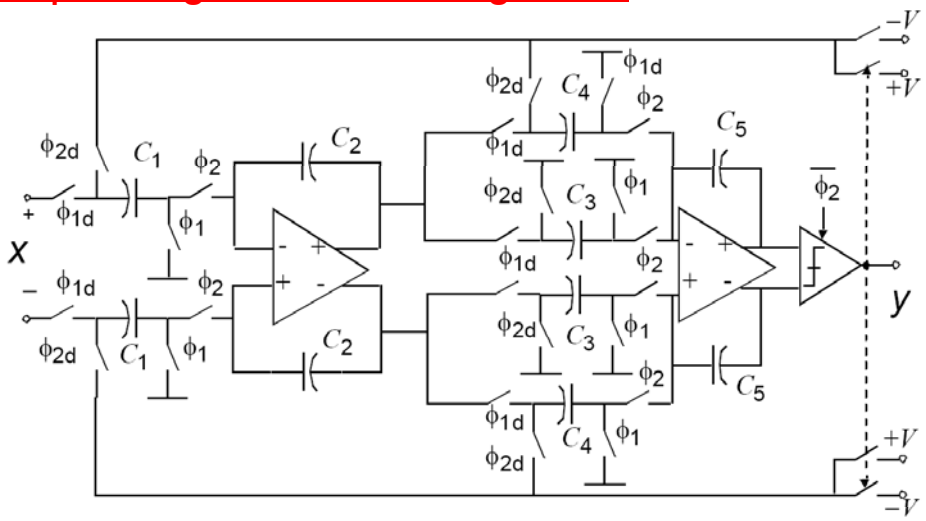
DAC Non-linearity



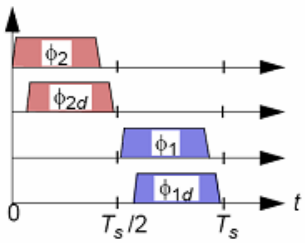
… among others …

DT-ΣΔMs: Overview of non-idealities

- Depending on the building-block:



Fully-diff SC schematic of a 2nd-order ΣΔM



Clock:
- Jitter

Amplifiers:
- Output swing
- DC gain
- Dynamic limitations (GB, SR)
- Thermal and 1/f noise
- Gain non-linearity

Switches:
- Finite on-resistance
- Thermal noise
- Charge injection
- Clock feedthrough
- Non-linearity

References:
- Thermal and 1/f noise
- Output impedance

Capacitors:
- Mismatch
- Non-linearity

Comparators:
- Hysteresis
- Offset

Multi-bit ADCs & DACs:
- Gain error
- Offset error
- Non-linearity

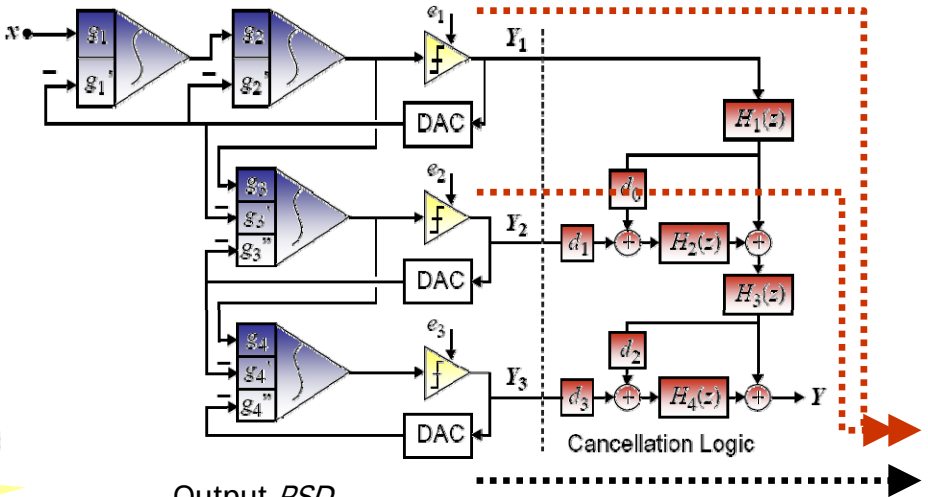
DT-ΣΔMs: Overview of non-idealities

- Depending on their effect:

ERRORS DEGRADING NTF

- AMPLIFIER DC GAIN
- CAPACITOR MISMATCH
- INTEGRATOR SETTLING
  - Amplifier GB
  - Amplifier SR
  - Switch R_{on}

Impact depends on topology



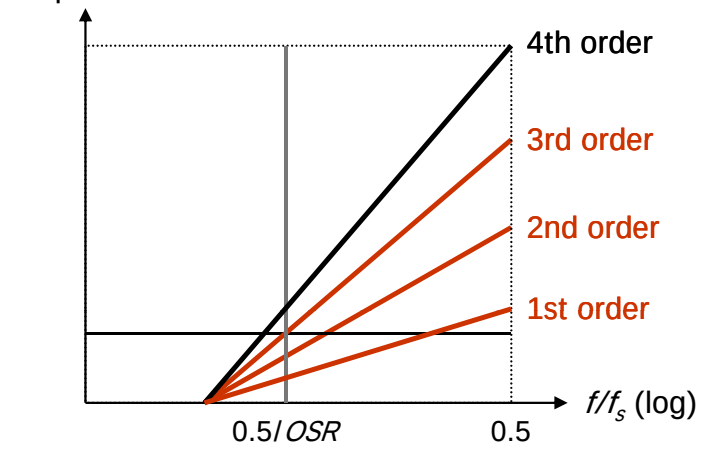
SINGLE-LOOP ΣΔMs

→ Low sensitivity

CASCADE ΣΔMs

→ **Noise leakages**

Imperfect cancellation of low-order quantization errors



DT-ΣΔMs: Overview of non-idealities

- Depending on their effect:

ERRORS DEGRADING NTF

- AMPLIFIER DC GAIN
- CAPACITOR MISMATCH
- INTEGRATOR SETTLING
  - Amplifier GB
  - Amplifier SR
  - Switch R_{on}

Impact depends on topology

SINGLE-LOOP ΣΔMs

→ Low sensitivity

CASCADE ΣΔMs

→ **Noise leakages**

Imperfect cancellation of low-order quantization errors

MODELED AS ADDITIVE ERRORS

- CIRCUIT NOISE
  - Thermal noise (switches, opamps, refs)
  - 1/f noise (opamps, refs)
- CLOCK JITTER
- DISTORTION
  - Non-linear amplifier gain
  - Non-linear capacitors
  - Non-linear settling
  - Non-linear switches

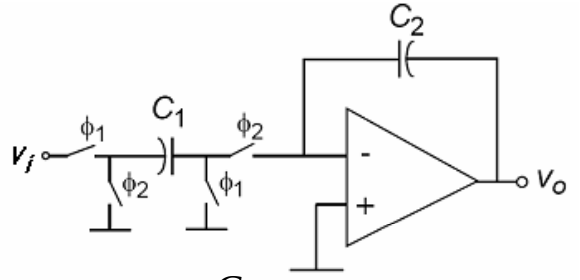
Front-end dominates

Similar impact on different topologies

DT-ΣΔMs: Integrator leakage

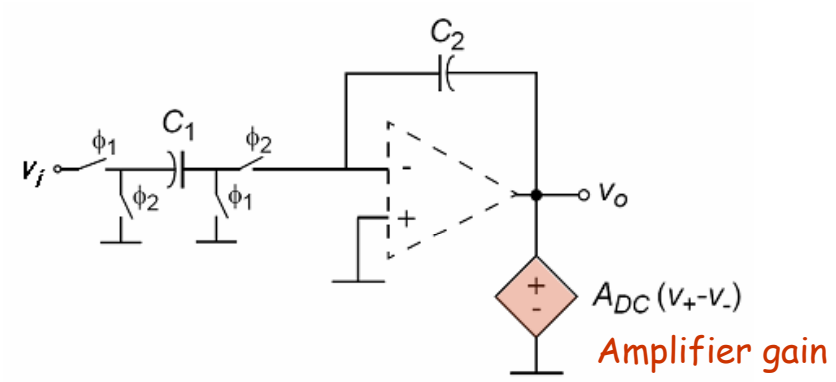
- Effect of amplifier gain on the integrator transfer function:

Ideal SC integrator



$$g = \frac{C_1}{C_2}$$

SC integrator considering amplifier finite gain



$$v_{o,n} = v_{o,n-1} + g \cdot v_{i,n-1} \rightarrow v_{o,n} = \frac{1}{1+\frac{(1+g)}{A_{DC}}}\left[\left(1+\frac{1}{A_{DC}}\right)\cdot v_{o,n-1} + g \cdot v_{i,n-1}\right]$$

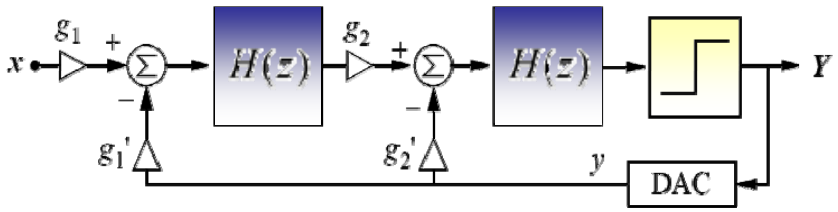
$$H(z) = g\frac{z^{-1}}{1-z^{-1}} \rightarrow H(z) \cong g\frac{z^{-1}}{1-z^{-1}\left(1-\frac{g}{A_{DC}}\right)} = g\frac{z^{-1}}{1-z^{-1}(1-g\mu)}$$

$$\mu = 1/A_{DC}$$

Shift of the pole from DC ($z = 1$)

DT-ΣΔMs: Integrator leakage

- Effect on single-loop ΣΔMs:



2nd-order ΣΔM

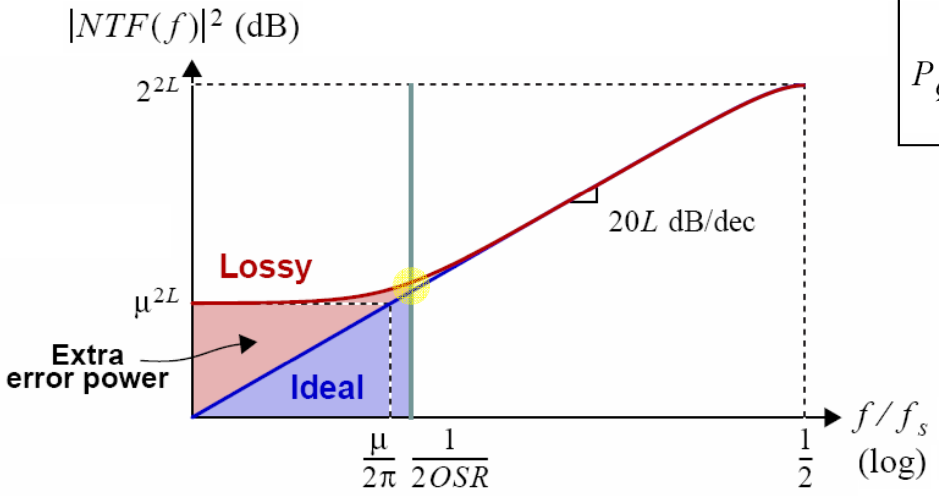
- Ideally: $H(z) = \dfrac{z^{-1}}{1-z^{-1}}$

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2 E(z)$$

- In practice: $H(z) = \dfrac{z^{-1}}{1-z^{-1}(1-\mu)}$

$$NTF(z) = [1-z^{-1}(1-\mu)]^2$$
$$= (1-z^{-1})^2 + 2\mu z^{-1}(1-z^{-1}) + \mu^2 z^{-2}$$

$$P_Q(\mu) \cong \frac{\Delta^2}{12}\left(\frac{\pi^4}{5OSR^5} + \frac{2\mu^2}{3OSR^3} + \frac{\mu^4}{OSR}\right)$$



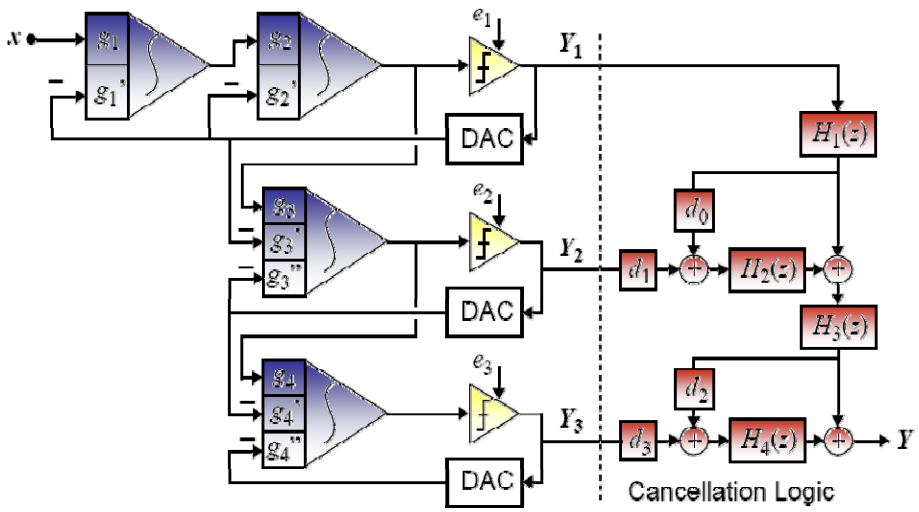
Lth-order ΣΔM:

$$\Delta P_Q \cong \frac{\Delta^2}{12}\frac{L\mu^2\pi^{2L-2}}{(2L-1)OSR^{(2L-1)}}$$

Quite insensitive to leakages (μ^2, L-1 shaping)

DT-ΣΔMs: Integrator leakage

- Effect on cascade ΣΔMs: **2-1-1 ΣΔM**



Analog	Digital	
$g_2' = 2g_1'g_2$	$d_0 - \frac{g_3'}{g_1'g_2g_3} - 1$	$H_1(z) = z^{-1}$
$g_4' = g_3''g_4$	$d_1 - \frac{g_3''}{g_1'g_2g_3}$	$H_2(z) = (1-z^{-1})^2$
	$d_2 = 0$	$H_3(z) = z^{-1}$
	$d_3 = \frac{g_4''}{g_1'g_2g_3g_4}$	$H_4(z) = (1-z^{-1})^3$

Mismatch between analog and digital filtering

- Ideally:

$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) + NTF_3(z)E_3(z)$$

$$\Rightarrow \begin{cases} STF(z) = z^{-4} \\ NTF_1(z) = 0 \\ NTF_2(z) = 0 \\ NTF_3(z) = d_2(1-z^{-1})^4 \end{cases}$$

- In practice: $H(z) = \dfrac{z^{-1}}{1 - z^{-1}(1-\mu)}$

$$P_Q(\mu) \cong \frac{\Delta_1^2}{12}\left(\frac{4\mu^2\pi^2}{3OSR^3}\right) + \frac{\Delta_2^2}{12}d_1^2\left(\frac{\mu^2\pi^4}{5OSR^5}\right)$$

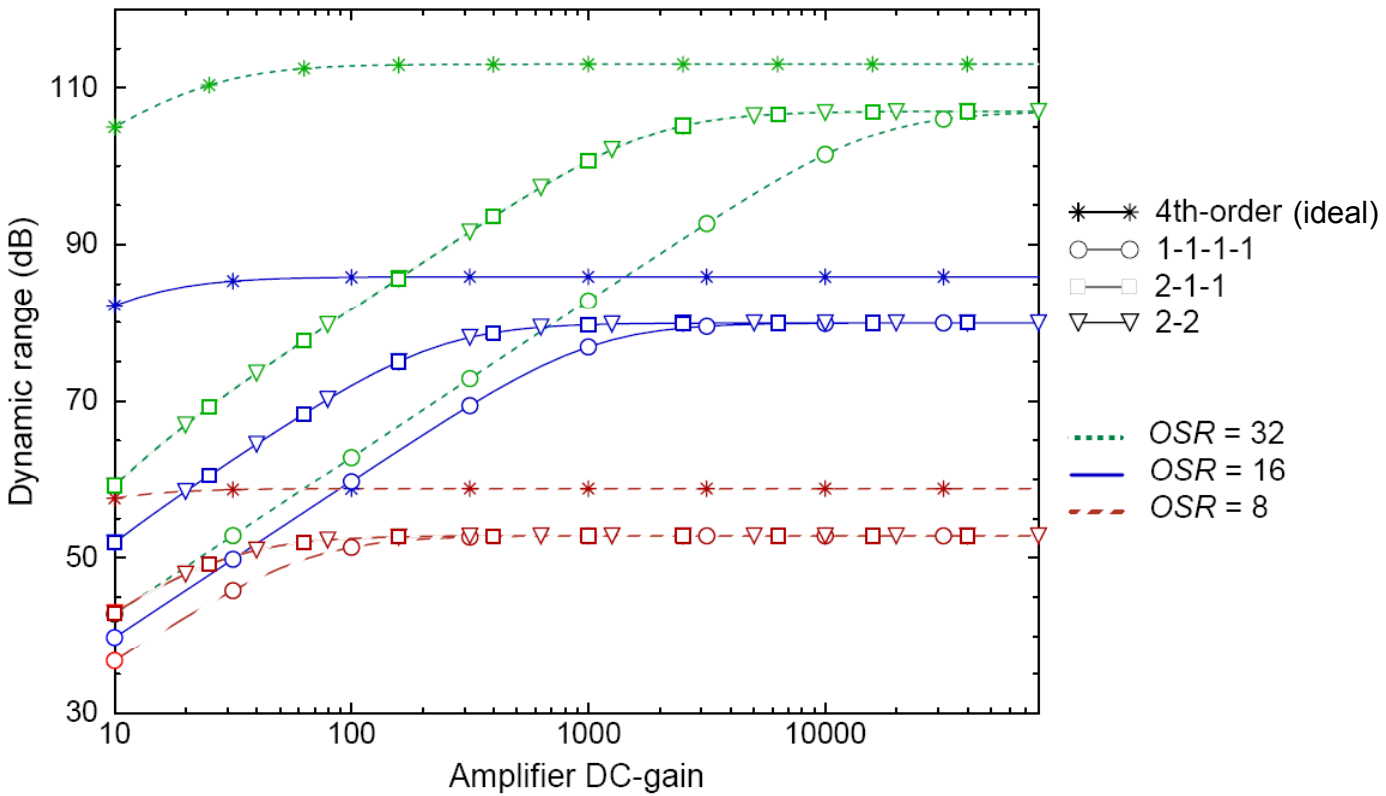
$$\Rightarrow + \frac{\Delta_3^2}{12}d_3^2\left(\frac{\mu^2\pi^6}{7OSR^7} + \frac{\pi^8}{9OSR^9}\right)$$

low-order leakages

(L_1-1, L_2-1, …)

DT-ΣΔMs: Integrator leakage

Comparison of integrator leakage effect on 4th-order ΣΔMs



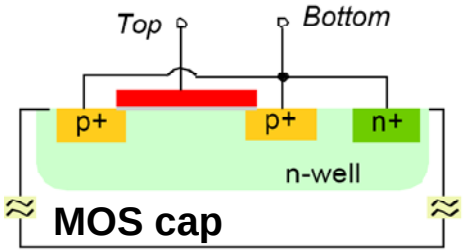
→ Sensitivity to int. leakages of cascades increases with OSR and L

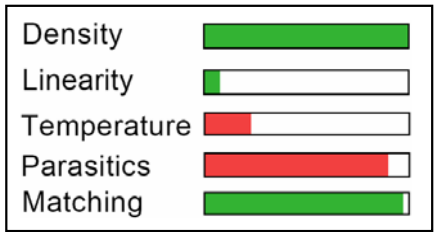
→ 1st-stage leakages dominate (L_1-1 shaping)

DT-ΣΔMs: Capacitor mismatch

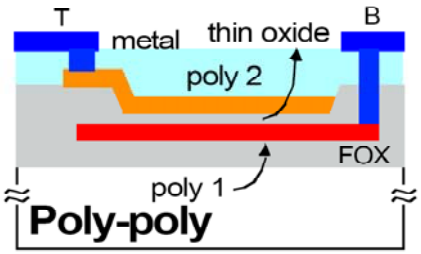
- Circuit primitive:

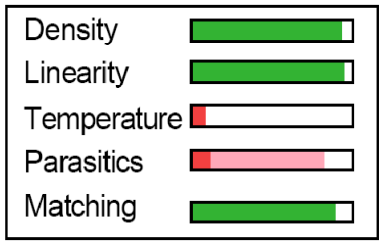
- Physical implementations:



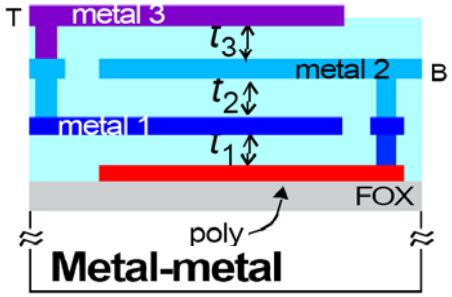


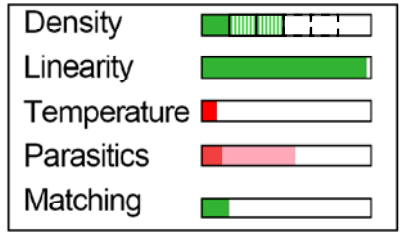
"Analog" CMOS



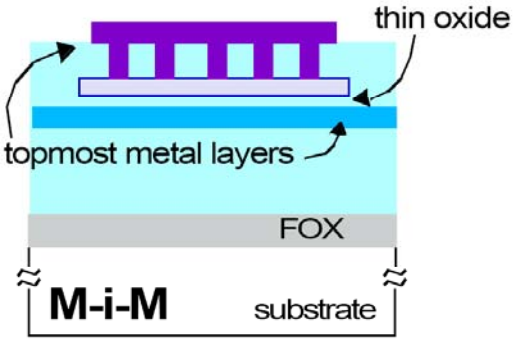


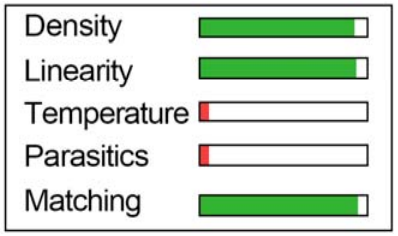
"Digital" CMOS





"Mixed" CMOS





DT-ΣΔMs: Capacitor mismatch

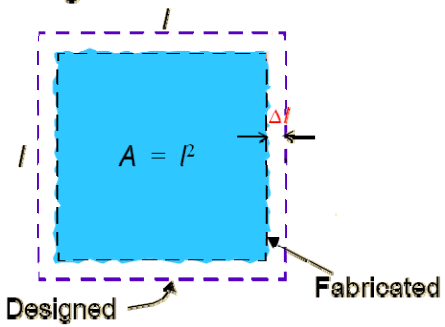
$C = C^{*}_{oxc} \cdot (W \cdot L)$

Actual ≠ Ideal

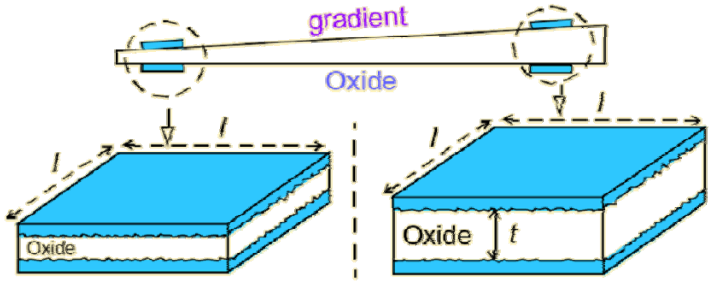
Local and global errors in:

- Area
- Capacitance per Unit Area

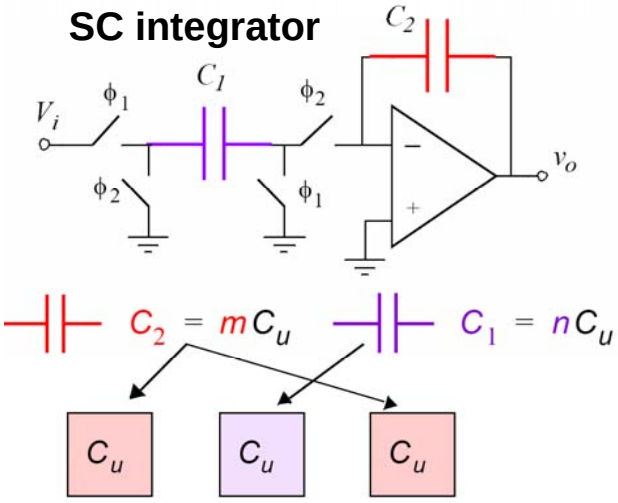
- Edge Errors



- Errors in thickness and dielectric constant



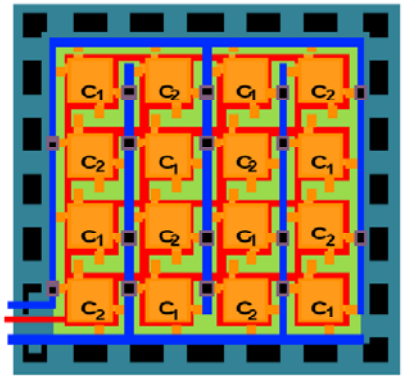
SC integrator



$$g = \frac{C_1}{C_2} = \frac{nC_u}{mC_u}$$

$$\frac{\sigma_g}{g} = \sqrt{\frac{1}{n} + \frac{1}{m}} \cdot \frac{\sigma_{Cu}}{C_u}$$

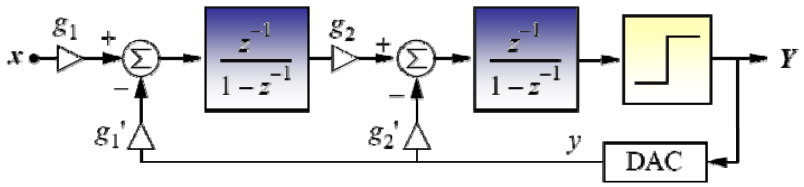
σ_C ~ 0.05% - 0.1% using good quality caps and adequate layout strategies



Centroid techniques

DT-ΣΔMs: Capacitor mismatch

- Effect on single-loop ΣΔMs:



2nd-order ΣΔM

- Ideally: $g_1 = g_1'$, $g_2' = 2g_1'g_2$

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2 E(z)$$

- In practice: $g_i^* = g_i(1 \pm \varepsilon_{g_i})$

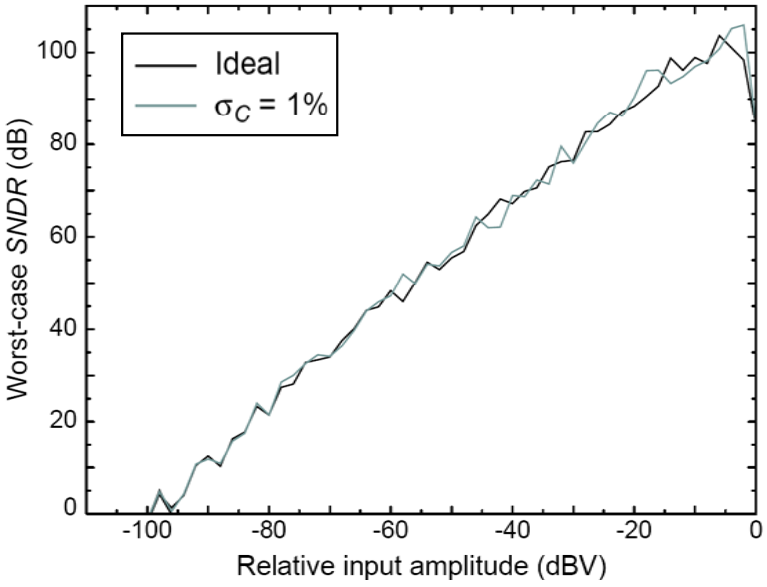
$$\varepsilon_{g_i} = 3\frac{\sigma_{g_i}}{g_i} = 3\sqrt{\frac{1}{m_i} + \frac{1}{n_i}}\sigma_C$$

$$STF(z) \cong (1 - |\varepsilon_{g_1'} - \varepsilon_{g_1}|)z^{-2} \cong z^{-2}$$

$$NTF(z) \cong (1+\varepsilon_g)(1-z^{-1})^2 \quad , \varepsilon_g = \varepsilon_{g_2} + \varepsilon_{g_1'}$$

Slight increase of error, but shaping is preserved

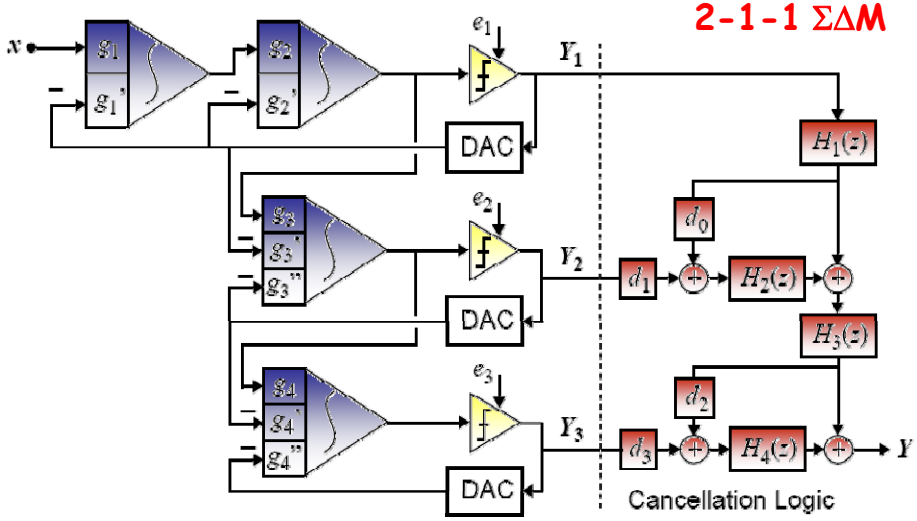
$$P_Q(\varepsilon_g) \cong \frac{\Delta^2}{12}\left[\frac{(1+\varepsilon_g)^2\pi^4}{5OSR^5}\right]$$



DT-ΣΔMs: Capacitor mismatch

- Effect on cascade ΣΔMs:

2-1-1 ΣΔM



Analog	Digital	
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$g_4' = g_3''g_4$	$d_1 = \frac{g_3''}{g_1'g_2g_3}$	$H_2(z) = (1-z^{-1})^2$
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	$d_3 = \frac{g_4''}{g_1'g_2g_3g_4}$	$H_4(z) = (1-z^{-1})^3$

Mismatch between analog and digital coeffs

- Ideally:

$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) + NTF_3(z)E_3(z)$$

$$\Rightarrow \begin{cases} STF(z) = z^{-4} \\ NTF_1(z) = 0 \\ NTF_2(z) = 0 \\ NTF_3(z) = d_2(1-z^{-1})^4 \end{cases}$$

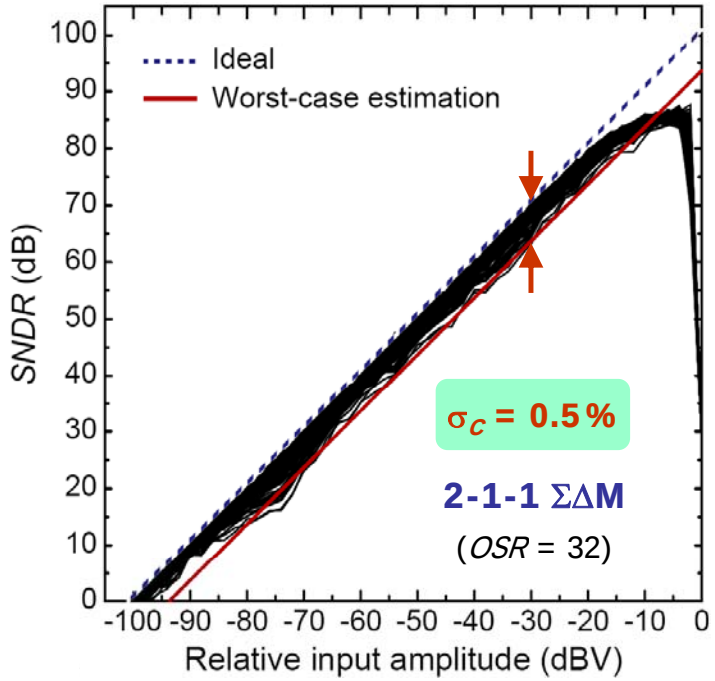
- In practice: $g_i^* = g_i(1 \pm \varepsilon_{g_i})$

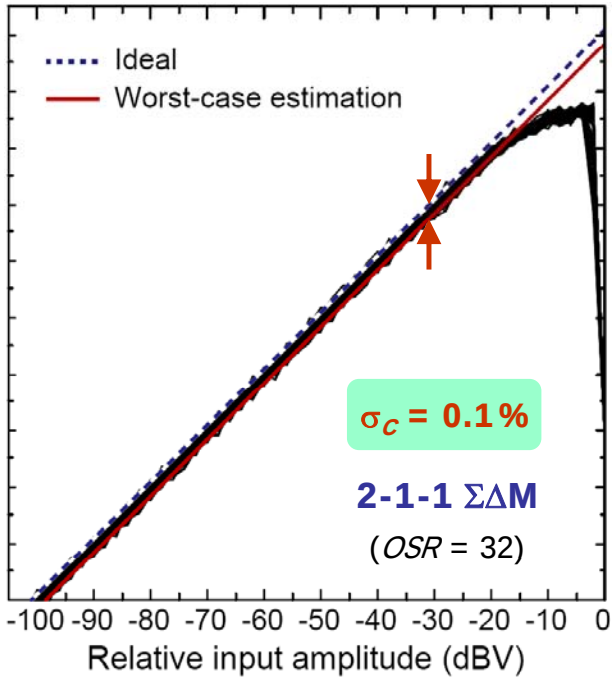
$$\Rightarrow \begin{cases} STF(z) \cong z^{-4} \\ NTF_1(z) \cong \varepsilon_1 z^{-2}(1-z^{-1})^2 \\ NTF_2(z) \cong d_1\varepsilon_2 z^{-1}(1-z^{-1})^3 \\ NTF_3(z) \cong d_2(1+\varepsilon_3)(1-z^{-1})^4 \end{cases}$$

☹ low-order leakages (L_1, L_2, …)

DT-ΣΔMs: Capacitor mismatch

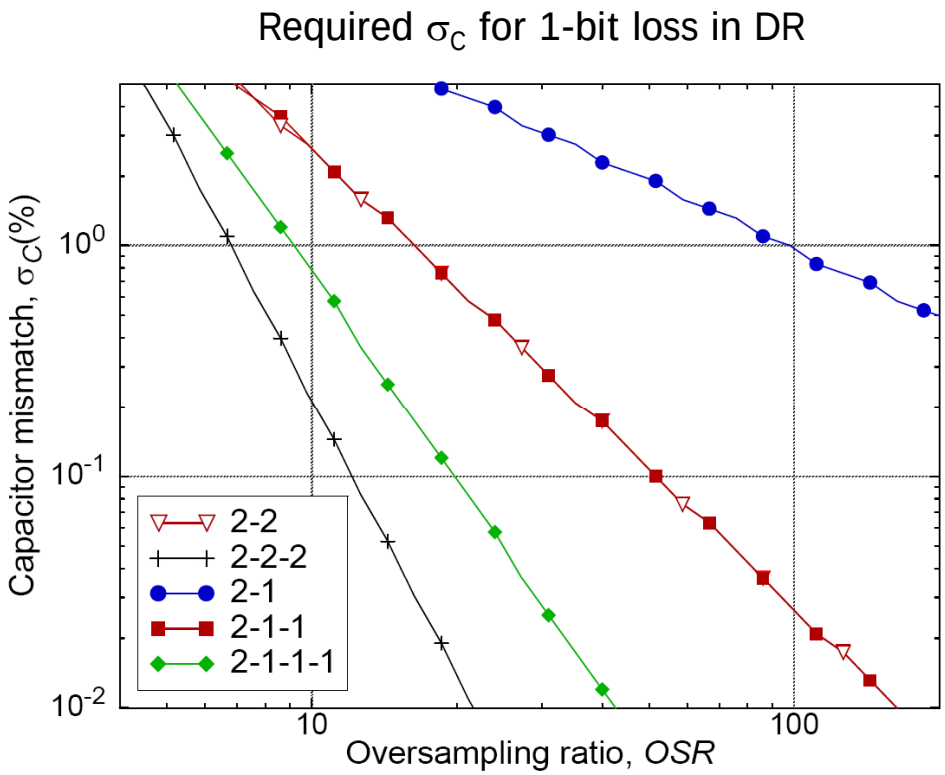
- Effect on cascade ΣΔMs:





DT-ΣΔMs: Capacitor mismatch

- Effect on cascade ΣΔMs:



Sensitivity to mismatch rapidly increases with:

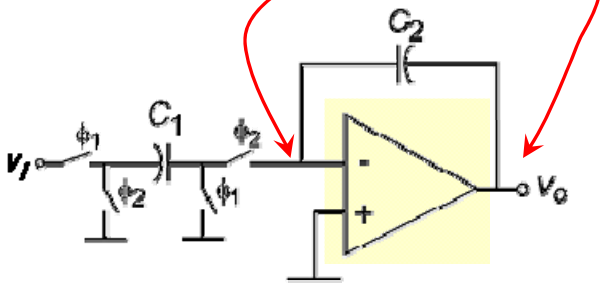
- Oversampling ratio (OSR)

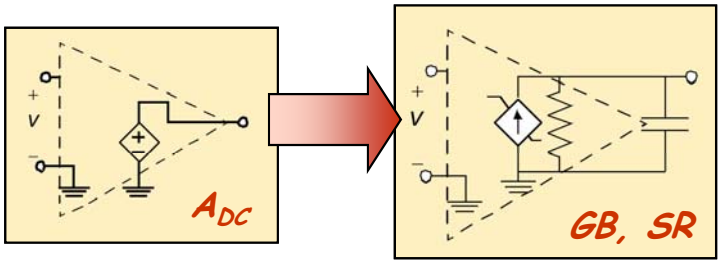
- Cascade order (*L*)

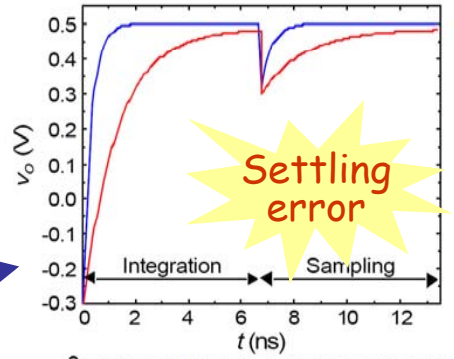
1st-stage leakages dominate (L_1 shaping)

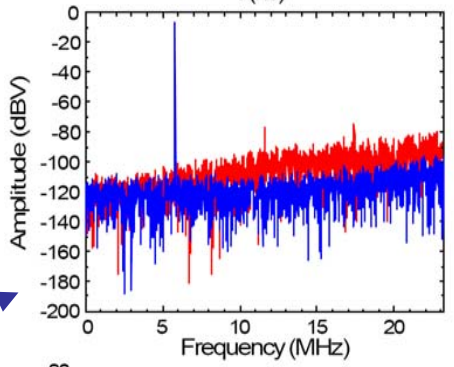
DT-ΣΔMs: Integrator incomplete settling

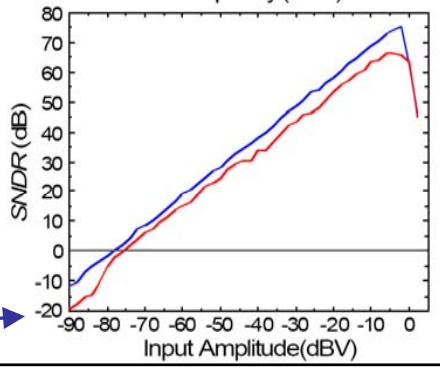
- The relationship between opamp input and output is non-linear and dynamic









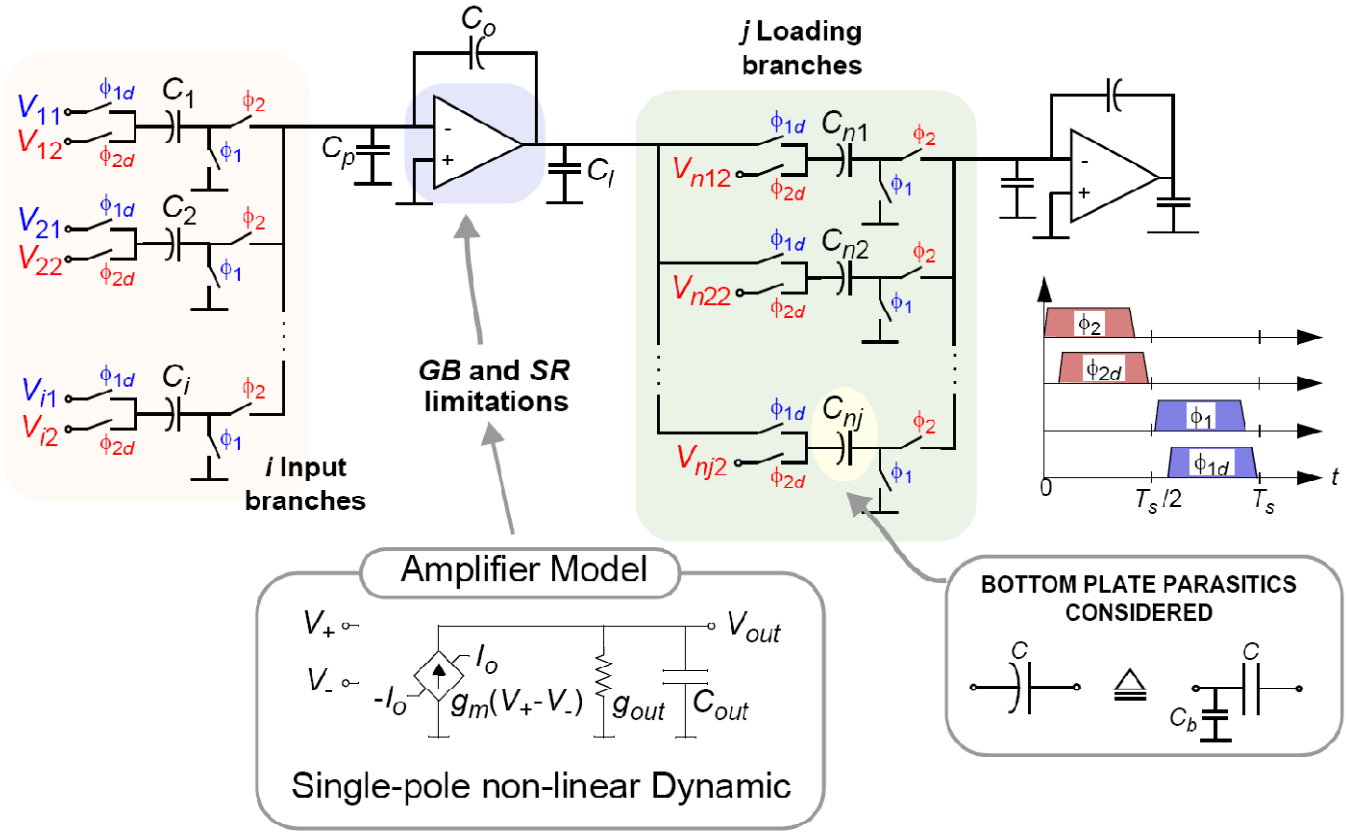


- Integrator temporal evolution
  - error due to amplifier finite bandwidth
  - slew-rate limitation
- Modulator output spectrum
  - increase on the noise floor
  - harmonic distortion due to slewing
- SNDR degradation

DT-ΣΔMs: Integrator incomplete settling

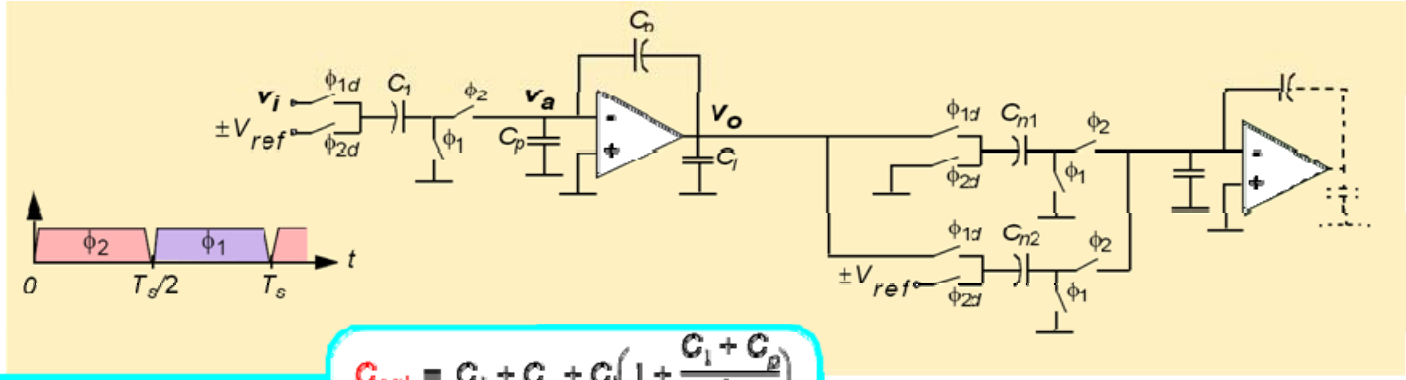
Integrator temporal evolution: [Rio00]

- Both integration and sampling dynamics considered
- 1 pole model + SR limitation in amplifiers
- All parasitic caps taken into account



DT-ΣΔMs: Integrator incomplete settling

Integrator temporal evolution: [Rio00]



$$C_{eql} = C_1 + C_p + C_l\left(1 + \frac{C_1 + C_p}{C_o}\right)$$

- **Integration-Phase:**
  - finite opamp dynamic
  - linear operation or slew

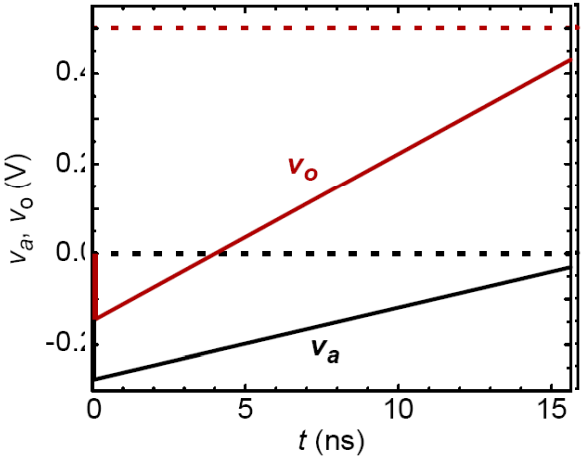
GB_i

$$v_a\left(\frac{T_s}{2}\right) = \begin{cases} v_{ai}\exp\left(\frac{g_m}{C_{eql}}\frac{T_s}{2}\right) & \text{Linear} \\ \frac{i_o}{g_m}\operatorname{sgn}(v_{ai})\exp\left[\frac{g_m}{C_{eql}}\left(\frac{T_s}{2} - t_{sl}\right)\right] & \text{Partial Slew} \\ v_{ai} - \frac{i_o}{C_{eql}}\operatorname{sgn}(v_{ai})\frac{T_s}{2} & \text{Slew} \end{cases}$$

SR_i

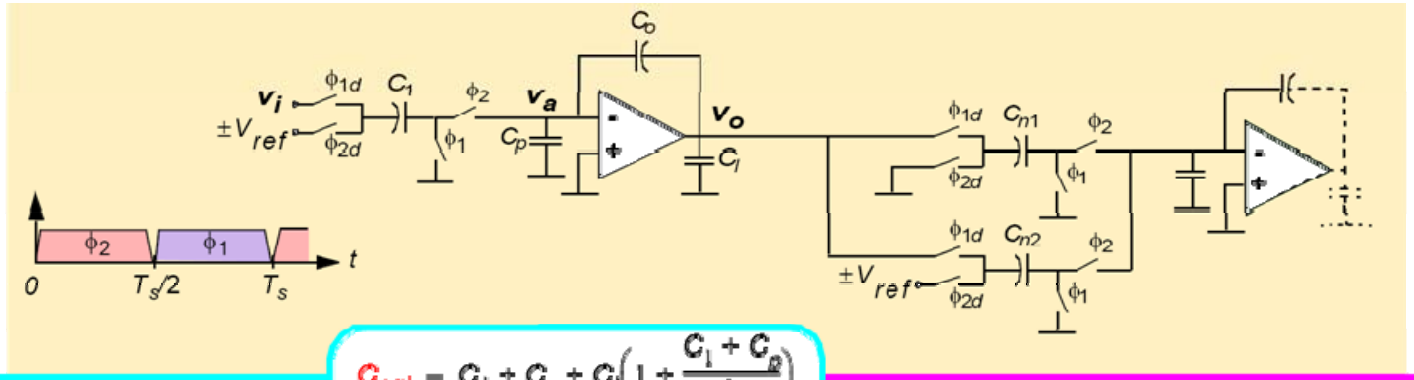
$$v_o\left(\frac{T_s}{2}\right) \quad v_{o,n} \; 1 \; \frac{C_1}{C_o}(v_i \pm V_{ref}) \; \left(1 \; \frac{C_p \; C_1}{C_o}\right) v_a\left(\frac{T_s}{2}\right)$$

Full slew



DT-ΣΔMs: Integrator incomplete settling

Integrator temporal evolution: [Rio00]



$$C_{eqi} = C_1 + C_p + C_f\left(1 + \frac{C_1 + C_p}{C_o}\right)$$

$$C_{eqs} = C_p + (C_f + C_{n1} + C_{n2})\left(1 + \frac{C_p}{C_o}\right)$$

- **Integration-Phase:**
  - finite opamp dynamic
  - linear operation or slew

GB_i

$$v_a\left(\frac{T_s}{2}\right) \begin{cases} v_{ai}\exp\left(\frac{g_m}{C_{eqi}}\frac{T_s}{2}\right) & \text{Linear} \\ \frac{I_o}{g_m}\mathrm{sgn}(v_{ai})\exp\left[\frac{g_m}{C_{eqi}}\left(\frac{T_s}{2} - t_{oi}\right)\right] & \text{Partial Slew} \\ v_{ai} - \frac{I_o}{C_{eqi}}\mathrm{sgn}(v_{ai})\frac{T_s}{2} & \text{Slew} \end{cases}$$

SR_i

$$v_o\left(\frac{T_s}{2}\right) \quad v_{o,n} \quad 1 \quad \frac{C_1}{C_o}(v_f \pm V_{ref}) \quad \left(1 \quad \frac{C_p \quad C_1}{C_o}\right) v_a\left(\frac{T_s}{2}\right)$$

- **Sampling-Phase:**
  - finite opamp dynamic
  - linear operation or slew

GB_s

$$v_a(T_s) \begin{cases} v_{ais}\exp\left(\frac{g_m}{C_{eqs}}\frac{T_s}{2}\right) & \text{Linear} \\ \frac{I_o}{g_m}\mathrm{sgn}(v_{ai})\exp\left[\frac{g_m}{C_{eqs}}\left(\frac{T_s}{2} - t_{os}\right)\right] & \text{Partial Slew} \\ v_{ais} - \frac{I_o}{C_{eqs}}\mathrm{sgn}(v_{ais})\frac{T_s}{2} & \text{Slew} \end{cases}$$

SR_s

$$v_o(T_s) \quad v_o\left(\frac{T_s}{2}\right) \quad \left(1 \quad \frac{C_p}{C_o}\right)\left[v_a(T_s) - v_a\left(\frac{T_s}{2}\right)\right]$$

DT-ΣΔMs: Integrator incomplete settling

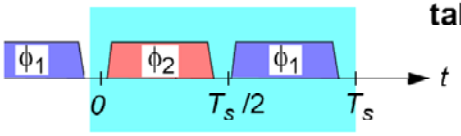
Integrator temporal evolution: [Rio00]

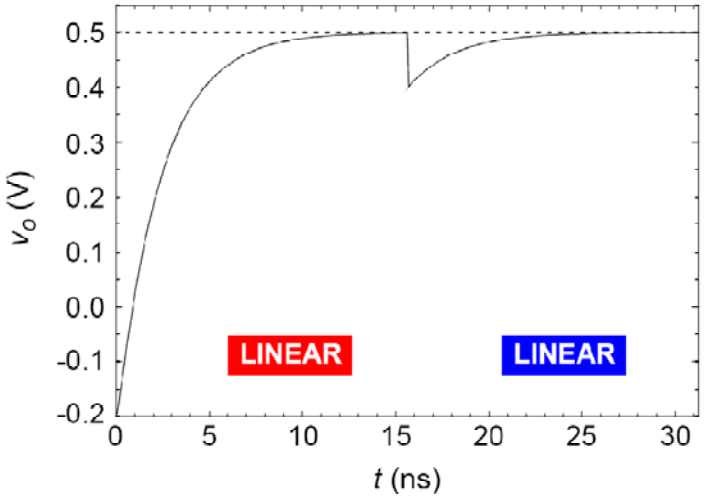
	INTEGRATION	SAMPLING
1	LINEAR	LINEAR
2	PARTIAL SLEW	LINEAR
3	SLEW	LINEAR
4	LINEAR	PARTIAL SLEW
5	PARTIAL SLEW	PARTIAL SLEW
6	SLEW	PARTIAL SLEW
7	LINEAR	SLEW
8	PARTIAL SLEW	SLEW
9	SLEW	SLEW

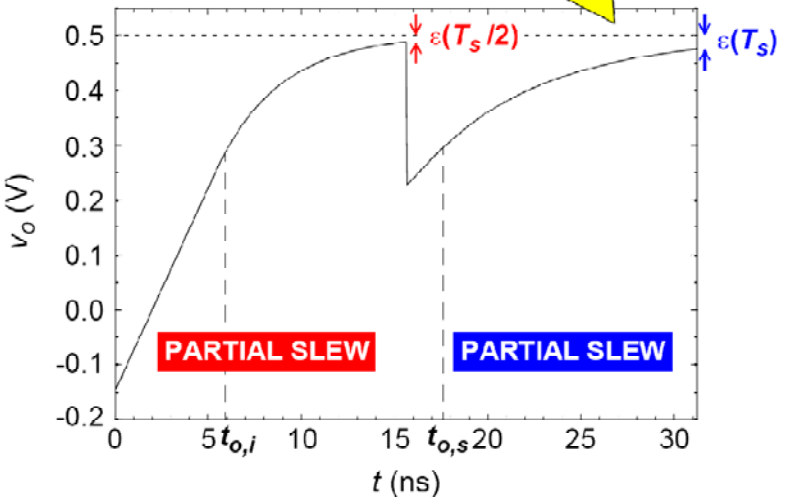
GB AND SR LIMITATIONS DURING BOTH CLOCK-PHASES

$$v_{o,n} \cong v_{o,n-1} - \frac{C_1}{C_o}(V_{12} - V_{11}) - \ldots - \frac{C_i}{C_o}(V_{i2} - V_{i1}) + \Theta(\tau_i) + \Theta(\tau_s)$$

Traditionally not taken into account

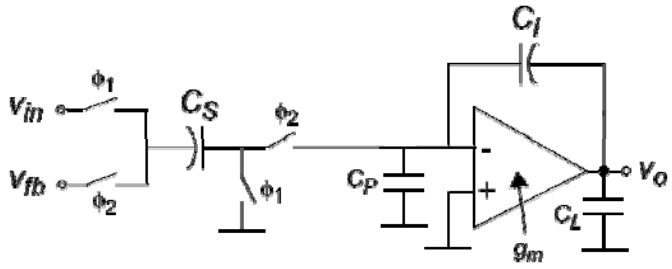






DT-ΣΔMs: Integrator incomplete settling

- Effect of the amplifier GB:

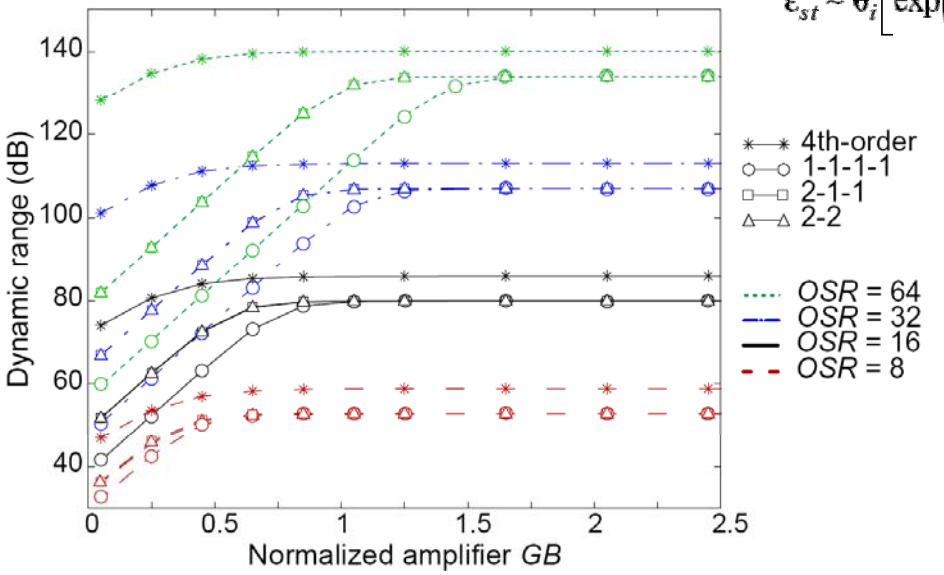


→ If only amplifier GB is considered (assuming no SR limitation)

$$GB_i = \frac{g_m}{C_{eq,i}} \qquad GB_s = \frac{g_m}{C_{eq,s}}$$

$$v_o(z) = \frac{C_S}{C_I}(1-\varepsilon_{st})\frac{z^{-1}v_{in}(z) - z^{-1/2}v_{fb}(z)}{1-z^{-1}}$$

$$\varepsilon_{st} \sim \theta_i\left[\exp\left(-GB_i\frac{T_s}{2}\right)\right] + \theta_s\left[\exp\left(-GB_s\frac{T_s}{2}\right)\right] + \theta_i \cdot \theta_s$$

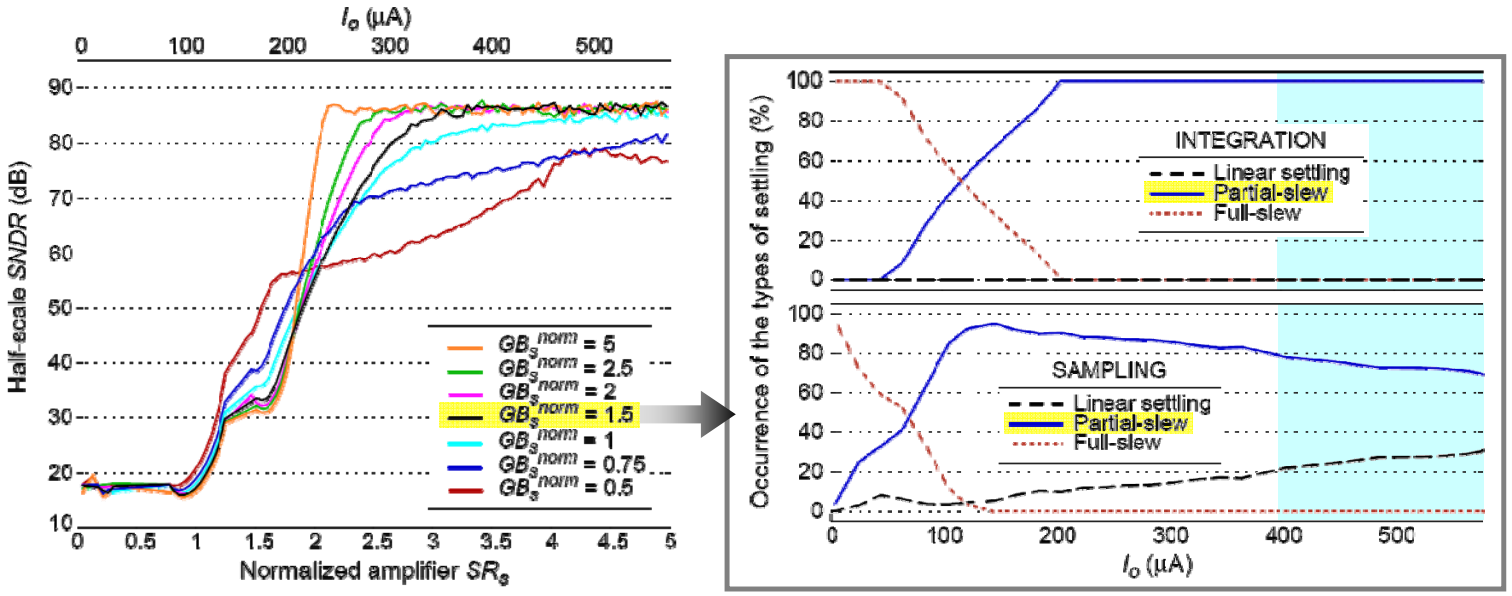


- Can be viewed as a systematic error in the integrator weight
- Effect on ΣΔMs similar to a mismatch between analog and digital coeffs
- It causes low-order noise leakages in cascade ΣΔMs

DT-ΣΔMs: Integrator incomplete settling

- Additional effect of the amplifier SR (+ GB):

  - "Dominant" linear dynamics are not mandatory in order to fulfill specs
  - SR can be traded for GB
  - It can be used to optimize the power consumption of amplifiers

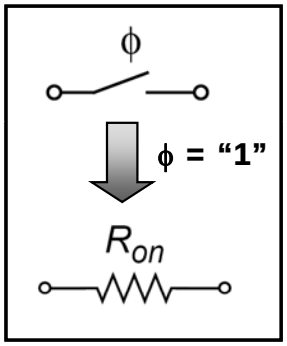


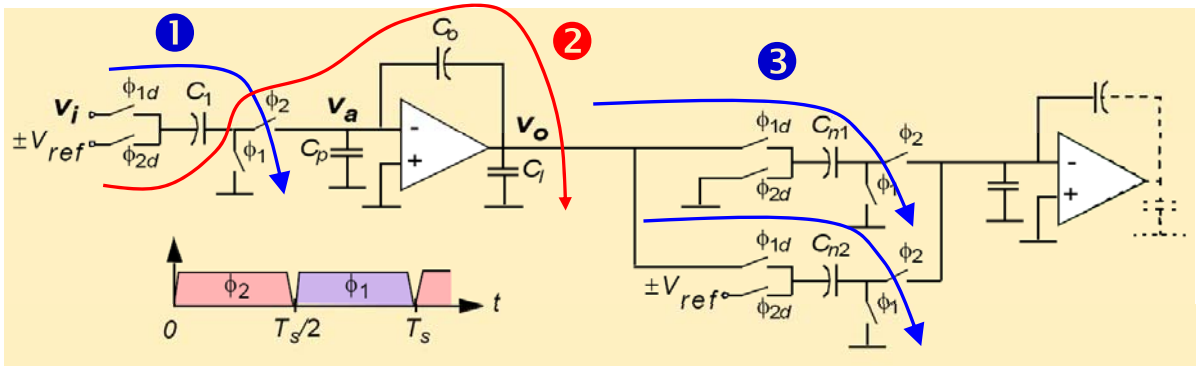
Non-linear dynamics cause distortion!

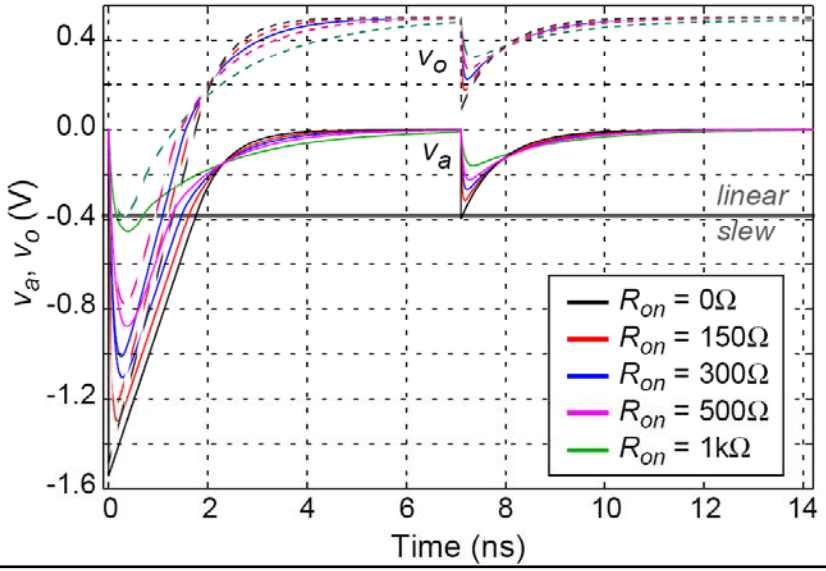
SR at the front-end integ must be carefully tackled

DT-ΣΔMs: Integrator incomplete settling

- Additional effect of the switches Ron (+ GB + SR):







→ Input is sampled with an error

1 $$\varepsilon_{on,s} = \exp\left(-\frac{1}{2R_{on}C_S}\frac{T_s}{2}\right)$$

→ Linear dynamics are slowed down

2 $$GB_{i,on} = \frac{GB_i}{1 + GB_i \cdot 2R_{on}C_S}$$

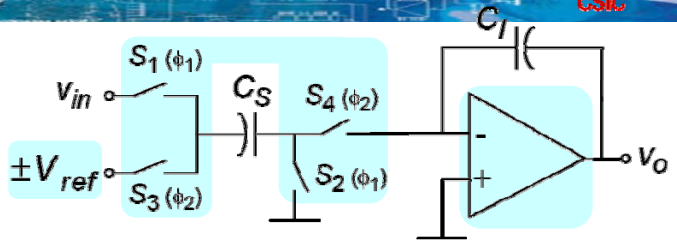
3 $$GB_{s,on} = \frac{GB_s}{1 + GB_s \cdot 2R_{non}C_{nS}}$$

→ Slew time shortens

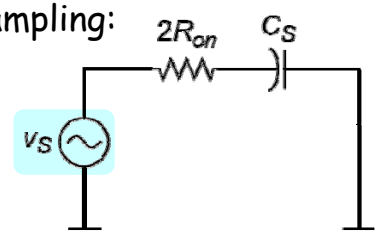
DT-ΣΔMs: Circuit noise

Main noise sources in SC integrators:

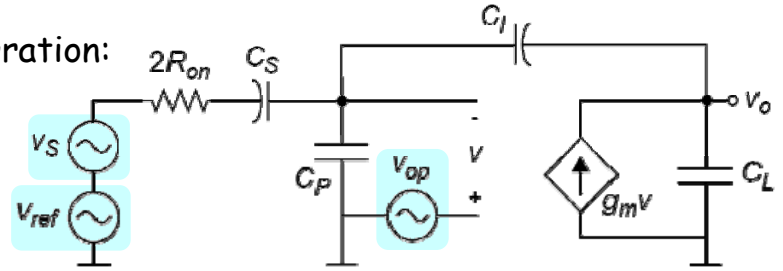
- Switches → Thermal noise
- Amplifiers → Thermal and flicker noise
- References → Thermal and flicker noise



Sampling:



Integration:



- Noise contribution of the switches (input-referred):

$$S_{in,S\phi_1}(f) = \frac{kT}{C_S f_s}\mathrm{sinc}^2(\pi f / f_s)$$

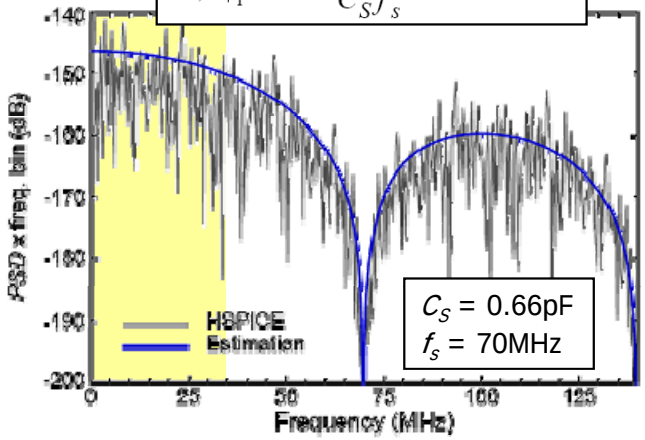
Switches for sampling $S_S = 2kT \cdot 2R_{on}$

$$H_{S\phi_1}(s) = \frac{1}{1 + s \cdot 2R_{on}C_S}$$

$$BW_{n,S\phi_1} = \int_0^{+\infty} |H_{S\phi_1}(f)|^2 df = \frac{1}{4 \cdot 2R_{on}C_S}$$

$$S_{in,S\phi_1}(f) \cong \frac{2BW_{n,S\phi_1}}{f_s} \cdot S_S \cong \frac{kT}{C_S f_s}$$

← Aliased component [Fisc82]



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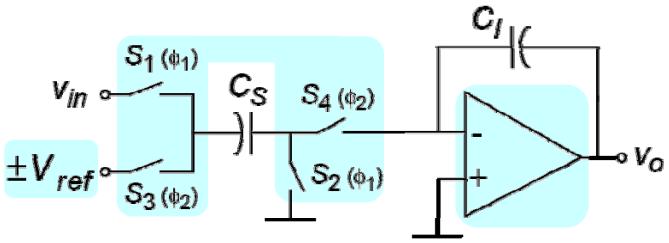
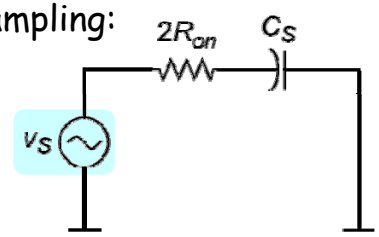
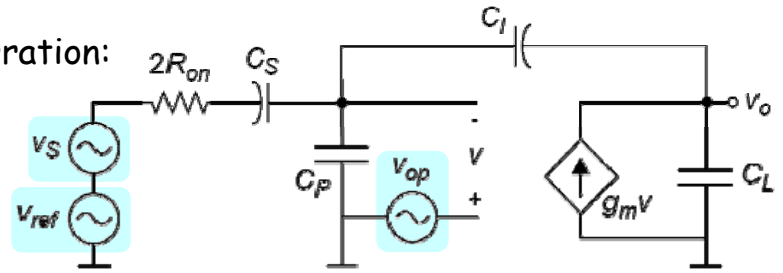


Sampling:



Integration:



- Noise contribution of the switches (input-referred):

Switches for sampling $S_S = 2kT \cdot 2R_{on}$ Switches for integration

$$H_{S\phi_1}(s) = \frac{1}{1 + s \cdot 2R_{on}C_S}$$

$$BW_{n,S\phi_1} = \int_0^{+\infty} |H_{S\phi_1}(f)|^2 df = \frac{1}{4 \cdot 2R_{on}C_S}$$

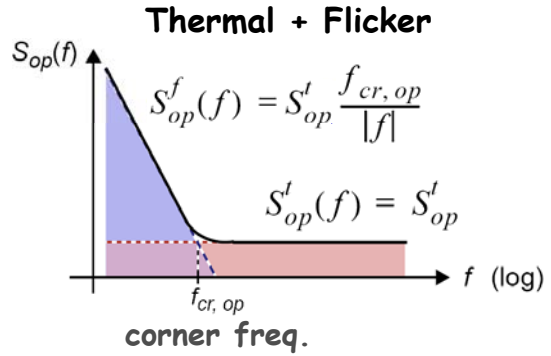
$$S_{in,S\phi_1}(f) \cong \frac{2BW_{n,S\phi_1}}{f_s} \cdot S_S \cong \frac{kT}{C_S f_s}$$

$$H_{S\phi_2}(s) = \frac{1 + s/z_1}{(1 + s/p_1)(1 + s/p_2)} \qquad z_1 = \frac{g_m}{C} \quad p_1 \cong \frac{g_m}{C_{eq,i}} \quad p_2 \cong \frac{C_{eq,i}}{C} \cdot \frac{1}{2R_{on}C_S}$$

$$BW_{n,S\phi_2} = \int_0^{+\infty} |H_{S\phi_2}(f)|^2 df \cong \frac{p_2}{4} \approx \frac{1}{4 \cdot 2R_{on}C_S}$$

$$S_{in,S\phi_2}(f) \cong \frac{2BW_{n,S\phi_2}}{f_s} \cdot S_S \cong \frac{kT}{C_S f_s}$$

- Noise contribution of the amplifier (input-referred):



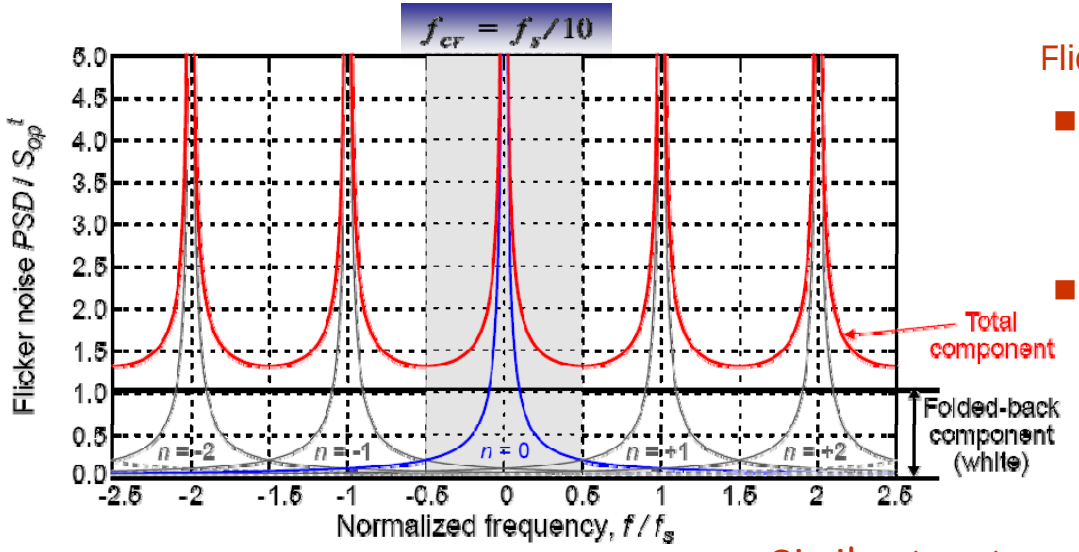
Thermal component

$$H_{op}(s) = \frac{1}{(1+s/p_1)(1+s/p_2)} \qquad p_1 \cong \frac{g_m}{C_{eq,i}} \qquad p_2 \cong \frac{C_{eq,i}}{C} \cdot \frac{1}{2R_{on}C_S}$$

$$BW_{n,op} = \int_0^{+\infty} |H_{op}(f)|^2 df \cong \frac{p_1}{4} \cong \frac{g_m}{4C_{eq,i}}$$

$$S_{in,op}^t(f) \cong \frac{2BW_{n,op}}{f_s} \cdot S_{op}^t \cong \frac{GB_i}{2f_s} \cdot S_{op}^t$$

← Aliased component



Flicker component

- Low-pass filtered version at the integ input:

$$S_{op}^f(f)|H_{op}(f)|^2 \cong S_{op}^t f_{cr,op}/|f|$$

- Folded tails are "submerged" into the aliased thermal noise

$$S_{in,op}^f(f) \cong S_{op}^t \frac{f_{cr,op}}{|f|}$$

Similar treatment for the references

DT-ΣΔMs: Circuit noise

Total noise PSD for the front-end integ:

$$S_{eq,in}(f) \cong \underbrace{\frac{2kT}{C_S f_s}}_{\text{switches}} + \underbrace{S_{op}^t\left(\frac{GB_i}{2f_s} + \frac{f_{cr,op}}{|f|}\right)}_{\text{amplifier}} + \underbrace{S_{ref}^t\left(\frac{GB_{ref}}{2f_s} + \frac{f_{cr,ref}}{|f|}\right)}_{\text{references}}$$

Switches:

- kT/C is the ultimate limitation on the converter resolution
- It can only be decreased by increasing Cs and/or fs (it does not depend on Ron!)
- x2 in fully-diff implementations (3-dB increase, but signal power is 6dB larger!)

Amplifiers & References:

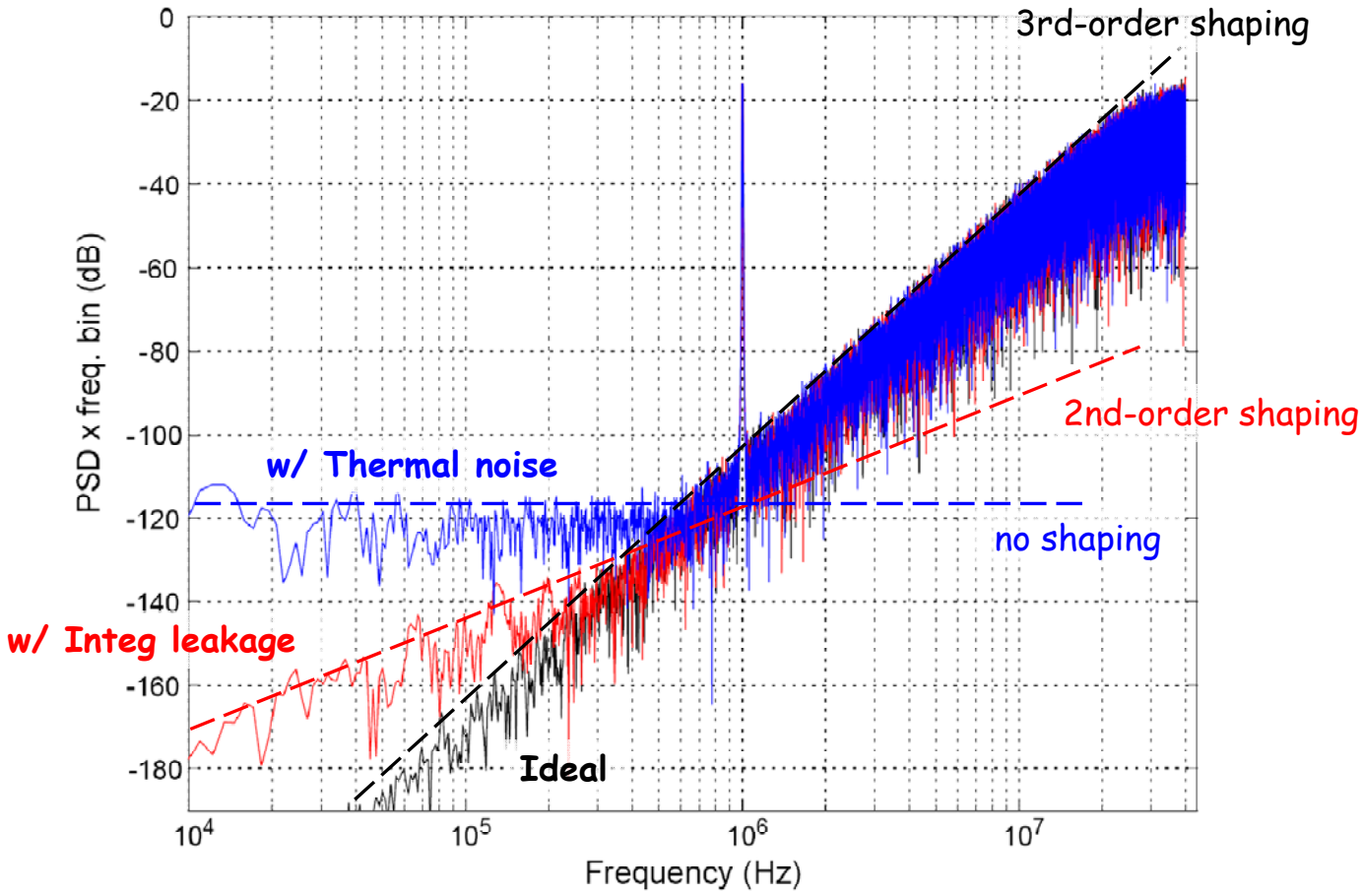
- GBs should be as low as settling errors allow (reduces folding!)
- 1/f contributions decrease with the corner frequency
- Adequate techniques can be applied in low-freq apps: CDS, chopper, … [Enz96]

$$P_{CN,in} \cong \left[\frac{2kT}{C_S} + S_{op}^t\frac{GB_i}{2} + S_{ref}^t\frac{GB_{ref}}{2}\right]\frac{1}{OSR} + 2\ln\left(\frac{f_b}{f_o}\right)\left(S_{op}^t f_{cr,op} + S_{ref}^t f_{cr,ref}\right)$$

In-band error power due to circuit noise in the ΣΔM

DT-ΣΔMs: Circuit noise

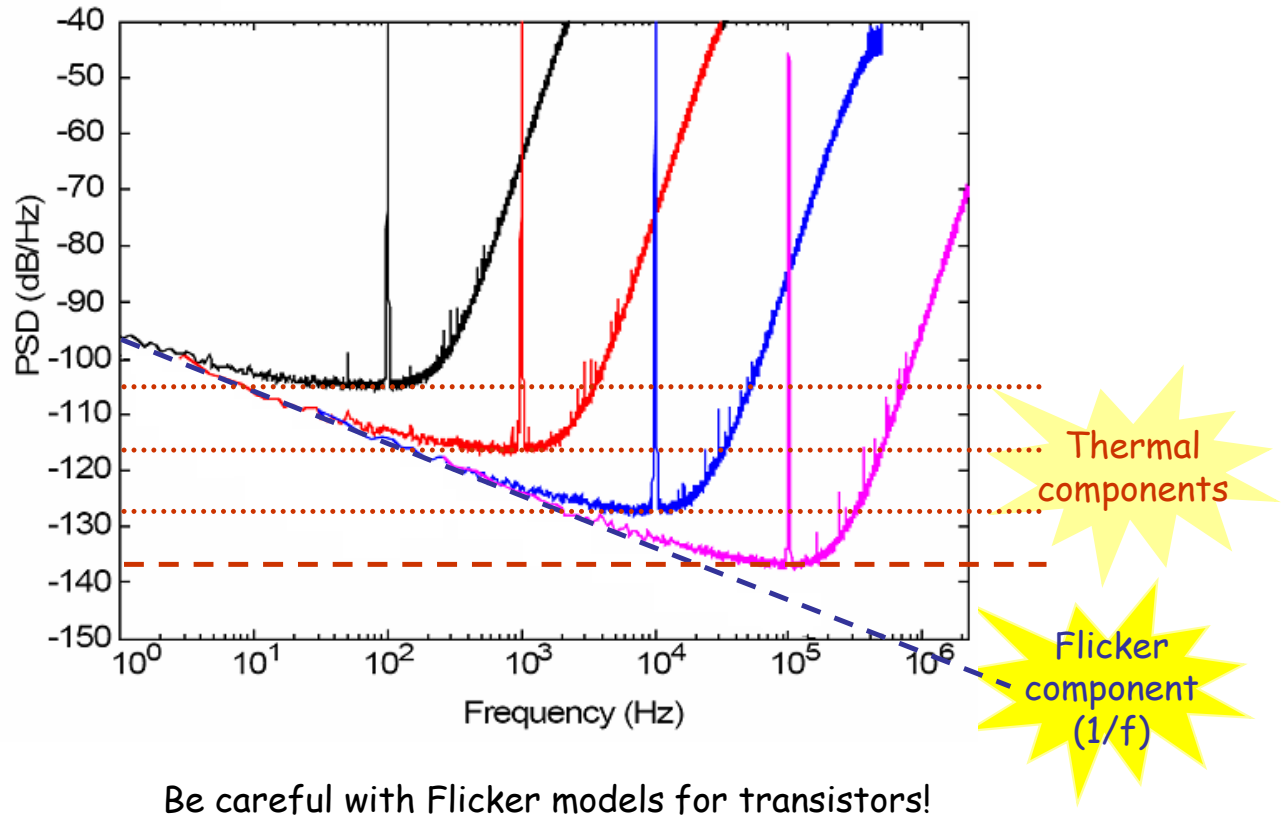
Effect of noise leakages and thermal noise on a 2-1 cascade



DT-ΣΔMs: Circuit noise

Effect of 1/f and thermal noise on the spectra of a 4th-order ΣΔM

(silicon results for several fs)

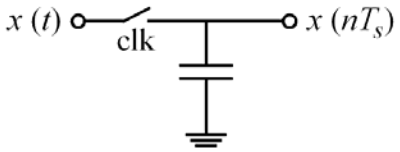


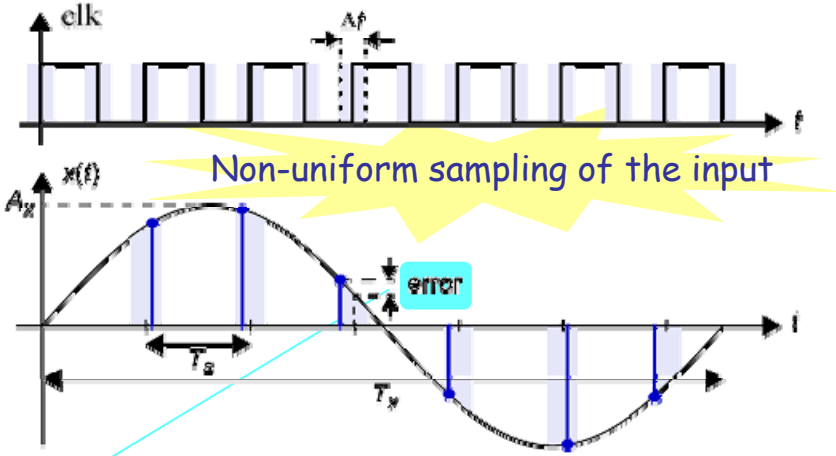
Be careful with Flicker models for transistors!

Front-end amplifier needed redesign!

DT-ΣΔMs: Clock jitter

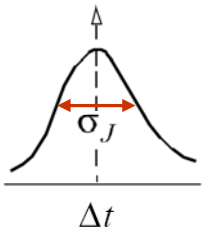
- Sampling time uncertainty [Boser88]:





Non-uniform sampling of the input

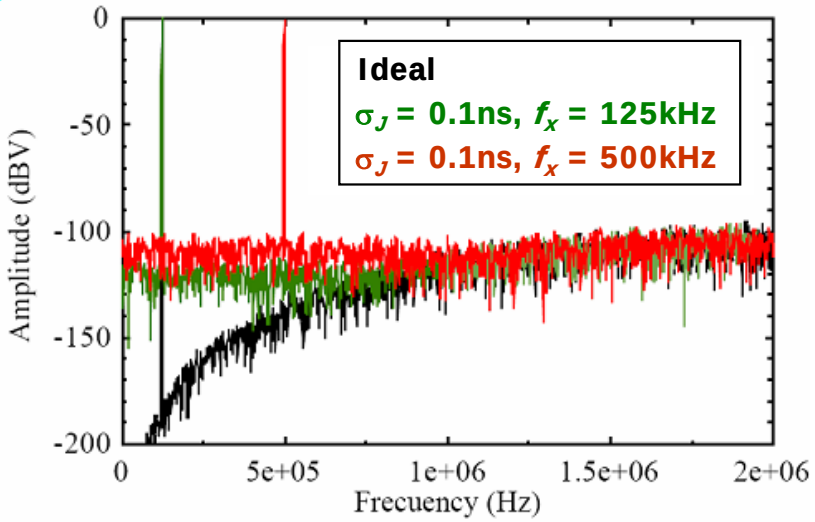
→ If jitter is modeled as random:



$$S_J = \frac{A_x^2}{2}\frac{(2\pi f_x \sigma_J)^2}{f_s}$$

$$P_J = \frac{A_x^2}{2}\frac{(2\pi f_x \sigma_J)^2}{OSR}$$

Error is larger, the larger input freq (wideband apps!)

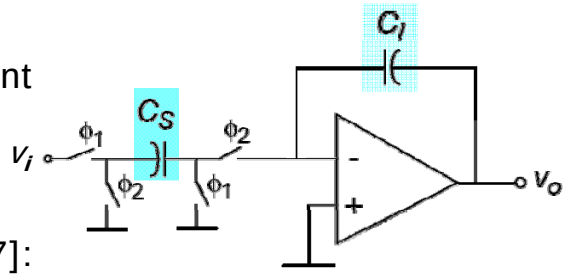


DT-ΣΔMs: Non-linearity of capacitors

→ In an ideal capacitor: dq = Cdv

→ In practice: dq = C(v)dv, with C being voltage-dependent

$$C(v) = C(1 + a_1 v + a_2 v^2 + \ldots)$$



→ Considering the effect of the sampling cap only [Bran97]:

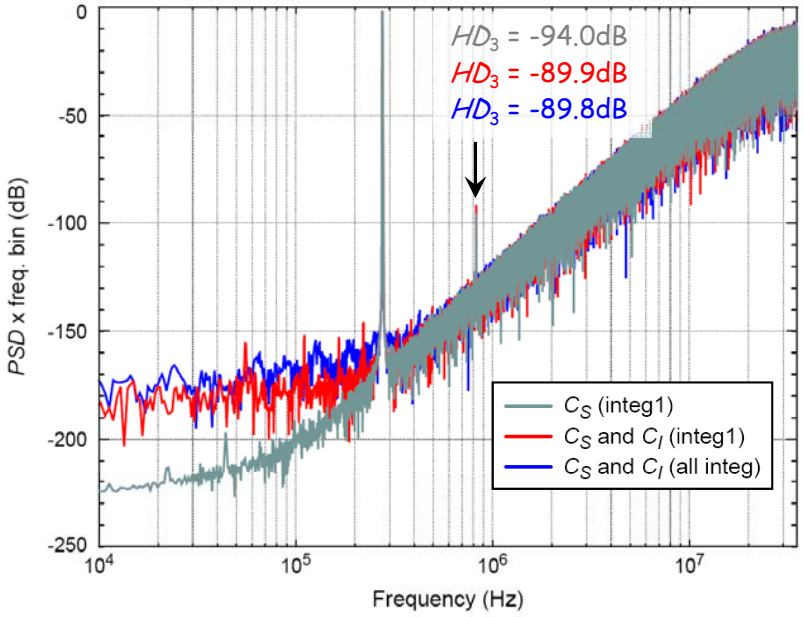
$$v_{o,n} \cong v_{o,n-1} + g_1 v_{in,n-1}\left(1 + \frac{a_1}{2} v_{in,n-1} + \frac{a_2}{3} v_{in,n-1}^2\right)$$

$$A_2 \cong \frac{1}{2}\left(\frac{a_1}{2} A_x^2\right) \Rightarrow HD_2 \cong 20\log_{10}\left(\frac{a_1}{4} A_x\right)$$

$$A_3 \cong \frac{1}{4}\left(\frac{a_2}{3} A_x^3\right) \Rightarrow HD_3 \cong 20\log_{10}\left(\frac{a_2}{12} A_x^2\right)$$

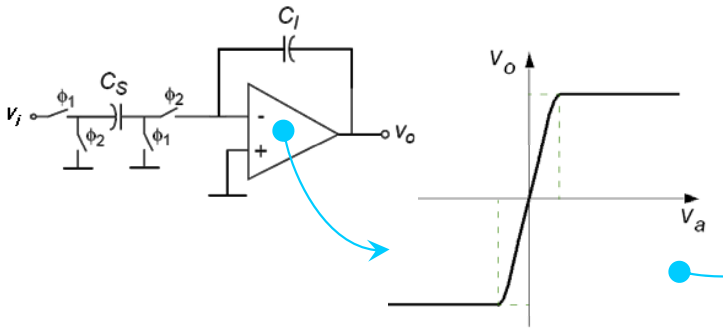
- Even-order distortion cancels w/ fully-diff
- Non-linearity of sampling cap dominates
- Valid for weak non-linearities (MOS caps are very non-linear!)

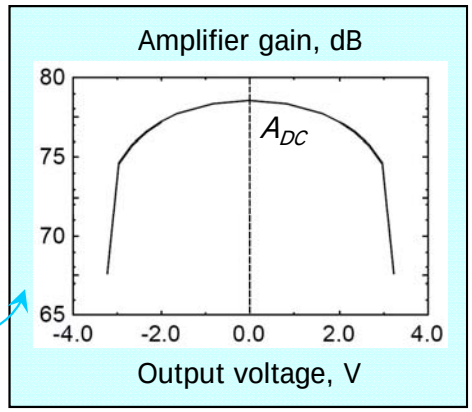
a_1 = 500ppm/V, a_2 = 500ppm/V²



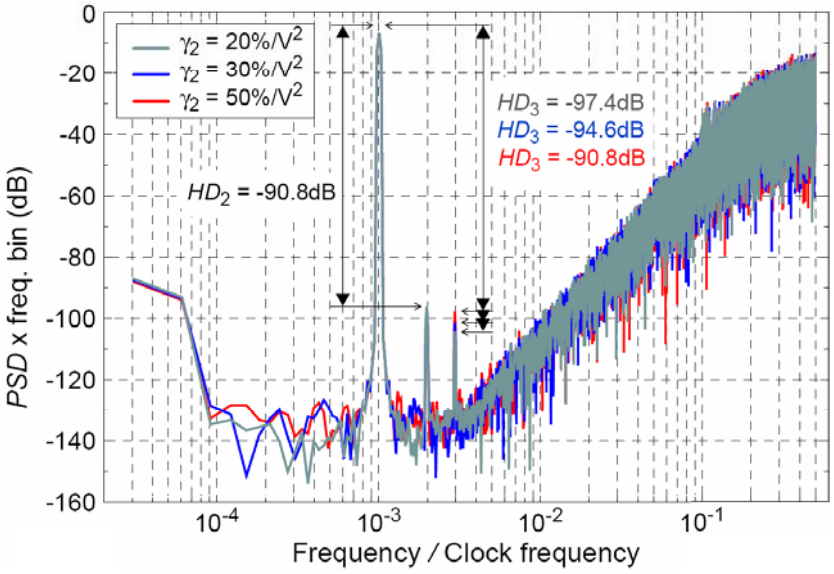
DT-ΣΔMs: Non-linear Amplifier Gain

→ Actual amplifier gain depends on output voltage:





A_{DC} = 500, γ_1 = 10%/V (single-ended ΣΔM)



$$A_{DC}(v_o) = A_{DC}(1 + \gamma_1 v_o + \gamma_2 v_o^2 + \ldots)$$

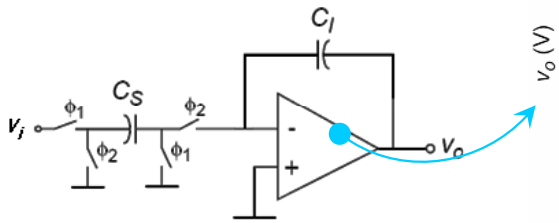
$$HD_2 \cong 20\log_{10}\left(\frac{\gamma_1}{2}\frac{(1+g)}{A_{DC}} g A_x\right)$$

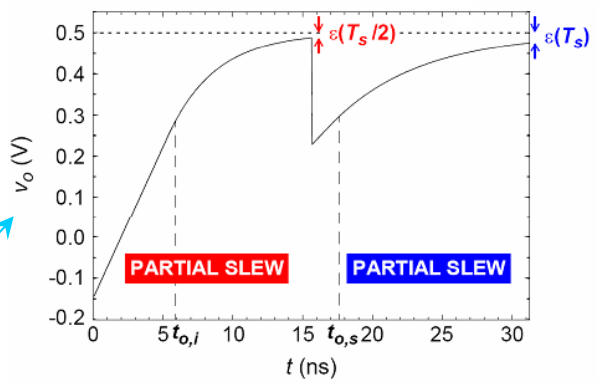
$$HD_3 \cong 20\log_{10}\left(\frac{\gamma_2}{4}\frac{(1+g)}{A_{DC}} g^2 A_x^2\right)$$ [Yin94]

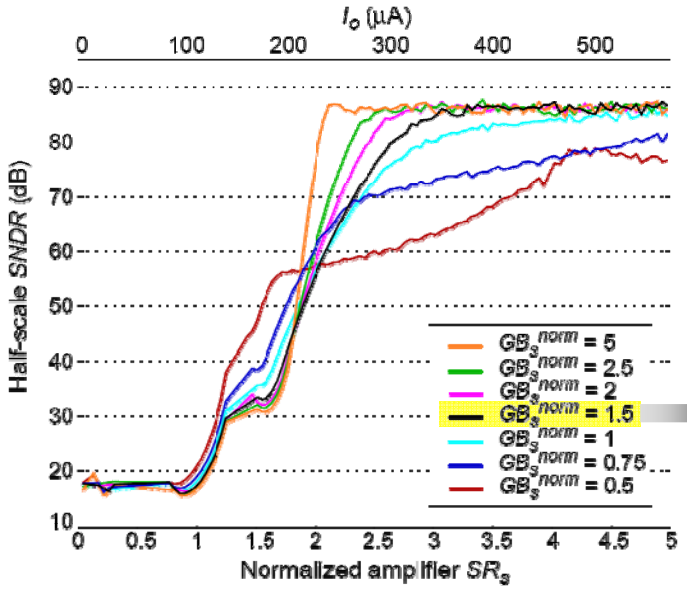
- Increasing A_{DC} helps a lot!
- A_{DC} at the front-end larger than noise leakages require

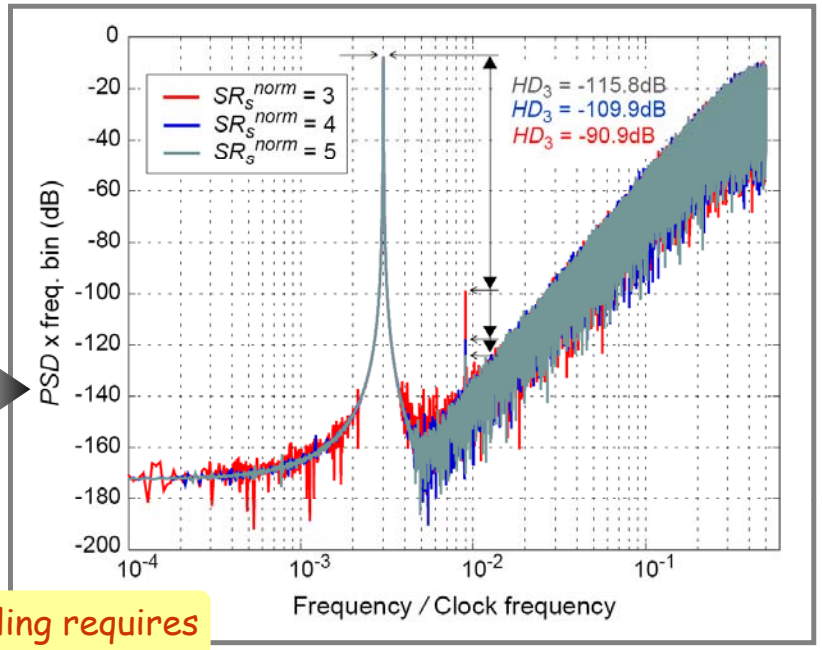
DT-ΣΔMs: Non-linear settling

→ SR can trade for GB in the integrator settling, but non-linear dynamics cause distortion:





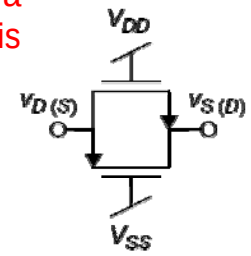


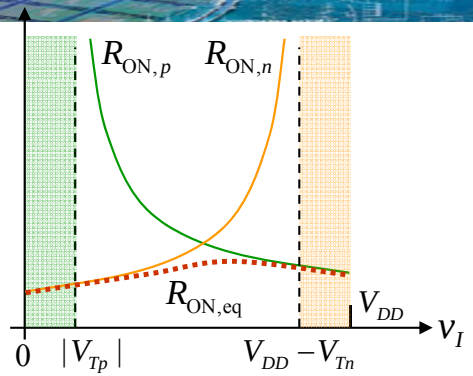


SR at the front-end larger than settling requires

DT-ΣΔMs: Non-linear switch resistance

→ Switches exhibit a finite R_{ON} which is also non-linear:



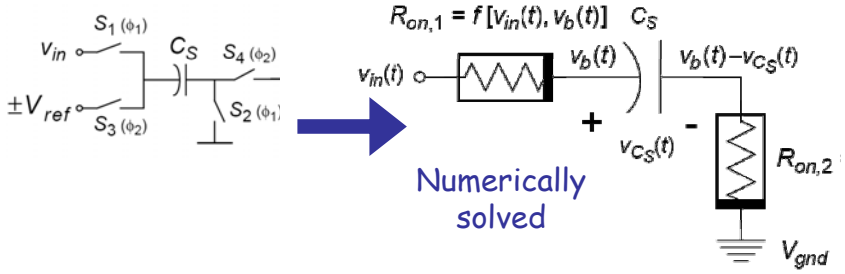


$$R_{ON,n} = \frac{1}{k'_n \left(\frac{W}{L}\right)_n (V_{DD} - v_I - V_{Tn})}$$

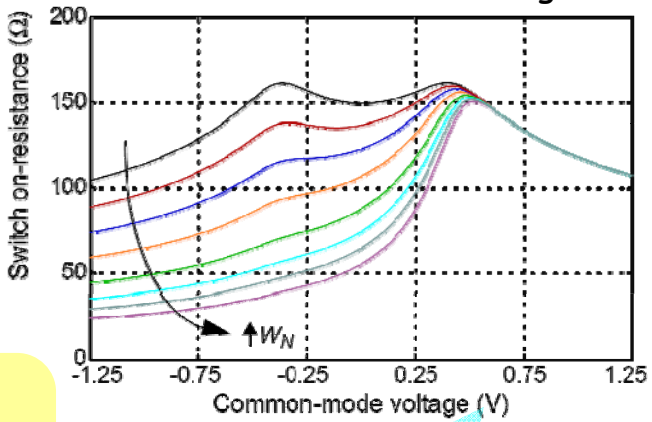
$$R_{ON,p} = \frac{1}{k'_p \left(\frac{W}{L}\right)_p (v_I - |V_{Tp}|)}$$

$$R_{ON,eq} = R_{ON,n} // R_{ON,p}$$

■ Non-linear sampling [Geer02]:



Alternative switch sizings

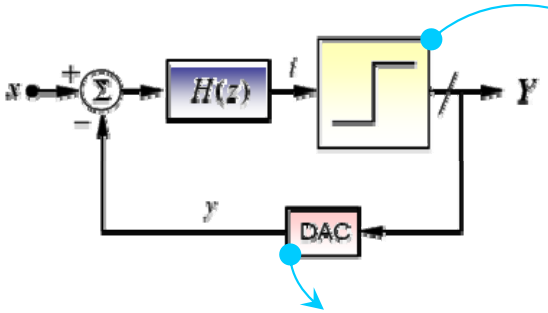


- Distortion is dynamic (increases with input freq!)
- Front-end switch dominates
- R_{ON} at the front-end smaller than settling requires
- Very important in low-voltage!

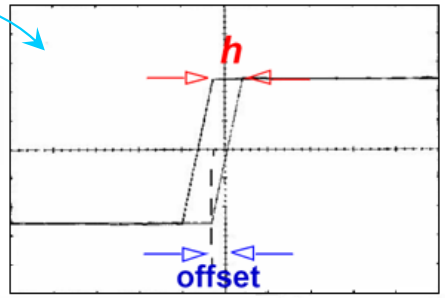
Most suited sizing depends on parasitics, Vref/Vsupply, ...

DT-ΣΔMs: Comparators and multi-bit quantizers

- Single-bit ΣΔMs:



Comparator:

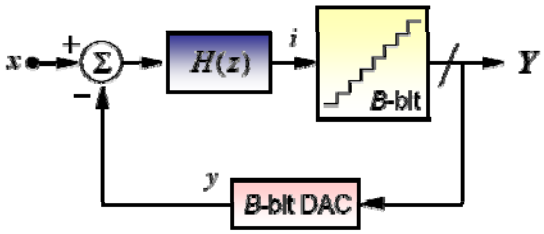


- **Offset** → Attenuated by the integrator DC gain
- **Hysteresis** → Shaped similarly to quantization error [Boser88]

$$P_h = 4h^2 \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}$$

1-bit DAC → Inherently linear

- Multi-bit ΣΔMs:



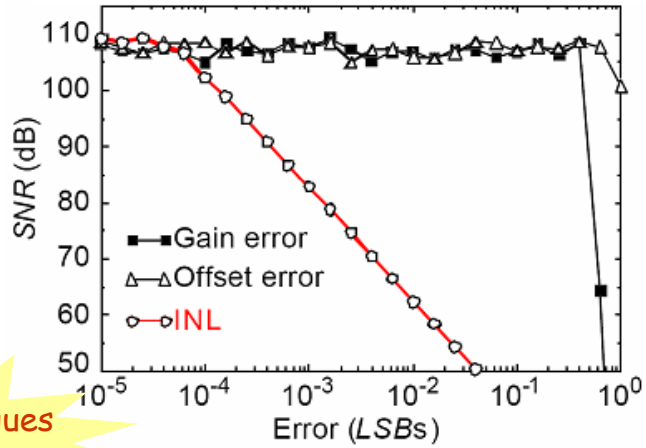
Multi-bit ADC → Errors attenuated/shaped

Multi-bit DAC → Non-linearity directly added to the input!

[Mede99]: $\sigma_D^2 = \frac{1}{2}\left(\frac{\Delta}{2^B - 1}\right)^2 \mathrm{INL}_{\mathrm{LSB}}^2$

DEM techniques
Dual quantization

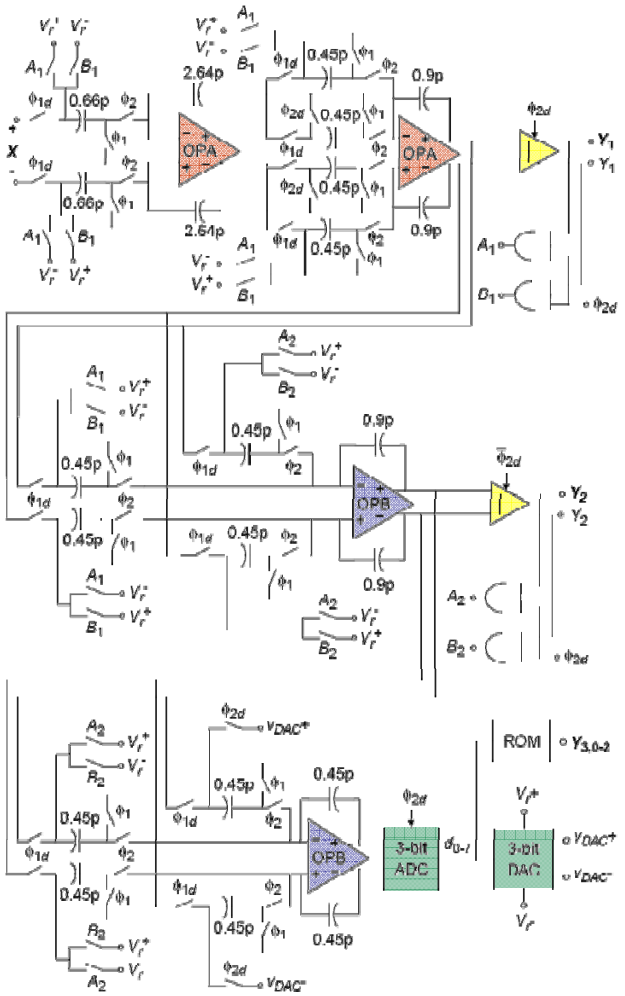
Effect of DAC errors on a 2nd-order 3-bit ΣΔM



A 2.5-V Cascade SDM in CMOS 0.25um for ADSL/ADSL+

2-1-1 w/ dual quantization

- Two different amplifiers: 2-stage OA in the 1st stage, and 1-stage OA in 2nd and 3rd stages.
- Standard CMOS switches (no clock-boosting).
- Only 2-branch integrators and 2x16 unit capacitors (MiM).
- Comparators: regenerative latch + preamplification stage.
- 3-bit quantizer in the last stage:
  - Resistive-ladder DAC (no calibration).
  - Flash ADC: Static differential input stage + latched comparators.
- Power-down control.



DT-ΣΔMs: Case study - Blocks Specs

Blocks Specs

EQUATION DATABASE

	Typical	Worst Case
Quantization noise	-88.1dB	-86.2dB
Ideal	-90.3dB	
DC gain leakage	-99.6dB	
Cap. mismatch/leakage (σ_C = 0.05% / 0.1%)	-95.4dB	-89.4dB
DAC error	-96.4dB	
Thermal noise	-84.8dB	-82.2dB
kT/C noise	-88.1dB	-86.0dB
Amplifier noise	-87.5dB	-84.5dB
Clock jitter	-90.1dB	
In-band error power	-82.3dB	-80.3dB
Dynamic range	82.8dB (13.5bit)	80.8dB (13.1bit)

Corner analysis:

- Fast and slow devices models
- Temperature range: [-40ºC, +110ºC]
- ±5% variation in the 2.5-V supply

MODULATOR	Topology	2-1-1(3b)
	Oversampling ratio	16
	Reference voltage	1.5V
	Clock frequency	70.4MHz
	Clock jitter	15ps (0.1%)
FRONT-END INTEGRATOR	Sampling capacitor	0.66pF
	Cap. sigma (MiM, 1pF)	0.05%
	Cap. tolerance	±20%
	Bottom parasitic cap.	1%
	Switch on-resistance	150Ω
AMPLIFIER	DC gain	3000 (70dB)
	GB (1.5pF)	265MHz
	Slew rate (1.5pF)	800V/μs
	Output swing	±1.8V
	Input equivalent noise	6nV/sqrt(Hz)
COMPARATORS	Hysteresis	20mV
	Offset	±10mV
	Resolution time	3ns
3-bit QUANTIZER	DAC *INL*	0.5%FS

DT-ΣΔMs: Case study

$$P_{CN} = P_{kT/C} + P_{op} = \frac{4kT}{C_S} \cdot \frac{1}{OSR} + \frac{2\pi \cdot GB_{eff}}{2OSR} S_{op}^{d}$$

$$GB_{eff} \cong \frac{GB}{1 + GB/f_{on}} = \frac{GB}{1 + GB \cdot 2\pi \cdot 2R_{on}C_S}$$

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Ideal	-90.3dB	
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	Oversampling ratio	16
	Reference voltage	1.5V
	Clock frequency	70.4MHz
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FRONT-END INTEGRATOR	Sampling capacitor	0.66pF
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	Cap. tolerance	±20%
	Bottom parasitic cap.	1%
	Switch on-resistance	150Ω
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COMPARATORS	Hysteresis	20mV
	Offset	±10mV
	Resolution time	3ns
3-bit QUANTIZER	DAC *INL*	0.5%FS

Integrator Dynamics

- $GB > 2.5 f_s$ is ideally enough to limit settling errors (this architecture w/ $OSR = 16$).
- Switch on-resistance slows down the effective amplifier response:

$$GB_{eff} \cong \frac{GB}{1 + GB/f_{on}} = \frac{GB}{1 + GB \cdot 2\pi \cdot 2R_{on}C_S}$$

$R_{on} \sim 150\Omega$ requires just $GB > 3.2 f_s$

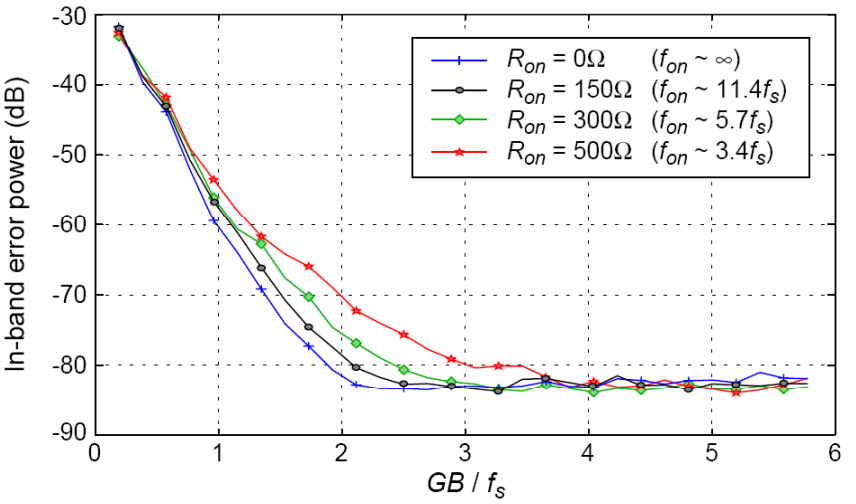
Standard switches
(no clock-boosting)

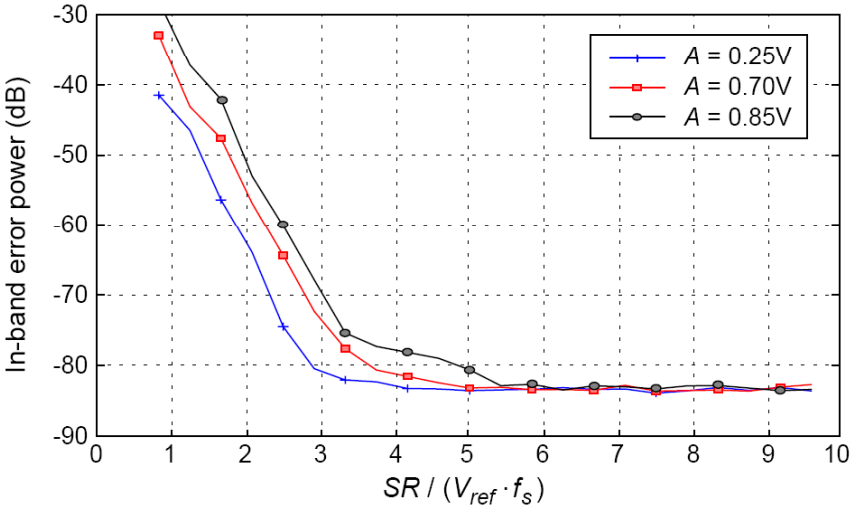
***GB* = 265MHz**
(assuming that 85% of the clock cycle is useful)

- Slew rate must be large enough to let the linear dynamic to correctly settle.

$SR/(V_{ref} \cdot f_s) = 6.5$ → ***SR* = 800V/μs**

- Partially slew-rate limited operation of the front-end integrator introduces distortion.





DT-ΣΔMs: Case study - Amplifiers

	INTEG. 1	INTEG. 2	INTEG. 3	INTEG. 4
Unit capacitor	0.66pF	0.45pF	0.45pF	
DC gain	3000 (70dB)		600 (56dB)	
GB (1.5pF)	265MHz		210MHz	
Slew rate (1.5pF)	800V/μs		350V/μs	
Output swing	±1.80V		±1.60V	
Input equivalent noise	6nV/sqrt(Hz)		50nV/sqrt(Hz)	

OPA **OPB**

- SC CMFB nets
- pMOS input scheme
  - Cancelled body effect (substrate noise coupling)
  - Smaller 1/f noise

DT-ΣΔMs: Case study - Amplifiers

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Unit capacitor	0.66pF	0.45pF	0.45pF	
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Output swing	±1.80V		±1.60V	
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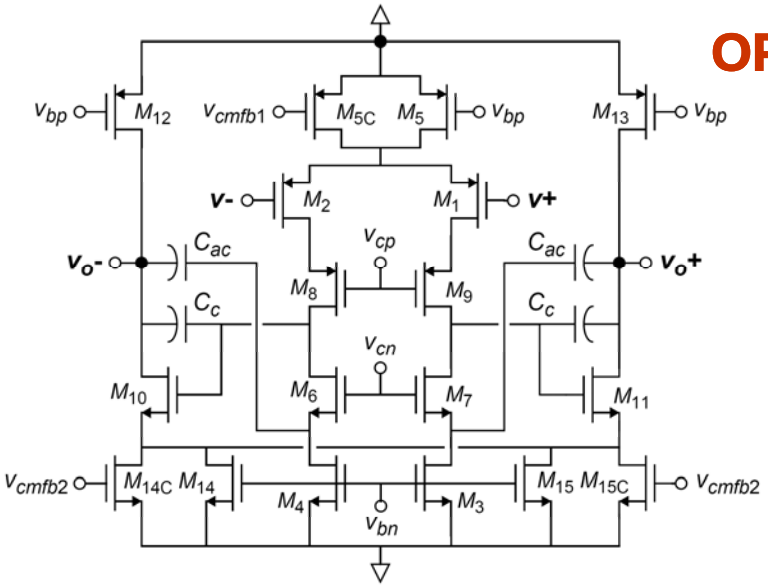
- SC CMFB nets
- pMOS input scheme
  - Cancelled body effect (substrate noise coupling)
  - Smaller 1/f noise



OPA 2-stage amplifier

Telescopic 1st stage
2-path compensation

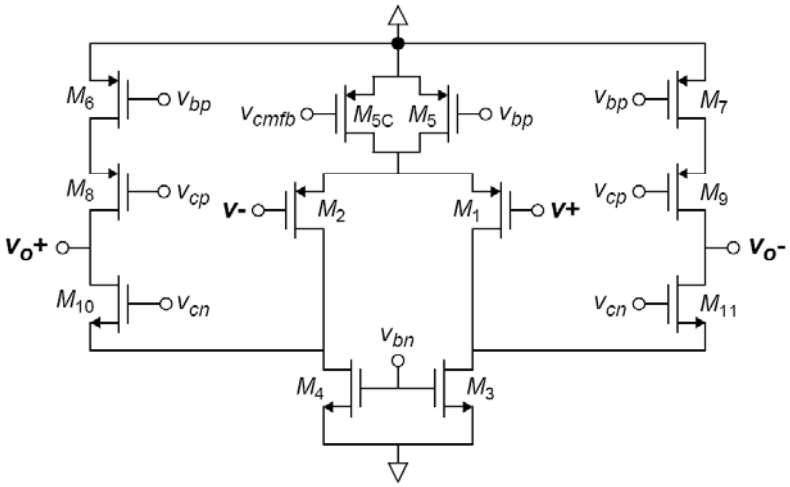
	Typical	Worst Case
DC gain	78.6dB	73.5dB
GB (1.5pF)	446.8MHz	331.5MHz
PM (1.5pF)	64.0º	57.9º
SR (1.5pF)	1059V/μs	883V/μs
Output swing	±2.09V	±1.86V
Input eq. noise	5.1nV/sqrt(Hz)	5.5nV/sqrt(Hz)
Input capacitance	126fF	129fF
Power consumption	17.2mW	19.4mW

	INTEG. 1	INTEG. 2	INTEG. 3	INTEG. 4
Unit capacitor	0.66pF	0.45pF	0.45pF	
DC gain	3000 (70dB)		600 (56dB)	
GB (1.5pF)	265MHz		210MHz	
Slew rate (1.5pF)	800V/μs		350V/μs	
Output swing	±1.80V		±1.60V	
Input equivalent noise	6nV/sqrt(Hz)		50nV/sqrt(Hz)	

- SC CMFB nets
- pMOS input scheme
  - Cancelled body effect (substrate noise coupling)
  - Smaller 1/f noise

OPB folded-cascode amplifier

	Typical	Worst Case
DC gain	58.0dB	56.8dB
GB (1.5pF)	393.5MHz	331.7MHz
PM (1.5pF)	70.3º	67.7º
SR (1.5pF)	377V/μs	373V/μs
Output swing	±1.97V	±1.72V
Input eq. noise	4.1nV/sqrt(Hz)	5.1nV/sqrt(Hz)
Input capacitance	300fF	343fF
Power consumption	6.6mW	6.9mW

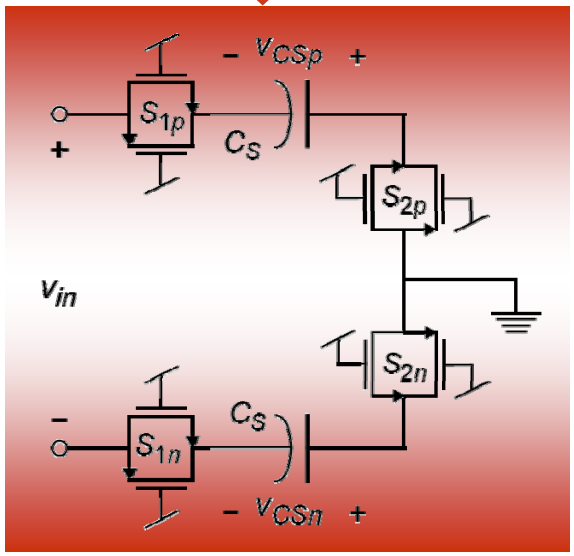


DT-ΣΔMs: Case study - Switch ON-Resistance

- **Slow-down of the integrators dynamics**
- **Incomplete sampling** (RC time constant)
- **Dynamic distortion** (front-end integrator)

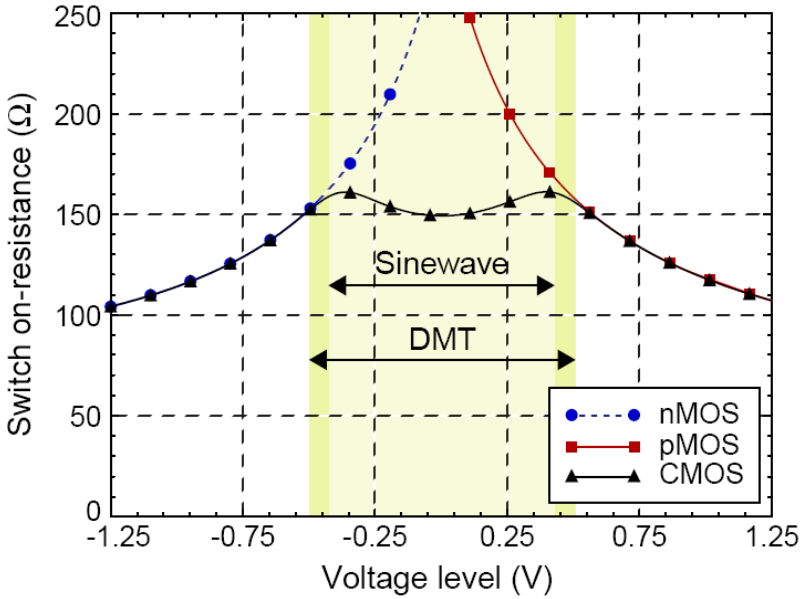
→ R_{on} ~ 150Ω

Standard CMOS switches



nMOS: 8.5/0.25
pMOS: 36.5/0.25

- No clock-boosting
- No low-Vt transistors



DT-ΣΔMs: Case study - Switch ON-Resistance

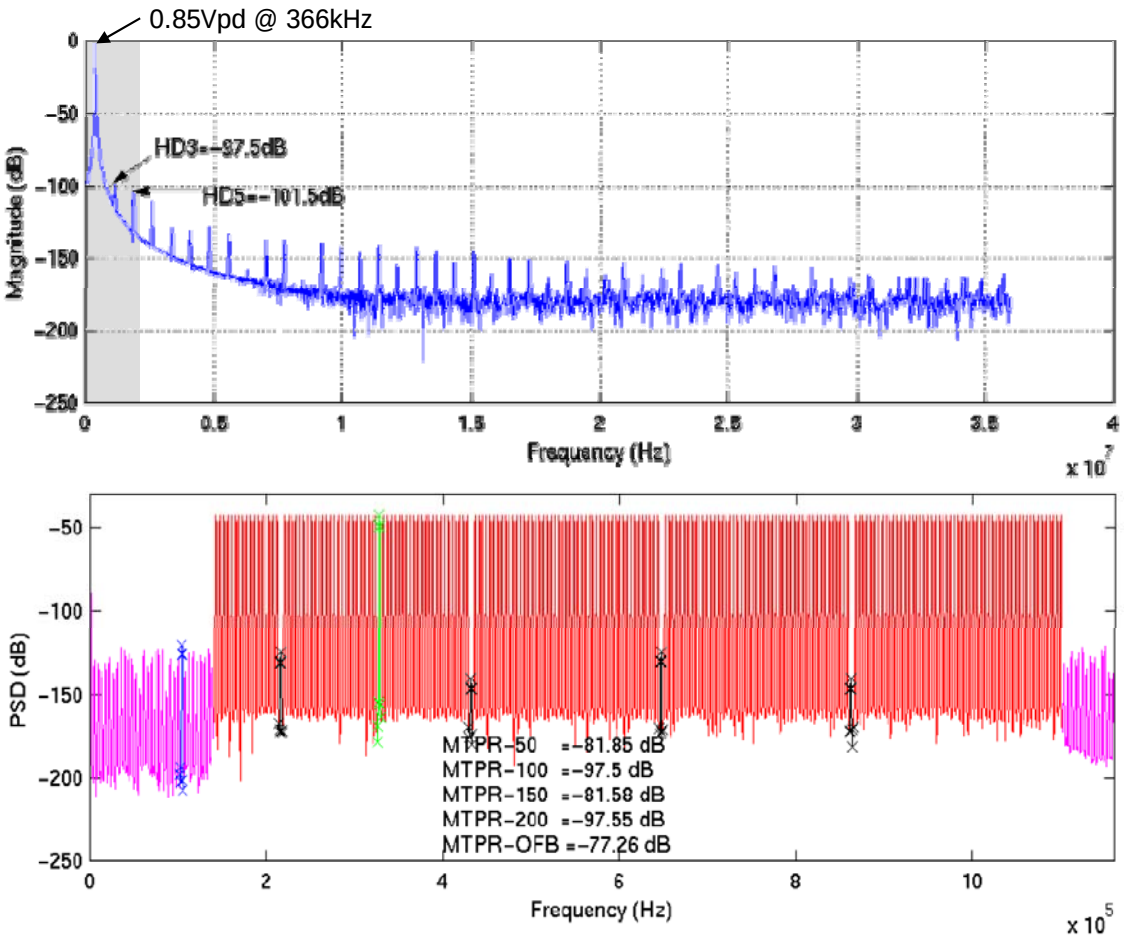
Dynamic distortion
evaluated through
electrical simulation

- **Sinewave input**

  THD < -96dB

- **DMT input**

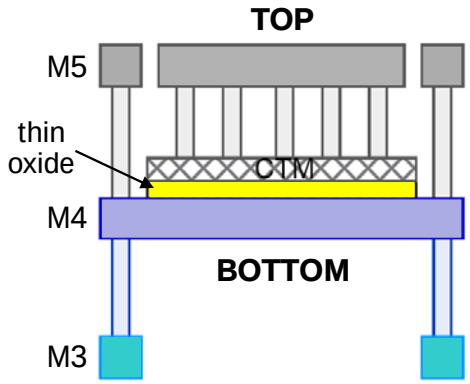
  MTPR < -81dB



DT-ΣΔMs: Case study - MiM Capacitors

CMOS tech with mixed-signal facilities

Thin oxide between metal 4 and metal 5



Cap. matching	0.05% (1pF)
Bottom plate parasitic	1%
Cap. spread	±20%

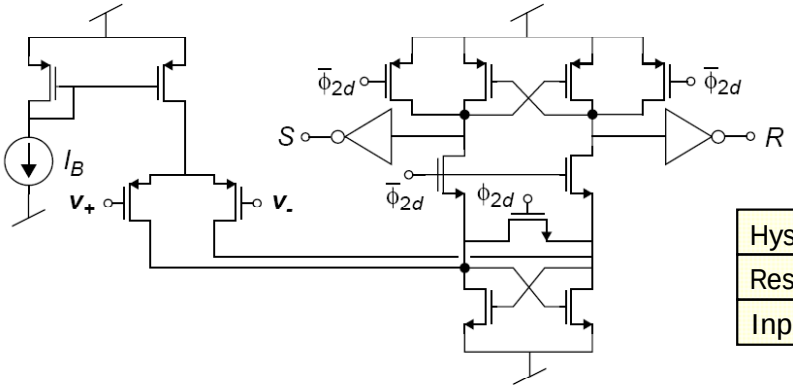
→ Very good matching (0.1% assumed for 6-σ design)

→ Helps to limit the capacitive load to integrators

→ **Integrators weights:**

- **Front-end integ, 0.66pF:** 27μm x 27μm
- **Remaining integs, 0.45pF:** 22μm x 22μm

→ **Also MiM caps in OPA, in the SC CMFB nets, and in the anti-aliasing filter**



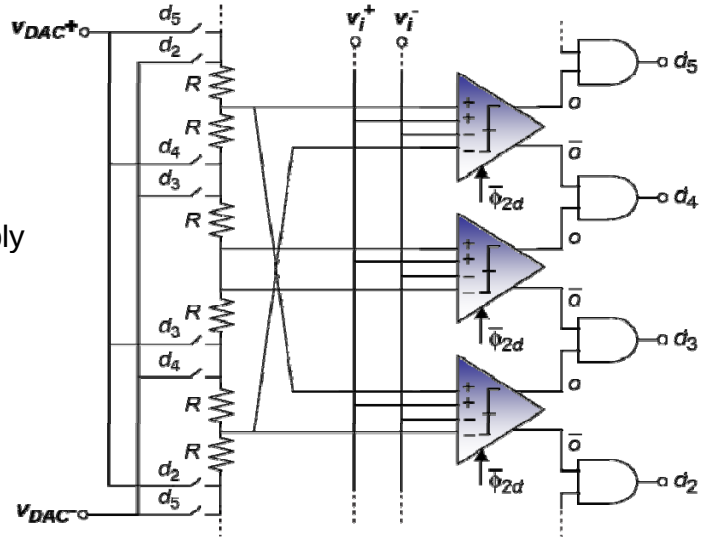
Comparator

Pre-amp + Regenerative latch + SR latch

(Different supplies)

Hysteresis	127.5μV	Offset	6.3mV
Resolution time, LH	3.9ns	Resolution time, HL	2.8ns
Input capacitance	100fF	Power consumption	0.3mW

3-bit Quantizer



Resistive-ladder DAC

- 700-Ω ladder between references +2V/+0.5V (14x50Ω, 3.21mW)
- Unsalicided *n*+ poly used in resistors
- References obtained from the on-chip analog supply

Flash ADC

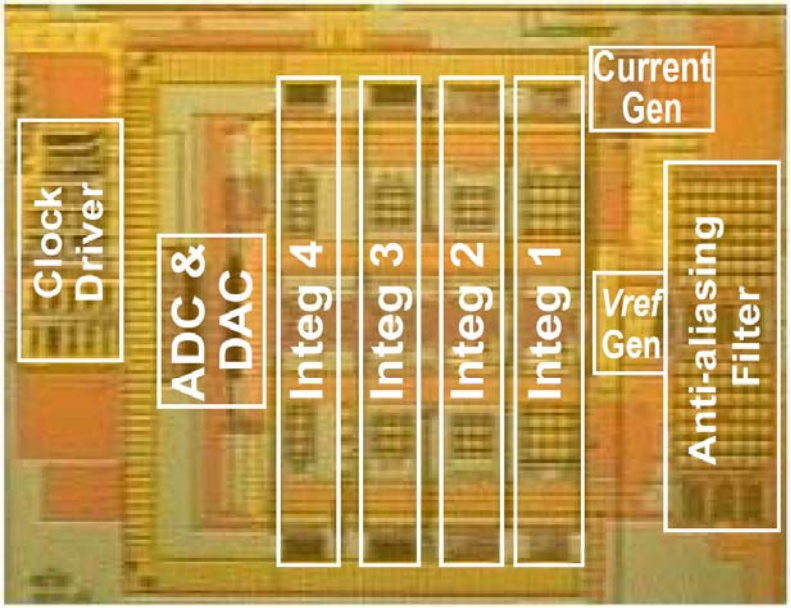
- Static input scheme (no caps)
  - Reduces capacitive load to 4th integrator
  - Saves silicon area
- Extra differential pair in comparators

DT-ΣΔMs: Case study - Layout & Prototyping

CMOS 0.25μm

2.78mm² w/o pads

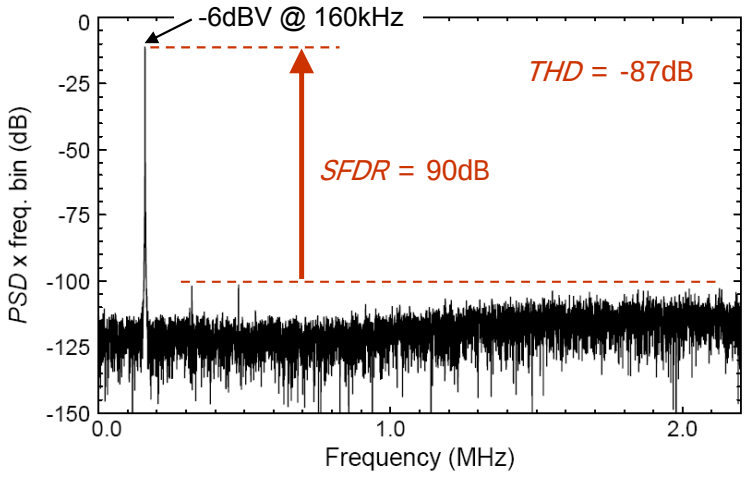
44-pin plastic QFP

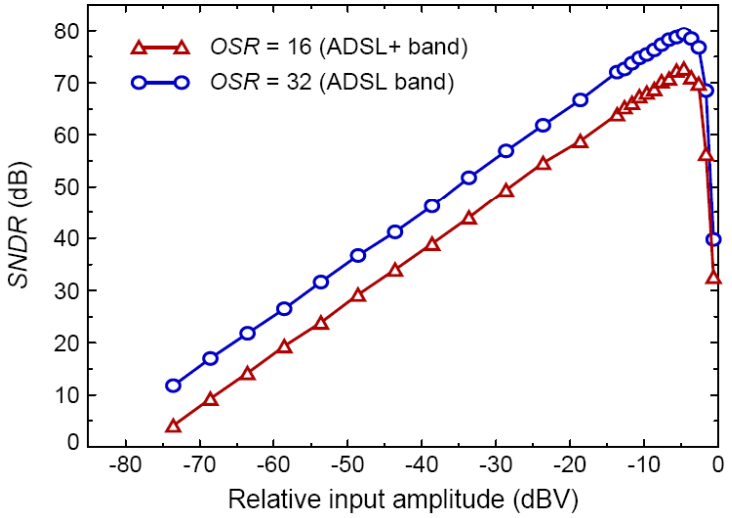


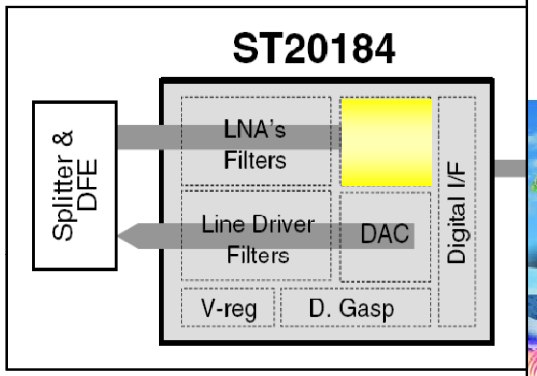
4-layer PCB

- Dedicated analog, mixed, and digital supplies
- Guard rings with dedicated pad/pin
- Increased distance among analog and digital blocks
- Layout symmetry and common-centroid techniques
- Shielded bus for distributing the clock signals
- Extensive on-chip decoupling
- Pad ring divided blocking cells
- Multiple bonding techniques

DT-ΣΔMs: Case study - Experimental results







Part of a commercial modem

In mass production (STMicroelectronics)

DT-ΣΔMs: References

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More details on errors and case study …

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