CMOS Sigma-Delta Converters - From Basics to State-of-the-Art

Circuits and Errors

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Ideal In-Band Error Power:

\[ P_Q = \frac{1}{12} \left( \frac{\Delta}{2^B - 1} \right)^2 \frac{\pi^{2L}}{(2L+1)\text{OSR}^{2L+1}} \]

Actual In-Band Error Power:

\[ P_T = P_Q + \Delta P_Q + P_{\text{TH}} + P_J + P_{\text{HD}} + \ldots \]

- Finite Amplifier Gain Non-Linearities
- Thermal Noise
- Comparator Hysteresis
- Capacitor Mismatch
- Settling Errors
- Clock Jitter
- DAC Non-linearity

... among others ...
**DT-ΣΔMs: Overview of non-idealities**

Depending on the building-block:

- **Amplifiers:**
  - Output swing
  - DC gain
  - Dynamic limitations (GB, SR)
  - Thermal and 1/f noise
  - Gain non-linearity

- **Switches:**
  - Finite on-resistance
  - Thermal noise
  - Charge injection
  - Clock feedthrough
  - Non-linearity

- **Capacitors:**
  - Mismatch
  - Non-linearity

- **Comparators:**
  - Hysteresis
  - Offset

- **References:**
  - Thermal and 1/f noise
  - Output impedance

- **Multi-bit ADCs & DACs:**
  - Gain error
  - Offset error
  - Non-linearity

**Clock:**
- Jitter

Fully-diff SC schematic of a 2nd-order ΣΔM

[Diagram of a 2nd-order ΔΣM circuit with labeled components and waveforms showing clock phases and signal flow]
DT-$\Sigma$Ms: Overview of non-idealities

- Depending on their effect:

**ERRORS DEGRADING NTF**
- AMPLIFIER DC GAIN
- CAPACITOR MISMATCH
- INTEGRATOR SETTLING
  - Amplifier GB
  - Amplifier SR
  - Switch $R_{on}$

Impact depends on topology

- SINGLE-LOOP $\Sigma$Ms
  - Low sensitivity

- CASCADE $\Sigma$Ms
  - Noise leakages
    - Imperfect cancellation of low-order quantization errors

![Diagram of DT-$\Sigma$Ms]
Depending on their effect:

**ERRORS DEGRADING NTF**
- **AMPLIFIER DC GAIN**
- **CAPACITOR MISMATCH**
- **INTEGRATOR SETTLING**
  - Amplifier GB
  - Amplifier SR
  - Switch $R_{on}$

**MODELED AS ADDITIVE ERRORS**
- **CIRCUIT NOISE**
  - Thermal noise (switches, opamps, refs)
  - 1/f noise (opamps, refs)
- **CLOCK JITTER**
- **DISTORTION**
  - Non-linear amplifier gain
  - Non-linear capacitors
  - Non-linear settling
  - Non-linear switches

- **SINGLE-LOOP $\Sigma\Delta$Ms**
  - Low sensitivity

- **CASCADE $\Sigma\Delta$Ms**
  - Noise leakages
    - Imperfect cancellation of low-order quantization errors

Impact depends on topology

Front-end dominates

Similar impact on different topologies
Effect of amplifier gain on the integrator transfer function:

**Ideal SC integrator**

\[ g = \frac{C_1}{C_2} \]

\[ v_{o, n} = v_{o, n-1} + g \cdot v_{i, n-1} \]

\[ H(z) = g \frac{z^{-1}}{1 - z^{-1}} \]

**SC integrator considering amplifier finite gain**

\[ v_{o, n} = \frac{1}{1 + \frac{1}{A_{DC}} \cdot A_{DC} \cdot (1 + g)} \cdot v_{o, n-1} + g \cdot v_{i, n-1} \]

\[ H(z) = g \frac{z^{-1}}{1 - \frac{g}{A_{DC}} \cdot z^{-1} \left(1 - \frac{g}{A_{DC}}\right)} = g \frac{z^{-1}}{1 - \frac{g}{A_{DC}} \cdot \left(1 - g\mu\right)} \]

\[ \mu = 1/A_{DC} \]

Shift of the pole from DC \((z = 1)\)
**Effect on single-loop ΣΔMs:**

- Ideally:
  \[ H(z) = \frac{z^{-1}}{1 - z^{-1}} \]

  \[ Y(z) = z^{-2}X(z) + (1 - z^{-1})^2E(z) \]

- In practice:
  \[ H(z) = \frac{z^{-1}}{1 - z^{-1}(1 - \mu)} \]

  \[ NTF(z) = [1 - z^{-1}(1 - \mu)]^2 \]
  \[ = (1 - z^{-1})^2 + 2\mu z^{-1}(1 - z^{-1}) + \mu^2 z^{-2} \]

  \[ P_Q(\mu) \approx \Delta^2 \left( \frac{\pi^4}{12 \times 5OSR^3} + \frac{2\mu^2}{3OSR^3} + \frac{\mu^4}{OSR} \right) \]

\[ \Delta P_Q \approx \frac{\Delta^2}{12 (2L - 1) OSR^{2L - 1}} \times \frac{L\mu^2 \pi^{2L-2}}{OSR} \]

Quite insensitive to leakages \((\mu^2, L-1\text{ shaping})\)
**DT-$\Sigma$Ms: Integrator leakage**

- **Effect on cascade $\Sigma$Ms:** 2-1-1 $\Sigma$M

- **Analog**
  
<table>
<thead>
<tr>
<th>$g_2'$</th>
<th>$g_1$</th>
<th>$d_0$</th>
<th>$H_1(z) = 1 - z^{-1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_4'$</td>
<td>$g_3$</td>
<td>$d_1$</td>
<td>$H_2(z) = (1 - z^{-1})^2$</td>
</tr>
<tr>
<td>$d_2$</td>
<td>0</td>
<td>$H_3(z) = 1$</td>
<td></td>
</tr>
<tr>
<td>$d_3$</td>
<td>$g_4'$</td>
<td>$g_1$</td>
<td>$H_4(z) = (1 - z^{-1})^3$</td>
</tr>
</tbody>
</table>

- **Mismatch between analog and digital filtering**

- **Ideally:**
  
  \[
  Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) + NTF_3(z)E_3(z)
  \]

- **In practice:**
  
  \[
  H(z) = \frac{z^{-1}}{1 - z^{-8}(1 - \mu)}
  \]

- **Low-order leakages**
  
  \[
  P_Q(\mu) \approx \frac{\Delta_l^2}{12d_1^2}\left(\frac{\mu^2\pi^4}{3OSR^3}\right) + \frac{\Delta_l^2}{12d_1^2}\left(\frac{\mu^2\pi^4}{5OSR^3}\right) + \frac{\Delta_l^2}{12d_1^2}\left(\frac{\mu^2\pi^6}{7OSR^7}\right) + \frac{\pi^8}{9OSR^9}
  \]

- **Cancellation Logic**
Comparison of integrator leakage effect on 4th-order $\Sigma\Delta$Ms

- Sensitivity to int. leakages of cascades increases with OSR and $L$
- 1st-stage leakages dominate ($L_1$-1 shaping)
DT-ΣΔMs: Capacitor mismatch

- **Circuit primitive:**
  - \[ \text{Capacitor mismatch} \]
  - Ms: Ms
- **Physical implementations:**
  - MOS cap
  - Density
  - Linearity
  - Temperature
  - Parasitics
  - Matching

"Analog" CMOS

- Poly-poly
- Density
- Linearity
- Temperature
- Parasitics
- Matching

"Digital" CMOS

- Metal-metal
- Density
- Linearity
- Temperature
- Parasitics
- Matching

"Mixed" CMOS

- M-i-M
- Density
- Linearity
- Temperature
- Parasitics
- Matching
Local and global errors in:

- Area
- Capacitance per Unit Area

\[ C = C_{oxc} \cdot (W \cdot L) \]

Actual ≠ Ideal

\[ C_{1} = nC_{u} \]
\[ C_{2} = mC_{u} \]

\[ g = \frac{C_{1}}{C_{2}} = \frac{nC_{u}}{mC_{u}} \]

\[ \sigma_{g} = \sqrt{\frac{1}{n} + \frac{1}{m}} \cdot \sigma_{C_{u}} \]

\[ \sigma_{C} \approx 0.05\% - 0.1\% \text{ using good quality caps and adequate layout strategies} \]
**Effect on single-loop \( \Sigma\Delta M \):**

- ** Ideally:**
  
  \[
  g_1 = g_1',
  \quad g_2' = 2g_1'g_2
  \]

  \[
  Y(z) = z^{-2}X(z) + (1 - z^{-1})^2E(z)
  \]

- ** In practice:**
  
  \[
  g^*_i = g_i(1 \pm \varepsilon_{g_i})
  \]

  \[
  \varepsilon_{g_i} = 3\frac{\sigma_{g_i}}{g_i} = 3\frac{1}{m_i} + \frac{1}{n_i}\sigma_c
  \]

  \[
  STF(z) \approx (1 - |\varepsilon_{g_1'} - \varepsilon_{g_1}|)z^{-2} \approx z^{-2}
  \]

  \[
  NTF(z) \approx (1 + \varepsilon_{g_2})(1 - z^{-1})^2, \quad \varepsilon_{g_2} = \varepsilon_{g_2} + \varepsilon_{g_1'}
  \]

Slight increase of error, but shaping is preserved

\[
P_Q(\varepsilon_g) \equiv \frac{\Delta^2}{12} \left[ \frac{(1 + \varepsilon_g)^2}{5OSR^5} \right]
\]
Effect on cascade $\Sigma\Delta$Ms:

- Ideally:
  \[ Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) + NTF_3(z)E_3(z) \]
  \[
  \begin{align*}
  STF(z) &= z^{-4} \\
  NTF_1(z) &= 0 \\
  NTF_2(z) &= 0 \\
  NTF_3(z) &= d_2(1 - z^{-1})^4
  \end{align*}
  \]

- In practice:
  \[ g_i^* = g_i(1 \pm \epsilon_i) \]

Mismatch between analog and digital coeffs

Mismatch between analog and digital coeffs

Low-order leakages

(L₁, L₂, ...)

Analog

<table>
<thead>
<tr>
<th>Digital</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_2' = 2g_1g_2$</td>
</tr>
<tr>
<td>$g_4' = g_3g_4$</td>
</tr>
<tr>
<td>$d_2 = 0$</td>
</tr>
<tr>
<td>$d_3 = \frac{g_4}{g_1g_2g_3g_4}$</td>
</tr>
</tbody>
</table>
Effect on cascade $\Sigma\Delta$Ms:

- $\sigma_c = 0.5\%$
- $\sigma_c = 0.1\%$

$2\text{-}1\text{-}1$ $\Sigma\Delta$M

(OSR = 32)
Effect on cascade $\Sigma \Delta$Ms:

Required $\sigma_C$ for 1-bit loss in DR

Sensitivity to mismatch rapidly increases with:
- Oversampling ratio (OSR)
- Cascade order ($L$)
1st-stage leakages dominate ($L_1$ shaping)
**DT-ΣΔMs: Integrator incomplete settling**

- The relationship between opamp input and output is non-linear and dynamic

- Integrator temporal evolution
  - Error due to amplifier finite bandwidth
  - Slew-rate limitation

- Modulator output spectrum
  - Increase on the noise floor
  - Harmonic distortion due to slewing

- SNDR degradation
Integrator temporal evolution: [Rio00]

- Both integration and sampling dynamics considered
- 1 pole model + SR limitation in amplifiers
- All parasitic caps taken into account

Amplifier Model

\[
\begin{align*}
V_+ & \downarrow \quad I_o \quad g_m(V_+ - V_-) \quad g_{out} \quad C_{out} \\
V_- & \downarrow \quad -I_o \\
\end{align*}
\]

Single-pole non-linear Dynamic
Integrator temporal evolution: [Rio00]

\[ C_{eq} = C_1 + C_p + C_f \left( 1 + \frac{C_1 + C_2}{C_0} \right) \]

- Integration-Phase:
  - finite opamp dynamic
  - linear operation or slew

\[
\begin{align*}
\left. v_a(t) \right|_{T_g/2} &= \frac{t_G}{g_m} \text{sgn}(v_{aH}) \exp \left( \frac{g_m T_g}{C_{eq}} \right) \\
\left. v_{aL} \right|_{T_g/2} &= \frac{I_e}{C_{eq}} \text{sgn}(v_{aL}) \exp \left( \frac{g_m T_g}{C_{eq}} \right) \\
\left. v_{oL} \right|_{T_g/2} &= \frac{1}{C_0} \left( v_m \pm V_{ref} \right) \left( 1 + \frac{C_0 + C_i}{C_0} \right) \frac{T_g}{2} \\
\end{align*}
\]

**Partial Slew**

**Linear**

**Full Slew**

\[ v_o \]

\[ v_a \]

\[ t (\text{ns}) \]

\[ 0 \]

\[ 15 \]

\[ 0.4 \]

\[ 0.2 \]

\[ -0.2 \]
Integrator temporal evolution: [Rio00]

\[ C_{eqI} = C_i + C_p + C_i \left( 1 + \frac{C_i + C_o}{C_c} \right) \]

\[ C_{eqS} = C_p + (C_i + C_{i1} + C_{i2})(1 + \frac{C_o}{C_c}) \]

Integration-Phase:
- finite opamp dynamic
- Linear operation or slew

\[ v_a(T_g) = \frac{i_o}{g_m} \exp \left( \frac{g_m}{C_{eqI}} \frac{T_g}{2} \right) \]

\[ v_a(T_g) = \frac{i_o}{g_m} \exp \left( \frac{g_m}{C_{eqI}} \frac{T_g}{2} \right) \]

Sampling-Phase:
- finite opamp dynamic
- Linear operation or slew

\[ v_a(T_g) = \frac{i_o}{g_m} \exp \left( \frac{g_m}{C_{eqS}} \frac{T_g}{2} \right) \]

\[ v_a(T_g) = \frac{i_o}{g_m} \exp \left( \frac{g_m}{C_{eqS}} \frac{T_g}{2} \right) \]
Integrator temporal evolution: [Rio00]

<table>
<thead>
<tr>
<th>INTEGRATION</th>
<th>SAMPLING</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LINEAR</td>
</tr>
<tr>
<td>2</td>
<td>PARTIAL SLEW</td>
</tr>
<tr>
<td>3</td>
<td>SLEW</td>
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<tr>
<td>7</td>
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</tr>
<tr>
<td>8</td>
<td>PARTIAL SLEW</td>
</tr>
<tr>
<td>9</td>
<td>SLEW</td>
</tr>
</tbody>
</table>

GB AND SR LIMITATIONS DURING BOTH CLOCK-PHASES

\[
v_{o,n} \approx v_{o,n-1} - \frac{C_i}{C_o} (V_{i1} - V_{i2}) - \ldots - \frac{C_i}{C_o} (V_{i2} - V_{i1}) + \Theta(\tau_i) + \Theta(\tau_2)
\]

Traditionally not taken into account

Traditionally not taken into account
**DT-ΣΔMs: Integrator incomplete settling**

- **Effect of the amplifier GB:**
  - If only amplifier GB is considered (assuming no SR limitation)
    - Can be viewed as a systematic error in the integrator weight
    - Effect on ΣΔMs similar to a mismatch between analog and digital coeffs
    - It causes low-order noise leakages in cascade ΣΔMs

\[
\begin{align*}
GB_f &= \frac{g_m}{C_{eq,i}} \\
GB_s &= \frac{g_m}{C_{eq,s}}
\end{align*}
\]

\[
v_o(z) = \frac{C_s}{C_f} (1 - \varepsilon_{st}) \frac{z^{-1}v_{in}(z) - z^{-1/2}v_{fb}(z)}{1 - z^{-1}}
\]

\[
\varepsilon_{st} - \theta_i \left[ \exp\left(-GB_f \frac{T_s}{2}\right) \right] + \theta_s \left[ \exp\left(-GB_s \frac{T_s}{2}\right) \right] + \theta_i \cdot \theta_s
\]
**DT-ΣΔMs: Integrator incomplete settling**

- Additional effect of the amplifier SR (+ GB):
  - “Dominant” linear dynamics are not mandatory in order to fulfill specs
  - SR can be traded for GB
  - It can be used to optimize the power consumption of amplifiers

Non-linear dynamics cause distortion!
SR at the front-end integ must be carefully tackled
**DT-ΣΔMs: Integrator incomplete settling**

- **Additional effect of the switches Ron (+ GB + SR):**

  - **Input is sampled with an error**
    
    \[ \epsilon_{on,s} = \exp \left( \frac{1}{2R_{on}C_S} T_d \right) \]

  - **Linear dynamics are slowed down**
    
    \[ GB_{t,on} = \frac{GB_t}{1 + GB_t \cdot 2R_{on}C_S} \]

    \[ GB_{s,on} = \frac{GB_s}{1 + GB_s \cdot 2R_{on}C_n} \]

  - **Slew time shortens**
**DT-ΣΔMs: Circuit noise**

Main noise sources in SC integrators:
- Switches → Thermal noise
- Amplifiers → Thermal and flicker noise
- References → Thermal and flicker noise

**Sampling:**

\[ T \] \[ 2R_{on} \] \[ C_s \]

\[ V_s \]

**Integration:**

\[ 2R_{on} \] \[ C_s \]

\[ C_p \]

\[ V_{op} \]

\[ g_m V \]

\[ C_L \]

- Noise contribution of the switches (input-referred):

Switches for sampling

\[ S_S = 2kT \cdot 2R_{on} \]

\[ H_{S_{\theta_1}}(s) = \frac{1}{1 + s \cdot 2R_{on}C_s} \]

\[ BW_{m,S_{\theta_1}} = \int_0^\infty |H_{S_{\theta_1}}(f)|^2 df = \frac{1}{4 \cdot 2R_{on}C_s} \]

\[ S_{in,S_{\theta_1}}(f) = \frac{2BW_{m,S_{\theta_1}}}{f_s} \cdot S_S = \frac{kT}{C_s f_s} \]

Aliased component [Fisc82]

\[ C_s = 0.66 \text{pF} \]

\[ f_s = 70 \text{MHz} \]
Main noise sources in SC integrators:
- Switches $\rightarrow$ Thermal noise
- Amplifiers $\rightarrow$ Thermal and flicker noise
- References $\rightarrow$ Thermal and flicker noise

Noise contribution of the switches (input-referred):

Switches for sampling: $S_S = 2kT \cdot 2R_{on}$

$H_{S_{\phi_1}}(s) = \frac{1}{1 + s \cdot 2R_{on}C_S}$

$BW_{n, S_{\phi_1}} = \int_0^{\infty} |H_{S_{\phi_1}}(f)|^2 df = \frac{1}{4 \cdot 2R_{on}C_S}$

$S_{in,S_{\phi_1}}(f) = \frac{2BW_{n, S_{\phi_1}}}{f_s} \cdot S_S \equiv \frac{kT}{C_S f_s}$

Switches for integration:

$H_{S_{\phi_2}}(s) = \frac{1 + s / z_1}{(1 + s / p_1)(1 + s / p_2)}$

$z_1 = \frac{g_m}{C} \quad p_1 = \frac{g_m}{C_{eq,i}} \quad p_2 = \frac{C_{eq,i}}{C} \cdot \frac{1}{2R_{on}C_S}$

$BW_{n, S_{\phi_2}} = \int_0^{\infty} |H_{S_{\phi_2}}(f)|^2 df \equiv \frac{p_2}{4} = \frac{1}{4 \cdot 2R_{on}C_S}$

$S_{in,S_{\phi_2}}(f) = \frac{2BW_{n, S_{\phi_2}}}{f_s} \cdot S_S \equiv \frac{kT}{C_S f_s}$
Noise contribution of the amplifier (input-referred):

**Thermal + Flicker**

- **Thermal component**

  \[ \begin{align*}
  H_{op}(s) &= \frac{1}{(1+s/p_1)(1+s/p_2)} \\
  BW_{n,op} &= \int_{0}^{\infty} |H_{op}(f)|^2 df = \frac{p_1}{4} = \frac{g_m}{4C_{eq,i}} \\
  S_{in,op}^f(f) &= \frac{2BW_{n,op}}{f_s} \cdot S_{op}^f = \frac{GB_i}{2f_s} \cdot S_{op}^f \\
  \end{align*} \]

- **Flicker component**

  - Low-pass filtered version at the integ input:
    \[ S_{op}^f(f)|H_{op}(f)|^2 \equiv S_{op}^f f_{cr,op}/|f| \]
  - Folded tails are “submerged” into the aliased thermal noise

**Similar treatment for the references**
Total noise PSD for the front-end integ:

\[ S_{\text{eq,in}}(f) = \frac{2kT}{C_S f_s} + S_{\text{op}}^i \left( \frac{GB_i}{2f_s} + \frac{f_{\text{cr,op}}}{f_s} \right) + S_{\text{ref}}^i \left( \frac{GB_{\text{ref}}}{2f_s} + \frac{f_{\text{cr,ref}}}{f_s} \right) \]

Switches:
- kT/C is the ultimate limitation on the converter resolution
- It can only be decreased by increasing Cs and/or fs (it does not depend on Ron!)
- x2 in fully-diff implementations (3-dB increase, but signal power is 6dB larger!)

Amplifiers & References:
- GBs should be as low as settling errors allow (reduces folding!)
- 1/f contributions decrease with the corner frequency
- Adequate techniques can be applied in low-freq apps: CDS, chopper, ... [Enz96]

In-band error power due to circuit noise in the ΣΔM

\[ P_{CN, \text{in}} = \left[ \frac{2kT}{C_S} + S_{\text{op}}^i \frac{GB_i}{2} + S_{\text{ref}}^i \frac{GB_{\text{ref}}}{2} \right] \frac{1}{\text{OSR}} + 2 \ln \left( \frac{f_d}{f_o} \right) \left( S_{\text{op,cr,op}}^i + S_{\text{ref,cr,ref}}^i \right) \]
Effect of noise leakages and thermal noise on a 2-1 cascade

- 3rd-order shaping
- 2nd-order shaping
- w/ Thermal noise
- w/ Integ leakage
- Ideal
- no shaping
Effect of 1/f and thermal noise on the spectra of a 4th-order ΣΔM

(silicon results for several fs)

Be careful with Flicker models for transistors!
Front-end amplifier needed redesign!
Sampling time uncertainty [Boser88]:

\[ S_j = \frac{A_x^2 (2\pi f_x \sigma_J)^2}{2 f_s} \]

→ If jitter is modeled as random:

\[ P_j = \frac{A_x^2 (2\pi f_x \sigma_J)^2}{2 \text{OSR}} \]

Error is larger, the larger input freq (wideband apps!)
**DT-ΣΔMs:** Non-linearity of capacitors

- In an ideal capacitor: \( dq = C dv \)
- In practice: \( dq = C(v)dv \), with \( C \) being voltage-dependent

\[
C(v) = C(1 + a_1 v + a_2 v^2 + \ldots)
\]

- Considering the effect of the sampling cap only [Bran97]:

\[
v_{o, n} = v_{o, n-1} + g_1 v_{in, n-1} \left( 1 + \frac{a_1}{2} v_{in, n-1} + \frac{a_2}{3} v_{in, n-1}^2 \right)
\]

\[
A_2 = \frac{1}{2} \left( \frac{a_1}{2} A_x^2 \right) \implies HD_2 = 20 \log_{10} \left( \frac{a_1}{4} A_x \right)
\]

\[
A_3 = \frac{1}{4} \left( \frac{a_2}{3} A_x^3 \right) \implies HD_3 = 20 \log_{10} \left( \frac{a_2}{12} A_x^2 \right)
\]

- Even-order distortion cancels w/ fully-diff
- Non-linearity of sampling cap dominates
- Valid for weak non-linearities (MOS caps are very non-linear!)

\[a_1 = 500 \text{ppm/V}, \ a_2 = 500 \text{ppm/V}^2\]
Actual amplifier gain depends on output voltage:

\[ A_{DC}(v_o) = A_{DC}(1 + \gamma_1 v_o + \gamma_2 v_o^2 + \ldots) \]

- Increasing \( A_{DC} \) helps a lot!
- \( A_{DC} \) at the front-end larger than noise leakages require
− SR can trade for GB in the integrator settling, but non-linear dynamics cause distortion:

SR at the front-end larger than settling requires
Switches exhibit a finite $R_{ON}$ which is also non-linear:

Non-linear sampling [Geer02]:

- Distortion is dynamic (increases with input freq!)
- Front-end switch dominates
- $R_{ON}$ at the front-end smaller than settling requires
- Very important in low-voltage!
**DT-ΣΔMs: Comparators and multi-bit quantizers**

- **Single-bit ΣΔMs:**
  - Comparator:
    - Offset → Attenuated by the integrator DC gain
    - Hysteresis → Shaped similarly to quantization error [Boser88]
    - Offset Δ → Shaped similarly to quantization error [Boser88]
    - Offset error $P_h = 4h^2 \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}$
  - 1-bit DAC → Inherently linear

- **Multi-bit ΣΔMs:**
  - Multi-bit ADC → Errors attenuated/shaped
  - Multi-bit DAC → Non-linearity directly added to the input!
  - [Mede99]: $\sigma_D^2 = \frac{1}{2} \left( \frac{\Delta}{2^b - 1} \right)^2 INL_{LSB}^2$

**Effect of DAC errors on a 2nd-order 3-bit ΣΔM**

- DEM techniques
- Dual quantization
A 2.5-V Cascade SDM in CMOS 0.25um for ADSL/ADSL+

2-1-1 w/ dual quantization

- Two different amplifiers: 2-stage OA in the 1st stage, and 1-stage OA in 2nd and 3rd stages.
- Standard CMOS switches (no clock-boosting).
- Only 2-branch integrators and 2x16 unit capacitors (MiM).
- Comparators: regenerative latch + preamplification stage.
- 3-bit quantizer in the last stage:
  - Resistive-ladder DAC (no calibration).
  - Flash ADC: Static differential input stage + latched comparators.
- Power-down control.
### Blocks Specs

#### EQUATION DATABASE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical</th>
<th>Worst Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantization noise</td>
<td>-88.1dB</td>
<td>-86.2dB</td>
</tr>
<tr>
<td>DC gain-leakage</td>
<td>-90.3dB</td>
<td></td>
</tr>
<tr>
<td>Cap. mismatch leakage</td>
<td>-95.4dB</td>
<td>-89.4dB</td>
</tr>
<tr>
<td>DAC error</td>
<td>-96.4dB</td>
<td></td>
</tr>
<tr>
<td>Thermal noise</td>
<td>-84.8dB</td>
<td>-82.2dB</td>
</tr>
<tr>
<td>kT/C noise</td>
<td>-88.1dB</td>
<td>-86.0dB</td>
</tr>
<tr>
<td>Amplifier noise</td>
<td>-87.5dB</td>
<td>-84.5dB</td>
</tr>
<tr>
<td>Clock jitter</td>
<td>-90.1dB</td>
<td></td>
</tr>
<tr>
<td>In-band error power</td>
<td>-82.3dB</td>
<td>-80.3dB</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>82.8dB</td>
<td>80.8dB</td>
</tr>
<tr>
<td>(13.5bit)</td>
<td></td>
<td>(13.1bit)</td>
</tr>
</tbody>
</table>

#### Corner analysis:
- Fast and slow devices models
- Temperature range: [-40°C, +110°C]
- ±5% variation in the 2.5-V supply

### MODULATOR

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology</td>
<td>2-1-1(3b)</td>
</tr>
<tr>
<td>Oversampling ratio</td>
<td>16</td>
</tr>
<tr>
<td>Reference voltage</td>
<td>1.5V</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>70.4MHz</td>
</tr>
<tr>
<td>Clock jitter</td>
<td>15ps (0.1%)</td>
</tr>
</tbody>
</table>

### FRONT-END INTEGRATOR

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling capacitor</td>
<td>0.66pF</td>
</tr>
<tr>
<td>Cap. sigma (MIM, 1pF)</td>
<td>0.05%</td>
</tr>
<tr>
<td>Cap. tolerance</td>
<td>±20%</td>
</tr>
<tr>
<td>Bottom parasitic cap.</td>
<td>1%</td>
</tr>
<tr>
<td>Switch on-resistance</td>
<td>1500Ω</td>
</tr>
</tbody>
</table>

### AMPLIFIER

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>3000 (70dB)</td>
</tr>
<tr>
<td>GB (1.5pF)</td>
<td>265MHz</td>
</tr>
<tr>
<td>Slew rate (1.5pF)</td>
<td>800V/µs</td>
</tr>
<tr>
<td>Output swing</td>
<td>±1.8V</td>
</tr>
<tr>
<td>Input equivalent noise</td>
<td>6nV/sqrt(Hz)</td>
</tr>
</tbody>
</table>

### COMPARATORS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hysteresis</td>
<td>20mV</td>
</tr>
<tr>
<td>Offset</td>
<td>±10mV</td>
</tr>
<tr>
<td>Resolution time</td>
<td>3ns</td>
</tr>
</tbody>
</table>

### 3-bit QUANTIZER

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC /NL</td>
<td>0.5%FS</td>
</tr>
</tbody>
</table>
**DT-ΣΔMs: Case study**

\[
P_{CN} = P_{\frac{kT}{C}} + P_{op} = \frac{4kT}{C_S} \frac{1}{OSR} + \frac{2\pi \cdot GB_{eff} \cdot S_{op}}{2OSR}
\]

\[
GB_{eff} \equiv \frac{GB}{1 + GB/f_{on}} = \frac{GB}{1 + GB \cdot 2\pi \cdot 2R_{on}C_S}
\]

<table>
<thead>
<tr>
<th><strong>Quantization noise</strong></th>
<th><strong>Typical</strong></th>
<th><strong>Worst Case</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal</td>
<td>-88.1dB</td>
<td>-86.2dB</td>
</tr>
<tr>
<td>DC gain leakage</td>
<td>-99.8dB</td>
<td></td>
</tr>
<tr>
<td>Cap. mismatch leakage</td>
<td>-95.4dB</td>
<td>-89.4dB</td>
</tr>
<tr>
<td>((\sigma_C = 0.05%)</td>
<td>0.1%)</td>
<td></td>
</tr>
<tr>
<td>DAC error</td>
<td>-96.4dB</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Thermal noise</strong></th>
<th><strong>Typical</strong></th>
<th><strong>Worst Case</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>KT/C noise</td>
<td>-88.1dB</td>
<td>-86.0dB</td>
</tr>
<tr>
<td>Amplifier noise</td>
<td>-87.5dB</td>
<td>-84.5dB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Clock jitter</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>-90.1dB</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>I(n)-band error power</strong></th>
<th><strong>Typical</strong></th>
<th><strong>Worst Case</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>-82.3dB</td>
<td>-80.3dB</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Dynamic range</strong></th>
<th><strong>Typical</strong></th>
<th><strong>Worst Case</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>82.8dB (13.5bit)</td>
<td>80.8dB</td>
<td>(13.1bit)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>MODULATOR</strong></th>
<th><strong>Topologies</strong></th>
<th><strong>Oversampling ratio</strong></th>
<th><strong>Reference voltage</strong></th>
<th><strong>Clock frequency</strong></th>
<th><strong>Clock jitter</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2-1-1(3b)</td>
<td>16</td>
<td>1.5V</td>
<td>70.4MHz</td>
<td>15ps (0.1%)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>FRONT-END INTEGRATOR</strong></th>
<th><strong>Sampling capacitor</strong></th>
<th><strong>Cap. sigma (MIM, 1pF)</strong></th>
<th><strong>Cap. tolerance</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.66pF</td>
<td>0.05%</td>
<td>±20%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>AMPLIFIER</strong></th>
<th><strong>DC gain</strong></th>
<th><strong>GB (1.5pF)</strong></th>
<th><strong>Slew rate (1.5pF)</strong></th>
<th><strong>Output swing</strong></th>
<th><strong>Input equivalent noise</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3000 (70dB)</td>
<td>265MHz</td>
<td>800V/(\mu)s</td>
<td>±1.8V</td>
<td>±6nV/(\sqrt{\text{Hz}})</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>COMPARATORS</strong></th>
<th><strong>Hysteresis</strong></th>
<th><strong>Offset</strong></th>
<th><strong>Resolution time</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>20mV</td>
<td>±10mV</td>
<td>3ns</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>3-bit QUANTIZER</strong></th>
<th><strong>DAC /NL</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.5%FS</td>
</tr>
</tbody>
</table>
Integrator Dynamics

- $\text{GB} > 2.5f_s$ is ideally enough to limit settling errors (this architecture w/ $\text{OSR} = 16$).
- Switch on-resistance slows down the effective amplifier response:
  \[
  \text{GB}_{\text{eff}} = \frac{\text{GB}}{1 + \text{GB} / f_{\text{on}}} = \frac{\text{GB}}{1 + \text{GB} \cdot 2\pi \cdot 2R_{\text{on}}C_S}
  \]
  $R_{\text{on}} \sim 150\Omega$ requires just $\text{GB} > 3.2f_s$

**Standard switches**  
$\text{GB} = 265\text{MHz}$  
(no clock-boosting) (assuming that 85% of the clock cycle is useful)

- Slew rate must be large enough to let the linear dynamic to correctly settle.
  \[
  \text{SR/(V}_{\text{ref}} \cdot f_s) = 6.5 \quad \Rightarrow \quad \text{SR} = 800\text{V/\mu s}
  \]
- Partially slew-rate limited operation of the front-end integrator introduces distortion.
### Amplifiers Case Study

<table>
<thead>
<tr>
<th></th>
<th>INTEG. 1</th>
<th>INTEG. 2</th>
<th>INTEG. 3</th>
<th>INTEG. 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit capacitor</td>
<td>0.66pF</td>
<td>0.45pF</td>
<td></td>
<td>0.45pF</td>
</tr>
<tr>
<td>DC gain</td>
<td>3000 (70dB)</td>
<td>600 (56dB)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$GB$ (1.5pF)</td>
<td>265MHz</td>
<td>210MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew rate (1.5pF)</td>
<td>800V/µs</td>
<td>350V/µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output swing</td>
<td>±1.80V</td>
<td>±1.60V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input equivalent noise</td>
<td>6nV/sqrt(Hz)</td>
<td>50nV/sqrt(Hz)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **SC CMFB nets**
- **pMOS input scheme**
  - Cancelled body effect (substrate noise coupling)
  - Smaller 1/f noise

**OPA**

**OPB**
DT-SAMs: Case study - Amplifiers

### INTEG. 1 | INTEG. 2 | INTEG. 3 | INTEG. 4
--- | --- | --- | ---
Unit capacitor | 0.66pF | 0.45pF | 0.45pF
DC gain | 3000 (70dB) | 600 (56dB)
\(GB\) (1.5pF) | 265MHz | 210MHz
Slew rate (1.5pF) | 800V/\(\mu\)s | 350V/\(\mu\)s
Output swing | \(\pm 1.80V\) | \(\pm 1.60V\)
Input equivalent noise | 6nV/sqrt(Hz) | 50nV/sqrt(Hz)

- **SC CMFB nets**
- **pMOS input scheme**
  - Cancelled body effect (substrate noise coupling)
  - Smaller 1/f noise

**OPA** 2-stage amplifier

Telescopic 1st stage
2-path compensation

<table>
<thead>
<tr>
<th></th>
<th>Typical</th>
<th>Worst Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>78.6dB</td>
<td>73.5dB</td>
</tr>
<tr>
<td>(GB) (1.5pF)</td>
<td>446.8MHz</td>
<td>331.5MHz</td>
</tr>
<tr>
<td>(PM) (1.5pF)</td>
<td>64.0(^0)</td>
<td>57.9(^0)</td>
</tr>
<tr>
<td>(SR) (1.5pF)</td>
<td>1059V/(\mu)s</td>
<td>883V/(\mu)s</td>
</tr>
<tr>
<td>Output swing</td>
<td>(\pm 2.09V)</td>
<td>(\pm 1.86V)</td>
</tr>
<tr>
<td>Input eq. noise</td>
<td>5.1nV/sqrt(Hz)</td>
<td>5.5nV/sqrt(Hz)</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>126fF</td>
<td>129fF</td>
</tr>
<tr>
<td>Power consumption</td>
<td>17.2mW</td>
<td>19.4mW</td>
</tr>
</tbody>
</table>
### DT-ΣΔMs: Case study - Amplifiers

#### Amplifiers

<table>
<thead>
<tr>
<th>INTEG. 1</th>
<th>INTEG. 2</th>
<th>INTEG. 3</th>
<th>INTEG. 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit capacitor</td>
<td>0.66pF</td>
<td>0.45pF</td>
<td>0.45pF</td>
</tr>
<tr>
<td>DC gain</td>
<td>3000 (70dB)</td>
<td>600 (56dB)</td>
<td></td>
</tr>
<tr>
<td>GB (1.5pF)</td>
<td>265MHz</td>
<td>210MHz</td>
<td></td>
</tr>
<tr>
<td>Slew rate (1.5pF)</td>
<td>800V/μs</td>
<td>350V/μs</td>
<td></td>
</tr>
<tr>
<td>Output swing</td>
<td>±1.80V</td>
<td>±1.60V</td>
<td></td>
</tr>
<tr>
<td>Input equivalent noise</td>
<td>6nV/sqrt(Hz)</td>
<td>50nV/sqrt(Hz)</td>
<td></td>
</tr>
</tbody>
</table>

- SC CMFB nets
- pMOS input scheme
  - Cancelled body effect (substrate noise coupling)
  - Smaller 1/f noise

### OPB folded-cascode amplifier

<table>
<thead>
<tr>
<th>Typical</th>
<th>Worst Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>58.0dB</td>
</tr>
<tr>
<td>GB (1.5pF)</td>
<td>393.5MHz</td>
</tr>
<tr>
<td>PM (1.5pF)</td>
<td>70.3°</td>
</tr>
<tr>
<td>SR (1.5pF)</td>
<td>377V/μs</td>
</tr>
<tr>
<td>Output swing</td>
<td>±1.97V</td>
</tr>
<tr>
<td>Input eq. noise</td>
<td>4.1nV/sqrt(Hz)</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>300fF</td>
</tr>
<tr>
<td>Power consumption</td>
<td>6.6mW</td>
</tr>
</tbody>
</table>
**DT-ΣΔMs: Case study - Switch ON-Resistance**

- **Slow-down of the integrators dynamics**
- **Incomplete sampling** (RC time constant)
- **Dynamic distortion** (front-end integrator)

\[ R_{on} \approx 150 \Omega \]

**Standard CMOS switches**

- nMOS: 8.5/0.25
- pMOS: 36.5/0.25

**Graph:**
- Color-coded switches:
  - Blue: nMOS
  - Red: pMOS
  - Black: CMOS

**Switch on-resistance (Ω):**
- Voltage level (V): -1.25 to 1.25
- Sinewave and DMT regions highlighted.

**Legend:**
- No clock-boosting
- No low-Vt transistors
**Dynamic distortion**

evaluated through electrical simulation

- **Sinewave input**
  - THD < -96dB

- **DMT input**
  - MTPR < -81dB
CMOS tech with mixed-signal facilities

Thin oxide between metal 4 and metal 5

<table>
<thead>
<tr>
<th>Cap. matching</th>
<th>0.05% (1pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bottom plate parasitic</td>
<td>1%</td>
</tr>
<tr>
<td>Cap. spread</td>
<td>±20%</td>
</tr>
</tbody>
</table>

**Very good matching** (0.1% assumed for 6-σ design)
**Helps to limit the capacitive load to integrators**

**Integrators weights:**
- **Front-end integ, 0.66pF:** 27µm x 27µm
- **Remaining integs, 0.45pF:** 22µm x 22µm

**Also MiM caps in OPA, in the SC CMFB nets, and in the anti-aliasing filter**
**Comparator**

Pre-amp + Regenerative latch + SR latch

(Different supplies)

<table>
<thead>
<tr>
<th></th>
<th>Hysteresis</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>127.5μV</td>
<td>6.3mV</td>
</tr>
<tr>
<td>Resolution time, LH</td>
<td>3.9ns</td>
<td>Resolution time, HL</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>100fF</td>
<td>Power consumption</td>
</tr>
</tbody>
</table>

**Resistive-ladder DAC**

- 700-Ω ladder between references +2V/+0.5V (14x50Ω, 3.21mW)
- Unsalicided n+ poly used in resistors
- References obtained from the on-chip analog supply

**Flash ADC**

- Static input scheme (no caps)
  - Reduces capacitive load to 4th integrator
  - Saves silicon area
- Extra differential pair in comparators
CMOS 0.25\(\mu\)m

- 2.78mm\(^2\) w/o pads
- 44-pin plastic QFP

Dedicated analog, mixed, and digital supplies
- Guard rings with dedicated pad/pin
- Increased distance among analog and digital blocks
- Layout symmetry and common-centroid techniques

- Shielded bus for distributing the clock signals
- Extensive on-chip decoupling
- Pad ring divided blocking cells
- Multiple bonding techniques

4-layer PCB
**Experimental results**

**Case study**

- **SFDR** = 90dB
- **THD** = -87dB
- **PSD x freq. bin (dB)**
- **Relative input amplitude (dBV)**

---

**Part of a commercial modem**

**In mass production (STMicroelectronics)**
### References


More details on errors and case study ...