CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

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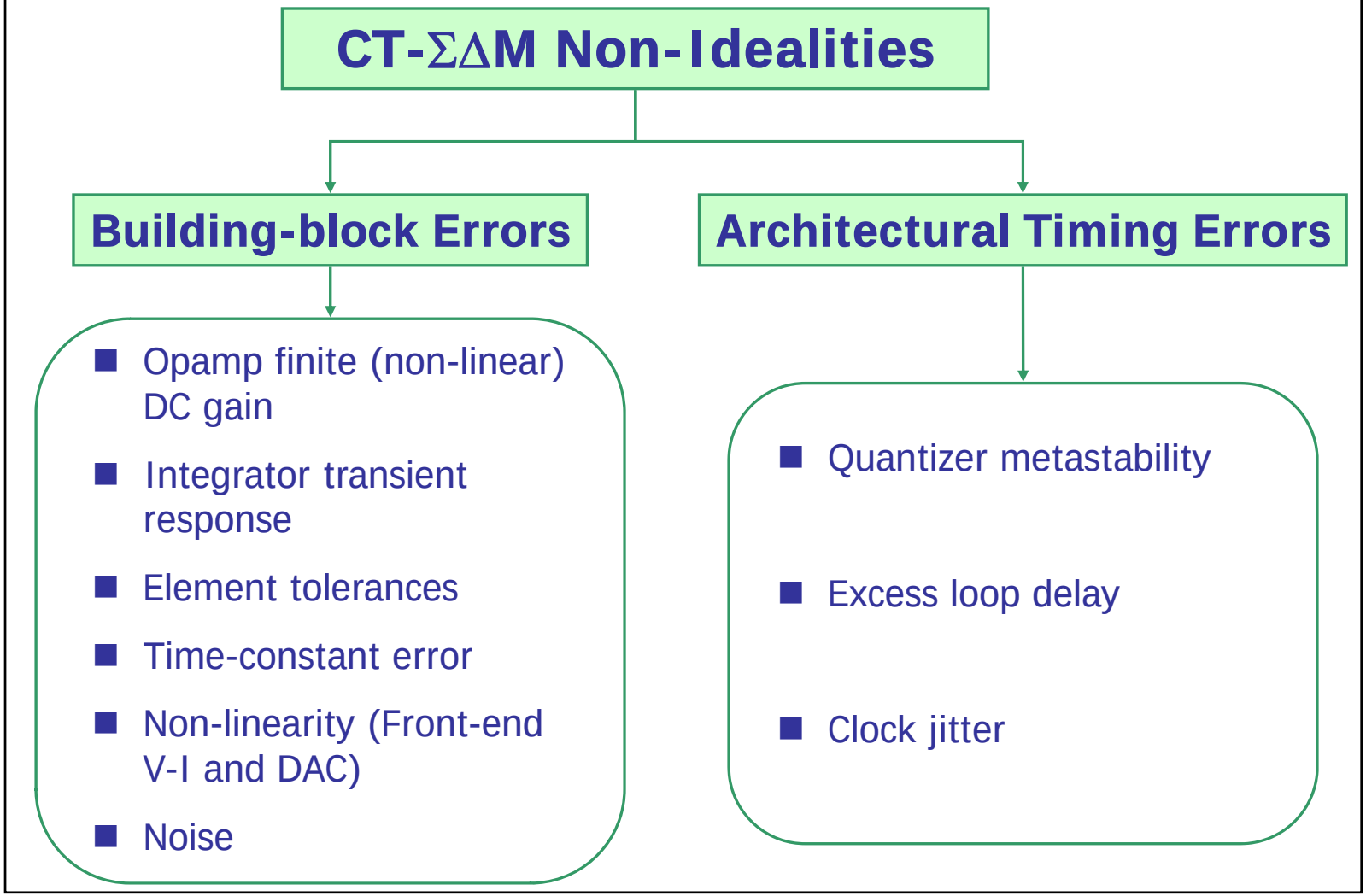
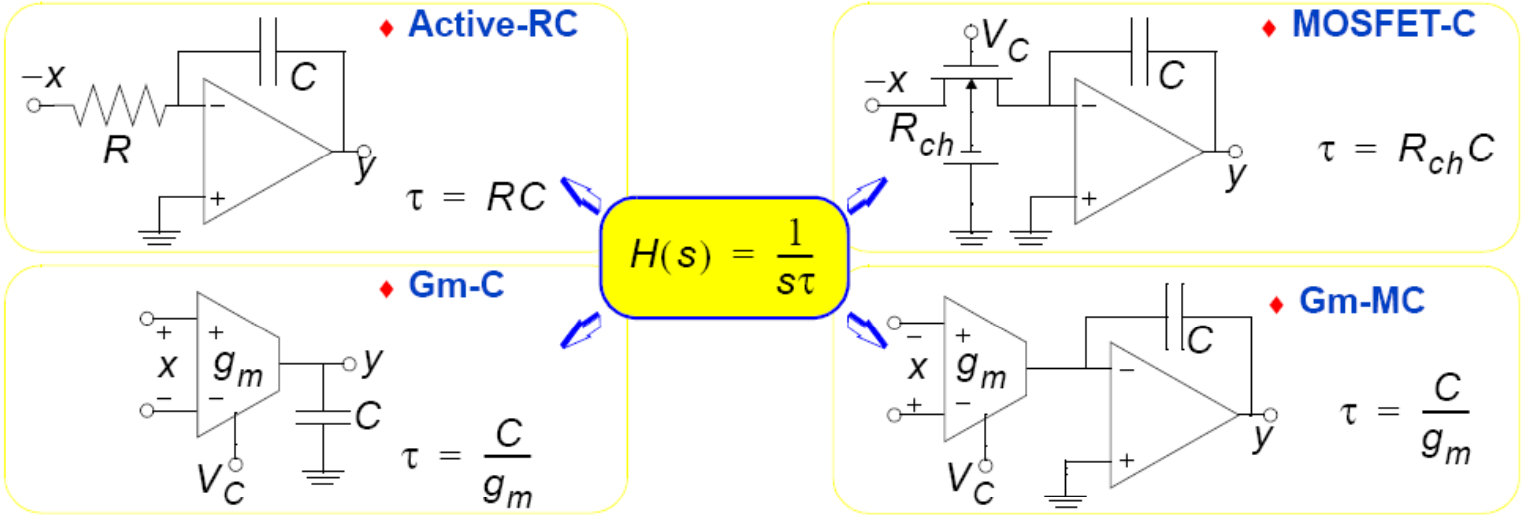
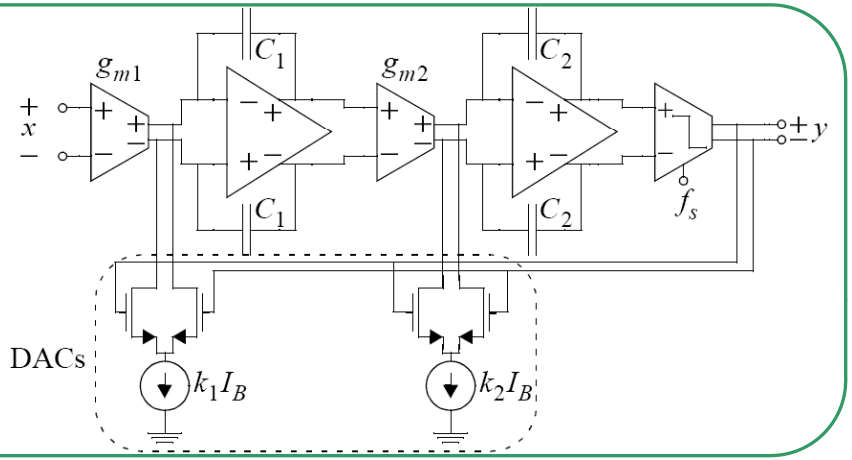
CT-ΣΔMs : Overview of CT-ΣΔM non-idealities



Basic building blocks – CT Integrators



- **A Gm-MC implementation**
  - 2nd-order single-loop ΣΔM
  - 1-bit switched-current DAC
  - 1-bit (latch) comparator



CT-ΣΔMs : Non-ideal integrator transfer function

❒ Integrator Transfer Function (ITF) degraded by circuit non-idealities

$$Y(s) = \frac{1}{\tau \cdot s} X(s) \quad \rightarrow \quad Y(s) = \left[\frac{1}{\varepsilon_\tau \cdot \tau \cdot s} T_{\varepsilon_H}(s)\right] X(s)$$

Ideal Transfer Characteristics

First-Order Actual Transfer Characteristics

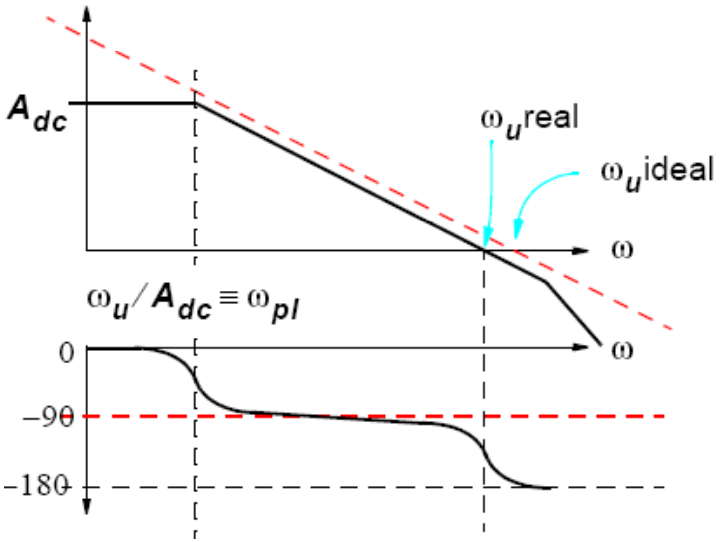
$$T_{\varepsilon_H}(s) = \frac{s}{s + \omega_{pl}}$$

$$T_{\varepsilon_H}(s) = \frac{s}{(s + \omega_{pl})(s + \omega_{ph})}$$

$$T_{\varepsilon_H}(s) = \frac{s(s + \omega_z)}{(s + \omega_{pl})(s + \omega_{ph})}$$

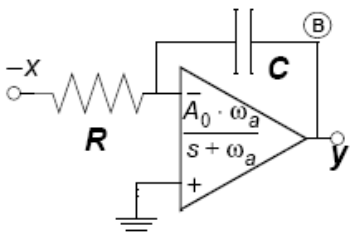
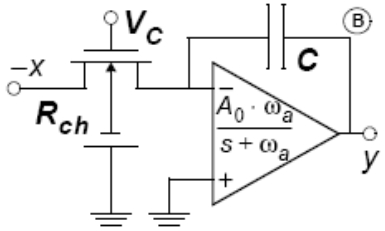
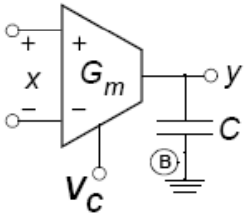
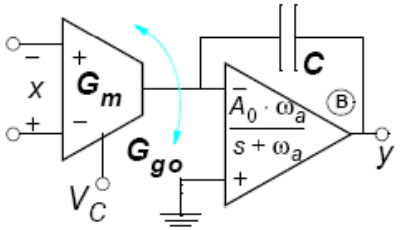
.....

- First-Order Non-Ideal Integrator Behaviours:
  - Deviations in the Unity Gain Frequency ε_τ
  - Low-Frequency Pole ω_{pl} . Due to Losses
    - Produce Finite DC Gain
    - Magnitude Errors for $\omega \gg \omega_{pl}$
    - Phase Errors for $\omega \gg \omega_{pl}$
  - High-Frequency Poles and Zeros $T_{\varepsilon_H}(s)$
    - Phase Errors for $\omega \ll \omega_{ph}, \omega_z, \ldots$



CT-ΣΔMs : Effect of finite DC gain error

Opamp finite DC gain (I)

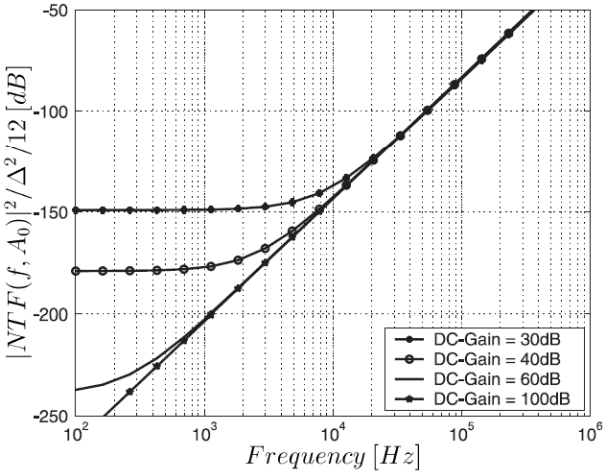
RC	MOSFET-C	Gm-C	Gm-MC
			
$\omega_{pl} < \frac{G}{C \cdot A_0} = \frac{\omega_u}{A_0}$	$\omega_{pl} < \frac{G_{ch}}{C \cdot A_0} = \frac{\omega_u}{A_0}$	$\omega_{pl} = \frac{\omega_u G_{go}}{\varepsilon_T G_m}$	$\omega_{pl} < \frac{G_{go}}{C \cdot A_0} = \frac{\omega_u}{A_0}\frac{G_{go}}{G_m}$

- RC integrators [Gerf03]

$$\mathrm{ITF}(s) = \frac{\alpha/\tau}{s+\gamma} \qquad \alpha = \frac{A_0}{1+A_0} \qquad \gamma = \frac{1/\tau}{1+A_0}$$

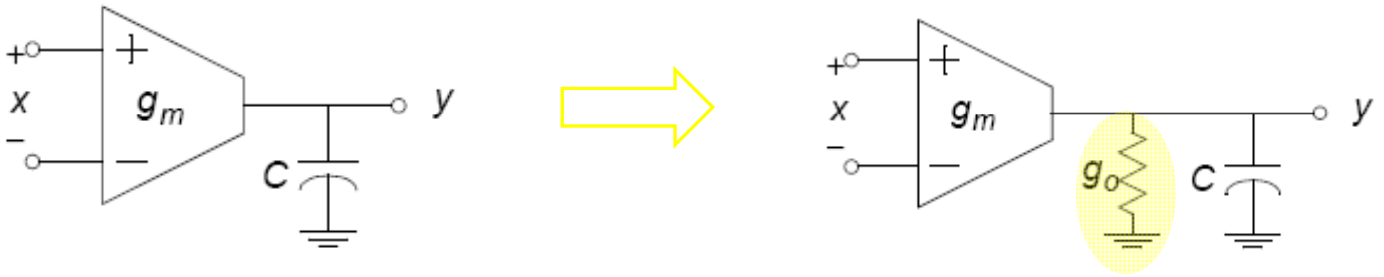
- Same IBN degradation as in SC ΣΔMs $\tau = 1/f_s$

$$P_{A_0} = \frac{\Delta^2}{12 k_1^2 k_q^2}\left[\frac{1}{A_0^{2L} M} + \sum_{m=1}^{L} \frac{\pi^{2l} L(L-1)\ldots(L-m+1)}{(2m+1) M^{2l+1} A_0^{2(L-m)} m!}\right]$$



CT-ΣΔMs : Effect of finite DC gain error

Opamp finite DC gain (II) – Gm-C integrators

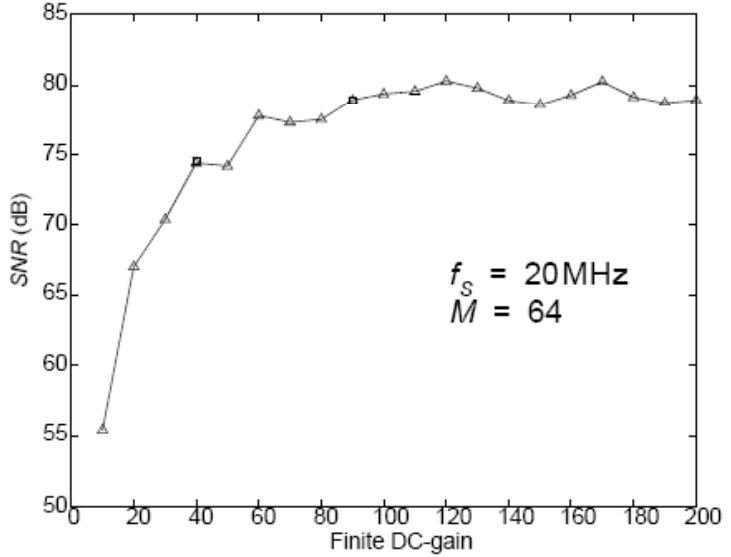


- Power Spectral Density of an *Lth*-order ΣΔM

$$S_q(f) = \left[\sum_{i=0}^{L-1} \binom{L}{i} \left(\frac{j\omega}{\omega_{pl}}\right)^i\right]^2 \cdot \frac{\Delta^2}{12 \cdot A_{dc}^{2L} \cdot f_s}$$

- Relative increase of P_Q in a 2nd-order ΣΔM

$$\frac{P_q}{P_q\big|_{A_{dc}\to\infty}} \approx \frac{5}{\pi^2}\left(\frac{M}{A_{dc}}\right)^4 + \frac{10}{3\pi^2}\left(\frac{M}{A_{dc}}\right)^2 + 1$$

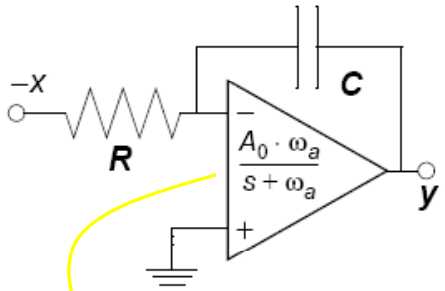


CT-ΣΔMs : Integrator transient response

Integrator transient response (I)

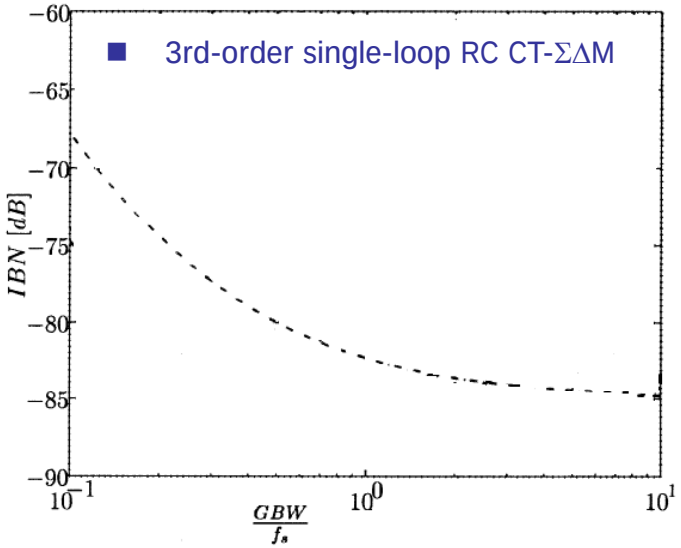
- Less critical than in DT ΣΔMs
- Need to be taken into account, specially in broadband applications

Influence of *GBW* [Gerf03]



$$P_{GBW} \cong \frac{\Delta^2}{12 k_1^2 k_q^2} \cdot \left[\frac{\pi^{2L-1}}{(2L+1)M^{2L+1}} \cdot \left(1 + \frac{k_1/\tau}{GBW_1}\right)^2 \prod_{i=2}^{L} \left(1 + \frac{1}{GBW_i \cdot \tau}\right)^2 \right]$$

$$GBW = A_0 \cdot \omega_a \quad \Rightarrow \quad ITF(s) \cong \frac{k_i}{s \cdot \tau} \cdot \frac{\frac{GBW}{GBW + k_i/\tau}}{\frac{s}{GBW + k_i/\tau} + 1}$$



Other dynamic effects

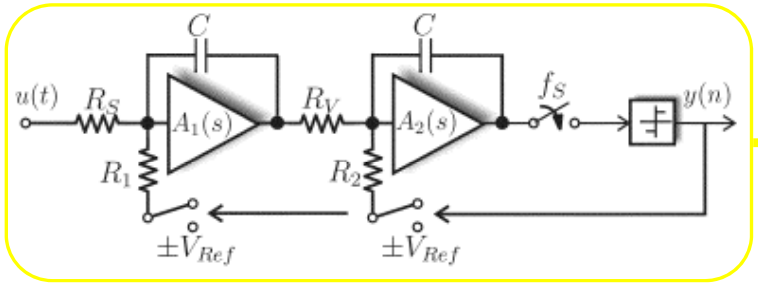
- *2nd-order poles*
- *Slew-rate*

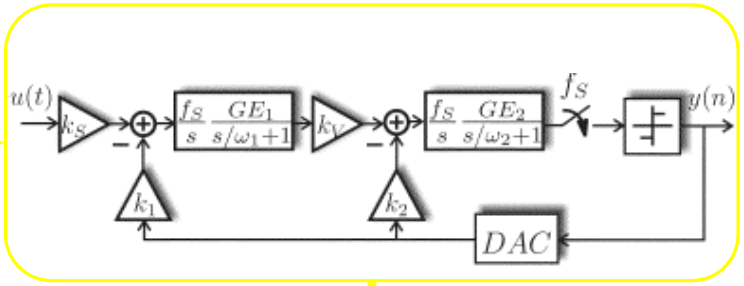
- Complex analysis
- Simulation-based study [Ruiz03]

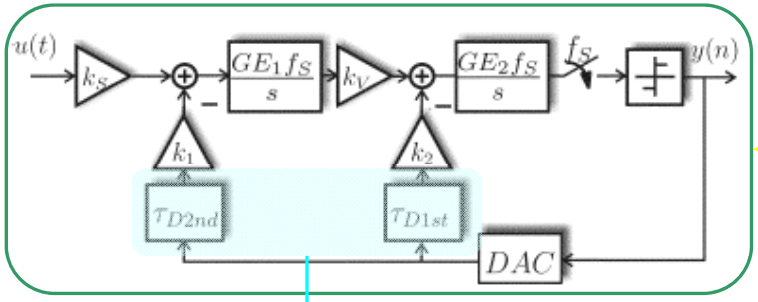
CT-ΣΔMs : Integrator transient response

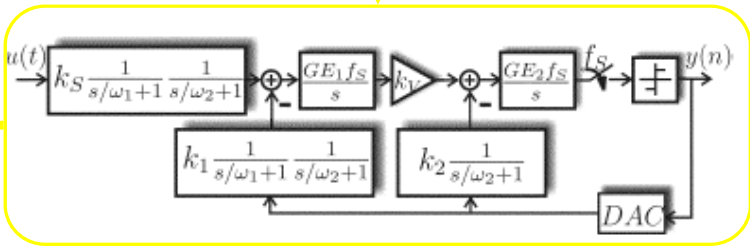
Model of *GBW* for RC-active based CT-ΣΔMs [Ortm04]

- Modeled as a gain error (GE) and extra loop delay
- Each delay is different for each feeback path









$$\tau_{D1st} = \frac{1 - e^{-\omega_2/f_S}}{\omega_2} \qquad \tau_{D2nd} = \frac{\omega_1^2(1 - e^{-\omega_2/f_S}) - \omega_2^2(1 - e^{-\omega_1/f_S})}{\omega_1\omega_2(\omega_1 - \omega_2)}$$

CT-ΣΔMs : Circuit element tolerances

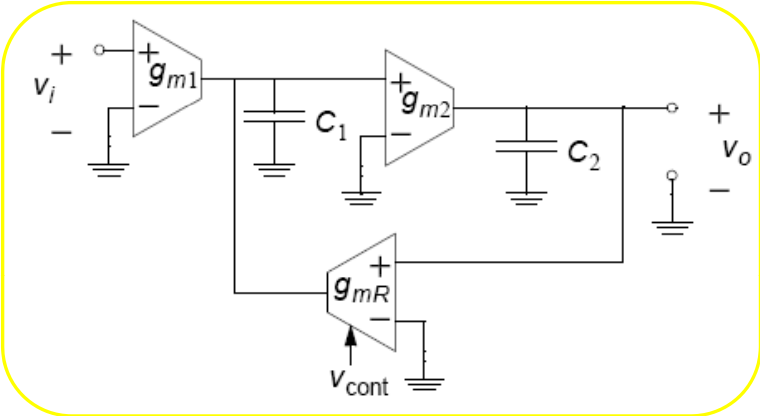
Element tolerances

- Scaling coefficients accuracy limited by random errors in resistors/capacitors

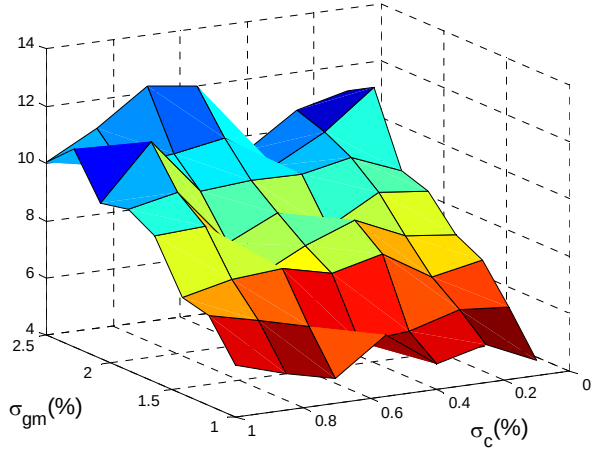
$$\frac{\Delta\tau}{\tau} = \frac{\Delta C}{C} - \frac{\Delta g_m}{g_m} \qquad \Rightarrow \qquad \sigma_\tau = \sqrt{\sigma_C^2 + \sigma_{g_m}^2}$$

- Especially critical in:
  - High-order single-loop architectures (instability)
  - Cascade architectures (analog/digital coefficient ratios)
- Two types of random errors:
  - Absolute tolerances: variations from chip to chip (10-20%)
  - Relative mismatches: variations from device to device on one chip (0.5-1%)

■ Electrical control of frequency tuning



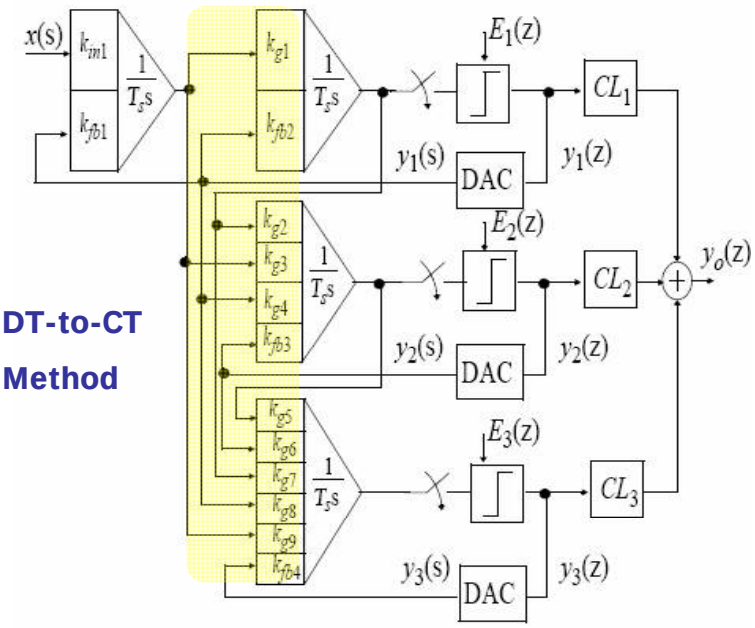
■ System-level optimization and synthesis method



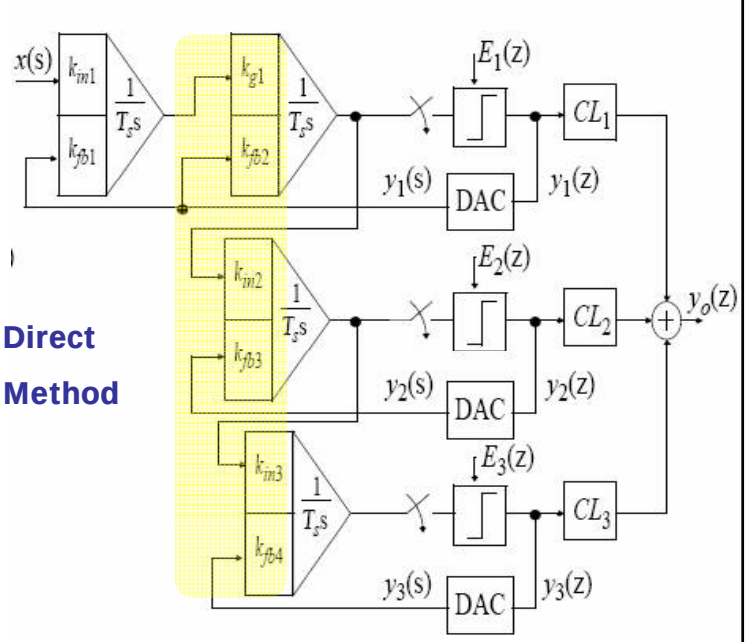
CT-ΣΔMs : Circuit element tolerances

❒ Direct synthesis method of CT cascade architectures [Tort06]:

- Optimum placement of poles/zeroes of the NTF
- Synthesis of both analog and digital part of the cascade CT ΣΔ Modulator
- Reduced number number of analog components
- Reduced sensitivity to element tolerances



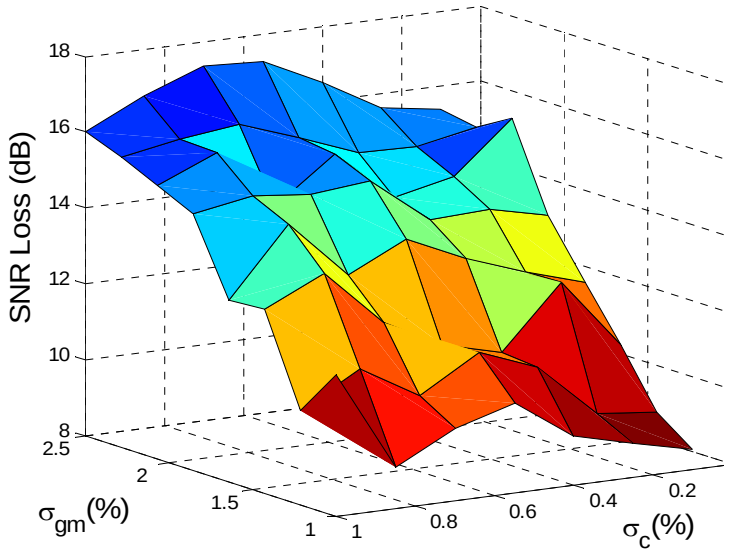
DT-to-CT Method



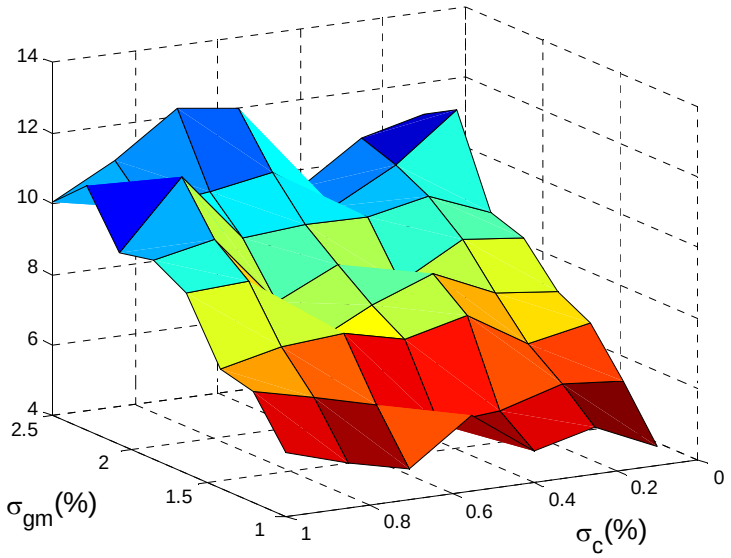
Direct Method

CT-ΣΔMs : Circuit element tolerances

- Direct synthesis of cascade architectures (I) [Tort06]
  - Sensitivity to mismatch (gm,C)
  - A 2-1-1 example



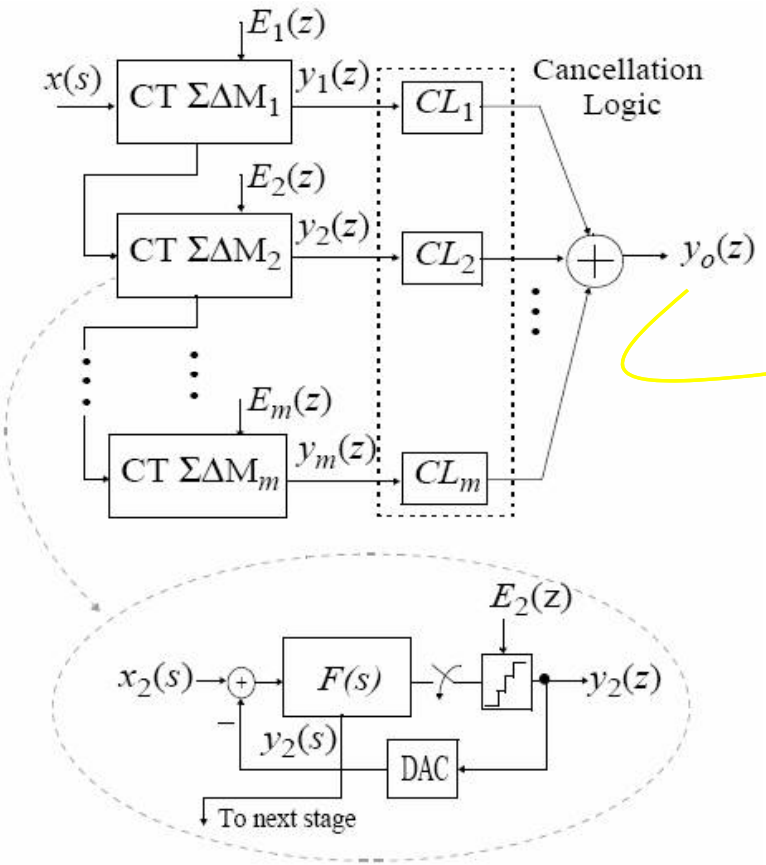
- DT-to-CT synthesis method



- Direct synthesis method

CT-ΣΔMs : Circuit element tolerances

- Direct synthesis of cascade architectures (II) [Tort06]



$$y_o(z) = \sum_{k=1}^{m} y_k(z) CL_k(z)$$

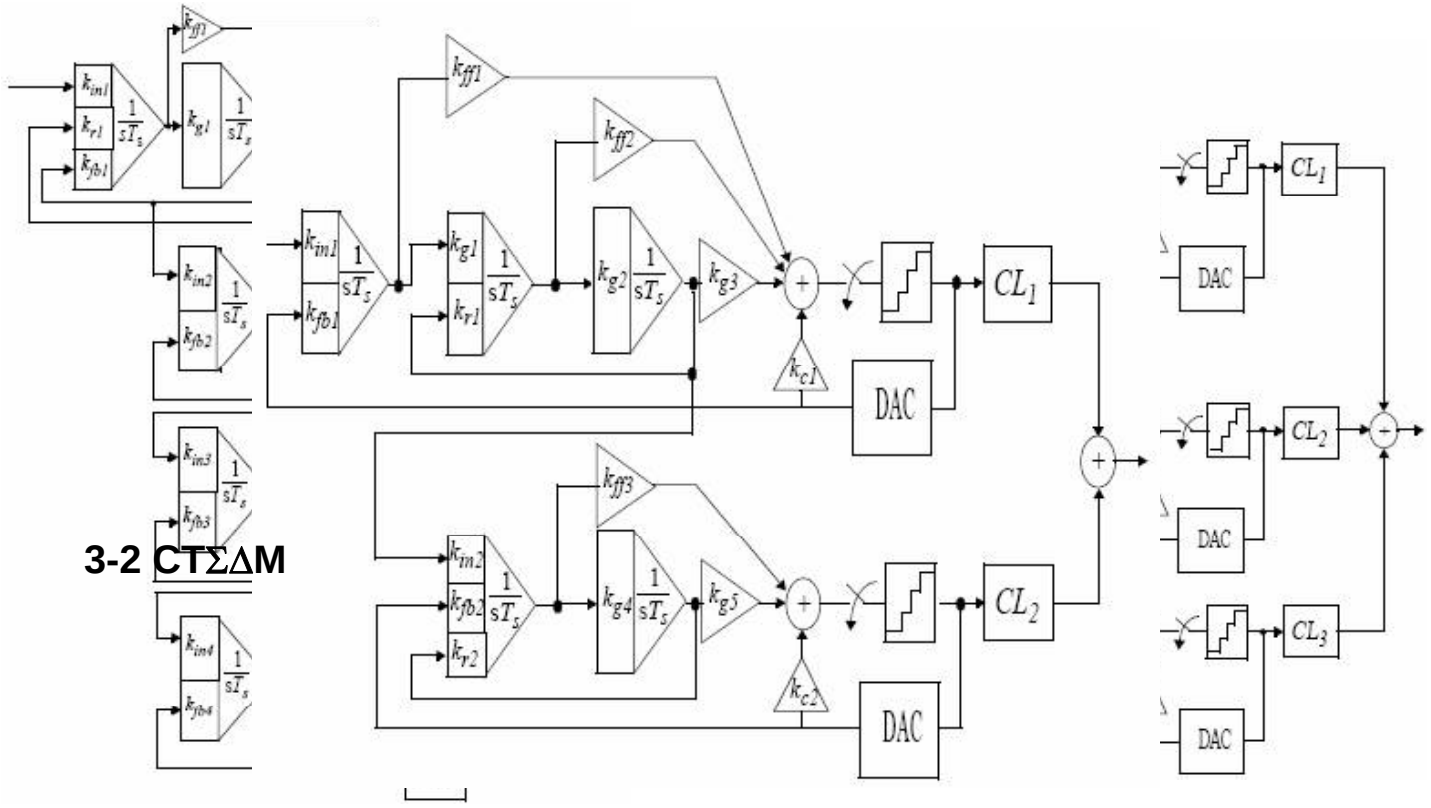
$$y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z_{ik} y_i(z)}{1 - Z_{kk}}$$

$$CL_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{mm}}$$

$$\left[Z_{km} \equiv Z\left(L^{-1}(H_D F_{km})\big|_{nT_s} \right) \right]$$

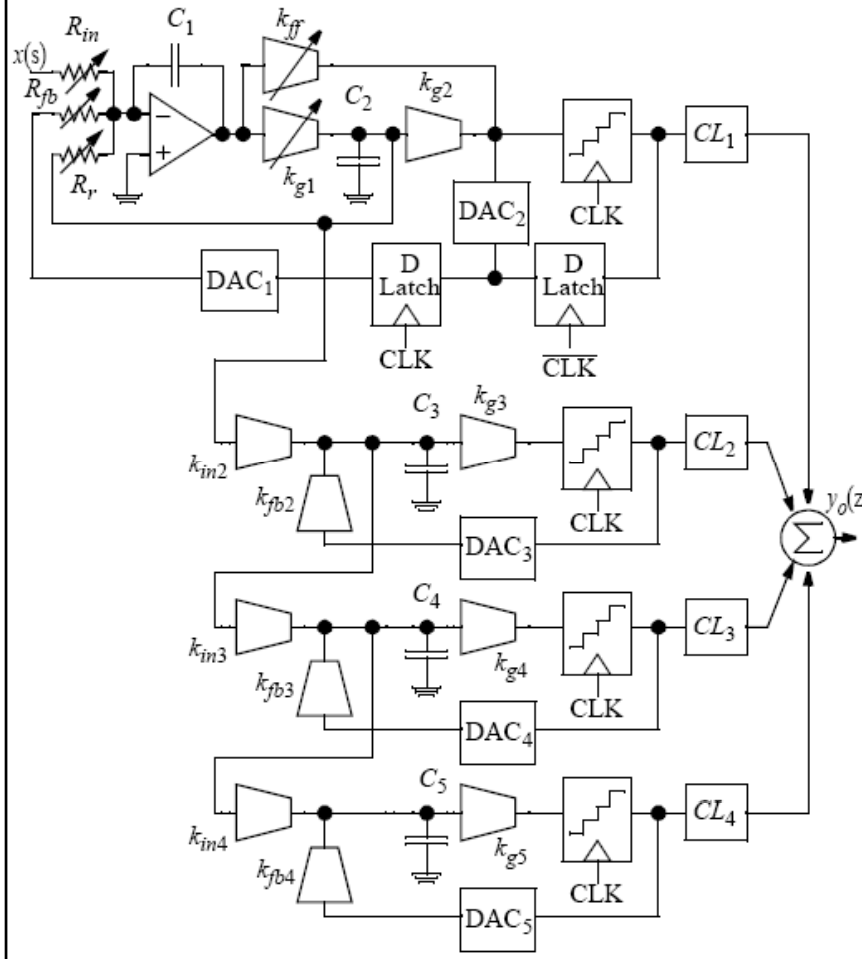
CT-ΣΔMs : Circuit element tolerances

- Synthesized cascaded CT SDMs to cope with 12-bit@20-MHz

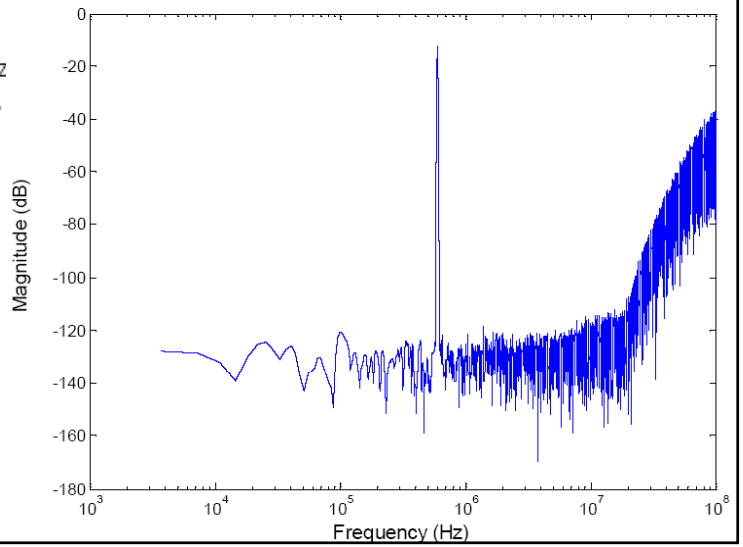


CT-ΣΔMs : Synthesis methods

- A case study: A 12-bit@20MHz, 4-b, 2-1-1 CT ΣΔM (RC/Gm Integrators)



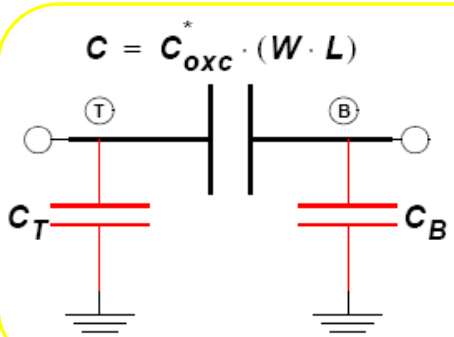
Parameter	Value
R_{in},R_{fb}	1kΩ
R_r	2.9kΩ
$k_{g2} \cdots k_{g5}$	50μA/V
k_{g1}	500μA/V
k_{ff}	120μA/V
$k_{in2} \cdots k_{in4}$,$-k_{fb2} \cdots -k_{fb4}$	450μA/V
C_1	7.5pF
$C_2 \cdots C_5$	1.875pF



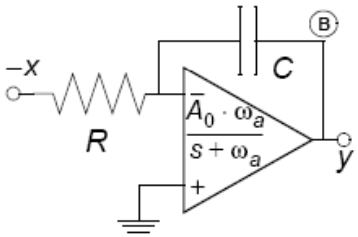
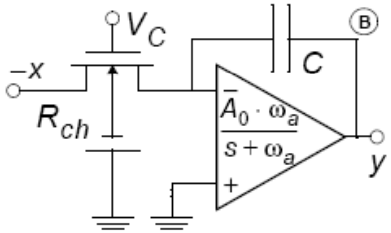
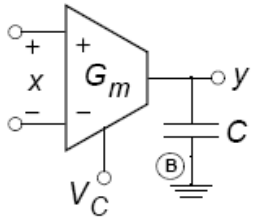
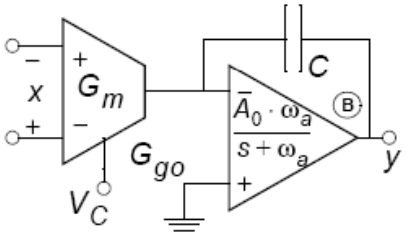
Integrator time-constant error (I)

$$\mathrm{ITF}(s) = \frac{A_o}{1 + sC(1+\varepsilon_\tau)/g_o}$$

$$\varepsilon_\tau = C_p / C$$



- Capacitor plate parasitic capacitances
- Parasitic capacitances of the interconnection lines
- Parasitic input capacitances of the circuits connected to the node
- Parasitic output capacitances of the circuits connected to the node

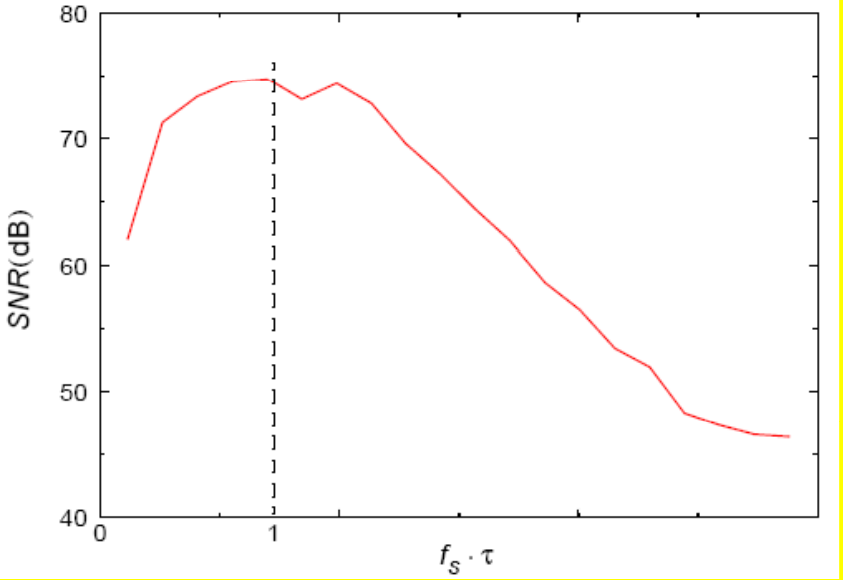
RC ε_τ	MOSFET-C ε_τ	Gm-C ε_τ	Gm-MC ε_τ
			
$1 + \frac{G}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0}$	$1 + \frac{G_{ch}}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0}$	$1 + \frac{C_T}{C}$	$1 + \frac{G_{go}}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0}$

Integrator time-constant error (II)

$$\Delta P_{Q_{A_o,\varepsilon_\tau}}\Big|_{\mathrm{dB}} \cong \begin{cases} \dfrac{3M^2}{\pi^2}\cdot\dfrac{1}{A_o^2}+(1+\varepsilon_\tau)^2 & \text{(1st-order modulator)} \\ (1+\varepsilon_\tau)^4+\dfrac{10}{3\pi^2}\cdot\dfrac{(1+\varepsilon_\tau)^2}{A_o^2}M^2+\dfrac{5}{\pi^4 A_o{}^4}M^4 & \text{(2nd-order modulator)} \end{cases}$$

Optimum SNR for:

$$\tau = 1/f_s$$

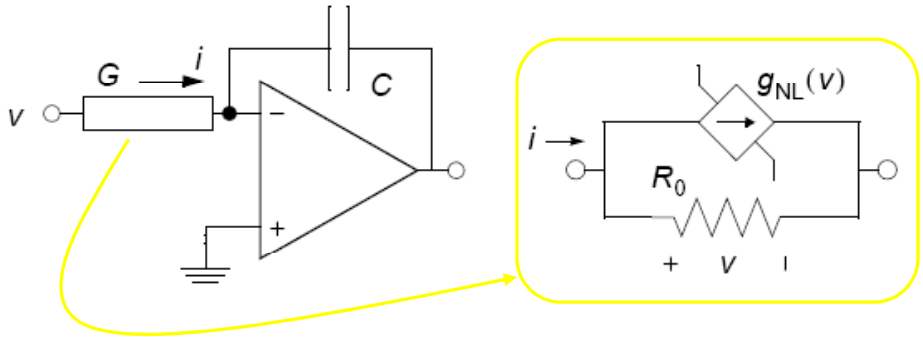


CT-ΣΔMs : Non-linear errors

Causes of Non-linearity

- Intrinsic non-linearity of the resistor material
- Modulation of thickness of the conductive layer with resistor voltage

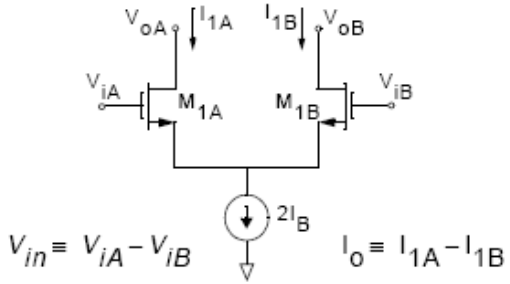
V-I transformation in RC integrators



$$\Rightarrow \textit{Ideally} \qquad i = R_0^{-1} \cdot v$$

$$g_{NL}(v) = R_0^{-1} \cdot \left\{ a_2 \cdot v^2 + a_3 \cdot v^3 + o(v) \right\}$$

V-I transformation in Gm-C integrators



Normalized Large Signal Characteristic

$$i(v) = \begin{cases} -1 & v \le -\sqrt{2} \\ v\sqrt{1-(v/2)^2} & |v| \le \sqrt{2} \\ 1 & v \ge \sqrt{2} \end{cases}$$

$$i = \frac{I_o}{2I_B} \qquad v = V_{in}\left(\frac{G_{m0}}{2I_B}\right)$$

$$G_{m0} = 2\sqrt{\frac{2\beta_1 I_B}{n}}$$

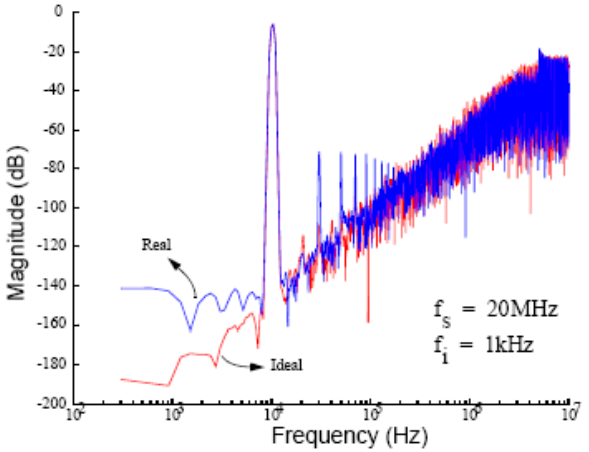
CT-ΣΔMs : Non-linear errors

- Effect on Non-linearity in Gm-C CT-ΣΔMs [Bree01]

$$i(v) = \beta v\sqrt{2I_B/\beta - v} \cong \sum_{k=1}^{\infty} g_{m_k} v^k$$

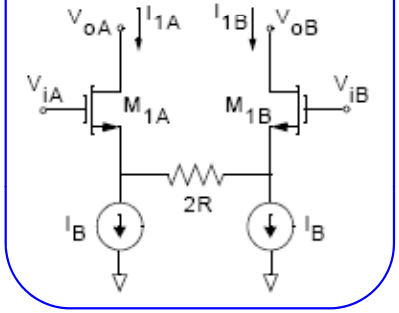
$$i(v) \cong g_{m_1} v + g_{m_3} v^3$$

$$THD \cong HD_3 \cong \frac{g_{m_3}}{g_{m_1}} V_i^2$$

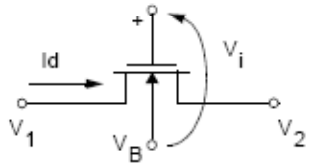


- Linearization strategies

Source Degeneration of Basic Differential Pairs



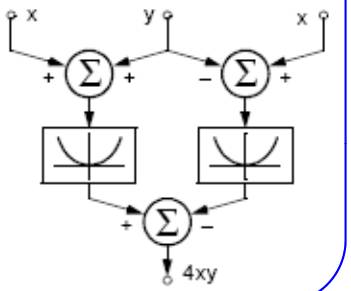
Exploiting the Ohmic Region of MOSTs



$$I_d = 2\beta(V_1 - V_2)\left[(V_i - V_{T0}) - \frac{n}{2}(V_1 + V_2)\right]$$

MOST Saturated Transconductors

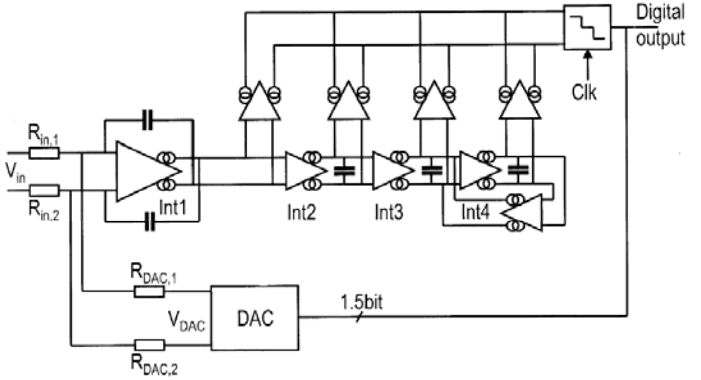
- Functional cancellation
- Square-law functions combination



CT-ΣΔMs : Nonlinearities and noise

Typical Nonlinear-Tolerant Architecture

- RC-active front-end integrator
- Gm-C subsequent integrators



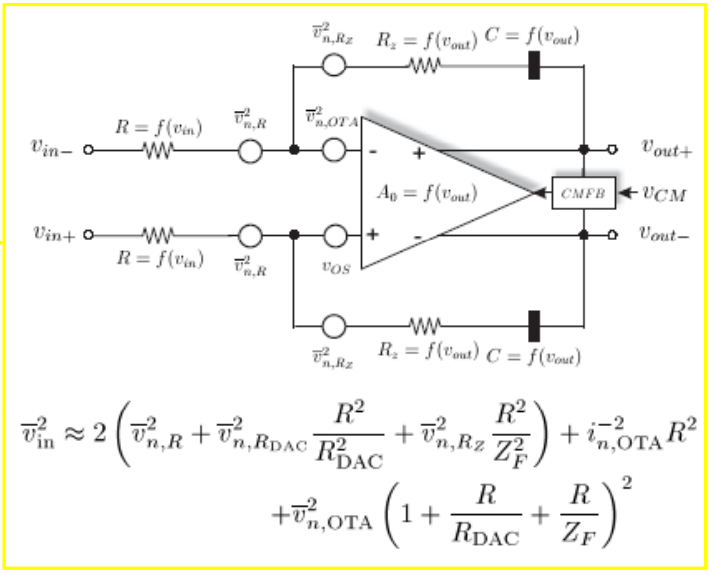
Other sources of non-linearity

- Multi-bit DACs
- Linearity must be the same or lower than the required resolution
- Corrected by same techniques as those employed in SC ΣΔMs
  - DEM
  - Calibration

Circuit noise

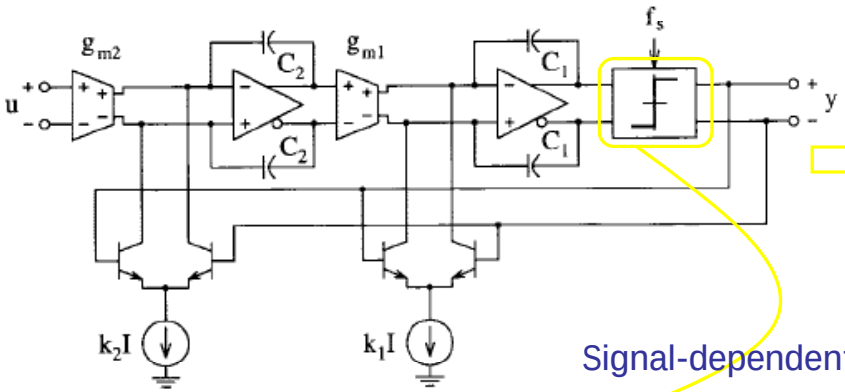
- Dominated by noise sources from the front-end integrator and DAC
- Flicker noise reduced by proper sizing and/or chopper techniques
- Unsampled noise – effect of sampling reduced by the loop gain

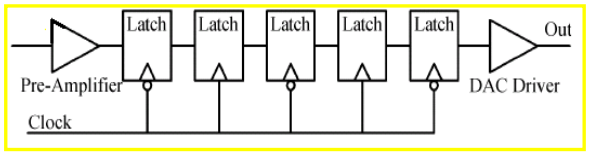
$$P_{Th} \cong \frac{KT}{4C}\frac{\pi^{2L}}{(2L+1)M^{2L+1}}$$



$$\overline{v}^2_{\text{in}} \approx 2\left(\overline{v}^2_{n,R} + \overline{v}^2_{n,R_{\text{DAC}}}\frac{R^2}{R^2_{\text{DAC}}} + \overline{v}^2_{n,R_Z}\frac{R^2}{Z^2_F}\right) + i^{-2}_{n,\text{OTA}}R^2 + \overline{v}^2_{n,\text{OTA}}\left(1 + \frac{R}{R_{\text{DAC}}} + \frac{R}{Z_F}\right)^2$$

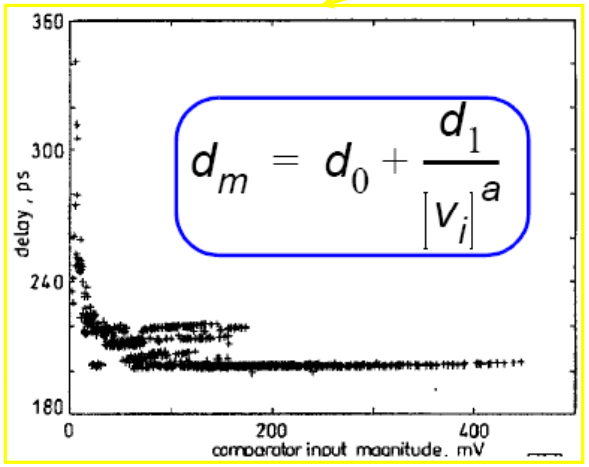
CT-ΣΔMs : Comparator metastability



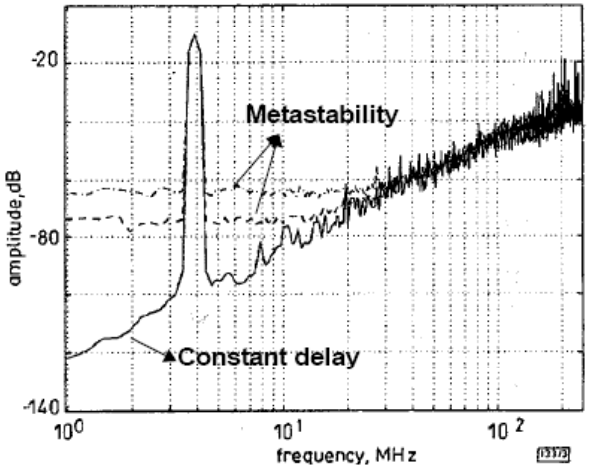


- Can be cancelled by using additiona latches [Dagh04]

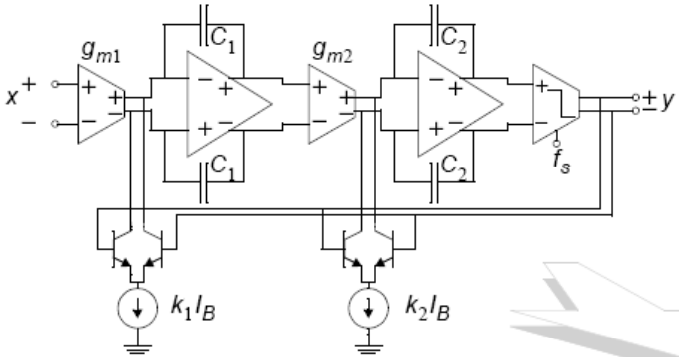
Signal-dependent Delay



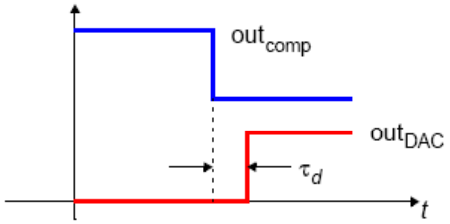
- Modeled as a jitter noise [Cher00]



CT-ΣΔMs : Excess loop delay

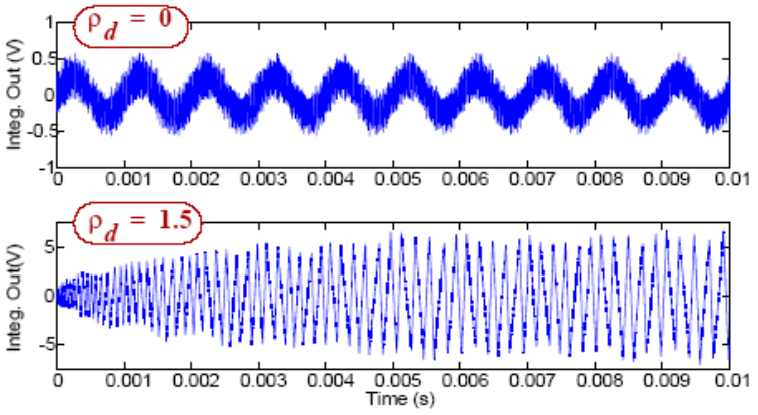


DAC transient response delay

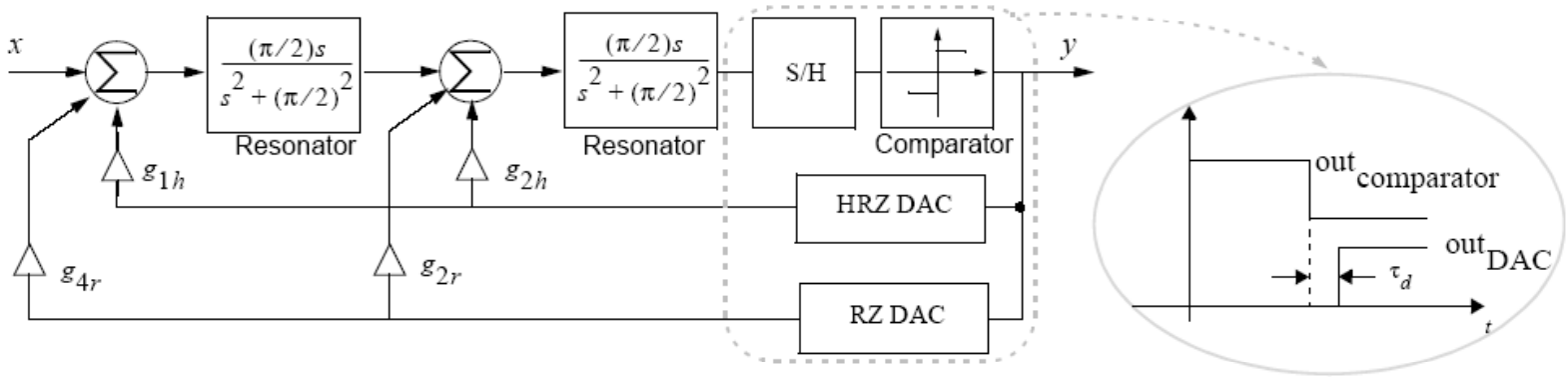


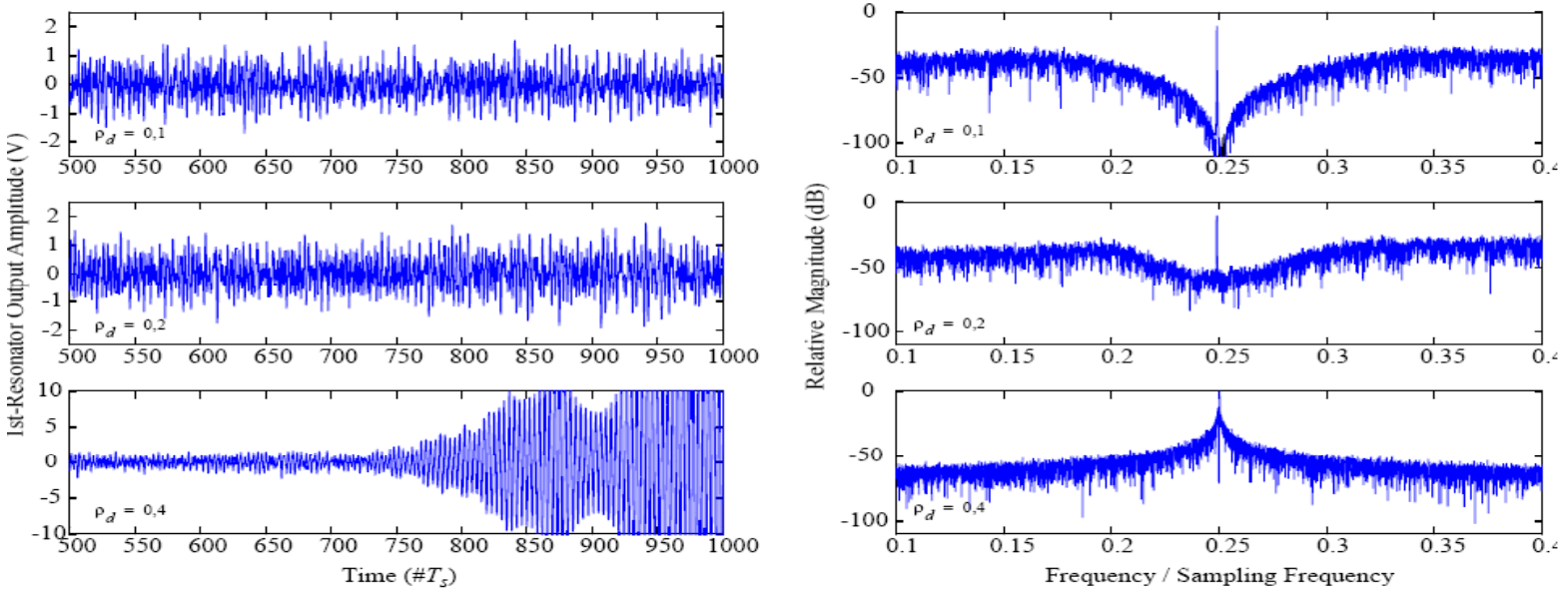
$$Y(f) = \frac{g_q g_1 g_2}{(s\tau)^2 + g_q g_1 {}' g_2 \cdot e^{-\tau_d s} + g_q g'_2 \cdot (s\tau) e^{-\tau_d s}} X(f) + \frac{(s\tau)^2}{(s\tau)^2 + g_q g_1 {}' g_2 \cdot e^{-\tau_d s} + g_q g'_2 \cdot (s\tau) e^{-\tau_d s}} E(f)$$

- Adds additional poles to STF/NTF
- Causes instability
- Stability condition:
  - 2nd-order $\rho_d \leq \frac{g'_2}{2 g'_1 g_2}$
  - *Lth*-order $\rho_d \propto \frac{1}{[H(f)]_{outband}}$



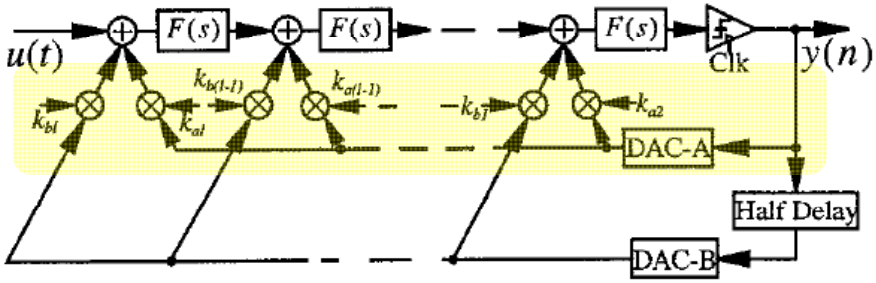
CT-ΣΔMs : Excess loop delay – Raising Instability

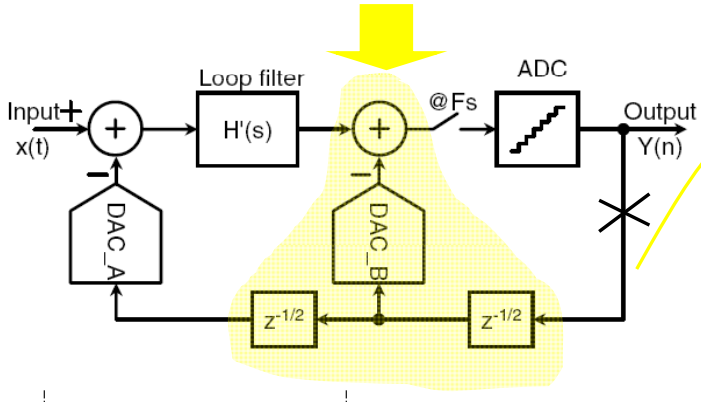


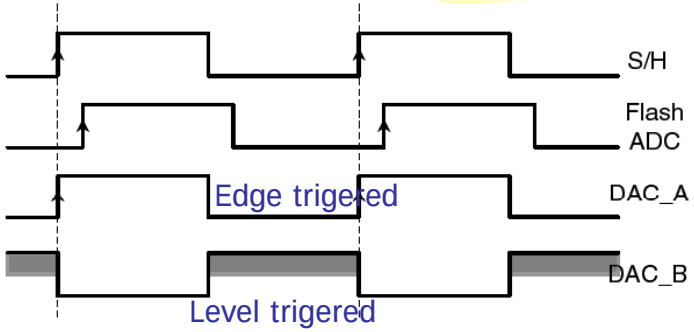


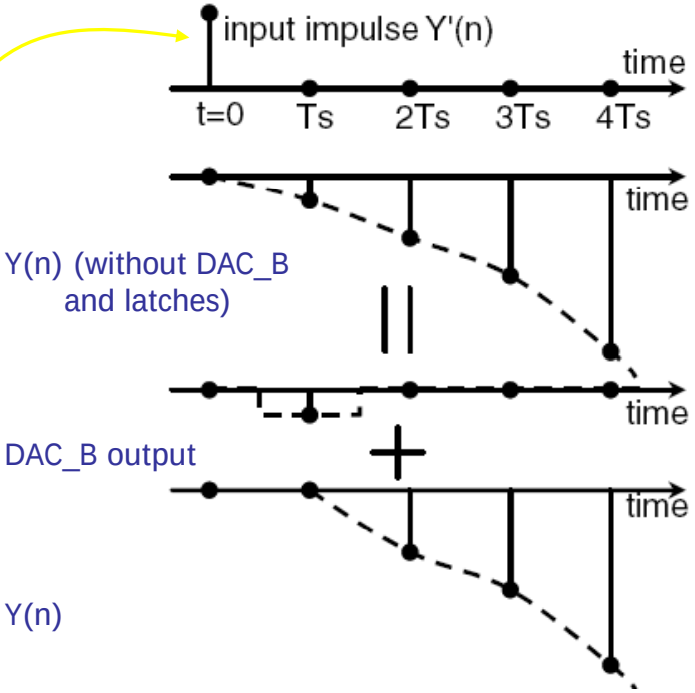
CT-ΣΔMs : Excess loop delay – Cancellation

- Extra feedback paths (DACs) with tunable gains [Cher00]
- Using only one additional DAC and two latches [Yan04]



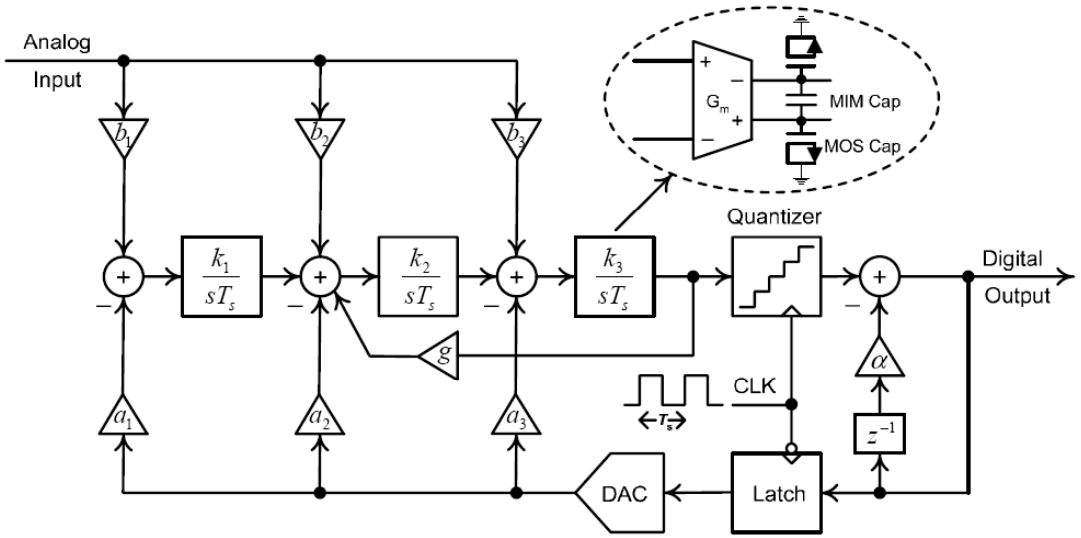






CT-ΣΔMs : Excess loop delay – Compensation

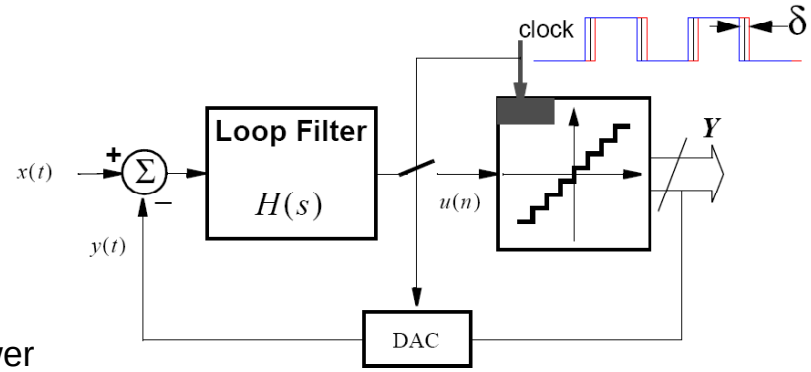
- Digital compensation [Font05]
  - Implemented in a 3rd-order single loop architecture with 5-level quantizer
    - 90nm CMOS
    - 74-dB SNDR-peak, 600kHz bandwidth
    - 6.0mW, 1.5V
  - Excess loop delay compensated in the digital domain
  - Half-a-clock-cycle delay
    - Relax comparators speed
    - Provide maximum isolation between quantizer and DAC switch events



CT-ΣΔMs : Clock jitter error

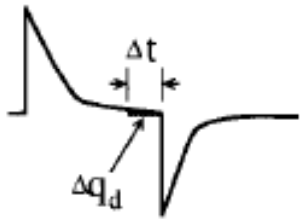
Clock jitter (I)

- S/H
  - Shaped by the modulator NTF
  - Can be neglected
- DAC
  - Directly adds with the input
  - Increases the in-band noise power

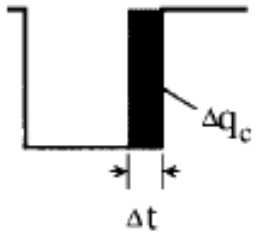


CT ΣΔMs are more sensitive to clock jitter than DT ΣΔMs

■ DT DAC waveform



■ CT DAC waveform

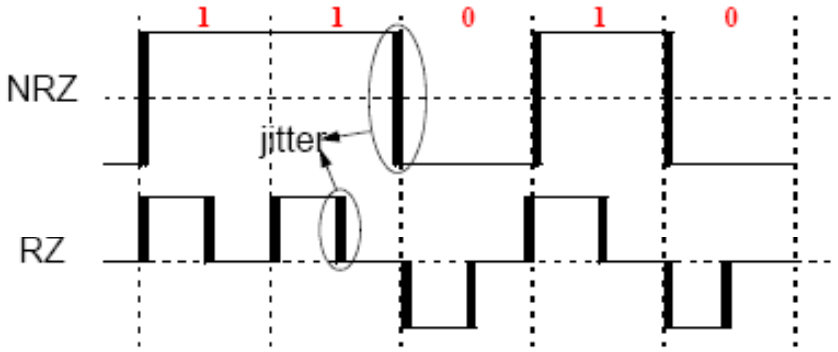


White noise model approximation (NRZ DAC) [Cher00][Zwan96]

- Standard deviation of jitter error: $\sigma_q^2 \cong \sigma_j^2 I_{\mathrm{DAC}}^2$
- SNR degradation: $SNR_{\mathrm{J}} = 10\log\left(\frac{1}{16MB_w^2\sigma_j^2}\right)$

$$\frac{\sigma_{j_{\mathrm{CT}}}}{\sigma_{j_{\mathrm{DT}}}} = \left(\frac{\pi}{2M}\right)^2$$

❒ Clock Jitter (II) – White noise model approximation (NRZ/RZ DAC) [Tao99a]



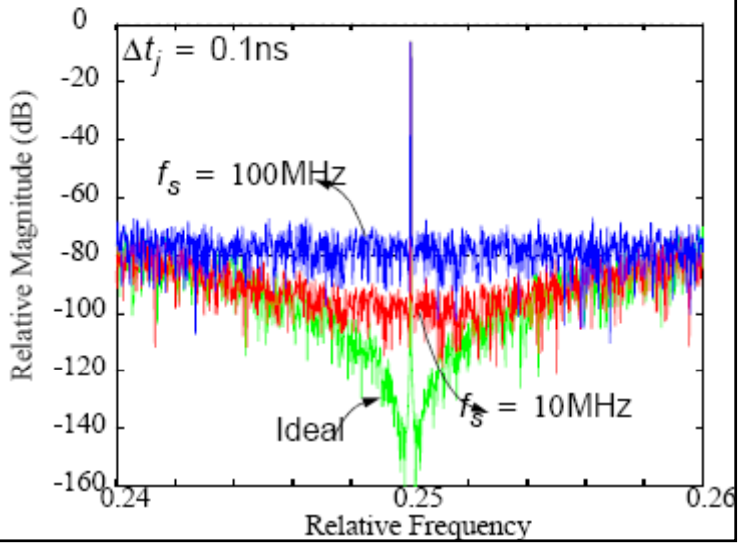
- Lowpass CT-ΣΔMs

$$P_{jitter}\big|_{RZ} \cong \left(\frac{T_s}{T_0}\right)^2 P_{jitter}\big|_{NRZ}$$

- Bandpass CT-ΣΔMs

$$SNR_J \cong \begin{cases} 10\log\left[\dfrac{\mathrm{sinc}(\pi f_n T_s)}{64\sigma_j^2 B_w^2 M}\right] & \text{NRZ} \\ 10\log\left[\dfrac{\mathrm{sinc}(\pi f_n T_s)}{64\left(\frac{T_s}{T_0}\right)^2 \sigma_j^2 B_w^2 M}\right] & \text{RZ} \end{cases}$$

$$\frac{\sigma_j^2\big|_{CT}}{\sigma_j^2\big|_{DT}} \cong 0.14$$



CT-ΣΔMs : Clock jitter error

Clock Jitter (III) – lingering effect [Olia03a]

- Jitter-induced noise includes both white and shaped components
- State-space analysis of CT-ΣΔMs with RZ DAC shows that:

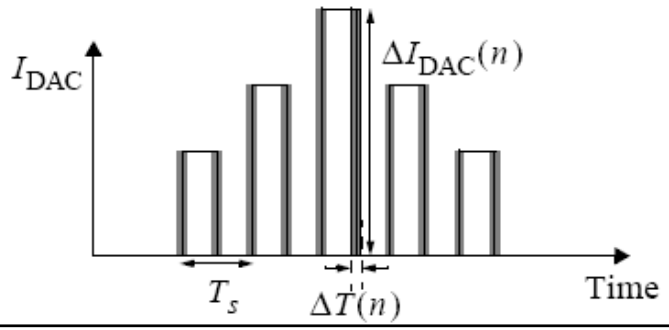
$$S_\varepsilon(z) = \left(\sigma_s^2 T\right) \sum_{m_2=1}^{N} \sum_{j_2=1}^{m_2-1} \sum_{m_1=1}^{N} \sum_{j_1=1}^{m_1-1} a_{m1} a_{m2} z^{j_1-j_2} \times \mathbf{C}\mathbf{A}^{m_1-j_1-1} \mathbf{\Lambda} \mathbf{A}_T^{m_2-j_2-1} \mathbf{C}_T$$

Multi-bit NRZ DACs

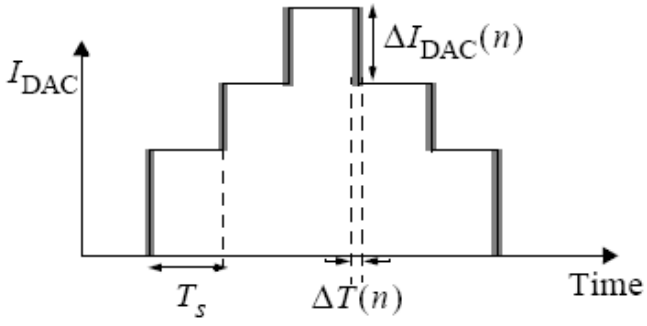
- Commonly used in CT-ΣΔMs for brodband telecom applications
- Less sensitive to clock jitter

$$\Delta Q(n) \cong \Delta I_{\mathrm{DAC}}(n) \cdot \Delta T(n)$$

- RZ DAC

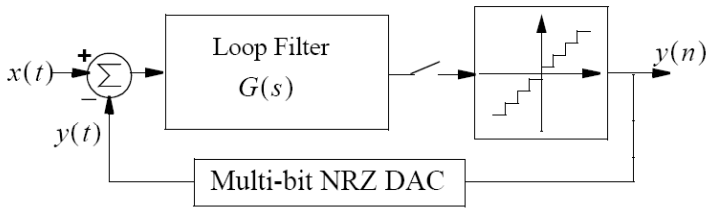


- NRZ DAC



CT-ΣΔMs : Clock jitter error

Clock Jitter (IV) – Multi-bit NRZ DACs [Tort05]



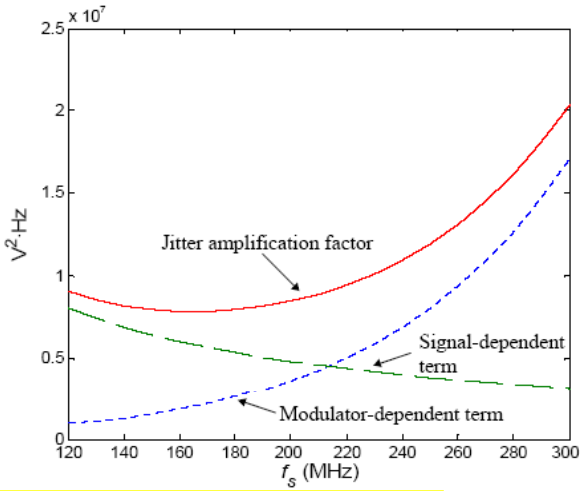
$$\varepsilon(n) = (y(n) - y(n-1))\frac{\Delta T(n)}{T_s}$$ [Ris94]

$$P_\varepsilon = E\{\varepsilon(n)^2\} = \frac{\sigma^2_{\Delta T}}{T_s^2} E\{[y(n) - y(n-1)]^2\}$$

- Using state-space formulation of NTF:

$$P_\varepsilon = \frac{\sigma^2_{\Delta T}}{T_s^2} \cdot \left(\frac{T_S^2 A^2 \omega_{in}^2}{2} + \frac{X_{FS}^2}{6(2^B - 1)^2} \cdot \psi(\bar{g}, \bar{p}, \bar{\lambda}, L) \right)$$

$$\psi(\bar{g}, \bar{p}, \bar{\lambda}, L) = 1 - \bar{g}^T \cdot \bar{p} + \sum_{k=1}^{L} \sum_{j=1}^{L} g_k p_k g_j p_j \frac{\lambda_k^{-1} - \lambda_k^{-1}\lambda_j^{-1}}{1 - \lambda_k^{-1}\lambda_j^{-1}}$$



$$SNR_{\text{jitter}} \equiv \frac{A^2}{2 \cdot P_{\varepsilon\_\text{band}}} = \frac{A^2}{2 \cdot B_w \cdot (\sigma_{\Delta T})^2 \cdot \left[\frac{A^2 \omega_i^2}{f_s} + \frac{X_{FS}^2 \cdot f_s}{3(2^B - 1)^2} \psi(\bar{g}, \bar{p}, \bar{\lambda}, L) \right]}$$

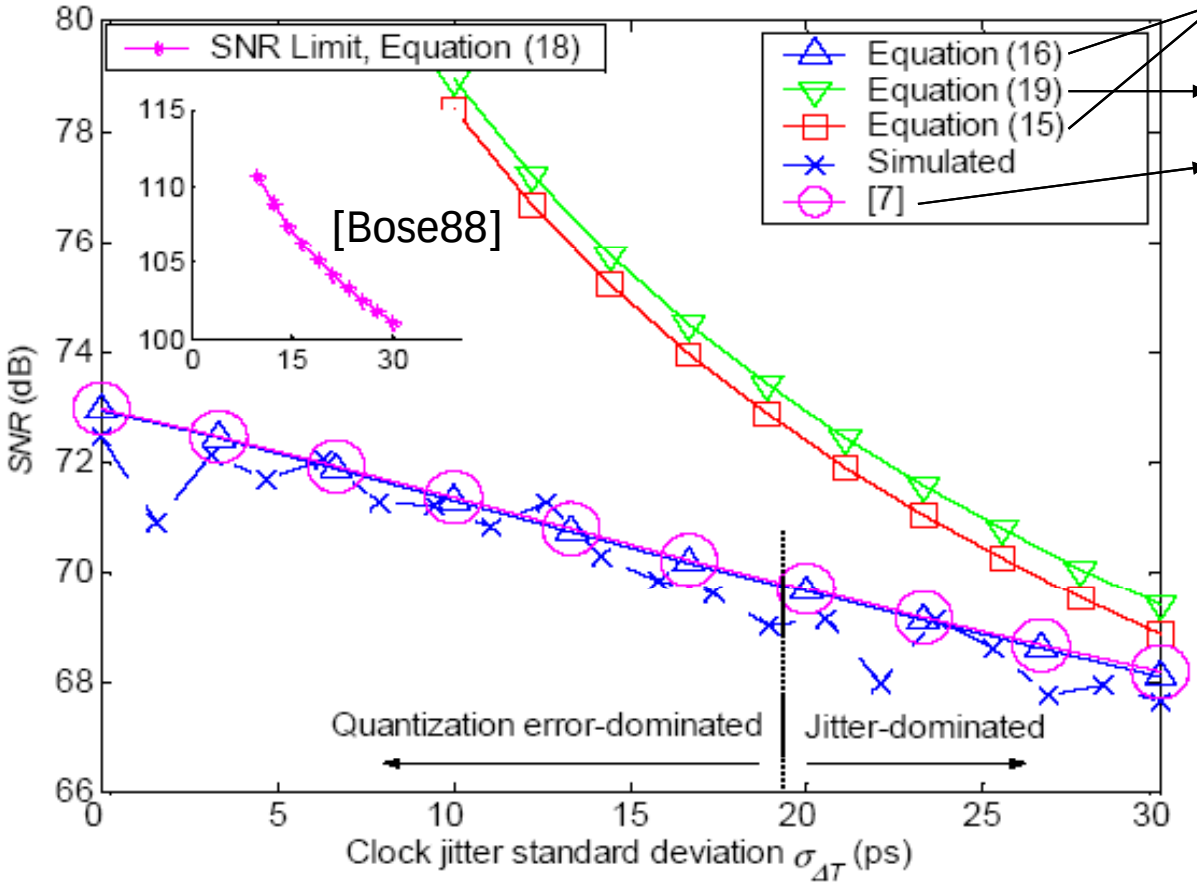
CT-ΣΔMs : Clock jitter error

❒ Clock Jitter (V): Comparison of [Tort05] with previous approaches

Assumin

2nd-order single-bit

If the



This work

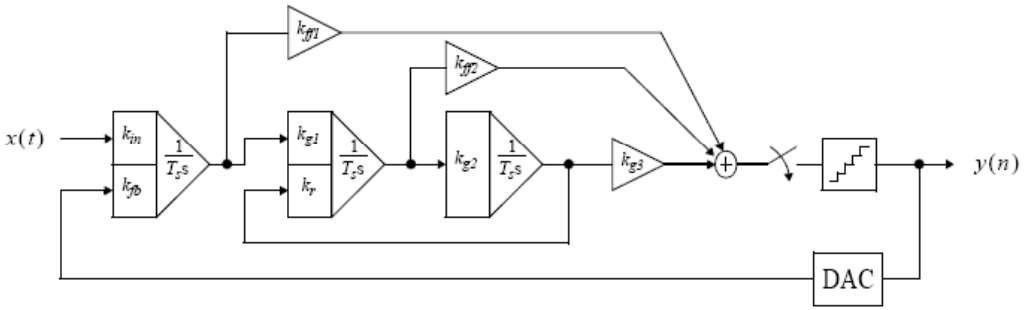
[Zwan96]

[Hern04]

, 1996]

CT-ΣΔMs : Clock jitter error

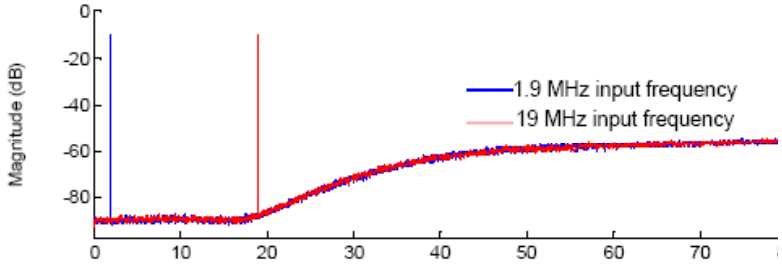
❒ Clock Jitter (V) – Multi-bit NRZ DACs [Tort05]



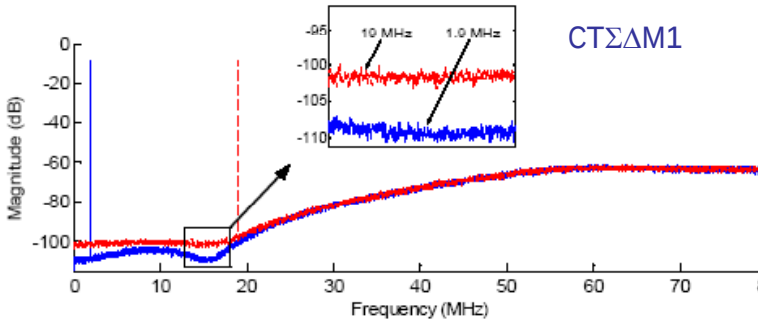
Two cases:

- CTΣΔM1: B=2bit, f_s=400MHz

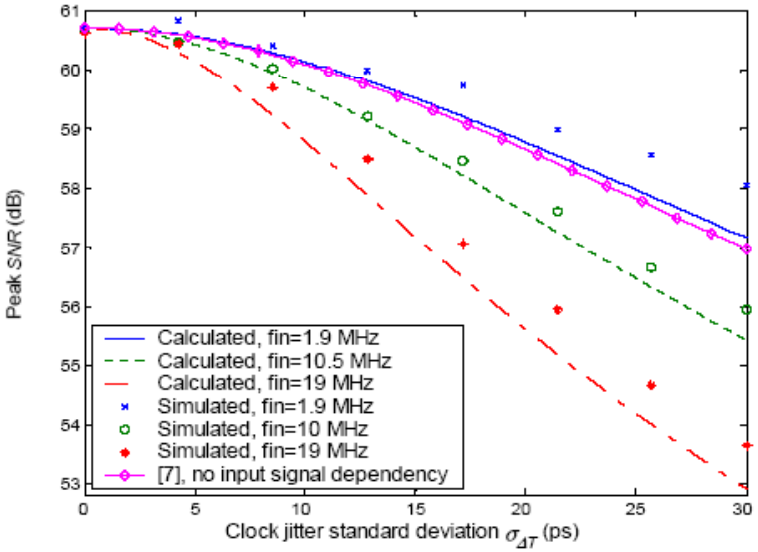
- CTΣΔM2: B=5bit, f_s=160MHz



CTΣΔM1

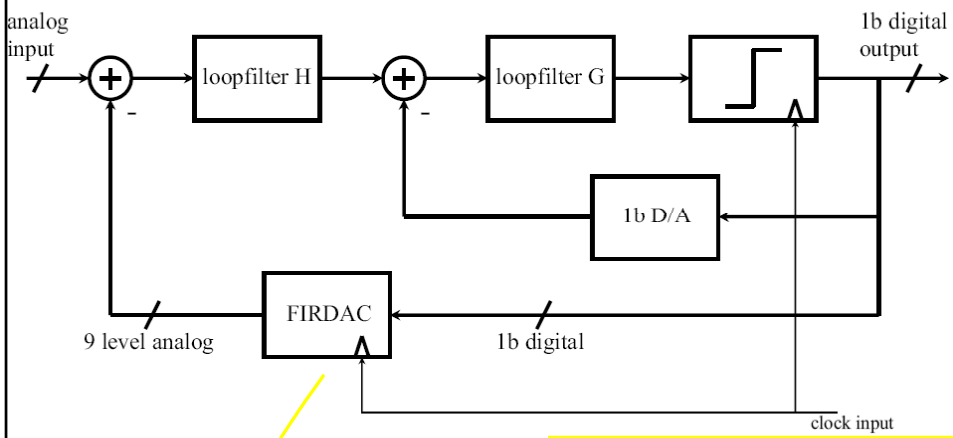


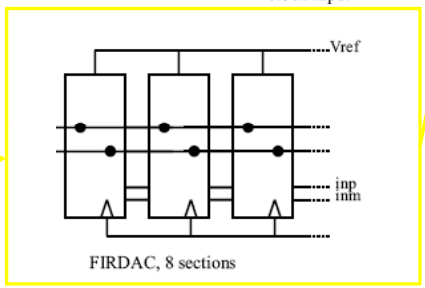
CTΣΔM2

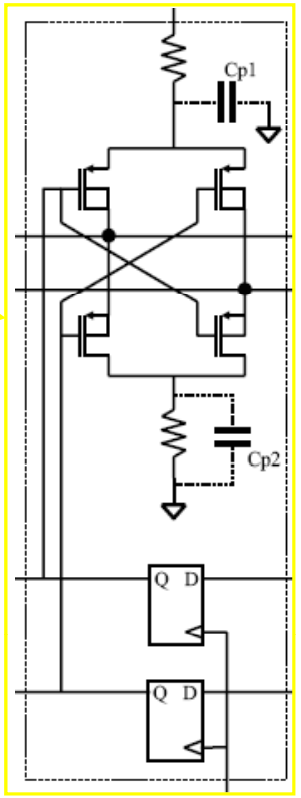


Clock Jitter (VI) – Compensation techniques

- Multi-bit quantization (non-linear DAC)
- Switched-capacitor DAC [Veld03]
  - Voltage-mode operation (proper for active RC integrators)
  - Slower than switched-current (current steering) DAC
- FIRDAC to generate a multilevel signal [Putt04]



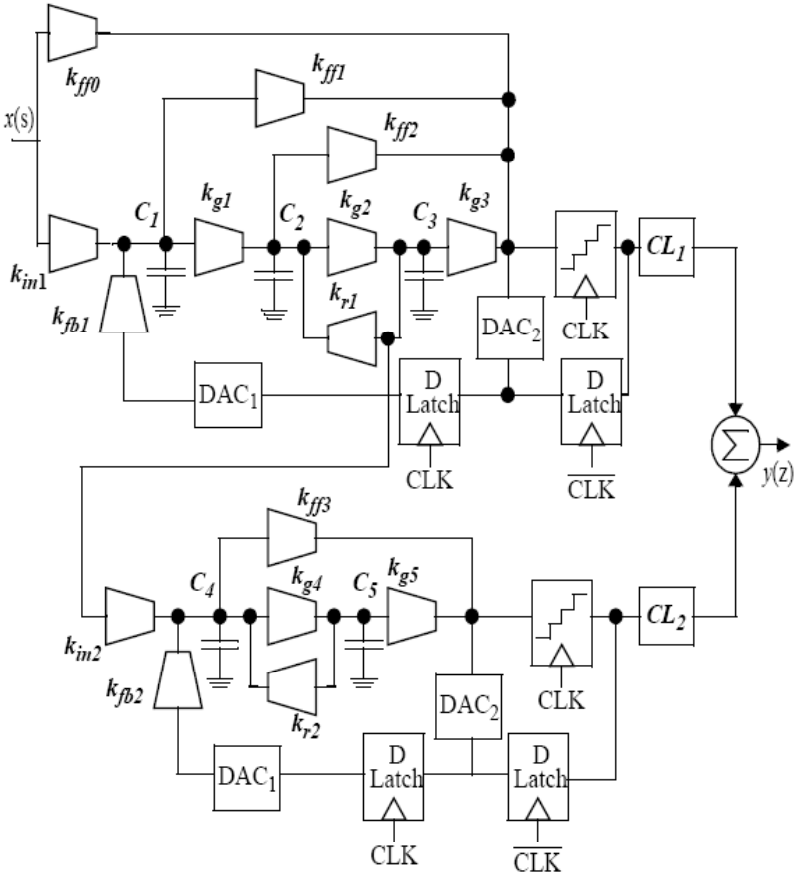




CT-ΣΔMs : Case studies

A case study: A Gm-C 12-bit@20MHz, 4-b, 3-2 CT ΣΔM

- 130nm mixed-signal CMOS, 1P8M
- Cascade 3-2 multi-bit (4b) CT ΣΔM
- Gm-C loop-filter implementation
- Current-steering feedback DACs + DEM
- 12-bit effective resolution
- 40MS/s output rate (20MHz bandwidth)
- 240MHz clock frequency
- 1.2V ± 10% analog/digital power supply
- On-chip tuning of analog components
- Estimated power consumption is 45mW



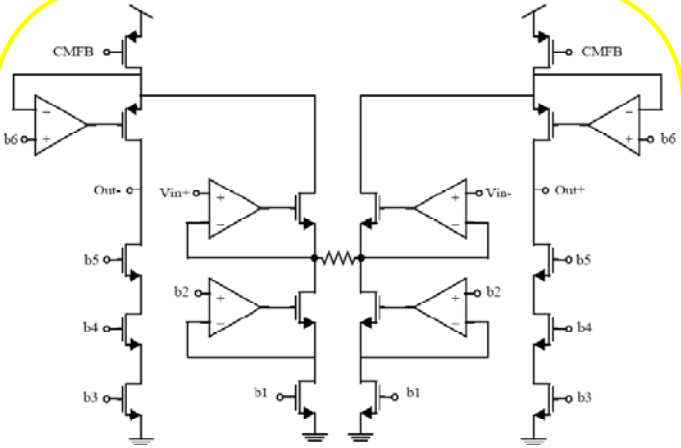
Loop-filter coefficients

$C_u = 3.65\ pF\ ;\ k_u = 190\,\mu A/V$
$C_1 = C_2 = C_3 = C_u\ ;\ C_4 = C_5 = 2C_u$
$k_{in1} = 852\ \mu A/V\ ;\ k_{fb1} = 730\ \mu A/V$
$k_{ff0} = 2k_u\ ;\ k_{ff1} = 4k_u\ ;\ k_{ff2} = 2k_u\ ;\ k_{ff3} = 5k_u$
$k_{g1} = k_{g5} = 3k_u\ ;\ k_{g2} = 5k_u\ ;\ k_{g3} = k_u\ ;$ $k_{g4} = 7k_u$
$k_{in2} = 5k_u\ ;\ k_{fb2} = 6k_u$
$k_{r1} = k_{r2} = k_u$

Finite output impedance	12MΩ
Settling Time	500ps

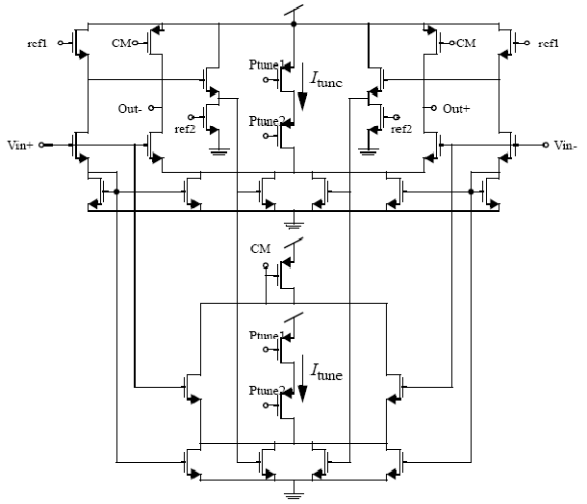
Transconductors

- Resistive source degenerated front-end transconductor
- Loop-filter transconductors based on quadratic term cancellation



Transistor-level performance

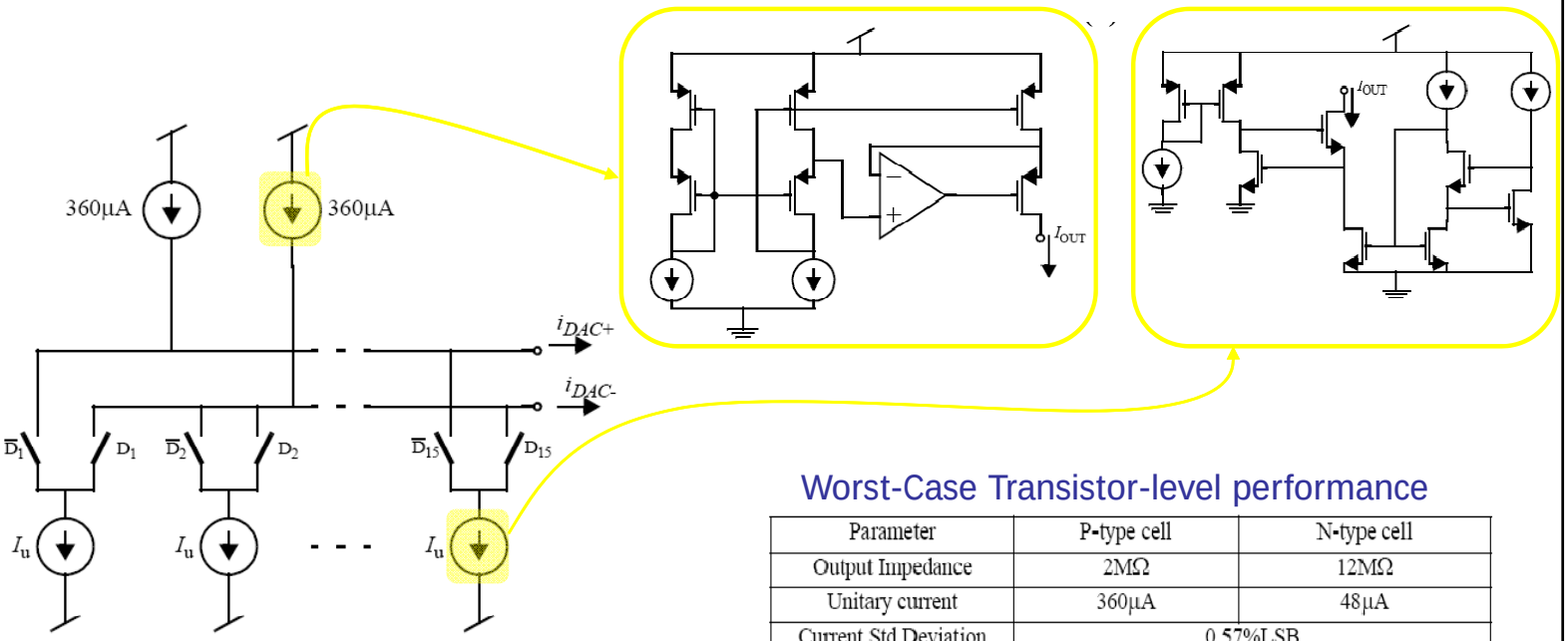
DC Gain	78.3 dB
Diff. Input Amplitude	0.3V
Diff. Output Amplitude	0.3V
HD3	−89dB
Power consumption	8.8mW



DC Gain	52dB
Diff. Input Amplitude	0.3V
Diff. Output Amplitude	0.3V
HD3	−60dB
Power consumption	622µW

Current-steering DACs

- 2 360-μA P-type gain-boosted current sources
- 15 N-type regulated-cascode current cells

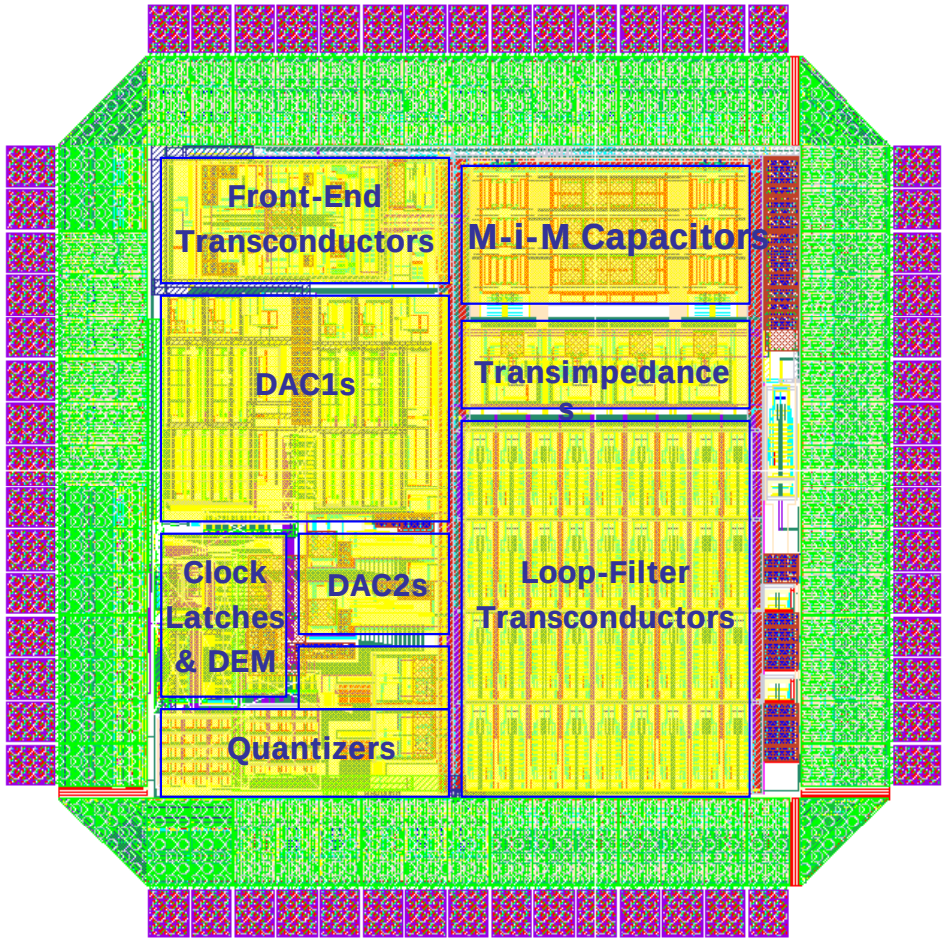


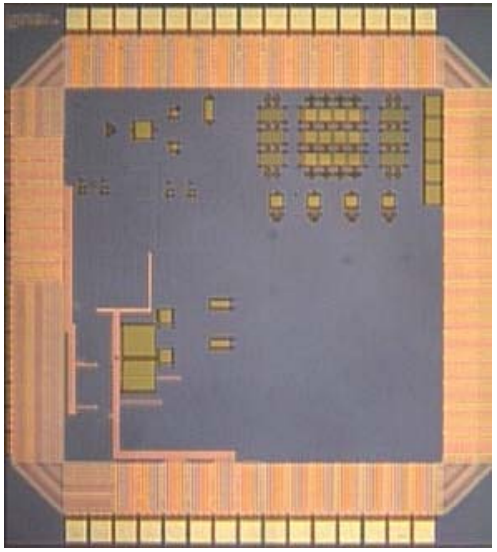
Worst-Case Transistor-level performance

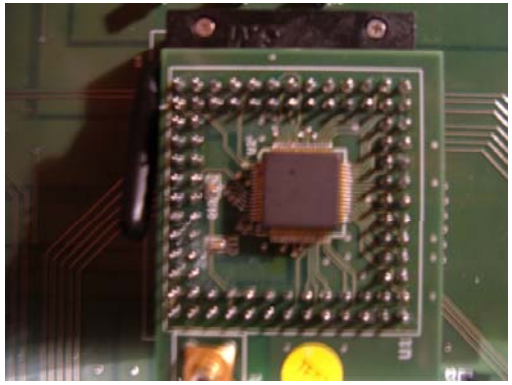
Parameter	P-type cell	N-type cell
Output Impedance	2MΩ	12MΩ
Unitary current	360μA	48μA
Current Std Deviation	0.57%LSB	
Settling Time	--	430ps
Power Cons. (mW)	0.49mW	0.1mW

CT-ΣΔMs : Case studies

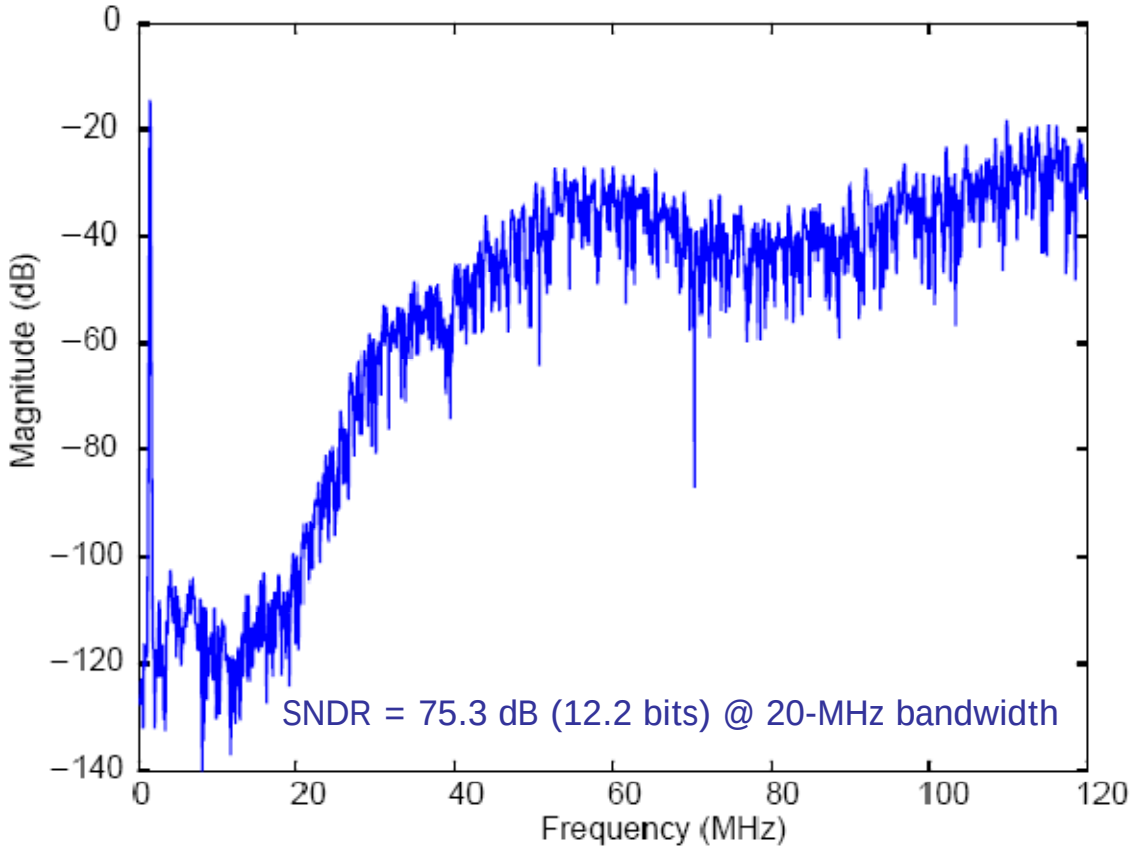
- Chip implementation





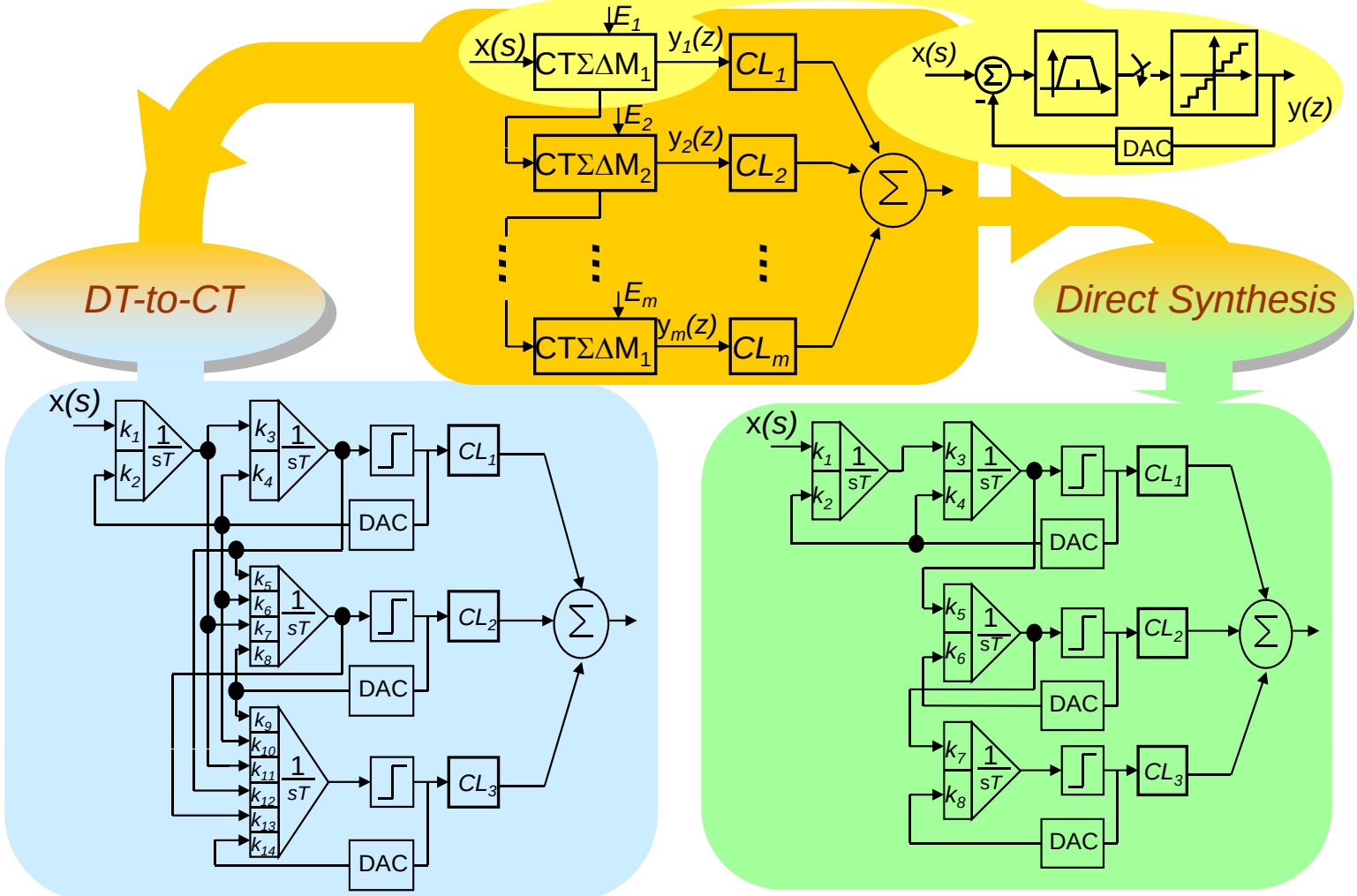


- Transistor-level simulation results



CT-ΣΔMs : Case studies

- A case study: A 1.2-V 13-bit@20MHz, 4-b, 2-2-1 CT ΣΔM



❒ Jitter optimization

Input-dependent Term

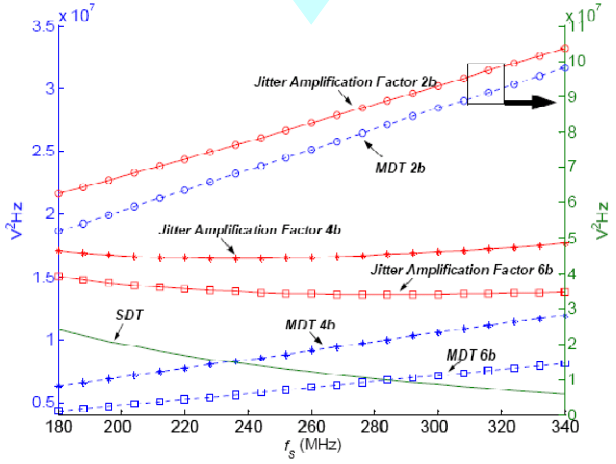
$$SDT = \frac{A^2 \omega_i^2}{f_s}$$

$$MDT = \frac{A_{FS}^2 f_s}{3(2^B - 1)^2} \psi(\bar{g}, \bar{p}, \bar{\lambda}, L)$$

$$SNR_{jitter} = 10\log \frac{A^2}{2B_w(\sigma_{\Delta T})^2 \left[\frac{A^2 \omega_i^2}{f_s} + \frac{X_{FS}^2 \cdot f_s}{3(2^B - 1)^2} \psi(\bar{g}, \bar{p}, \bar{\lambda}, L) \right]}$$

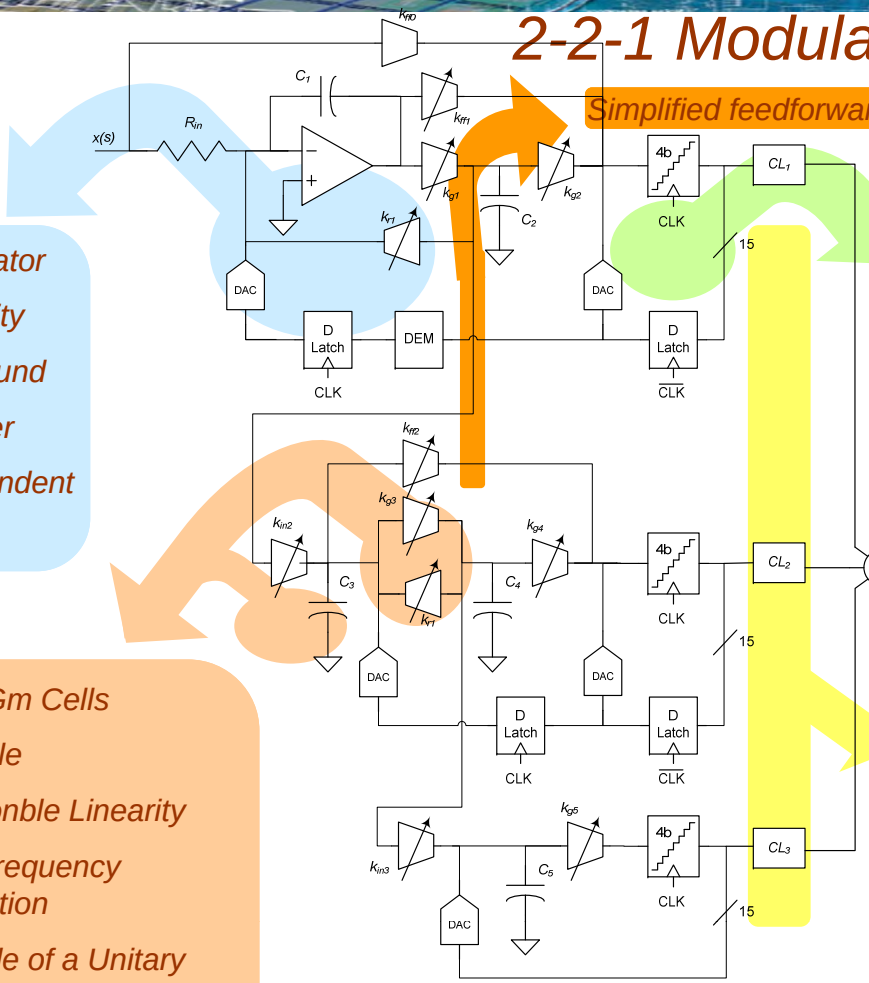
$$\psi(\bar{g}, \bar{p}, \bar{\lambda}, L) = 1 - \bar{g}^T \cdot \bar{p} + \sum_{k=1}^{L} \sum_{j=1}^{L} g_k p_k g_j p_j \frac{\lambda_k^{-1} - \lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}}$$

Filter-dependent Term



CT-ΣΔMs : Case studies

2-2-1 Modulator



RC-Amp Integrator

- ✓ *High linearity*
- ✓ *Virtual ground*
- ✖ *High Power*
- ✖ *GBW dependent delay*

4b Quantizers

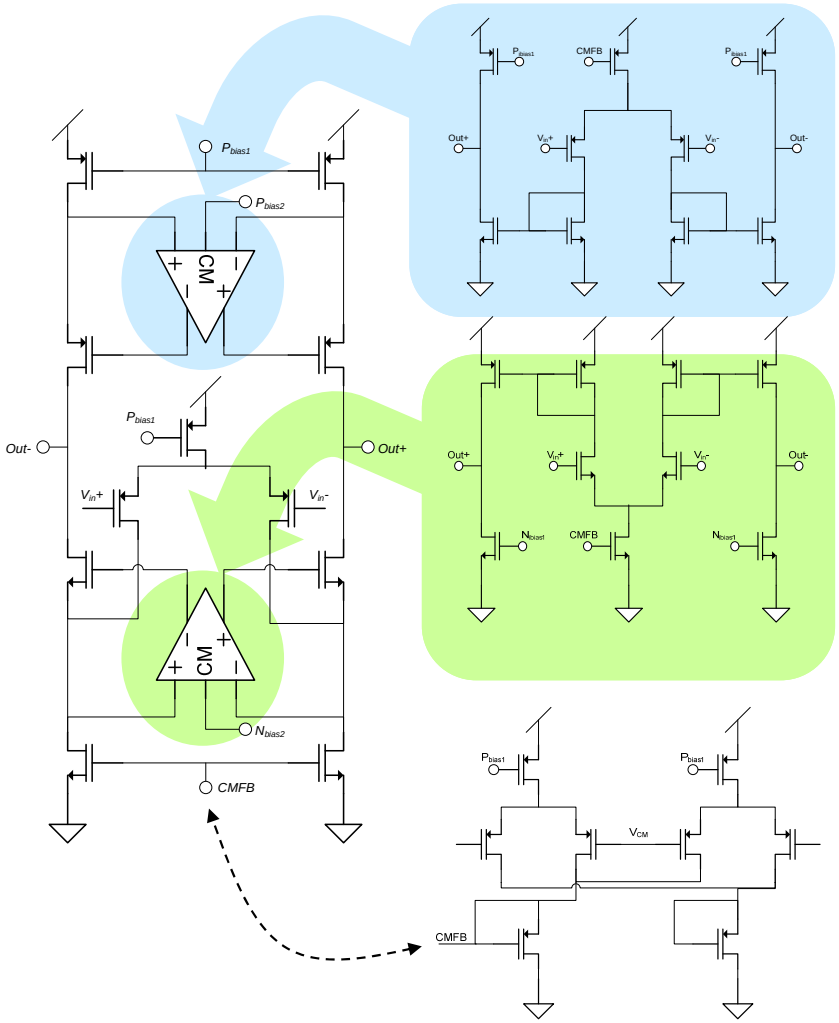
- • *NRZ scheme*
- ✓ *Low jitter sensitivity*
- ✓ *Optimized combination of number of bits, fs, and signal bandwidth*

Gm Cells

- ✓ *Tunable*
- ✓ *Reasonble Linearity*
- ✓ *High frequency Operation*
- ✓ *Multiple of a Unitary Transconductor*
- ✖ *Low Output Impedance*

Optimum Cancellation Logic

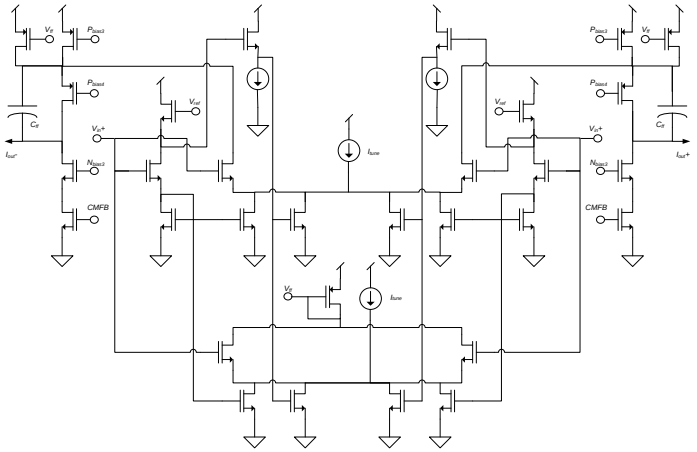
- ✓ *Sinthesized taking into acount inter-stage continuous-time integrating paths*

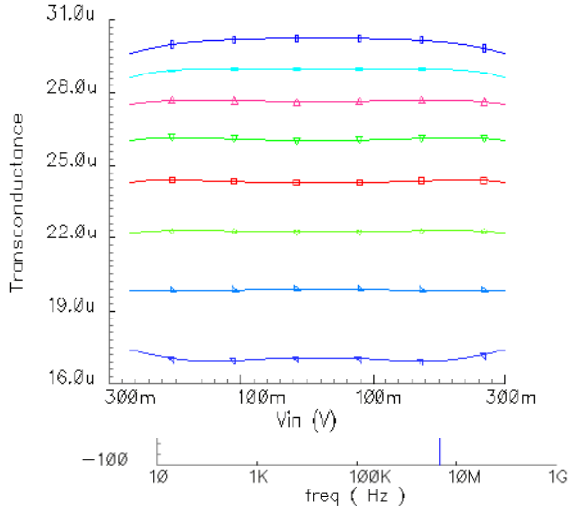


Input OpAmp

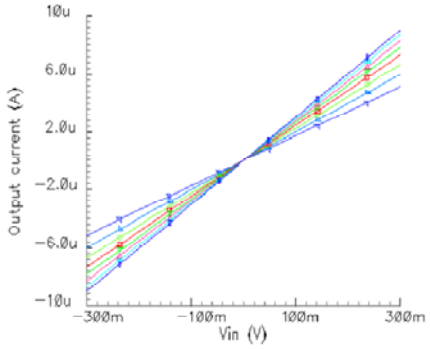
Amplifier Characteristics	
GB	600MHz
DC Gain	71dB
Phase Margin	80º
Parasitic Input Capacitance	0.36pF
Parasitic Output Capacitance	0.4pF
Differential Output Swing	0.7V
Power Consumption	20mW

Unitary Transconductor



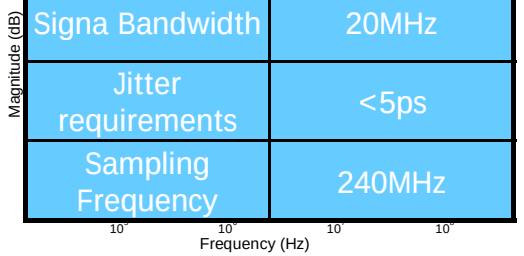


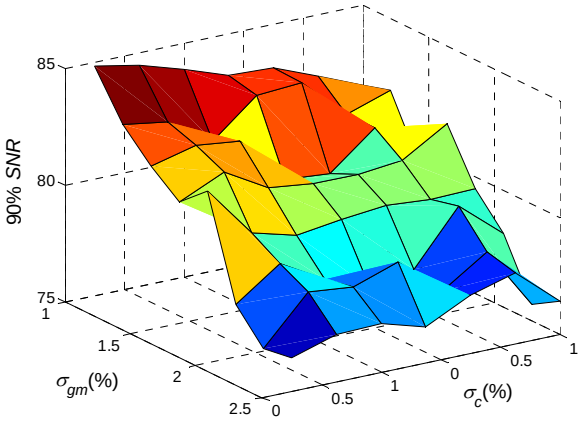
Transcoductor Characteristics	
DC Gain	58dB
Diff. Input Amp.	0.3V
Diff. Output Amp.	0.3V
HD3	-57dB
σ_{gm}/g_m	<1.5%
Power	350μW

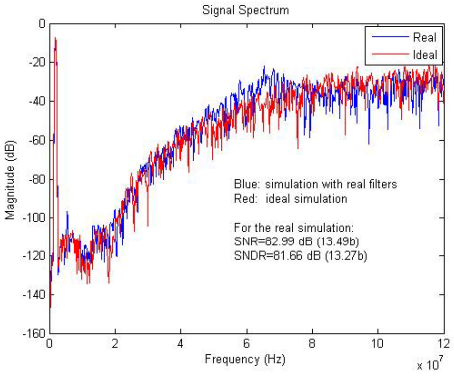


Simulation Results

SNDR	80dB
Power	65mW
Minimum SNDR due to mismatch	77dB
Signa Bandwidth	20MHz
Jitter requirements	<5ps
Sampling Frequency	240MHz







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