CMOS Sigma-Delta Converters - From Basics to State-of-the-Art

Circuits and Errors

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CT-ΣΔMs: Overview of CT-ΣΔM non-idealities

CT-ΣΔM Non-Idealities

Building-block Errors
- Opamp finite (non-linear) DC gain
- Integrator transient response
- Element tolerances
- Time-constant error
- Non-linearity (Front-end V-I and DAC)
- Noise

Architectural Timing Errors
- Quantizer metastability
- Excess loop delay
- Clock jitter
**Basic building blocks – CT Integrators**

- **Active-RC**

\[
\tau = RC
\]

\[
H(s) = \frac{1}{s\tau}
\]

- **MOSFET-C**

\[
\tau = R_{ch}C
\]

- **Gm-C**

\[
\tau = \frac{C}{g_m}
\]

- **Gm-MC**

\[
\tau = \frac{C}{g_m}
\]

**A Gm-MC implementation**

- 2nd-order single-loop \(\Sigma \Delta M\)
- 1-bit switched-current DAC
- 1-bit (latch) comparator
Integrator Transfer Function (ITF) degraded by circuit non-idealities

\[ Y(s) = \frac{1}{\tau \cdot s} X(s) \rightarrow Y(s) = \left[ \frac{1}{\xi \cdot \tau \cdot s} T_{\varepsilon_H}(s) \right] X(s) \]

- Ideal Transfer Characteristics
- First-Order Actual Transfer Characteristics

First-Order Non-Ideal Integrator Behaviours:
- Deviations in the Unity Gain Frequency \( \varepsilon_\tau \)
- Low-Frequency Pole \( \omega_{pl} \) Due to Losses
  - Produce Finite DC Gain
  - Magnitude Errors for \( \omega >> \omega_{pl} \)
  - Phase Errors for \( \omega >> \omega_{pl} \)
- High-Frequency Poles and Zeros \( T_{\varepsilon_H}(s) \)
- Phase Errors for \( \omega << \omega_{pl}, \omega_{z} \) ...
Opamp finite DC gain (1)

<table>
<thead>
<tr>
<th>RC</th>
<th>MOSFET-C</th>
<th>Gm-C</th>
<th>Gm-MC</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ \omega_{pl} &lt; \frac{G_{ch}}{C \cdot A_0} = \frac{\omega_u}{A_0} ]</td>
<td>[ \omega_{pl} &lt; \frac{G_{ch}}{C \cdot A_0} = \frac{\omega_u}{A_0} ]</td>
<td>[ \omega_{pl} = \frac{\omega_u G_{go}}{C \cdot A_0} ]</td>
<td>[ \omega_{pl} &lt; \frac{G_{go}}{C \cdot A_0} = \frac{\omega_u G_{go}}{A_0 C_m} ]</td>
</tr>
</tbody>
</table>

RC integrators [Gerf03]

\[ \text{ITF}(s) = \frac{\alpha / \tau}{s + \gamma} \]
\[ \alpha = \frac{A_0}{1 + A_0} \]
\[ \gamma = \frac{1 / \tau}{1 + A_0} \]

- Same IBN degradation as in SC ΣΔMs

\[ \tau = \frac{1}{f_s} \]

\[ \begin{align*}
P_{A_0} &= \frac{\Delta^2}{12k_1^2k_2^2} \left[ \frac{1}{A_0^{2L}} \sum_{m=1}^{\infty} \frac{\pi^2 L(L-1) \ldots (L-m+1)}{(2m+1)(2m+1)^{2L-1}} \frac{1}{A_0^{2(L-m)} m!} \right]
\end{align*} \]
Opamp finite DC gain (II) - Gm-C integrators

Power Spectral Density of an \( L \)-th order \( \Sigma \Delta M \)

\[
S_Q(f) = \left| \sum_{i=0}^{L-1} \left( \frac{j \omega}{\omega_p f_i} \right)^i \right|^2 \frac{\Delta^2}{12 \cdot A_{dc}^{2L} f_s}
\]

Relative increase of \( P_Q \) in a 2nd-order \( \Sigma \Delta M \)

\[
\frac{P_Q}{P_Q|_{A_{dc} \to \infty}} \approx \frac{5}{\pi^2} \left( \frac{M}{A_{dc}} \right)^4 + \frac{10}{3 \pi^2} \left( \frac{M}{A_{dc}} \right)^2 + 1
\]

\( f_s = 20 \text{MHz} \)
\( M = 64 \)
**CT-ΣΔMs: Integrator transient response**

- Integrator transient response (1)
  - Less critical than in DT ΣΔMs
  - Need to be taken into account, specially in broadband applications

- Influence of $GBW$ [Gerf03]

\[
P_{GBW} = \frac{\Delta^2}{12k_2k_2^2} \left[ \frac{2L^2 - 1}{(2L + 1)M^2 + 1} \left( 1 + \frac{k_1/\tau}{GBW_1} \right)^2 \prod_{i=2}^{L} \left( 1 + \frac{1}{GBW_i \cdot \tau} \right)^2 \right]
\]

- Other dynamic effects
  - 2nd-order poles
  - Slew-rate

- Simulation-based study [Ruiz03]
Model of GBW for RC-active based CT-$\Sigma\Delta$Ms [Ortm04]

- Modeled as a gain error (GE) and extra loop delay
- Each delay is different for each feedback path

$$\tau_{D1st} = \frac{1 - e^{-\omega_2/f_s}}{\omega_2} \quad \tau_{D2nd} = \frac{\omega_1^2(1 - e^{-\omega_2/f_s}) - \omega_2^2(1 - e^{-\omega_1/f_s})}{\omega_1\omega_2(\omega_1 - \omega_2)}$$
Element tolerances

- Scaling coefficients accuracy limited by random errors in resistors/capacitors
  \[ \frac{\Delta \tau}{\tau} = \frac{\Delta C}{C} - \frac{\Delta g_m}{g_m} \Rightarrow \sigma_\tau = \sqrt{\sigma_C^2 + \sigma_{g_m}^2} \]

- Especially critical in:
  - High-order single-loop architectures (instability)
  - Cascade architectures (analog/digital coefficient ratios)
- Two types of random errors:
  - Absolute tolerances: variations from chip to chip (10-20%)
  - Relative mismatches: variations from device to device on one chip (0.5-1%)

- Electrical control of frequency tuning

- System-level optimization and synthesis method
Direct synthesis method of CT cascade architectures [Tort06]:

- Optimum placement of poles/zeroes of the NTF
- Synthesis of both analog and digital part of the cascade CT ΣΔ Modulator
- Reduced number of analog components
- Reduced sensitivity to element tolerances
Direct synthesis of cascade architectures (I) [Tort06]

- Sensitivity to mismatch (\(gm,C\))
- A 2-1-1 example

![Diagram showing sensitivity to mismatch and SNR Loss](image-url)
Direct synthesis of cascade architectures (II) [Tort06]

\[
E_o(z) = \sum_{k=1}^{m} y_k(z) CL_k(z)
\]

\[
E_k(z) + \sum_{i=1}^{k-1} Z_{ik} y_i(z)
\]

\[
y_k(z) = \frac{i=1}{1 - Z_{kk}}
\]

\[
CL_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{mm}}
\]

\[
Z_{km} = Z \left( L^{-1} \left( H_D F_{km} \right) \bigg| _{nT_s} \right)
\]
Synthesized cascaded CT SDMs to cope with 12-bit@20-MHz
A case study: A 12-bit@20MHz, 4-b, 2-1-1 CT $\Sigma$ΔM (RC/Gm Integrators)

Parameter | Value
---|---
$R_{in}$, $R_f$ | 1kΩ
$R_f$ | 2.9kΩ
$k_{g2}$, $k_{g5}$ | 50μA/V
$k_{g3}$ | 500μA/V
$k_{ff}$ | 120μA/V
$k_{m2}$, ..., $k_{m4}$, $k_{fb2}$, ..., $k_{fb4}$ | 450μA/V
$C_1$ | 7.5pF
$C_2$ ..., $C_5$ | 1.875pF
**Integrator time-constant error (I)**

\[ |TF(s)| = \frac{A_o}{1 + sC(1 + \varepsilon_t)/g_0} \]

- \( \varepsilon_t = C_{\rho}/C \)

**CT-ΣΔMs : Integrator time-constant error**

- Capacitor plate parasitic capacitances
- Parasitic capacitances of the inter-connection lines
- Parasitic input capacitances of the circuits connected to the node
- Parasitic output capacitances of the circuits connected to the node

<table>
<thead>
<tr>
<th>RC ( \varepsilon_t )</th>
<th>MOSFET-C ( \varepsilon_t )</th>
<th>Gm-C ( \varepsilon_t )</th>
<th>Gm-MC ( \varepsilon_t )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 + ( \frac{G}{C \cdot A_0 \cdot \omega_a} ) + ( \frac{C + C_T}{C \cdot A_0} )</td>
<td>1 + ( \frac{G_{ch}}{C \cdot A_0 \cdot \omega_a} ) + ( \frac{C + C_T}{C \cdot A_0} )</td>
<td>1 + ( \frac{C_T}{C} )</td>
<td>1 + ( \frac{G_{go}}{C \cdot A_0 \cdot \omega_a} ) + ( \frac{C + C_T}{C \cdot A_0} )</td>
</tr>
</tbody>
</table>
Integrator time-constant error (II)

\[
\Delta P_{Q_{\Delta o}^{\ast r}} \mid_{\text{dB}} = \begin{cases} 
\frac{3M^2}{\pi^2} \cdot \frac{1}{A_o^2} + (1 + \varepsilon_{\tau})^2 & \text{(1st-order modulator)} \\
(1 + \varepsilon_{\tau})^2 + \frac{10}{3\pi^2} \cdot \frac{(1 + \varepsilon_{\tau})^2}{A_o^2} M^2 + \frac{5}{\pi^4 A_o^4} M^4 & \text{(2nd-order modulator)}
\end{cases}
\]

Optimum SNR for:
\[
\tau = \frac{1}{f_s}
\]
Causes of Non-linearity

- Intrinsic non-linearity of the resistor material
- Modulation of thickness of the conductive layer with resistor voltage

V-I transformation in RC integrators

\[ I = R_0^{-1} \cdot V \]

\[ g_{NL}(V) = R_0^{-1} \left\{ a_2 \cdot V^2 + a_3 \cdot V^3 + o(V) \right\} \]

V-I transformation in Gm-C integrators

\[ V_{in} = V_{iA} - V_{iB} \]

\[ I_0 = I_{1A} - I_{1B} \]

Normalized Large Signal Characteristic

\[ \kappa(V) = \begin{cases} 
-1 & v \leq -\sqrt{2} \\
\frac{1}{\sqrt{1-(V/2)^2}} & |V| \leq \sqrt{2} \\
1 & v \geq \sqrt{2} 
\end{cases} \]

\[ G_{m0} = \frac{2B_1B}{n} \]

\[ V_{in} = \frac{G_{m0}}{2B_1B} \]
Effect on Non-linearity in Gm-C CT-ΣΔMs [Bree01]

\[ i(v) = \beta v \sqrt{2IB/\beta} - v \approx \sum_{k=1}^{\infty} g_{m_k} v^k \]

\[ THD \approx HD_3 \approx \frac{g_{m_3} v^2}{g_{m_1}} \]

\[ i(v) \approx g_{m_1} v + g_{m_3} v^3 \]

Linearization strategies

Source Degeneration of Basic Differential Pairs

Exploiting the Ohmic Region of MOSTs

MOST Saturated Transconductors
- Functional cancellation
- Square-law functions combination

\[ I_d = 2\beta(v_1 - v_2) \left( v_1 - v_{T0} \right) - \frac{3}{2}(v_1 + v_2) \]
CT-ΣΔMs: Nonlinearities and noise

- **Typical Nonlinear-Tolerant Architecture**
  - RC-active front-end integrator
  - Gm-C subsequent integrators

- **Other sources of non-linearity**
  - Multi-bit DACs
  - Linearity must be the same or lower than the required resolution
  - Corrected by same techniques as those employed in SC ΣΔMs
    - DEM
    - Calibration

- **Circuit noise**
  - Dominated by noise sources from the front-end integrator and DAC
  - Flicker noise reduced by proper sizing and/or chopper techniques
  - Unsampled noise – effect of sampling reduced by the loop gain

\[ P_{th} \approx \frac{KT}{4C} \frac{\pi^2L}{(2L+1)M^2L+1} \]
CT-ΣΔMs: Comparator metastability

Signal-dependent Delay

Can be cancelled by using additional latches [Dagh04]

Modeled as a jitter noise [Cher00]

\[ d_m = d_0 + \frac{d_1}{v_i} a \]
CT-ΣΔMs: Excess loop delay

- Adds additional poles to STF/NTF
- Causes instability
- Stability condition:
  - 2nd-order
    \[ \rho_d \leq \frac{g_2^2}{2g_1^2g_2} \]
  - Lth-order
    \[ \rho_d \approx \frac{1}{|H(f)|_{\text{outband}}} \]
CT-ΣΔMs: Excess loop delay - Raising Instability

\[ \frac{(\pi/2)s}{s^2 + (\pi/2)^2} \]

Resonator

Resonator

S/H

Comparator

HRZ DAC

RZ DAC

\[ g_1 \]

\[ g_2 \]

\[ g_4 \]

\[ g_2' \]

\[ g_1' \]

\[ g_4' \]

Excess loop delay

Raising Instability

\[ \tau_d \]

\[ t \]

\[ \rho_d \]

Time (\#T_s)

Relative Magnitude (dB)

Frequency / Sampling Frequency
Extra feedback paths (DACs) with tunable gains [Cher00]

Using only one additional DAC and two latches [Yan04]
Digital compensation [Font05]

- Implemented in a 3rd-order single loop architecture with 5-level quantizer
  - 90nm CMOS
  - 74-dB SNDR-peak, 600kHz bandwidth
  - 6.0mW, 1.5V

- Excess loop delay compensated in the digital domain
- Half-a-clock-cycle delay
  - Relax comparators speed
  - Provide maximum isolation between quantizer and DAC switch events
Clock jitter (I)

- S/H
  - Shaped by the modulator NTF
  - Can be neglected
- DAC
  - Directly adds with the input
  - Increases the in-band noise power

CT-ΣΔMs are more sensitive to clock jitter than DT-ΣΔMs

White noise model approximation (NRZ DAC) [Cher00][Zwan96]

- Standard deviation of jitter error: \[ \sigma_j^2 \approx \sigma_j^2 I_{DAC} \]
- SNR degradation: \[ SNR_J = 10 \log \left( \frac{1}{16MB_w^2 \sigma_j^2} \right) \] 
  \[ \frac{\sigma_{j_{CT}}}{\sigma_{j_{DT}}} = \left( \frac{\pi}{2M} \right)^2 \]
Clock Jitter (II) – White noise model approximation (NRZ/RZ DAC) [Tao99a]

Lowpass CT-ΣΔMs

\[ P_{jitter|_{RZ}} = \left( \frac{T_s}{T_0} \right)^2 P_{jitter|_{NRZ}} \]

Bandpass CT-ΣΔMs

\[
SNR_j = \begin{cases} 
10 \log \left( \frac{\text{sinc}(\pi T_s f_s)}{B_w M} \right) & \text{NRZ} \\
10 \log \left( \frac{\text{sinc}(\pi T_s f_s)}{B_w M} \right) & \text{RZ}
\end{cases}
\]

\[ \frac{\sigma_j^2_{CT}}{\sigma_j^2_{DT}} \approx 0.14 \]

\[ \Delta f_j = 0.1 \text{ns} \]

\[ f_s = 100 \text{MHz} \]

Ideal

\[ f_s = 10 \text{MHz} \]
Clock Jitter (III) – lingering effect [Olia03a]

- Jitter-induced noise includes both white and shaped components
- State-space analysis of CT-ΣΔMs with RZ DAC shows that:

\[
S_e(z) = (\sigma_e^2 T) \sum_{m_2=1}^{N} \sum_{j_2=1}^{N} \sum_{m_1=1}^{m_2-1} \sum_{j_1=1}^{m_1-1} a_{m_1} a_{m_2} z^{j_1-j_2} \times C A^{m_1-j_1-1} \Delta A^{m_2-j_2-1} \Gamma
\]

Multi-bit NRZ DACs

- Commonly used in CT-ΣΔMs for broadband telecom applications
- Less sensitive to clock jitter

- RZ DAC: \( \Delta Q(n) \simeq \Delta I_{DAC}(n) \cdot \Delta T(n) \)
- NRZ DAC: \( \Delta I_{DAC}(n) \)
Clock Jitter (IV) – Multi-bit NRZ DACs [Tort05]

\[ \varepsilon(n) = (y(n) - y(n-1)) \frac{\Delta T(n)}{T_s} \]  
[Ris94]

\[ P_e = E\{\varepsilon(n)^2\} = \frac{\sigma^2 \Delta T}{T_s^2} E\{[y(n) - y(n-1)]^2\} \]

- Using state-space formulation of NTF:

\[ P_e = \frac{\sigma^2 \Delta T}{T_s^2} \left( \frac{T_s A^2 \omega_{BR}^2}{2} + \frac{\chi_{FS}^2}{6(2^B - 1)^2} \cdot \psi(\overline{g}, \overline{p}, \overline{\lambda}, L) \right) \]

\[ \psi(\overline{g}, \overline{p}, \overline{\lambda}, L) = 1 - \overline{g} \cdot \overline{p} + \sum_{k=1}^{L} \sum_{j=1}^{L} \frac{\lambda_k^{-1} - \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}} \psi(g_k, p_j, \overline{g}, \overline{p}, \overline{\lambda}, L) \]

\[ SNR_{jitter} = \frac{A^2}{2 \cdot P_e\text{band}} = \frac{A^2}{2 \cdot B_w \cdot (\sigma_{\Delta T})^2} \cdot \left[ \frac{A^2 \omega_i^2}{f_z} + \frac{\chi_{FS}^2 \cdot f_z}{3(2^B - 1)^2} \psi(\overline{g}, \overline{p}, \overline{\lambda}, L) \right] \]
Clock Jitter (V): Comparison of [Tort05] with previous approaches

Assuming that SNR jitter is dominated by the signal-dependent term:

- If the modulator-dependent term dominates (single-bit quantization):
  - [Boser, JSSC, 1988]

- If the clock jitter error dominates (single-bit quantization):
  - [Zwan96]
  - [Hern04]

2nd-order single-bit

Quantization error-dominated

Jitter-dominated

This work
Clock Jitter (V) – Multi-bit NRZ DACs [Tort05]

Two cases:

- CTΣΔM1: $B=2$ bit, $f_s=400$ MHz
- CTΣΔM2: $B=5$ bit, $f_s=160$ MHz
Clock Jitter (VI) – Compensation techniques

- Multi-bit quantization (non-linear DAC)
- Switched-capacitor DAC [Veld03]
  - Voltage-mode operation (proper for active RC integrators)
  - Slower than switched-current (current steering) DAC
- FIRDAC to generate a multilevel signal [Putt04]
A case study: A Gm-C 12-bit@20MHz, 4-b, 3-2 CT ΣΔM

- 130nm mixed-signal CMOS, 1P8M
- Cascade 3-2 multi-bit (4b) CT ΣΔM
- Gm-C loop-filter implementation
- Current-steering feedback DACs + DEM
- 12-bit effective resolution
- 40MS/s output rate (20MHz bandwidth)
- 240MHz clock frequency
- 1.2V ± 10% analog/digital power supply
- On-chip tuning of analog components
- Estimated power consumption is 45mW

### Loop-filter coefficients

<table>
<thead>
<tr>
<th>Coefficient</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_u$</td>
<td>3.65 pF</td>
</tr>
<tr>
<td>$k_u$</td>
<td>100 μA/V</td>
</tr>
<tr>
<td>$C_1 = C_2 = C_3 = C_4 = C_5 = 2C_u$</td>
<td></td>
</tr>
<tr>
<td>$k_{m1} = 852 \mu A/V$</td>
<td></td>
</tr>
<tr>
<td>$k_{f0} = 2k_u, k_{f1} = 4k_u, k_{f2} = 2k_u, k_{f3} = 5k_u$</td>
<td></td>
</tr>
<tr>
<td>$k_{g1} = k_{g5} = 3k_u, k_{g2} = 5k_u, k_{g3} = k_u$</td>
<td></td>
</tr>
<tr>
<td>$k_{g4} = 7k_u$</td>
<td></td>
</tr>
<tr>
<td>$k_{in2} = 5k_u, k_{fb2} = 6k_u$</td>
<td></td>
</tr>
<tr>
<td>$k_{r1} = k_{r2} = k_u$</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Finite output impedance</th>
<th>12MOΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Settling Time</td>
<td>500ps</td>
</tr>
</tbody>
</table>
CT-ΣΔMs: Case studies

- Resistive source degenerated front-end transconductor
- Loop-filter transconductors based on quadratic term cancellation

Transistor-level performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>78.3 dB</td>
</tr>
<tr>
<td>Diff. Input Amplitude</td>
<td>0.3 V</td>
</tr>
<tr>
<td>Diff. Output Amplitude</td>
<td>0.3 V</td>
</tr>
<tr>
<td>HD3</td>
<td>-89 dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>8.8 mW</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>52 dB</td>
</tr>
<tr>
<td>Diff. Input Amplitude</td>
<td>0.3 V</td>
</tr>
<tr>
<td>Diff. Output Amplitude</td>
<td>0.3 V</td>
</tr>
<tr>
<td>HD3</td>
<td>-60 dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>622 μW</td>
</tr>
</tbody>
</table>
Current-steering DACs

- 2 360-μA P-type gain-boosted current sources
- 15 N-type regulated-cascode current cells

Worst-Case Transistor-level performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>P-type cell</th>
<th>N-type cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Impedance</td>
<td>2MΩ</td>
<td>12MΩ</td>
</tr>
<tr>
<td>Unitary current</td>
<td>360μA</td>
<td>48μA</td>
</tr>
<tr>
<td>Current Std Deviation</td>
<td>0.57%LSB</td>
<td></td>
</tr>
<tr>
<td>Settling Time</td>
<td>--</td>
<td>430ps</td>
</tr>
<tr>
<td>Power Cons. (mW)</td>
<td>0.48mW</td>
<td>0.1mW</td>
</tr>
</tbody>
</table>
Chip implementation

- Front-End Transconductors
- M-i-M Capacitors
- DAC1s
- Transimpedance
- DAC2s
- Clock Latches & DEM
- Quantizers
- Loop-Filter Transconductors
- Quantizers

Case studies
Transistor-level simulation results

SNDR = 75.3 dB (12.2 bits) @ 20-MHz bandwidth
A case study: A 1.2-V 13-bit@20MHz, 4-b, 2-2-1 CT \( \Sigma \Delta M \)
Jitter optimization

Input-dependent Term

\[ SDT = \frac{A^2 \omega_i^2}{f_s} \]

\[ MDT = \frac{A^2 \omega_i^2}{f_s} \psi(g, \bar{p}, \bar{\lambda}, L) \]

Filter-dependent Term

\[ SNR_{jitter} = 10 \log \left( \frac{A^2}{2B_w(\sigma_{\Delta T})} \left( \frac{A^2 \omega_i^2}{f_s} + \frac{X_{FS} \cdot f_s}{3(2^B - 1)} \psi(g, \bar{p}, \bar{\lambda}, L) \right) \right) \]

\[ \psi(g, \bar{p}, \bar{\lambda}, L) = 1 - g^T \cdot \bar{p} + \sum_{k=1}^{L} \sum_{j=1}^{L} \frac{\lambda_k^{-1} - \lambda_j^{-1}}{1 - \lambda_k \lambda_j} \]

Diagram showing graphs of jitter amplification factors with axes labeled.
2-2-1 Modulator

RC-Amp Integrator
- High linearity
- Virtual ground
- High Power
- GBW dependent delay

Gm Cells
- Tunable
- Reasonable Linearity
- High frequency Operation
- Multiple of a Unitary Transconductor
- Low Output Impedance

4b Quantizers
- NRZ scheme
- Low jitter sensitivity
- Optimized combination of number of bits, fs, and signal bandwidth

OptimumCancellation Logic
- Synthesized taking into account inter-stage continuous-time integrating paths
**Input OpAmp**

**Amplifier Characteristics**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>GB</td>
<td>600MHz</td>
</tr>
<tr>
<td>DC Gain</td>
<td>71dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>80º</td>
</tr>
<tr>
<td>Parasitic Input Capacitance</td>
<td>0.36pF</td>
</tr>
<tr>
<td>Parasitic Output Capacitance</td>
<td>0.4pF</td>
</tr>
<tr>
<td>Differential Output Swing</td>
<td>0.7V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>20mW</td>
</tr>
</tbody>
</table>
Unitary Transconductor

Transconductor Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>58dB</td>
</tr>
<tr>
<td>Diff. Input Amp.</td>
<td>0.3V</td>
</tr>
<tr>
<td>Diff. Output Amp.</td>
<td>0.3V</td>
</tr>
<tr>
<td>HD3</td>
<td>-57dB</td>
</tr>
<tr>
<td>$\sigma_{gm}/g_m$</td>
<td>&lt;1.5%</td>
</tr>
<tr>
<td>Power</td>
<td>350 $\mu$W</td>
</tr>
</tbody>
</table>
Simulation Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNDR</td>
<td>80dB</td>
</tr>
<tr>
<td>Power</td>
<td>65mW</td>
</tr>
<tr>
<td>Minimum SNDR due to mismatch</td>
<td>77dB</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>20MHz</td>
</tr>
<tr>
<td>Jitter requirements</td>
<td>&lt;5ps</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>240MHz</td>
</tr>
</tbody>
</table>

SNR and Power Consumption

Jitter requirements <5ps

Sampling Frequency: 240MHz

Signal Spectrum

Blue: Simulation with real filters
Red: Ideal simulation
For the real simulation, with the optimal layout, SNDR=91.66 dB (3.2%)


