CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Basic Concepts and Architectures

Angel Rodríguez-Vázquez

CSIC

angel@imse.cnm.es

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH

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Materials in this course have been contributed by Fernando Medeiro, José M. de la Rosa, Rocío del Río, Belén Pérez-Verdú and Angel Rodríguez-Vázquez

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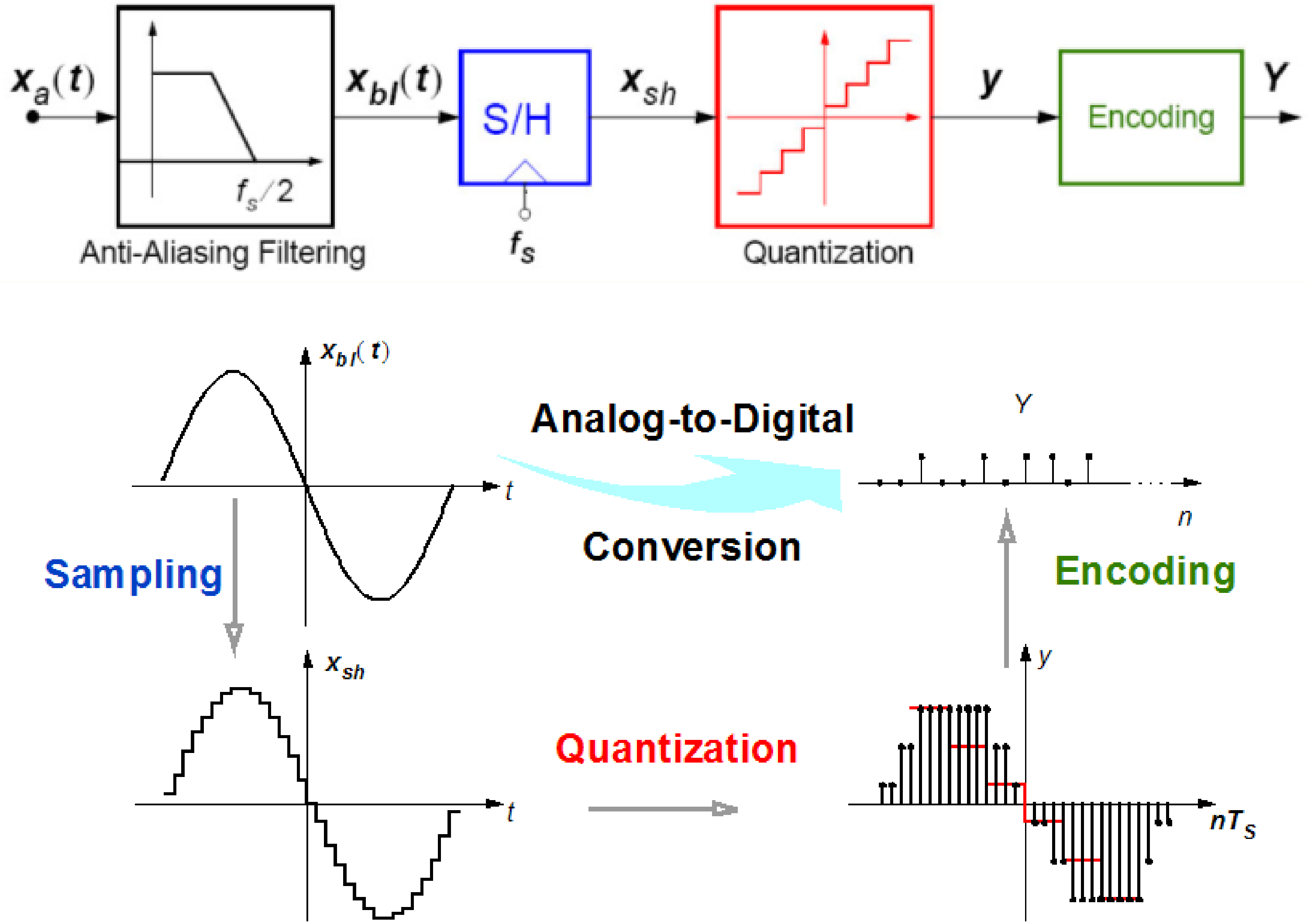
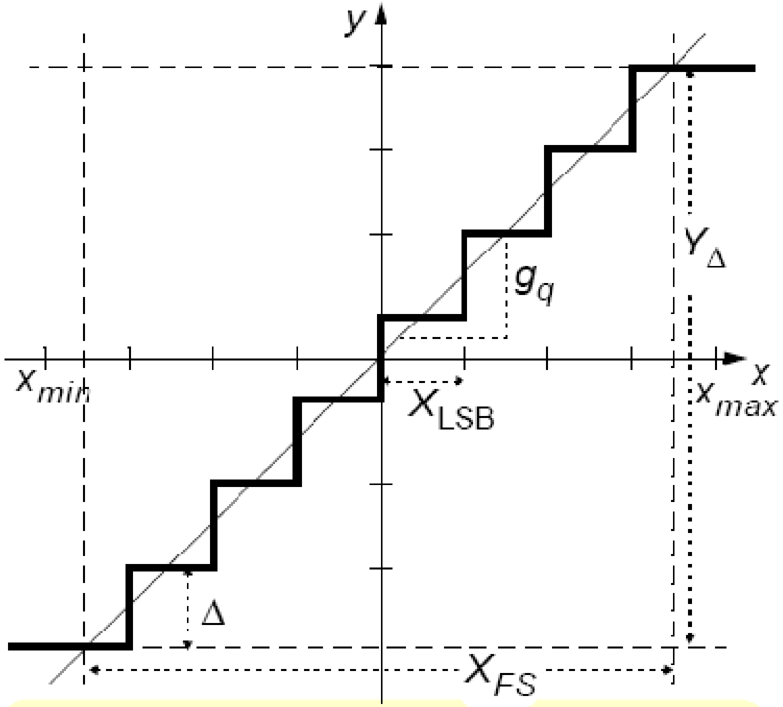
2. Fundamentals of ΣΔ ADCs
   - Oversampling
   - Quantization noise shaping
   - Basic architecture
   - Classification of ΣΔ ADCs
3. Discrete-Time ΣΔ Modulators
   - Single-bit single-quantizer architectures
   - Dual quantization
   - Multi-bit quantization
   - Bandpass ΣΔ modulators
4. Continuous-Time ΣΔ Modulators
   - Basic concepts and topologies
   - Synthesis methods

Introduction: Basic ADC Process

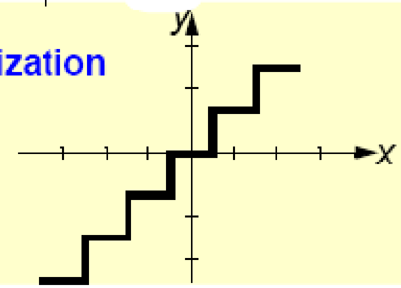


Introduction: Quantization

Midrise uniform quantization



Midtread quantization



- **Resolution (bits):**

$$B = \log_2(\#\text{ levels})$$

- **Separation between adjacent input levels:**

$$X_{\text{LSB}} = \frac{X_{\text{FS}}}{(2^B - 1)}$$

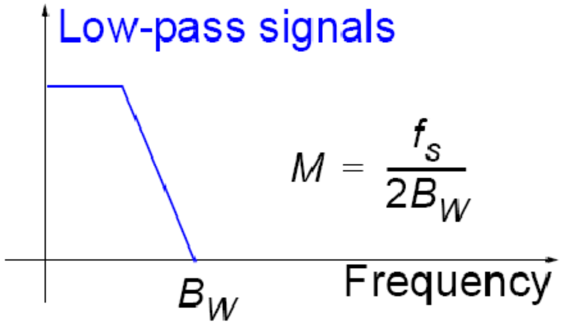
- **Separation between adjacent output levels:**

$$\Delta = \frac{Y_\Delta}{(2^B - 1)}$$

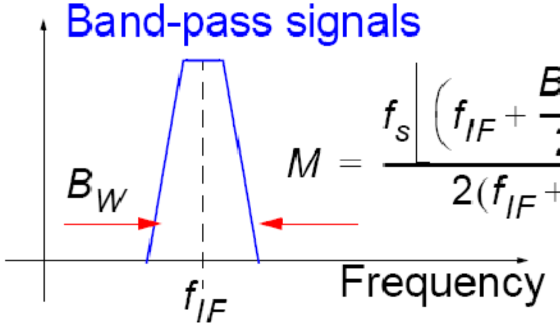
- **Full-scale input range:** X_{FS}
- **Gain:**

$$g_q = \frac{\Delta}{X_{\text{LSB}}} = \frac{Y_\Delta}{X_{FS}}$$

❒ Oversampling



$$M = \frac{f_s}{2B_W}$$

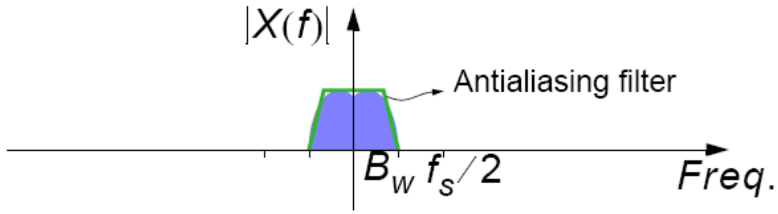


$$M = \frac{f_s \left\lfloor \left(f_{IF} + \frac{B_W}{2}\right) / B_W \right\rfloor}{2(f_{IF} + B_W)} \cong \frac{f_s}{2B_W}$$

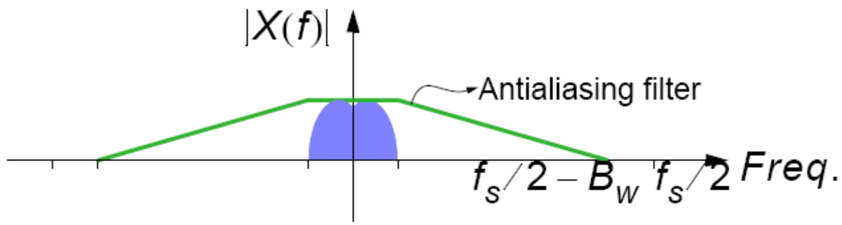
$OSR \equiv M \equiv$ Oversampling Ratio

❒ Classification of ADCs

- Nyquist-rate ADCs (*M*~1)



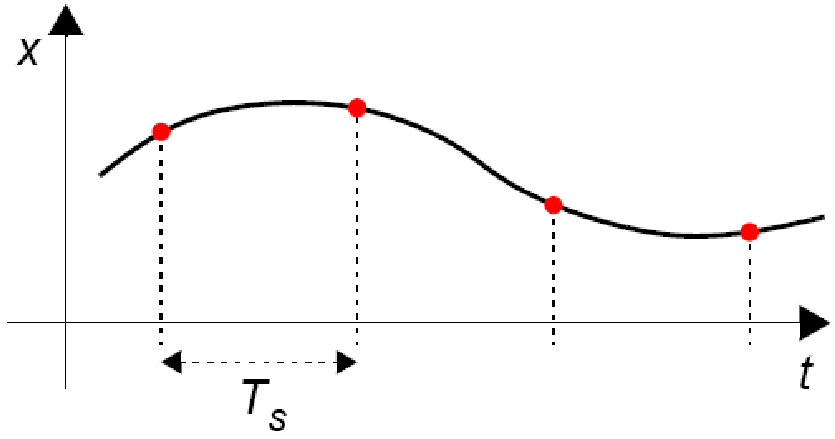
- Oversampling ADCs (*M*>>1)



Introduction: Taxonomy of ADCs

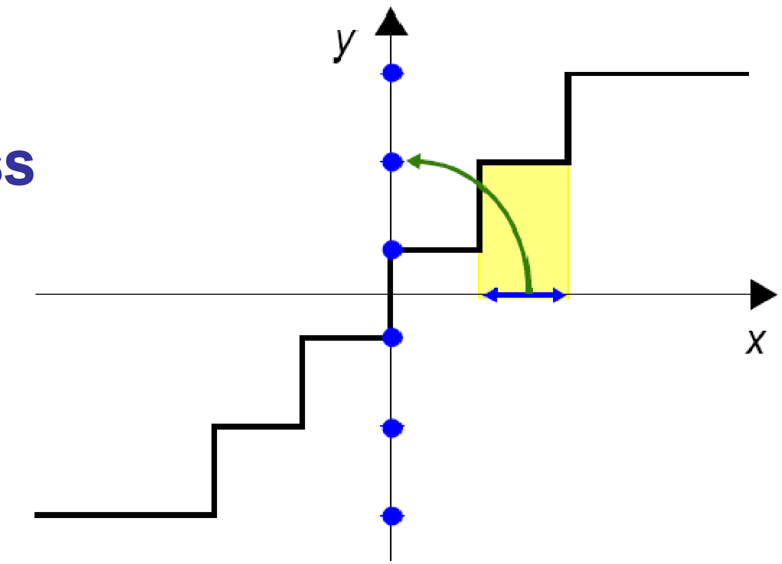
❐ Sampling process

- Limits the input signal frequency
- **Speed** of the ADC



❐ Quantization process

- Limits the input signal accuracy
- **Resolution** of the ADC



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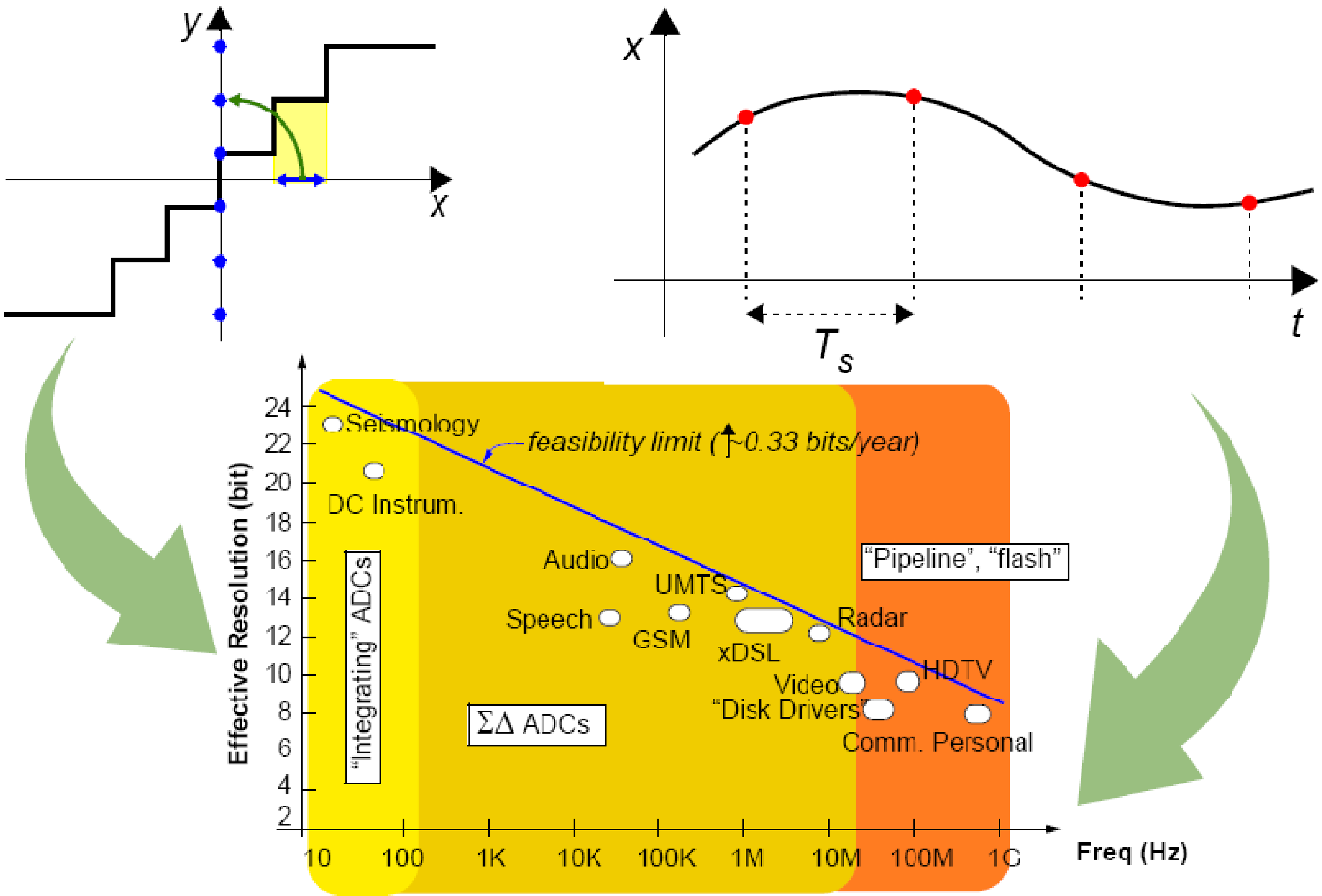
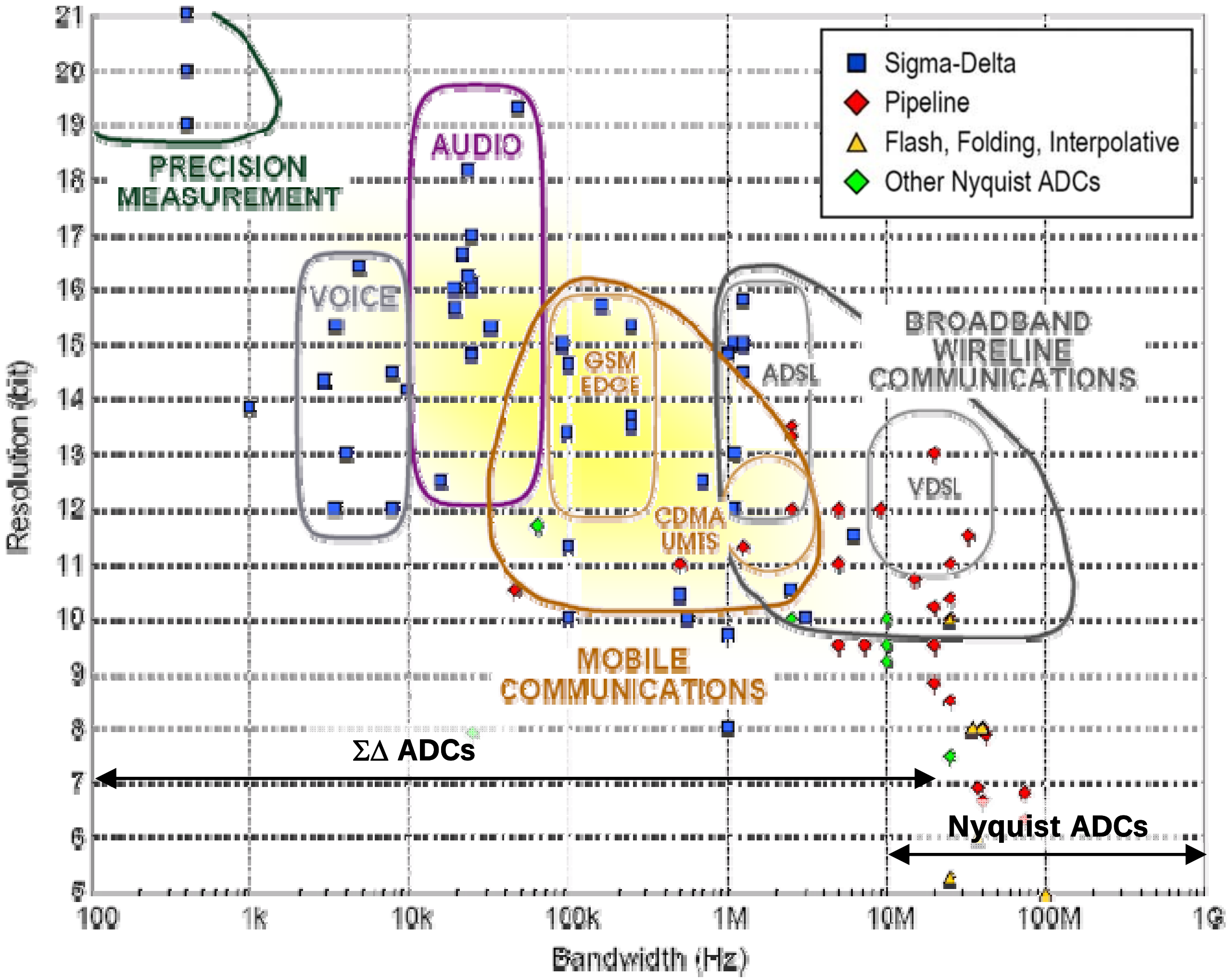


Introduction: About ADC taxonomy

Type	Resolution Number of Bits	Bandwidth	Sampling Rate	Latency	Applications
Integrating Dual-Ramp ADC	$> 16\text{bits}$	$< f_S/2$	$\rightarrow 1\text{kS/s}$	2^{N+1}cycles	DVM, Instrumentation, Sensors
Incremental ADC	$> 16\text{bits}$	$< f_S/2$	$\rightarrow 1\text{kS/s}$	2^{N}cycles	Instrumentation
Sigma-Delta Oversampled	$\sim (10\text{bits}, 18\text{bits})$	$\rightarrow 5\text{MHz}$	$\rightarrow 400\text{MS/s}$	N.A.	Sensors, Audio CODECs, XDSL, Wireless Trans., ...
Algorithmic ADC	$\sim 12\text{bits}$	$< f_S/2$	$\rightarrow 10\text{MS/s}$	$> N\text{cycles}$	Wide Range Low-power medical to telecom
Successive Approximation	$\sim 10\text{bits}$	$< f_S/2$	$\rightarrow 10\text{MS/s}$	$> N\text{cycles}$	Wide Range Low-power medical to telecom
Pipeline (*M* stages)	$\sim 10\text{bits}$	$< f_S/2$	$\rightarrow 100\text{MS/s}$	$> M\text{cycles}$	Telecom, Video
Two-Step Flash	$\sim 10\text{bits}$	$< f_S/2$	$\rightarrow 500\text{MS/s}$	$> 2\text{cycles}$	Video, Multi-Channel Base Stations
Flash Parallel	$\sim 8\text{bits}$	$< f_S/2$	$\rightarrow GS/s$	$> 1\text{cycles}$	Video

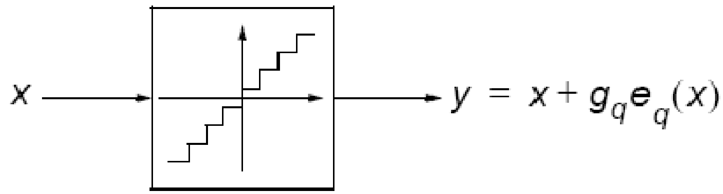
Introduction: Resolution vs. conversion rate

CMOS ADCs

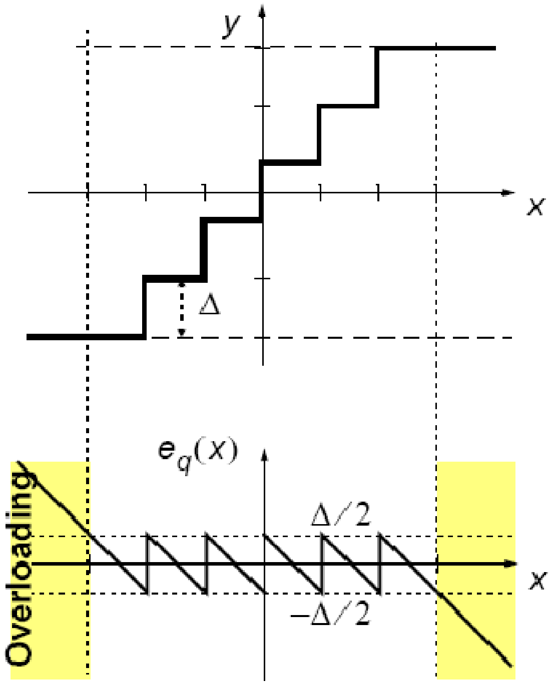


Introduction: Quantization error

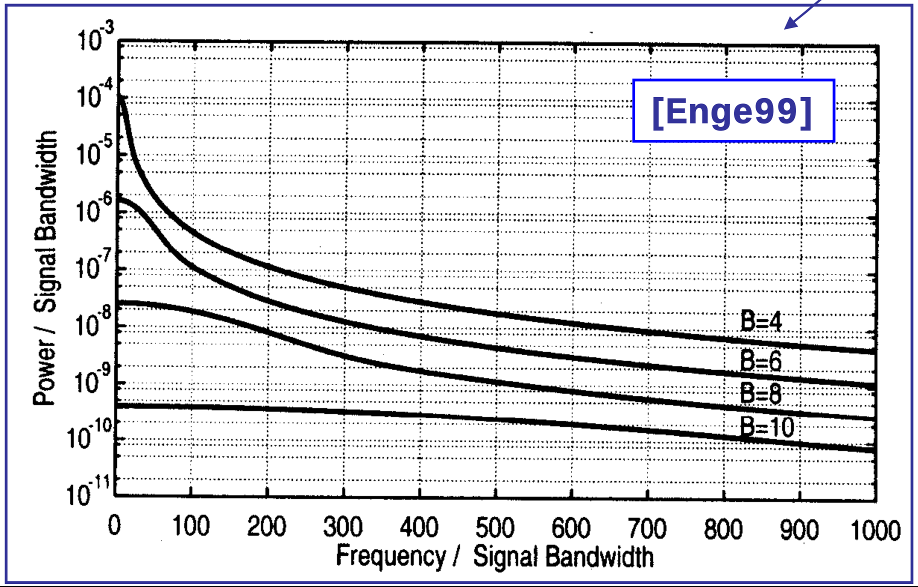
- **Quantization output-input characteristic**



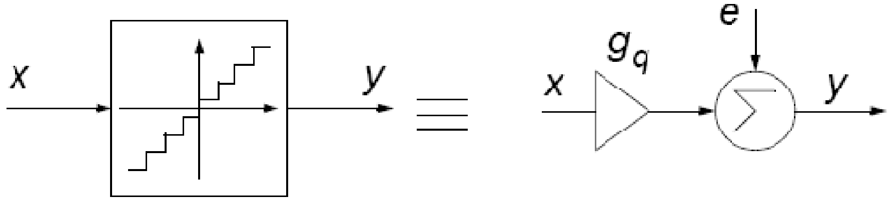
- **Quantization error**



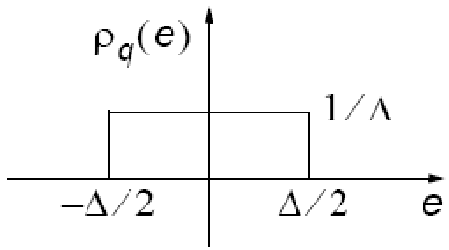
- **White noise model**
  - If x varies randomly from sample to sample
  - If the # of quantizer levels is high



Introduction: Quantization error noise model



Probability Density Function

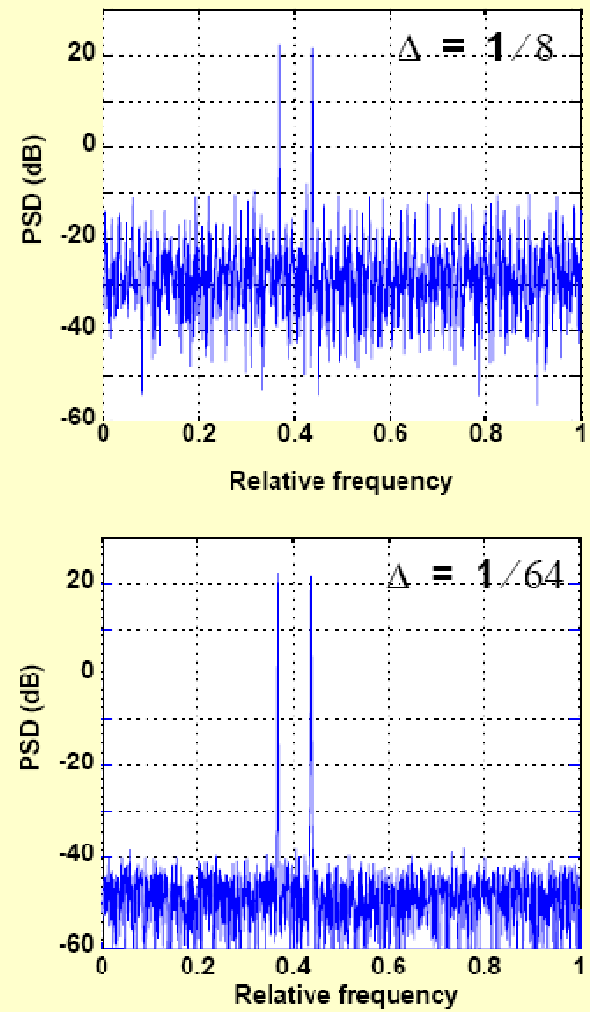


Quantization error power

$$\sigma^2(e) = \left[\frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de\right] = \frac{\Delta^2}{12}$$

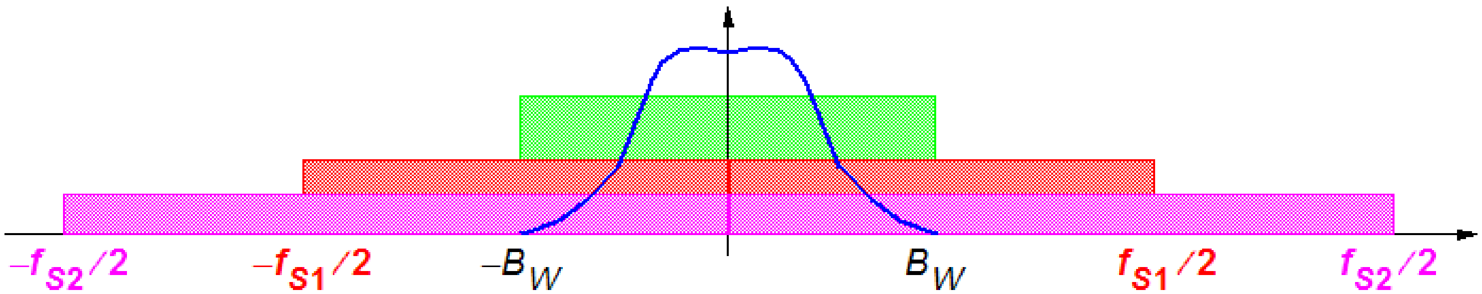
Quantization error Power Spectral Density

$$S_E(f) = \frac{\sigma^2(e)}{f_s} = \frac{\Delta^2}{12 f_s}$$



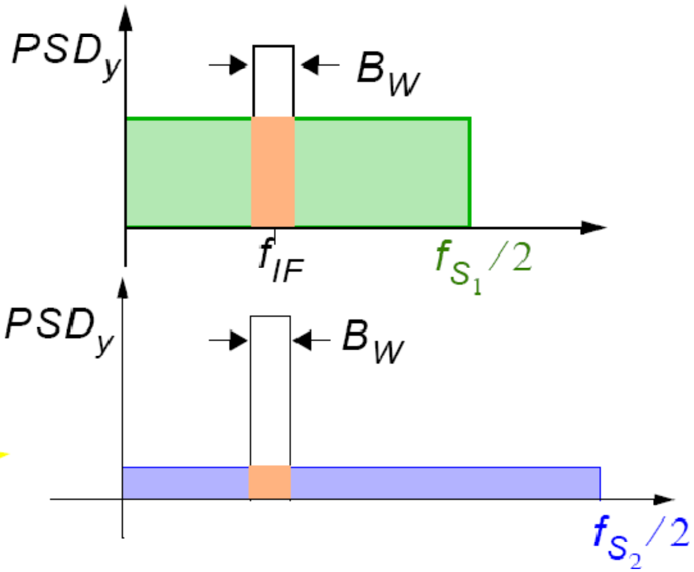
Fundamentals of ΣΔ ADCs: Oversampling

- **PSD of oversampled quantization noise**

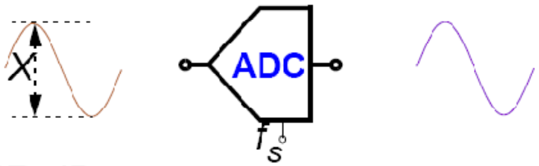


- **In-Band Noise power (IBN or P_Q)**

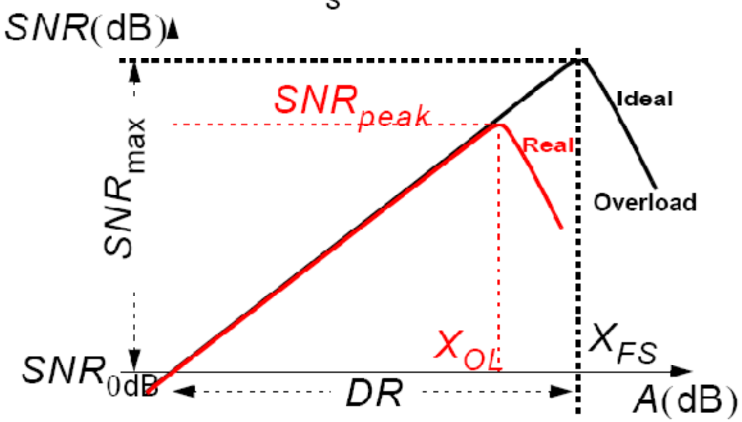
$$P_Q = \int_{f_{IF}-B_w/2}^{f_{IF}+B_w/2} 2S_E(f)df = \frac{B_w}{6f_s}\Delta^2 = \frac{\Delta^2}{12M}$$



Fundamentals of ΣΔ ADCs: Oversampling



$P_{sig} = \frac{X^2}{8}$ +  $P_Q = \frac{B_w}{6f_s}\Delta^2$



$$SNR(\mathrm{dB}) = 10\log_{10}\left(\frac{P_{sig}}{P_Q}\right) =$$

$$= 10\log_{10}\left[\frac{3}{2}M(2^B-1)^2\left(\frac{X}{X_{FS}}\right)^2\right]$$

$$SNR_{max}(\mathrm{dB}) = 10\log_{10}\left[\frac{3}{2}M(2^B-1)^2\right]$$

$$DR = 10\log_{10}\left[\frac{(X_{FS}/2)^2}{2P_Q}\right]$$

- ***N*-bit Nyquist-Rate ADC**
  - $f_{s1} = f_N \equiv 2B_w$
  - $SNR_{max} = 10\log_{10}\left[\frac{3}{2}(2^N-1)^2\right]$

- ***B*-bit Oversampled ADC**
  - $f_{s2} = Mf_N (M > 1)$
  - $SNR_{max} = 10\log_{10}\left[\frac{3}{2}M(2^B-1)^2\right]$

⇨ ***ENOB***

$$N \cong \frac{SNR_{max} - 1.76}{6.02} \cong \log_2(2^B-1) + \frac{1}{2}\log_2(M) \quad (N > 1)$$

- *SNDR / SINAD*:

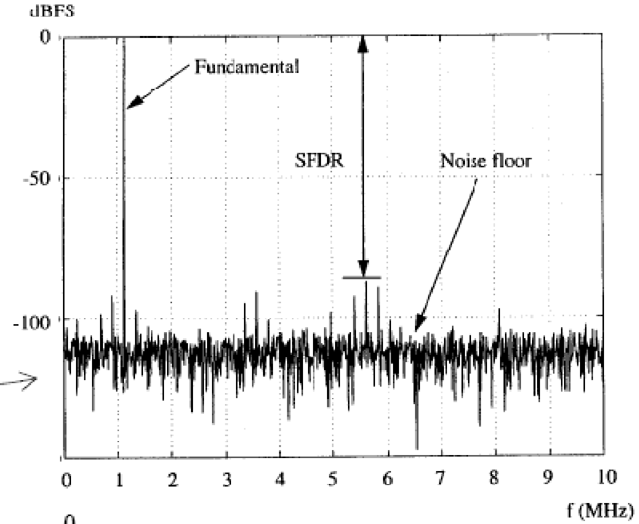
$$SNDR(\mathrm{dB}) = 10\log_{10}\left(\frac{P_{sig}}{P_Q + P_H}\right)$$

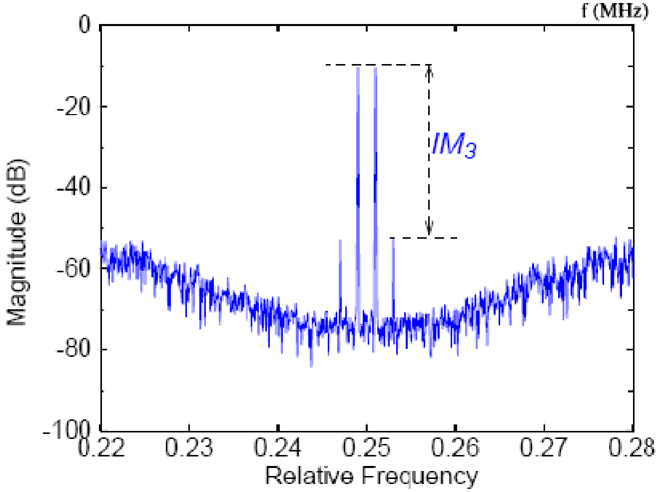
- **Effective Number Of Bits** *ENOB*:

$$ENOB \cong \frac{SNDR - 1.76}{6.02}$$

- *SFDR*: **Spurious-Free Dynamic Range**

- **Harmonic Distortion**:
  - HD_k, THD,
  - IM_3, IP_3
  - ...

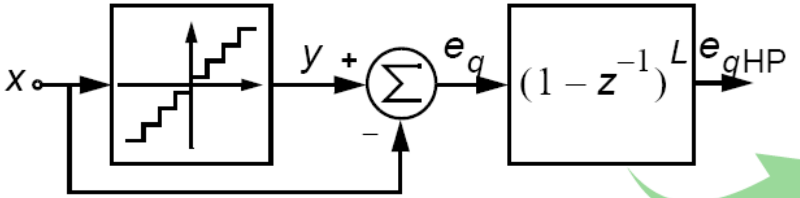




Fundamentals of SD ADCs: Quantization noise shaping

- **Processing of the quantization error**

◆ If $f_i \ll f_s$, $|e_q(n) - e_q(n-1)| \ll |e_q(n)|$



$L = 1$

$e_{qHP}(n) = e_q(n) - e_q(n-1)$

$L = 2$

$e_{qHP}(n) = e_q(n) + e_q(n-2) - 2e_q(n-1)$

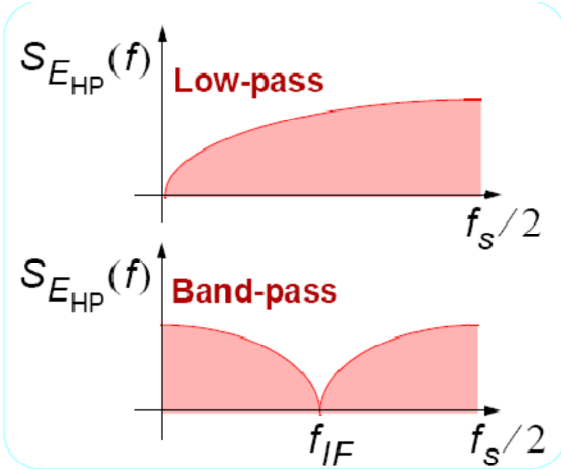
⋮ ⋮ ⋮ ⋮

- **In-band noise power and effective resolution**

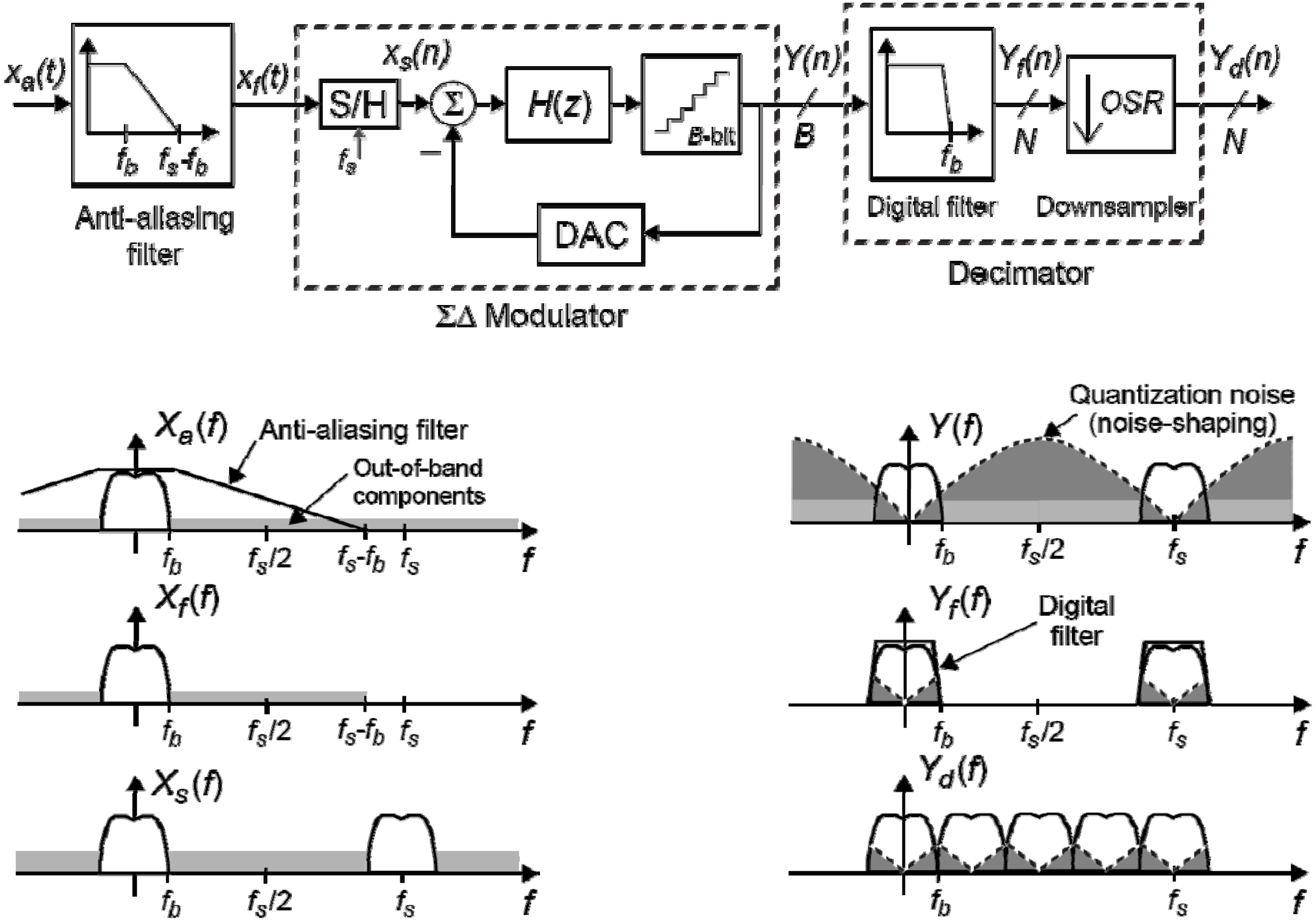
$$N_{TF}(z) = (1 - z^{-1})^L \Rightarrow S_{E_{HP}} = |N_{TF}(f)|^2 S_E$$

$$P_{E_{HP}} = \int_0^{B_w} S_{E_{HP}}(f)df \cong \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)M^{2L+1}}$$

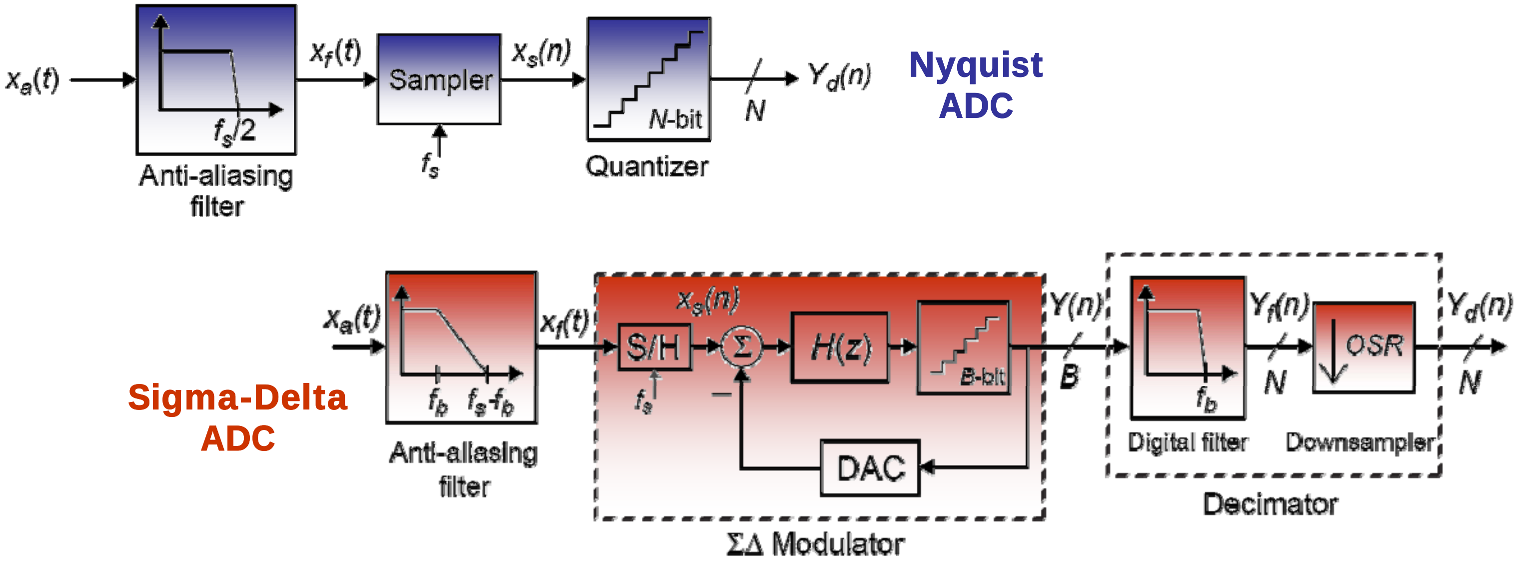
$$N \cong \log_2\left[\frac{(2^B - 1)(2L+1)}{\pi^{2L}}\right] + \left(L + \frac{1}{2}\right)\log_2(M)$$



Fundamentals of ΣΔ ADCs: Basic ΣΔ ADC architecture



Fundamentals of ΣΔ ADCs: Nyquist-rate vs. ΣΔ ADCs

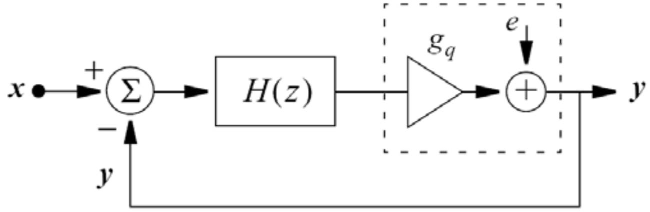


- HIGH-SELECTIVITY ANALOG FILTER for anti-aliasing
- Overall resolution obtained using HIGH-ACCURACY ANALOG BLOCKS

- LOW-SELECTIVITY ANALOG FILTER for anti-aliasing (1st/2nd order)
- High overall resolution obtained using LOW/MODERATE-ACCURACY ANALOG BLOCKS
- HIGH-SELECTIVITY DIGITAL FILTER

EASIER AND MORE ROBUST IN MODERN CMOS

Fundamentals of ΣΔ ADCs: Basic ΣΔM architecture



$$Y(z) = STF(z)X(z) + NTF(z)E(z)$$

$$STF(z) = \frac{g_q H(z)}{1 + g_q H(z)} \rightarrow STF(z) \approx 1$$

$$NTF(z) = \frac{1}{1 + g_q H(z)} \rightarrow NTF(z) \approx \frac{1}{g_q H(z)} \ll 1$$

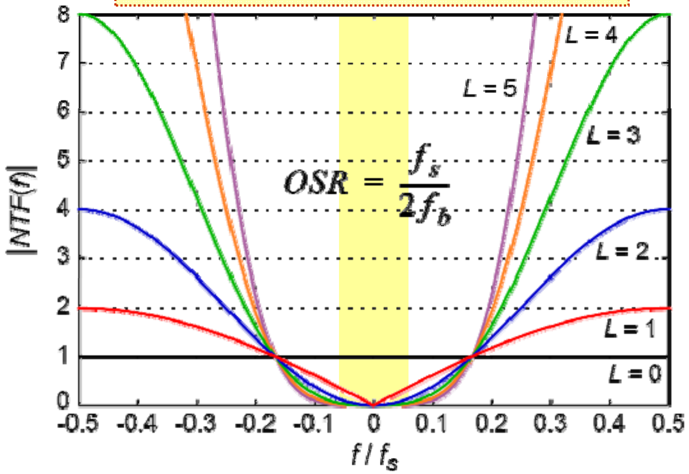
H(z) with large gain within the signal band

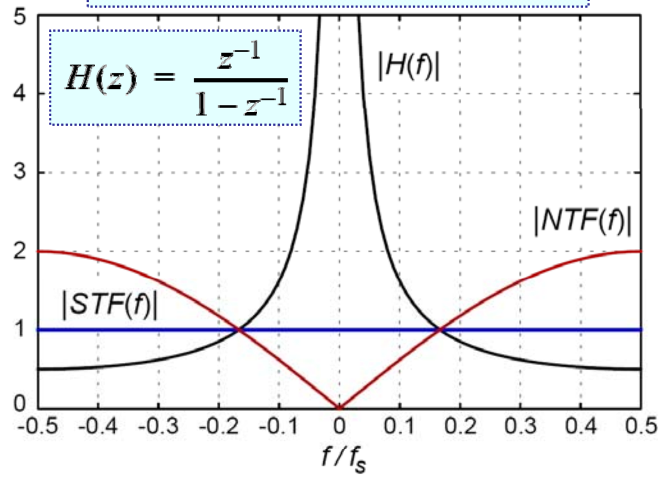
L th-order ΣΔM

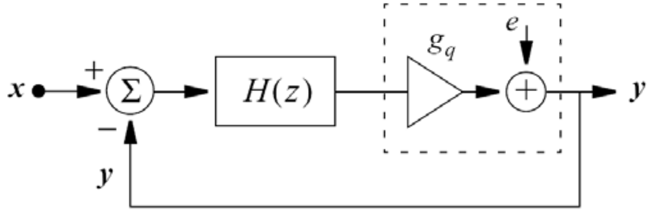
$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^L E(z)$$

1st-order ΣΔM

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z)$$







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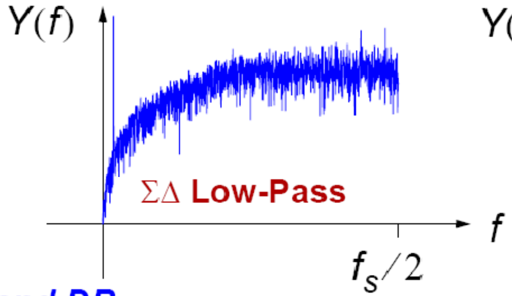
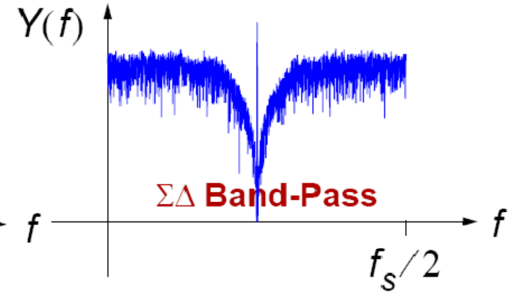
H(z) with large gain within the signal band

Within the signal bandwidth

$$|S_{TF}(z)| = \frac{H(z)}{1 + H(z)} \rightarrow 1$$

$$N_{TF}(z) = \frac{1}{1 + H(z)} \rightarrow 0$$





In-band noise power, SNR and DR

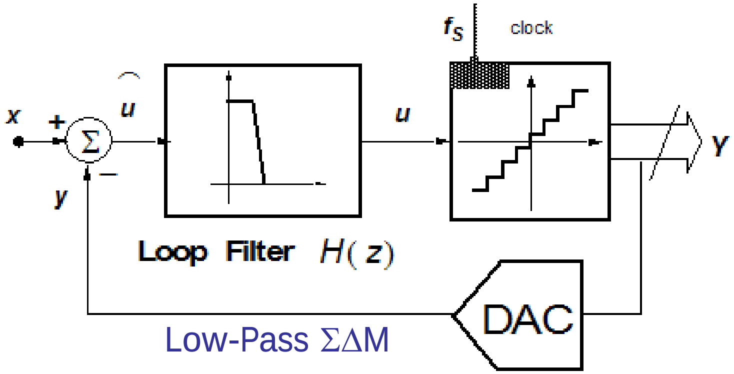
$$P_Q = \begin{cases} \dfrac{\Delta^2}{6f_s} \displaystyle\int_0^{B_w} |N_{TF}(f)|^2 df & \text{for LP}\Sigma\Delta \\ \dfrac{\Delta^2}{6f_s} \displaystyle\int_{f_n - B_w/2}^{f_n + B_w/2} |N_{TF}(f)|^2 df & \text{for BP}\Sigma\Delta \end{cases}$$

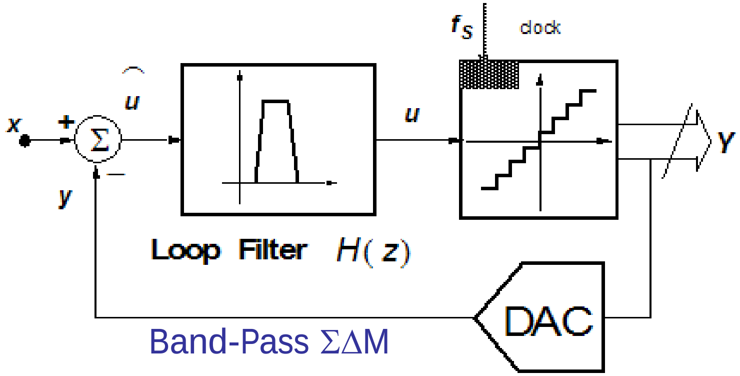
$$SNR = 10\log_{10}\left(\frac{A^2/2}{P_Q}\right)$$

$$DR = 10\log_{10}\left[\frac{(X_{FS})^2/2}{P_Q}\right]$$

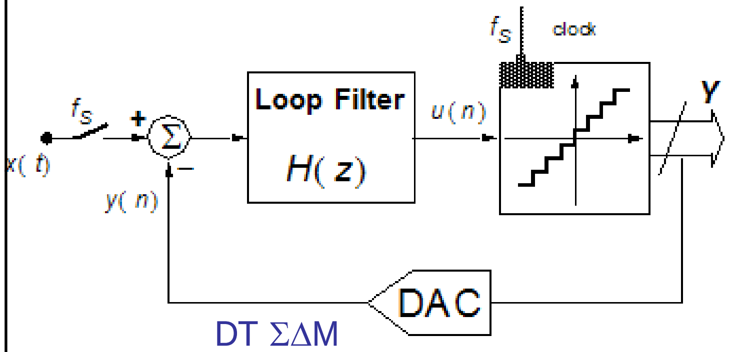
Fundamentals of ΣΔ ADCs: Classification of ΣΔMs

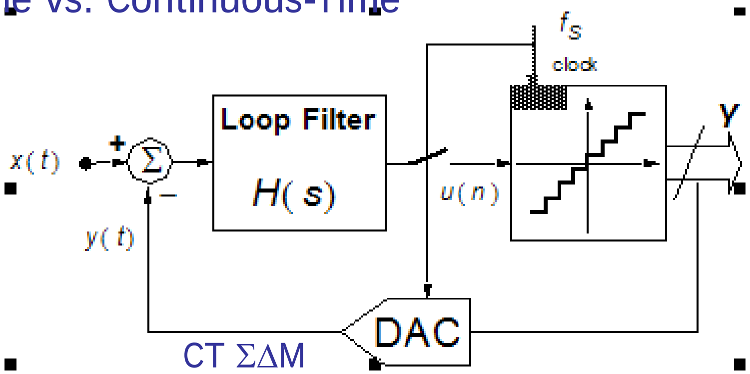
- Nature of the signals being handled: Low-pass vs. Band-pass





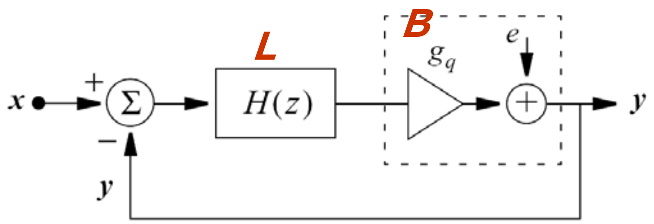
- Dynamics of the loop filter: Discrete-Time vs. Continuous-Time





- Number of bits of the embedded quantizer: single-bit vs. multi-bit
- Number of quantizers employed: single-loop, cascade, etc..
- Type of primitives available in the fabrication technology...

Fundamentals of ΣΔ ADCs: Basic control parameters



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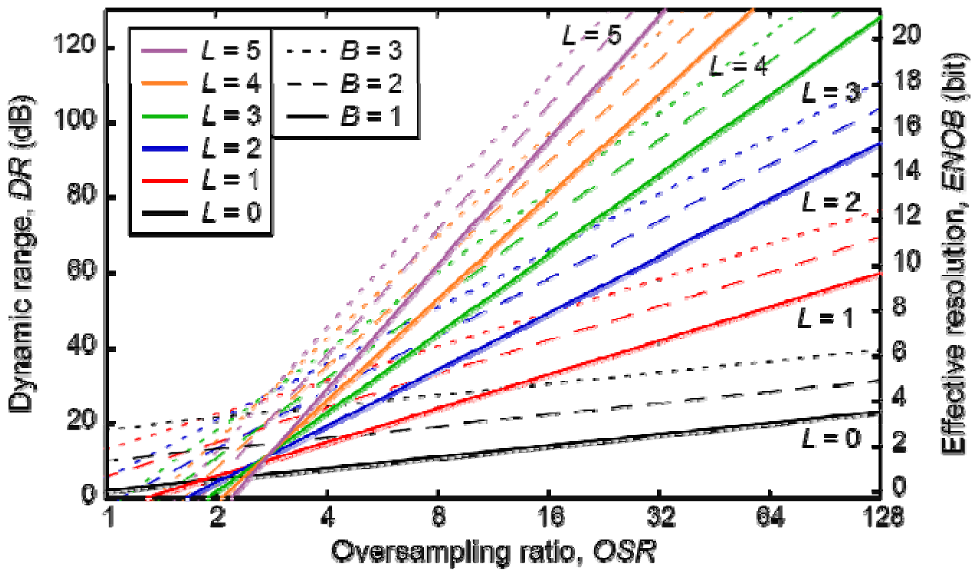
H(z) with large gain within the signal band

L th-order ΣΔM

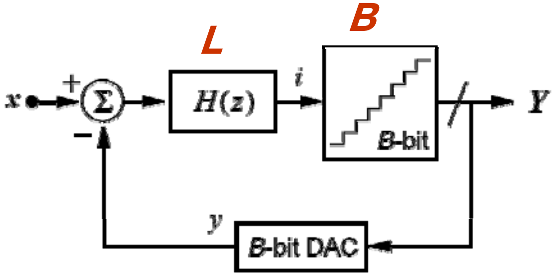
$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^L E(z)$$

$$DR \approx \frac{3}{2}(2^B - 1)^2 \cdot \frac{(2L+1)OSR^{(2L+1)}}{\pi^{2L}}$$



- **Oversampling, *OSR***
  Speed of analog circuitry
- **Order of the shaping, *L***
  Stability of the ΣΔM
- **Resolution of the internal quantizer, *B***
  Linearity of the DAC

Fundamentals of ΣΔ ADCs: Basic control parameters



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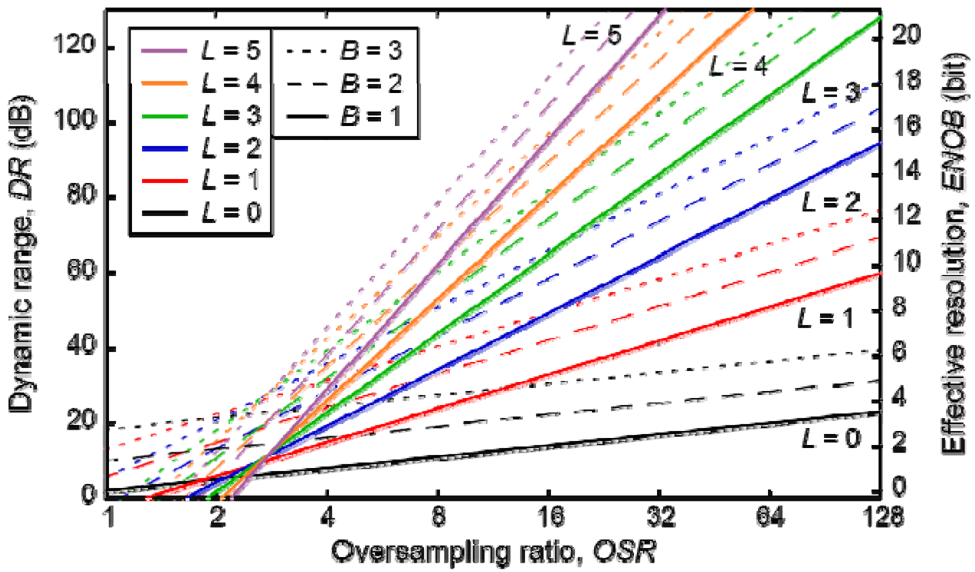
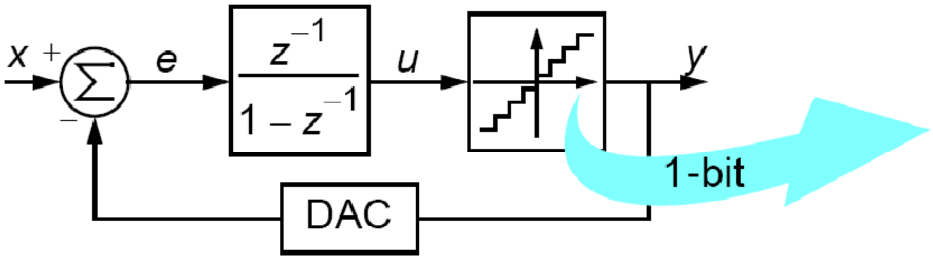


- **Oversampling, *OSR***
  Speed of analog circuitry
- **Order of the shaping, *L***
  Stability of the ΣΔM
- **Resolution of the internal quantizer, *B***
  Linearity of the DAC

DT-ΣΔ Ms: 1st-order LP ΣΔ modulator

$$N_{TF}(z)\big|_{z=1} \to 0 \quad \Rightarrow \quad \left.\frac{1}{1+H(z)}\right|_{z=1} \to 0 \quad \Rightarrow \quad \boxed{H(z) = \frac{1}{z-1}}$$

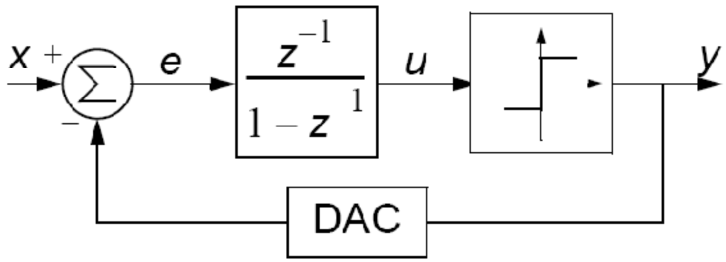


$$\begin{aligned} e(n) &= x(n) - y(n) \\ u(n) &= u(n-1) + e(n) \\ y(n) &= \mathrm{sgn}[u(n)] \end{aligned}$$

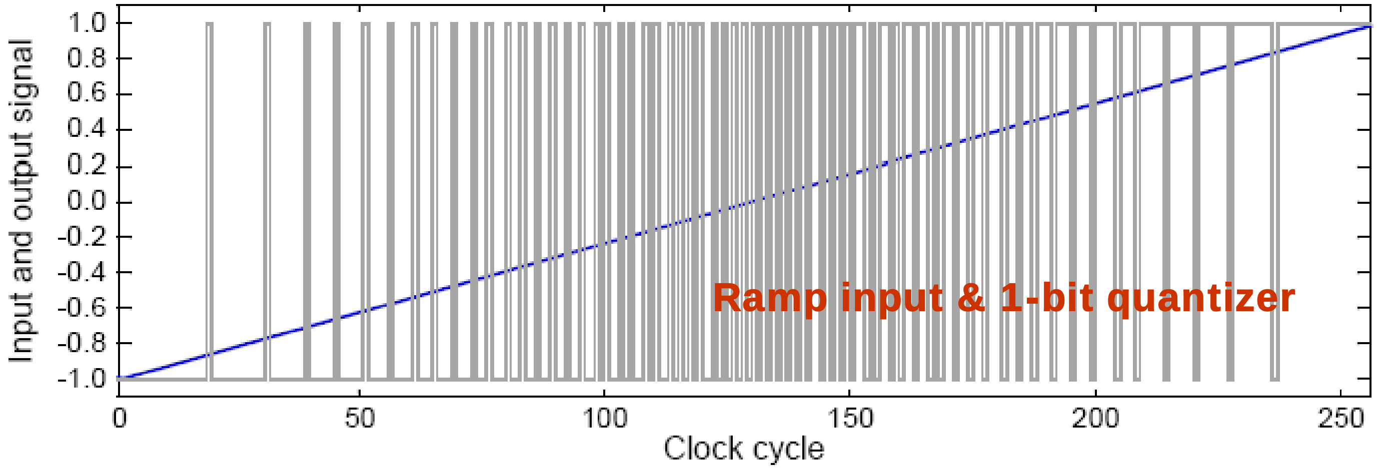
- Using a linear model for the quantizer

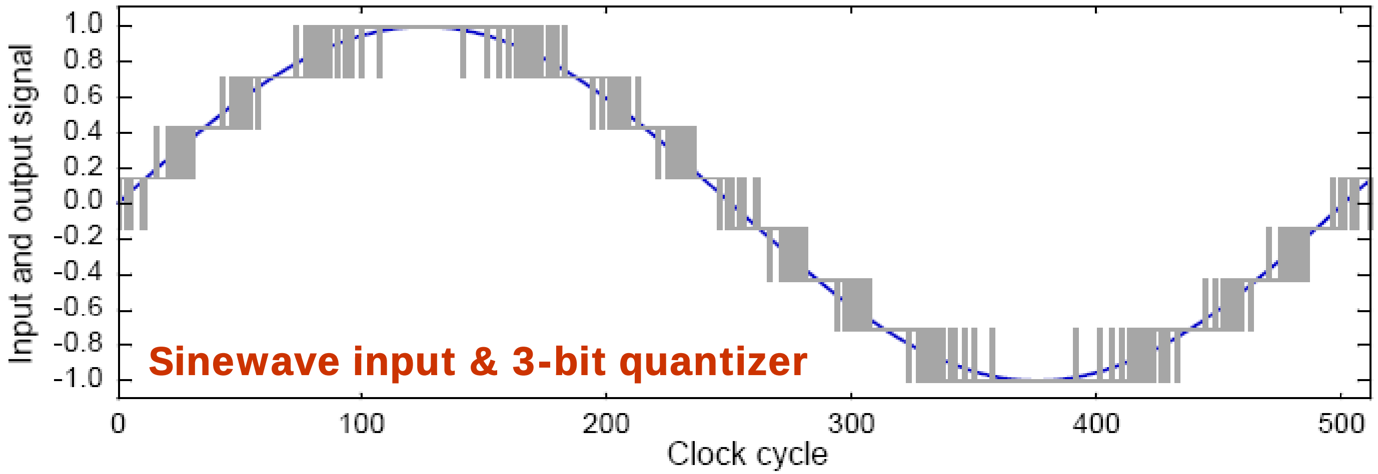
$$Y(z) = z^{-1}X(z) + (1-z^{-1})E(z)$$

$$DR(\mathrm{dB}) \cong 10\log_{10}\left(\frac{9M^3}{2\pi^2}\right)$$



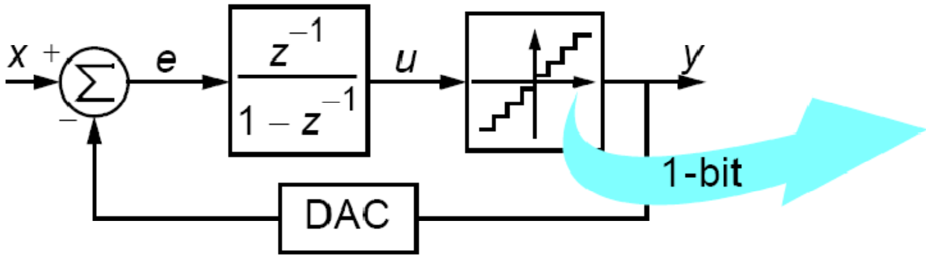
DT- ΣΔ Ms: 1st-order LP ΣΔ Modulator





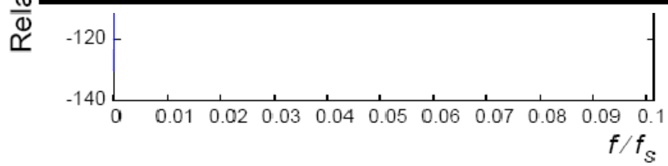
DT-ΣΔ Ms: 1st-order LP ΣΔ modulator

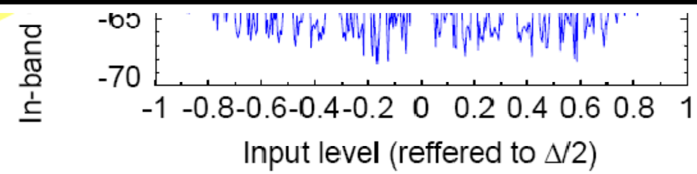
- Noise pattern



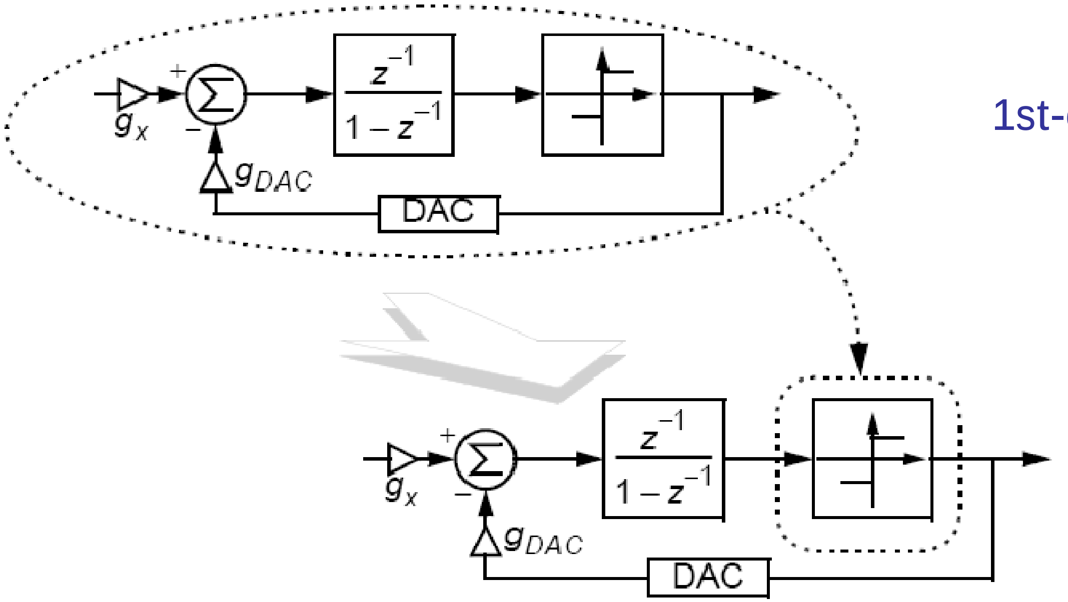
$$e(n) = x(n) - y(n)$$
$$u(n) = u(n-1) + e(n)$$
$$y(n) = \mathrm{sgn}[u(n)]$$

	$x = 0$			$x = 1/3$			$x = 1/2$		
n	u	y	e	u	y	e	u	y	e
0	0	1	-1	0	1	-2/3	0	1	-1/2
1	-1	-1	1	-2/3	-1	4/3	-1/2	-1	3/2
2	0	1	-1	2/3	1	-2/3	1	1	-1/2
3	-1	-1	1	0	1	-2/3	1/2	1	-1/2
4	0	1	-1	-2/3	-1	4/3	0	1	-1/2



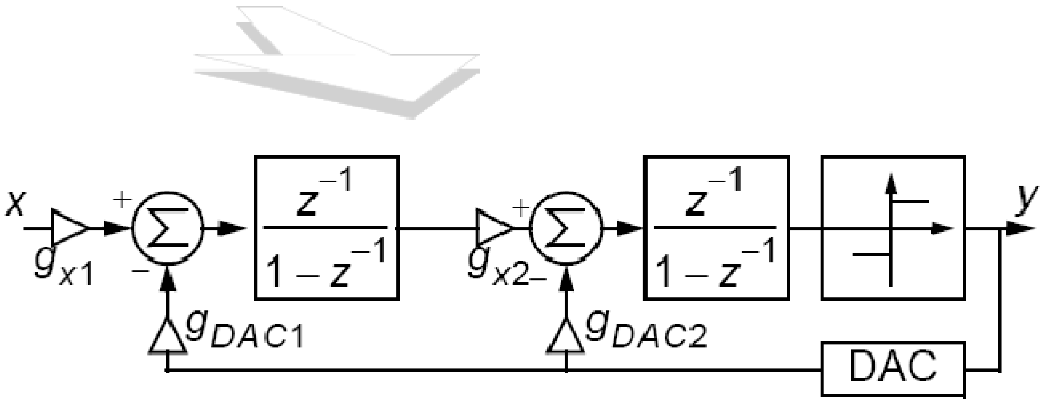


DT-ΣΔ Ms: 2nd-order LP ΣΔ modulator

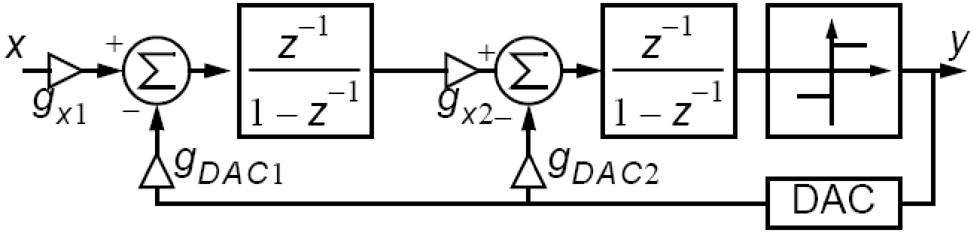


1st-order ΣΔ Modulator

2nd-order ΣΔ Modulator



DT-ΣΔ Ms: 2nd-order LP ΣΔ modulator



Stability conditions:

$$g_{DAC1}g_{x2}g_q = 1$$

$$g_{DAC2} = 2g_{DAC1}g_{x2}$$

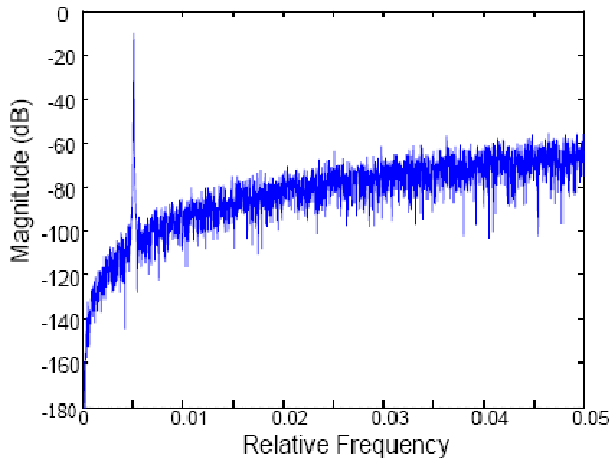
- Linear analysis

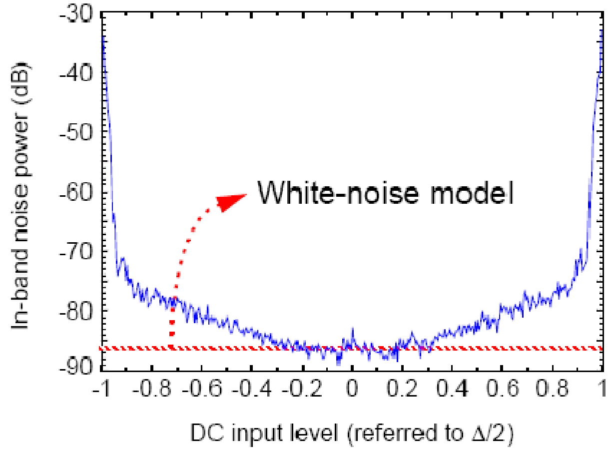
$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z)$$

$$P_Q \cong \frac{\Delta^2\pi^4}{60M^5} \Rightarrow DR \cong \frac{15M^5}{2\pi^4}$$

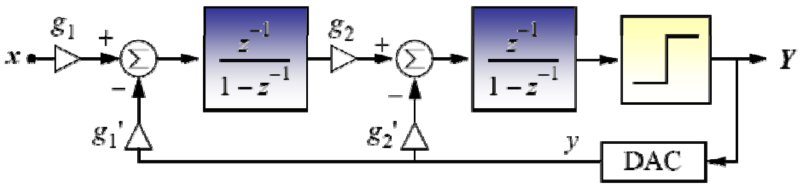
- **Dependence on M: 15 dB/oct.**
- **Example: digitize a 10kHz signal with 16 bits**
  - M = 150 (f_s = 3 MHz) for a 2nd-order ΣΔM
  - M = 1500 (f_s = 30 MHz) for a 1st-order ΣΔM

- Output spectrum and noise pattern





DT-ΣΔ Ms: High-order single-loop ΣΔ modulators

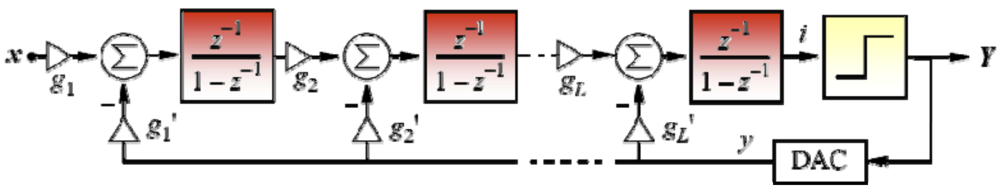


2nd-order ΣΔM

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z)$$

$$g_1'g_2g_q = 1$$
$$g_2' = 2g_1'g_2$$

Stable for inputs in $[-0.9\Delta/2, +0.9\Delta/2]$ if $g_2' > 1.25g_1'g_2$ [Candy85]

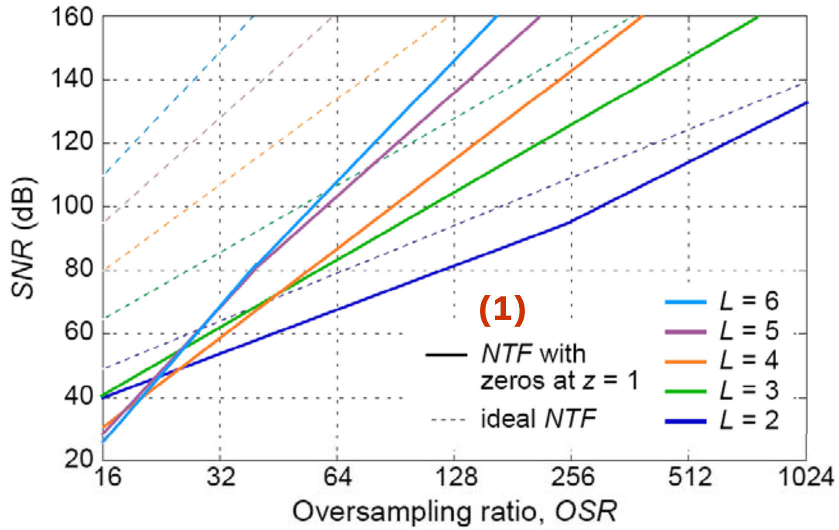


L th-order ΣΔM

$$Y(z) = z^{-L}X(z) + (1-z^{-1})^LE(z)$$

pure-differentiator FIR *NTF*

$\|NTF\|_\infty = 2^L$ Prone to instability



High-order ΣΔ loops are only conditionally stable [OptE90]

IIR *NTFs* [Lee87]

$$NTF(z) = \frac{(z-1)^L}{D(z)} \quad (1)$$

- Zeros at $z = 1$
- Butterworth/Chebyshev poles

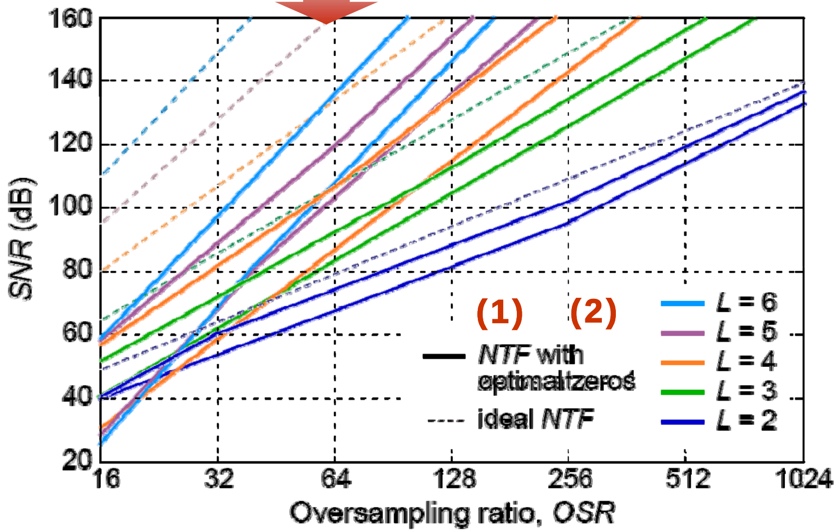
Gain adjusted to satisfy $\|NTF\|_\infty \sim 1.5$

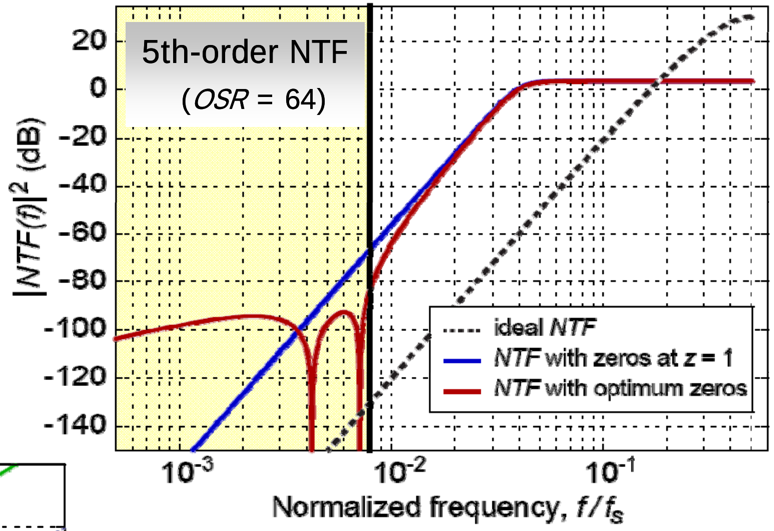
DT-ΣΔ Ms: High-order single-loop ΣΔ modulators

OPTIMIZED IIR *NTF*s [Schr93]

$$\min\left[\int_0^{f_b} |NTF(f)|^2 df\right] \quad (2)$$

- Complex zeros at $|z| = 1$ with optimal positions within the signal band
- Butterworth/Chebyshev poles





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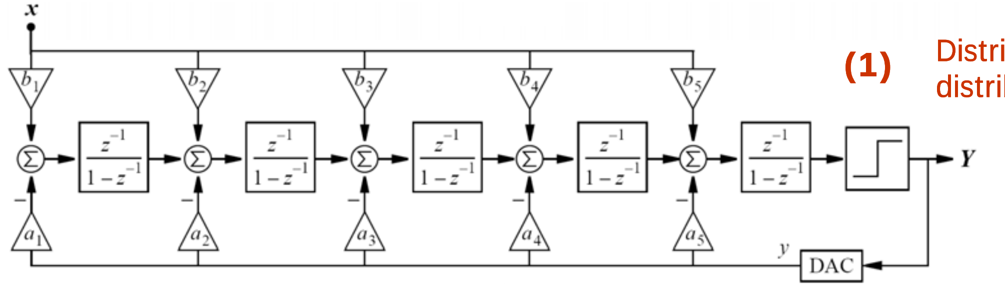
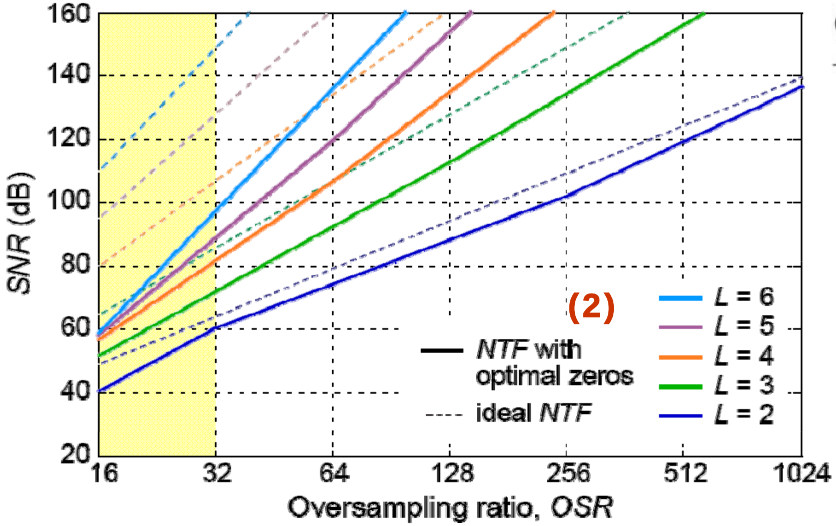
DT-ΣΔ Ms: High-order single-loop ΣΔ modulators

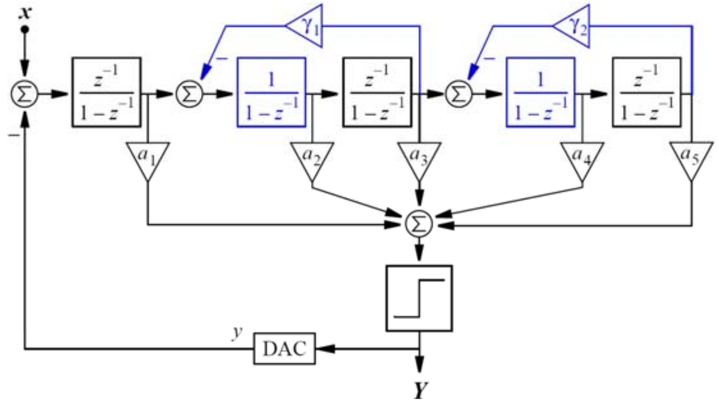


(1) Distributed feedback and distributed feedforward input

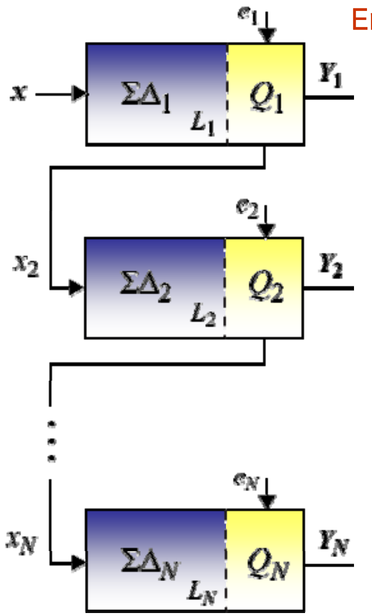
- Complexity (many feedback/feedforward coeffs)
- Large spread of coeffs (area, power)
- Not suited at low oversampling (stand-alone)



(2) Feedforward summation + local resonators



DT- ΣΔ Ms: High-order cascade ΣΔ modulators



Error Cancellation Logic (ECL)

$$Y(z) = z^{-L}X(z) + d_{2N-3}(1 - z^{-1})^{L}E_N(z)$$

$$L = L_1 + L_2 + \ldots + L_N$$

- HIGH-ORDER STABLE OPERATION is ensured by cascading low-order stages (L_i = 1, 2).
- Relationships among ECL and ΣΔM to be fulfilled for perfect cancellation (NOISE LEAKAGE).

d > 1, interstage coupling

$$P_Q \cong d_{2N-3}^2 \cdot \frac{\Delta_N^2}{12} \cdot \frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}}$$

Systematic loss of resolution, but:

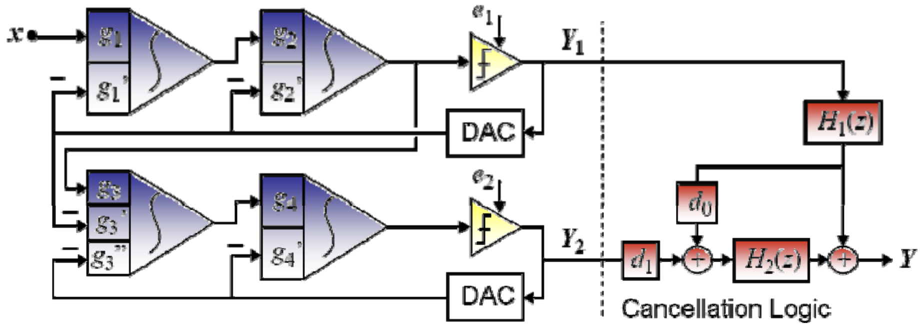
- Smaller than for single loops
- Independent of *OSR*

MASH ΣΔMs

- Each stage re-modulates a signal containing the quantization error in the previous one.
- Digital processing is used to cancel out all quantization errors, but that in the last stage.

$$NTF_i(z) = 0 \quad , i = 1, \ldots, N-1$$

- Small spread of analog coeffs
- ECL can be easily implemented
- Performance close to ideal
- Suited at low oversampling



2-2 ΣΔM [Kare90]

4th-order 2-stage cascade

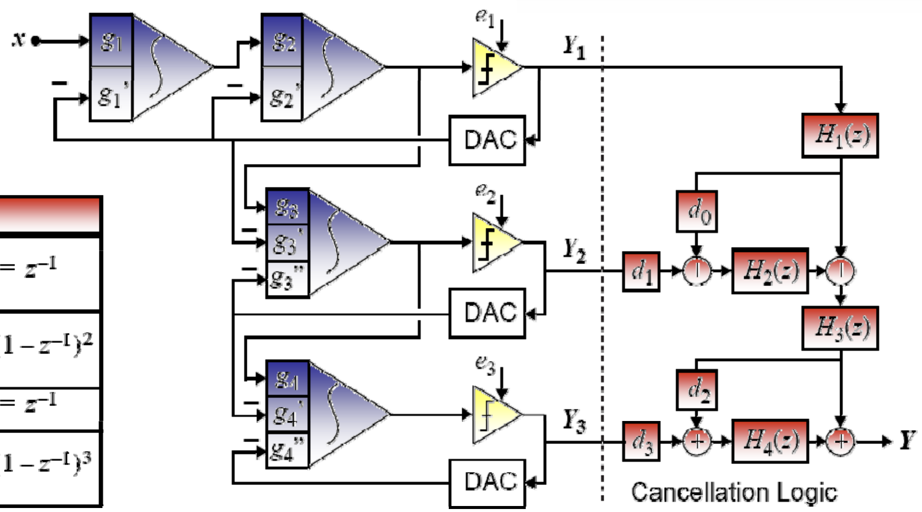
Analog	Digital	
$g_2' = 2g_1'g_2$	$d_0 = \frac{g_3'}{g_1'g_2g_3} - 1$	$H_1(z) = z^{-2}$
$g_4' = 2g_3''g_4$	$d_1 = \frac{g_3''}{g_1'g_2g_3}$	$H_2(z) = (1-z^{-1})^2$

- **1-1-1 ΣΔM** [Mats87]
- **2-1 ΣΔM** [Longo88]
- **2-2-1 ΣΔM** [Vleu01]
- **2-1-1-1 ΣΔM** [Rio00]
- **2-2-2 ΣΔM** [Dedic94]

Noise leakage precludes the cascading of a large number of stages to be practical

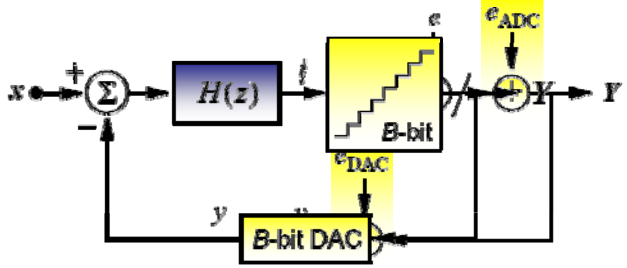
2-1-1 ΣΔM [Yin94]

4th-order 3-stage cascade

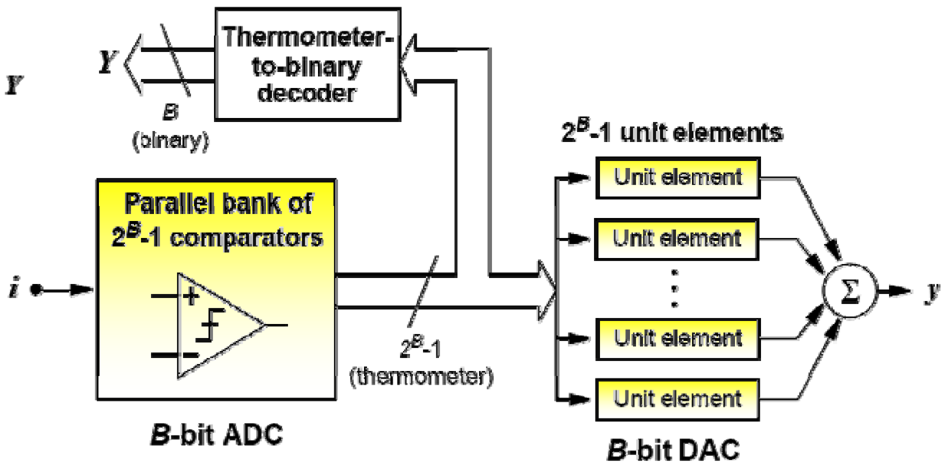


Analog	Digital	
$g_2' = 2g_1'g_2$	$d_0 = \frac{g_3'}{g_1'g_2g_3} - 1$	$H_1(z) = z^{-1}$
$g_4' = g_3''g_4$	$d_1 = \frac{g_3''}{g_1'g_2g_3}$	$H_2(z) = (1-z^{-1})^2$
	$d_2 = 0$	$H_3(z) = z^{-1}$
	$d_3 = \frac{g_4''}{g_1'g_2g_3g_4}$	$H_4(z) = (1-z^{-1})^3$

DT-ΣΔ Ms: Multi-bit ΣΔ modulators



- Increased dynamic range
  - *B* can trade for *OSR* (wideband)
- Better stability properties
  - More aggressive high-order *NTF*s
- DAC non-linearities are directly added to the input
  - The linearity of the ΣΔM will be no better than that



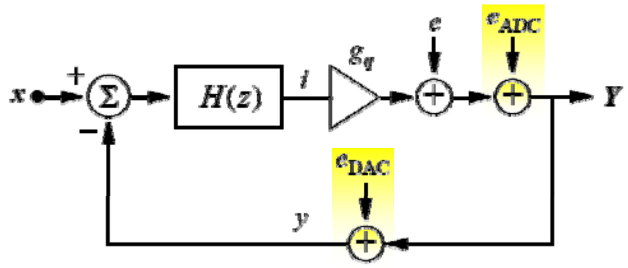
FULL-PARALLEL ADC / DAC
(Typically $B < 6$)

DAC linearity limited by component mismatch

POSSIBLE APPROACHES

- Correcting DAC errors
  - Element Trimming
  - Analog Calibration
  - Digital Correction
- Decorrelating DAC errors from the input
  - DEM techniques
- Introducing DAC errors at a non-critical position
  - Dual quantization

DT-ΣΔ Ms: Multi-bit ΣΔ modulators



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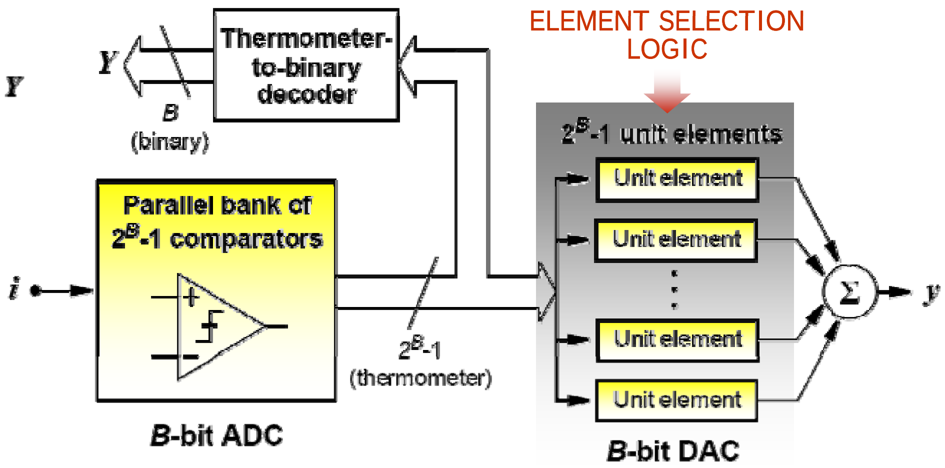


FULL-PARALLEL ADC/DAC
(Typically $B < 6$)

DAC linearity limited by component mismatch

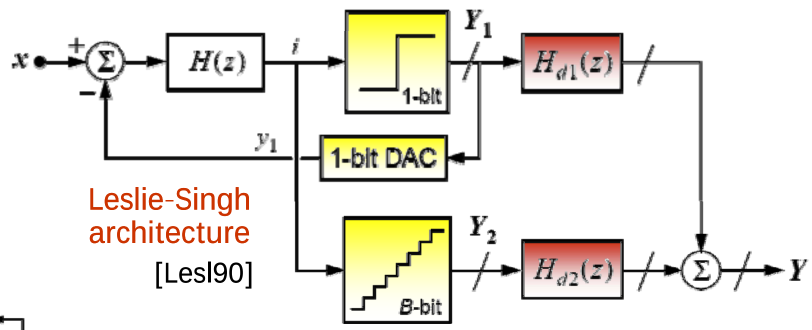
Dynamic Element Matching (DEM)

- Elements selected to make DAC errors independent of the input signal
- Algorithms that try to average the error in each DAC level to zero (to push DAC errors to high freq.)
  - Randomization: Distortion transforms into white noise
  - Rotation: Distortion moves out of band (CLA)
  - Mismatch-shaping: 1st/2nd order (ILA, DWA, DDS)

DT-ΣΔ Ms: Dual-quantization ΣΔ modulators

Dual Quantization

- Combines 1-bit and multi-bit quantizers (linearity/reduced error)



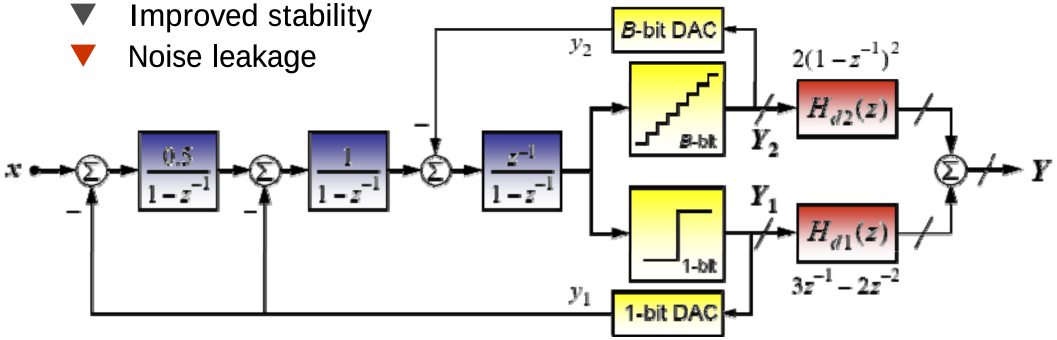
Leslie-Singh architecture

[Lesl90]

- *L*-0 cascade ΣΔM
- Suffers from noise leakage
- Multi-bit quantization does not improve stability

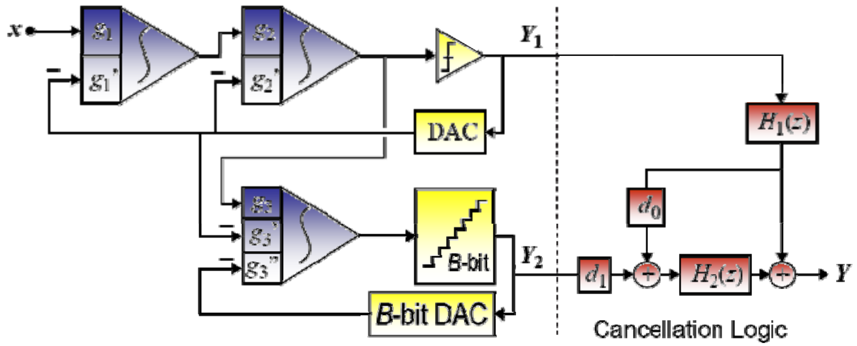
Concept applied to single-loop ΣΔMs [Hair91]

- Improved stability
- Noise leakage

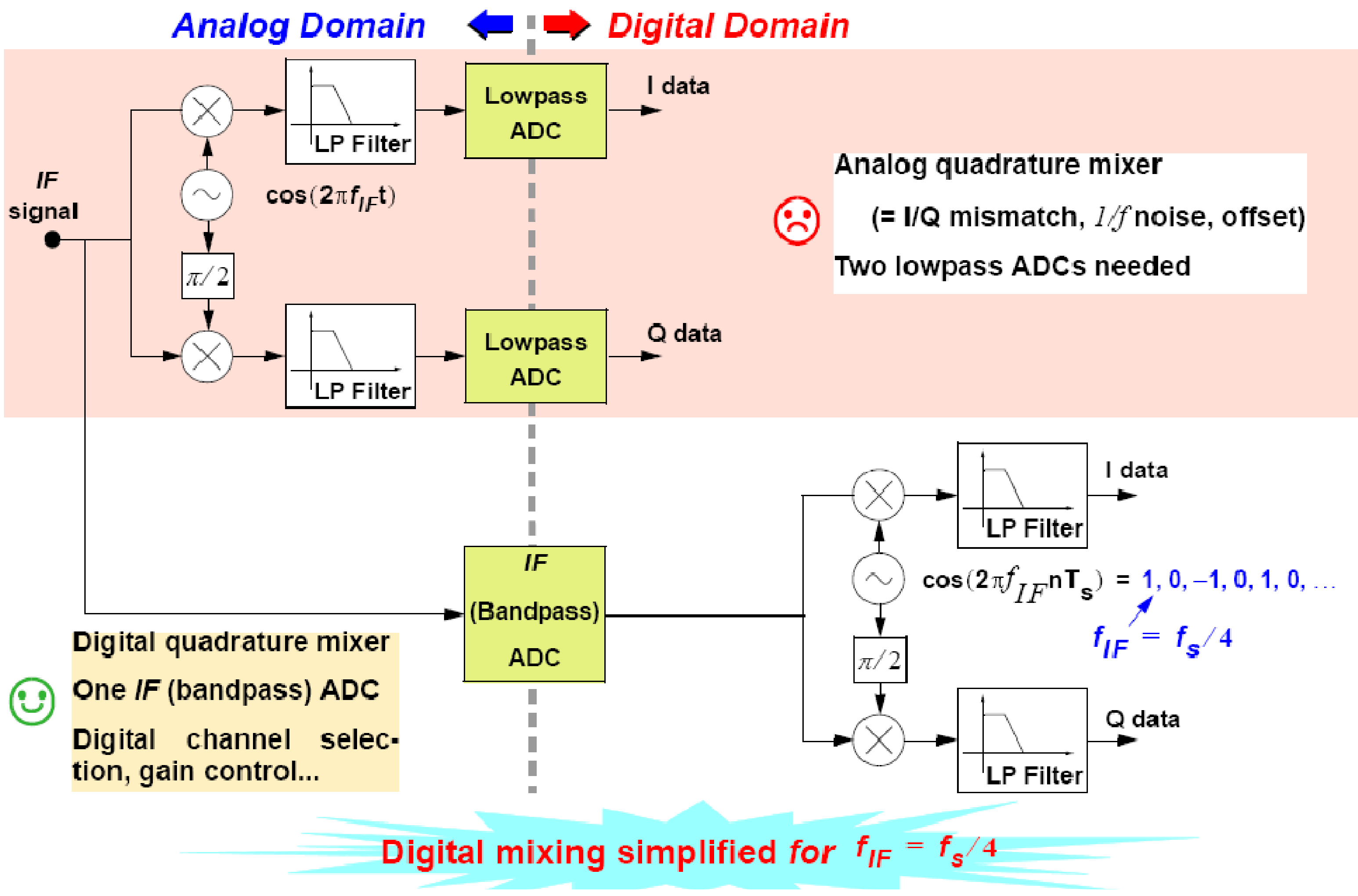


Concept applied to cascade ΣΔMs [Bran91]

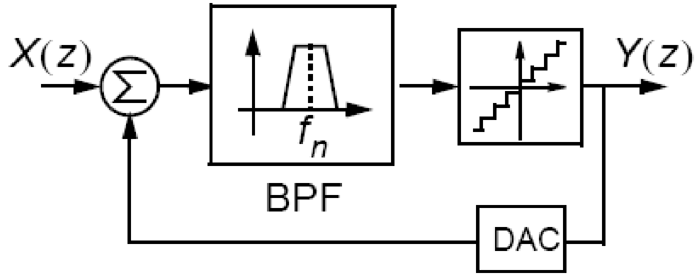
- Multi-bit quantization usually applied only in the last stage
- DAC errors shaped by L-L_N
  Relaxes DAC requirements
- Noise leakage (inherent to cascades)

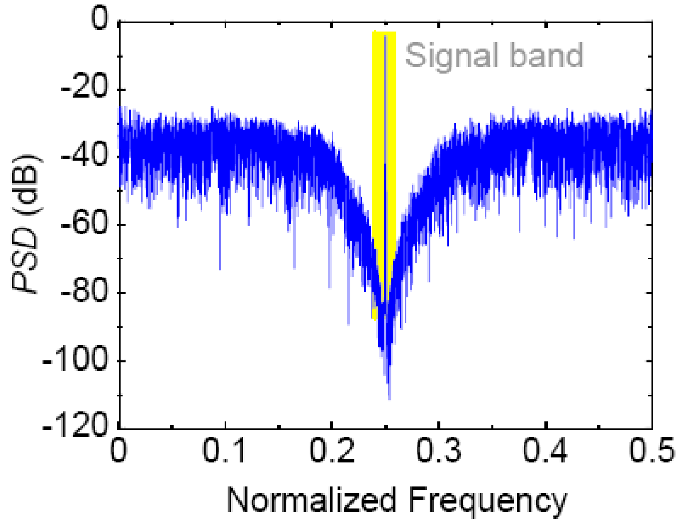


DT-ΣΔ Ms: Bandpass ΣΔ modulators – IF digitization

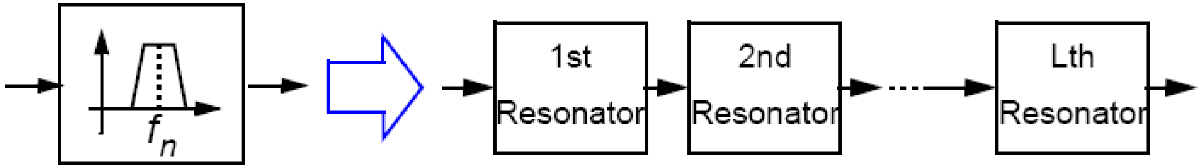


DT-ΣΔ Ms: Bandpass ΣΔ modulators





$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z)$$



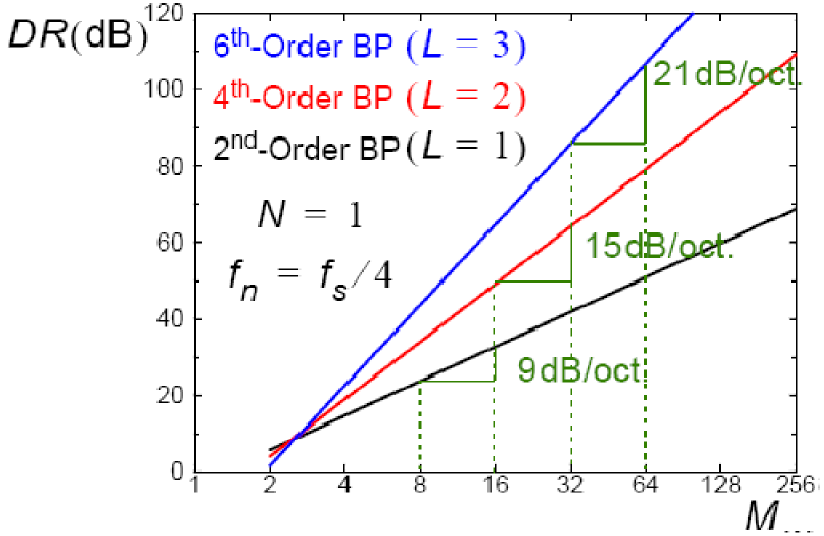
$$H_{bp}(z) = \left[\frac{N_{RES}(z)}{(1 - z^{-1}z_n)(1 - z^{-1}z_n{}^*)}\right]^L \qquad (z_n = e^{2\pi f_n T_s})$$

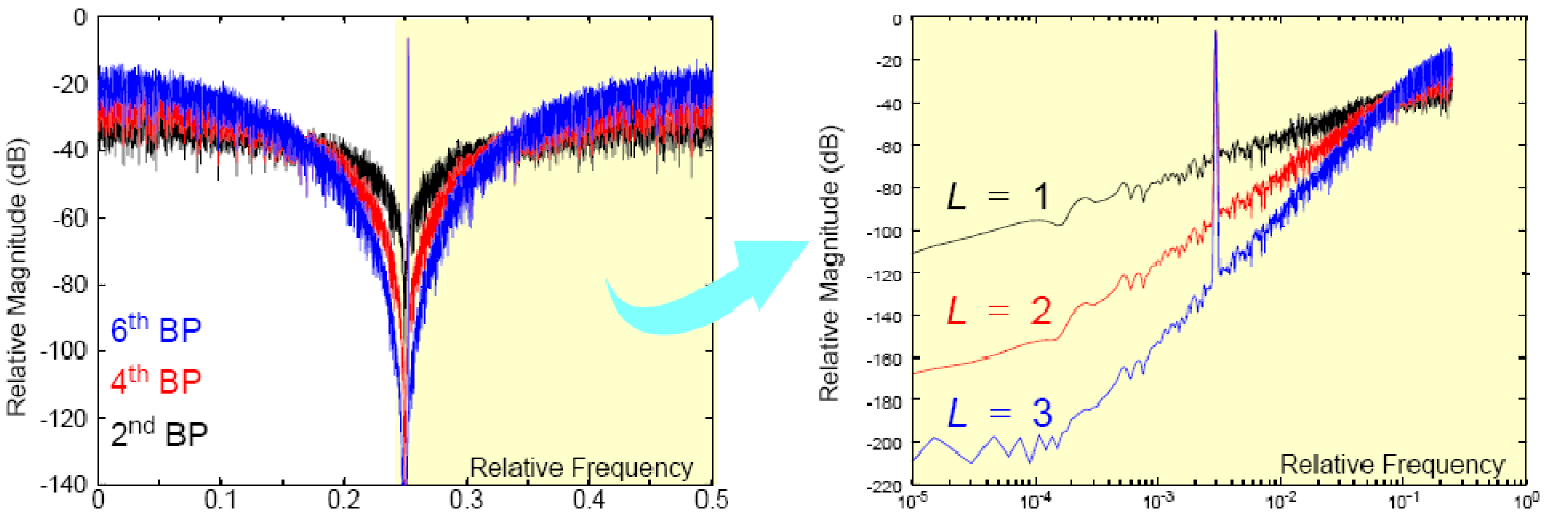
$$(N_{RES}(z) + (1 - z^{-1}z_n)(1 - z^{-1}z_n{}^*) = 1) \Rightarrow N_{TF}(z) = [1 - 2\cos(2\pi f_n T_s)z^{-1} + z^{-2}]^L$$

DT-ΣΔ Ms: Bandpass ΣΔ modulators

$$P_Q \cong \frac{(\sin[2\pi f_n T_s])^{2L}\pi^{2L}X_{FS}^2}{12(2^N-1)^2(2L+1)M^{(2L+1)}}$$

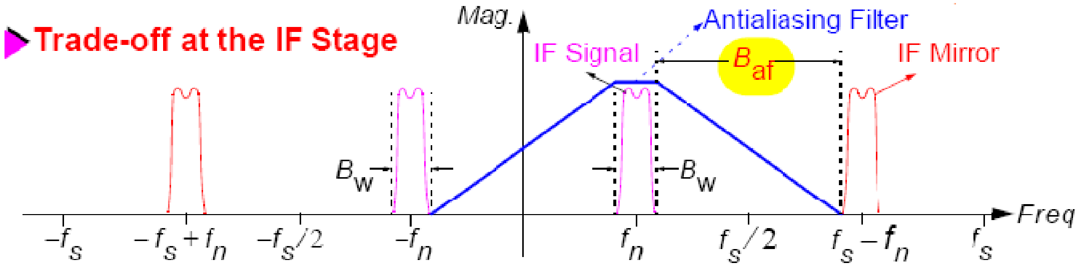
$$DR \cong \frac{3(2^N-1)^2(2L+1)M^{2L+1}}{2\pi^{2L}(\sin[2\pi f_n T_s])^{2L}}$$





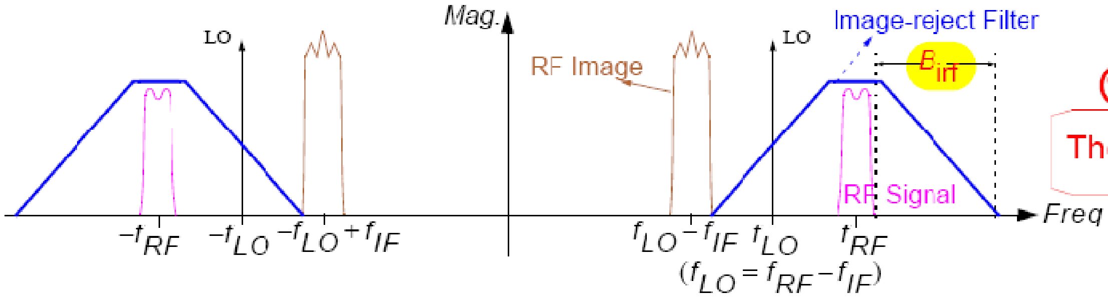
DT-ΣΔ Ms: Bandpass ΣΔMs – Signal band location

Trade-off at the IF Stage



☹ The larger f_n the lower B_{af}

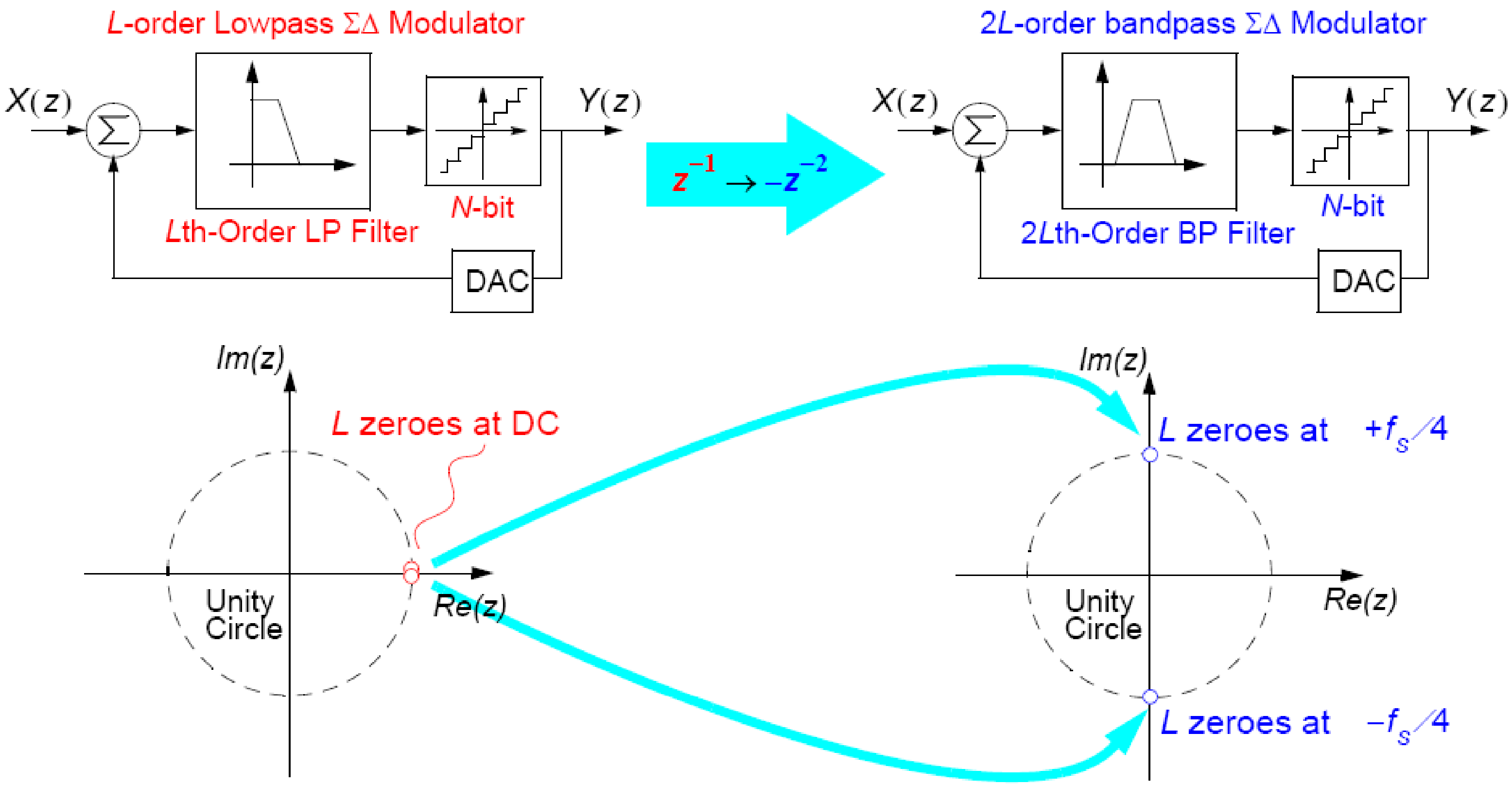
Trade-off at the RF Stage



☹ The lower f_n the lower B_{irf}

- **Optimum location for** $f_n = f_s/4$ **(at the middle of Nyquist band)**
  - Forward path (analog) modulator filter realization can be simplified
  - Simplifies LP-to-BP transformation, $z^{-1} \rightarrow -z^{-2}$
  - Digital mixing to baseband is notoriously simplified:
    $\cos(2\pi f_{IF} n T_s) = 1, 0, -1, 0, 1, 0, \ldots$

DT- ΣΔ Ms: LP-to-BP transformation method

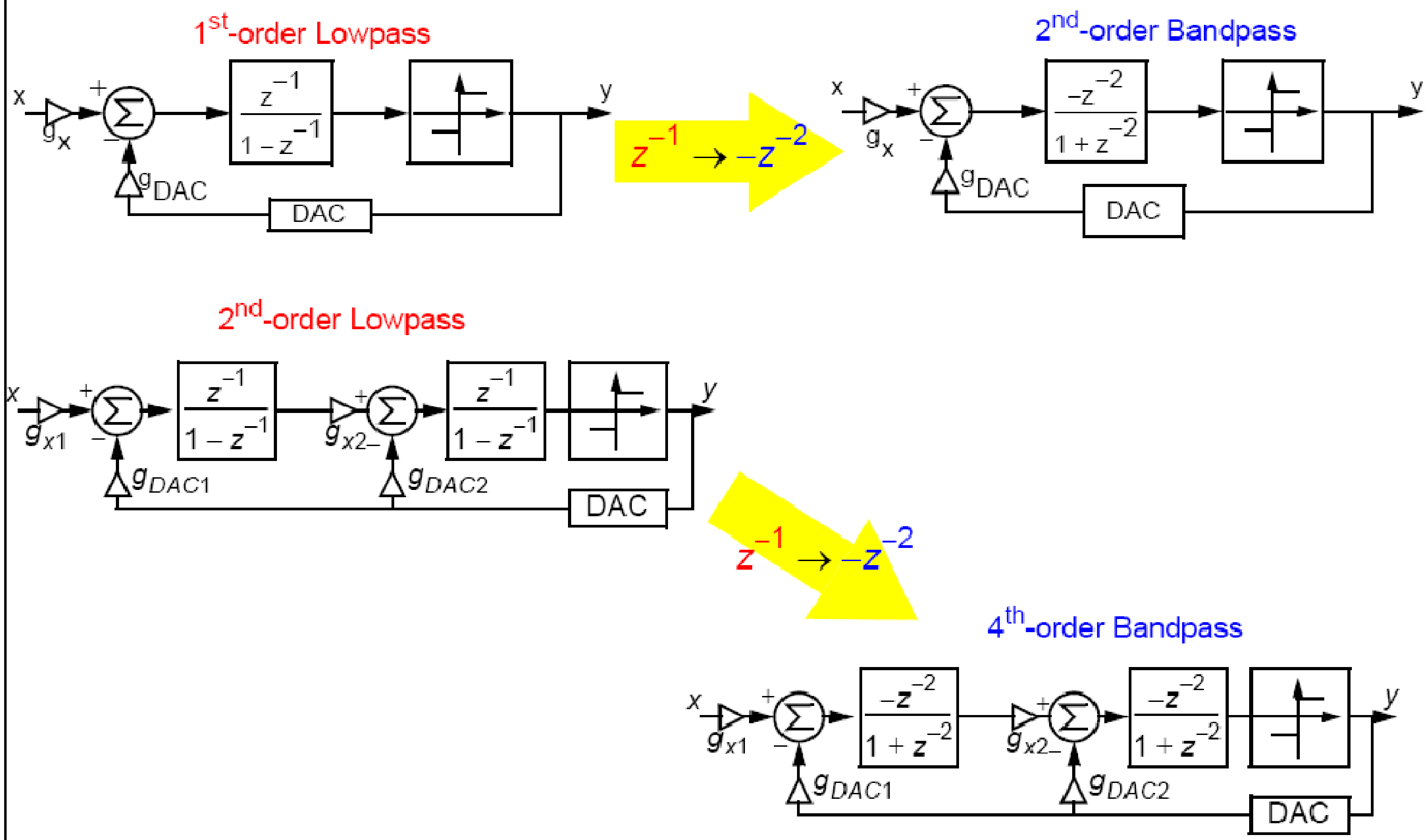


$$S_{TF} = z^{-L}$$
$$N_{TF} = (1 - z^{-1})^{L}$$

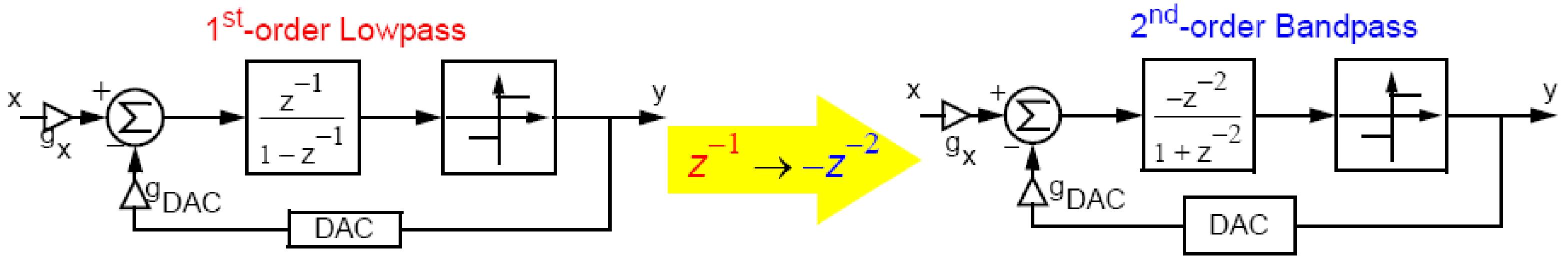
$$SNR_Q = \frac{12(2^{B}-1)^{2}(2L+1)M^{2L+1}}{8\pi^{2L}}$$

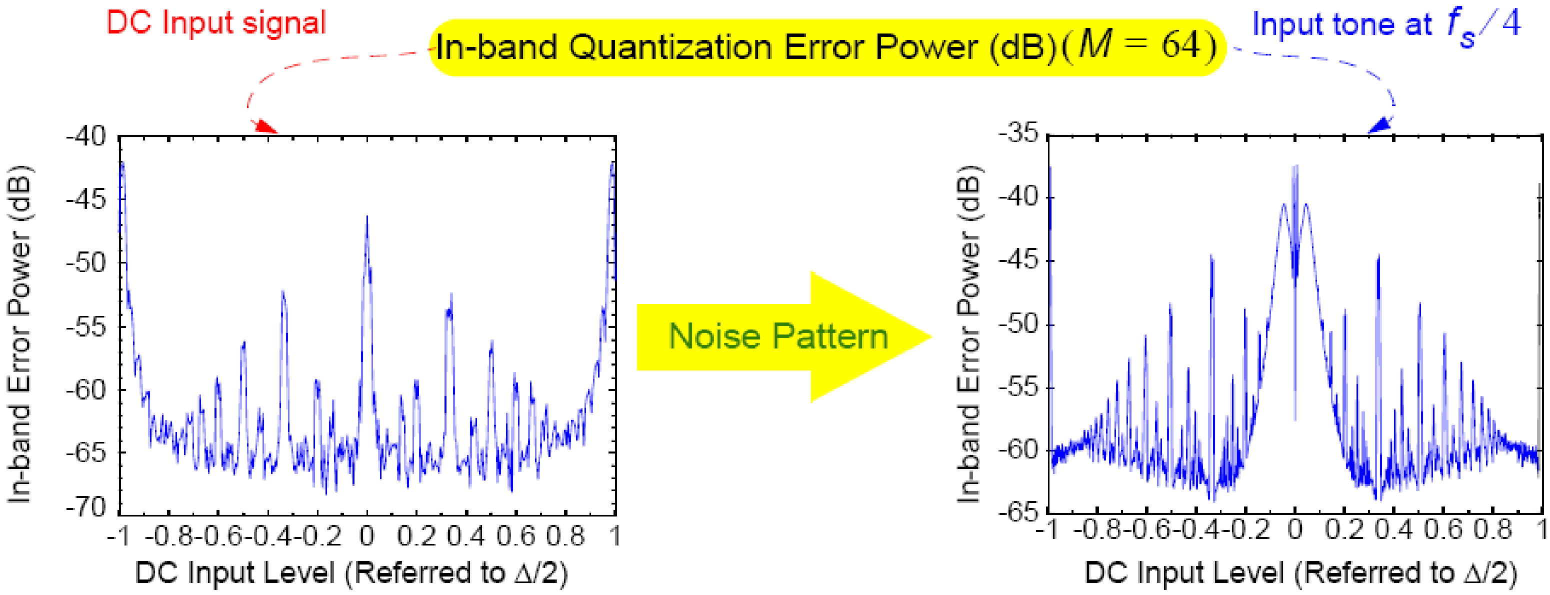
$$S_{TF} = (-z^{-2})^{L}$$
$$N_{TF} = (1 + z^{-2})^{L}$$

DT-ΣΔ Ms: LP-to-BP transformation method

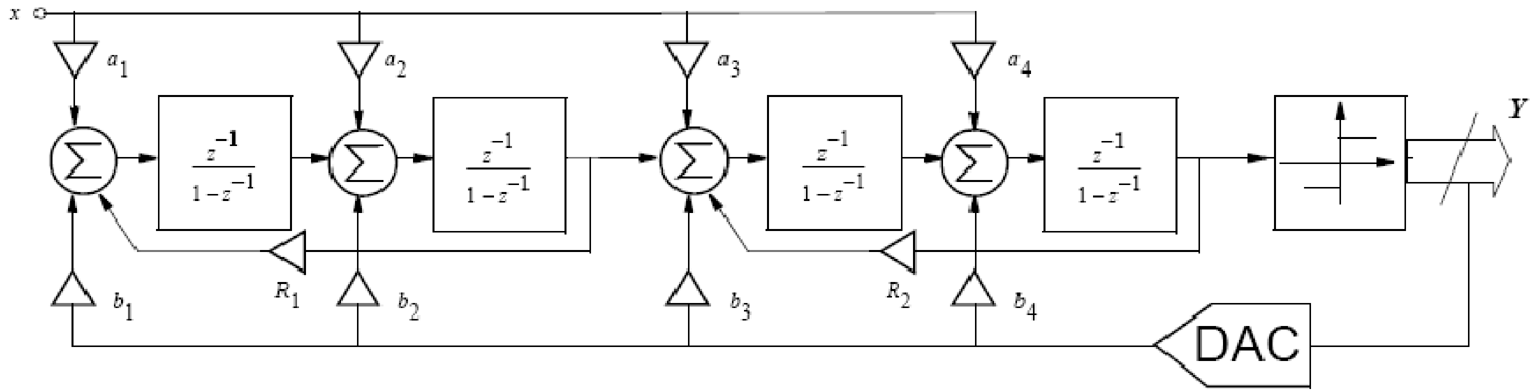


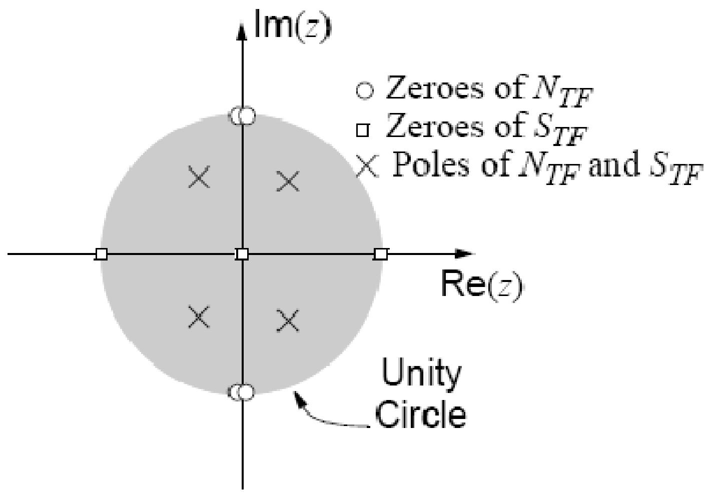
DT-ΣΔ Ms: LP-to-BP transformation method

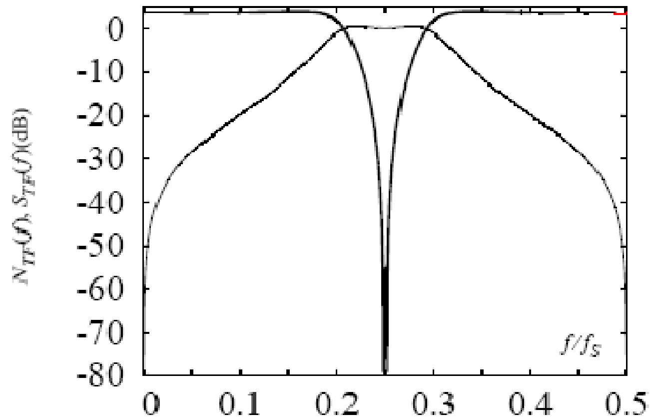




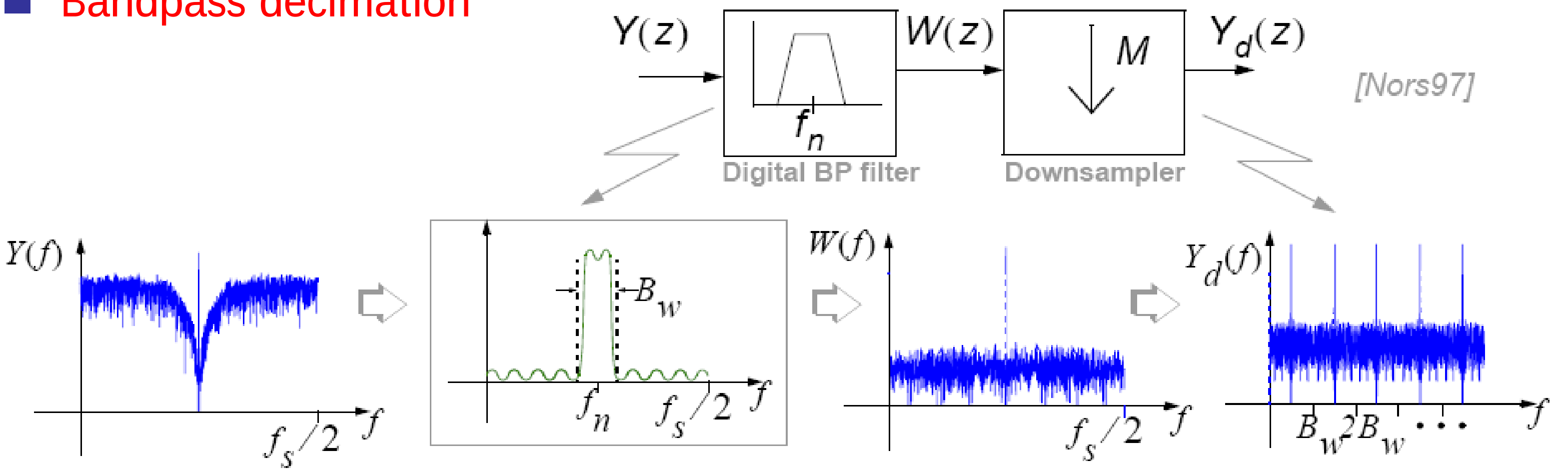
- Other BP-ΣΔM architectures



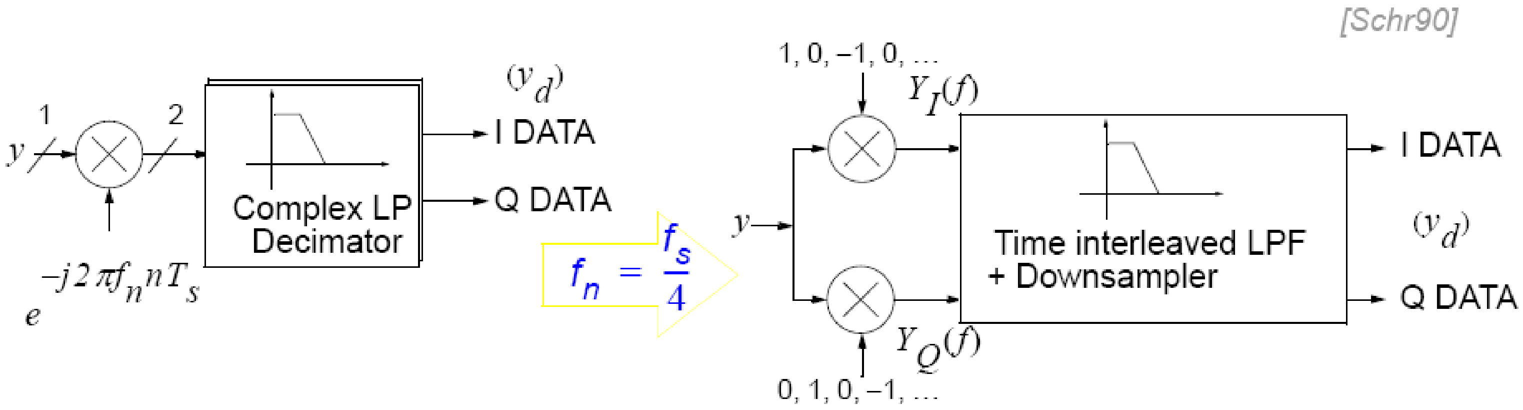




- Bandpass decimation



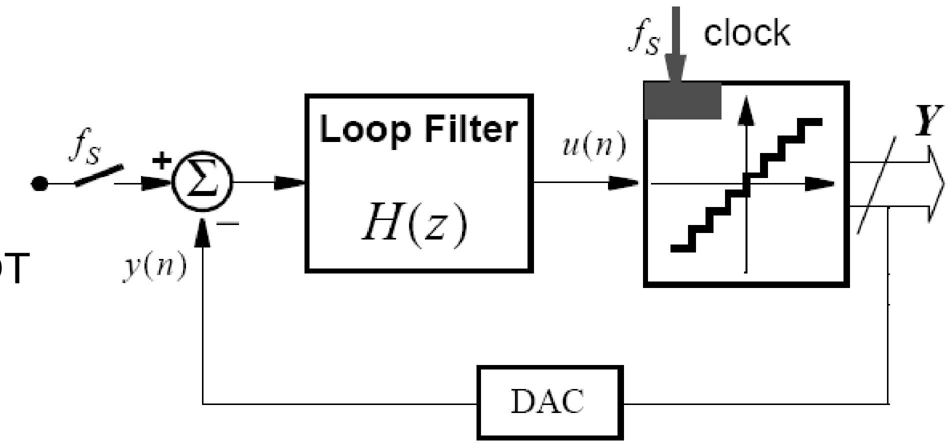
- Efficient decimation



CT-ΣΔ Ms: Basic concepts

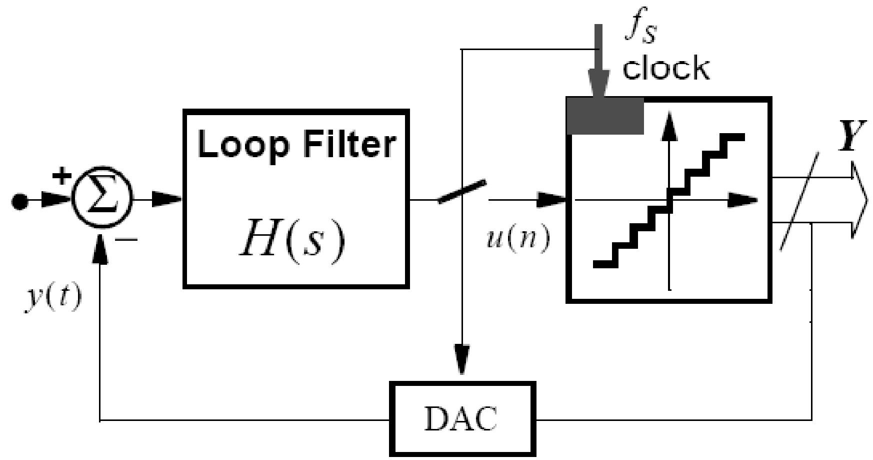
❐ Discrete-Time ΣΔMs

- DT loop filter
- All internal signals are DT
- Sampling at the input

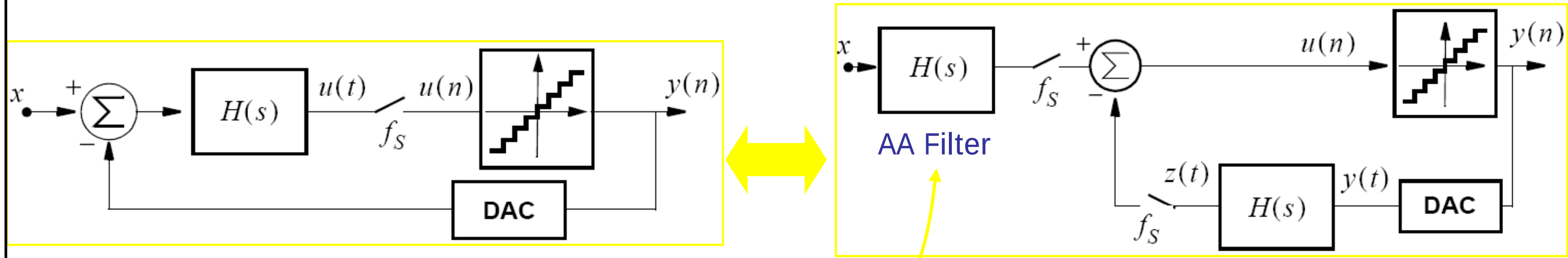


❐ Continuous-Time ΣΔMs

- CT front (loop filter) part
- DT back (quantizer) part
- Sampling inside the loop



CT-ΣΔ Ms: Basic concepts



❒ Pros of CT-ΣΔMs

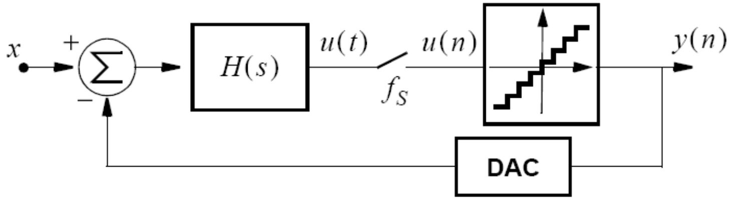
- Implicit anti-aliasing filter
- Less impact of sampling errors
- No input switches – potentially better for low-voltage supply
- No "settling" error at the loop filter circuitry
- Potentially larger operation speed with less power consumption
- No sampling of the noise at the input capacitors
- Reduced digital noise coupling

❒ Counters of CT-ΣΔMs

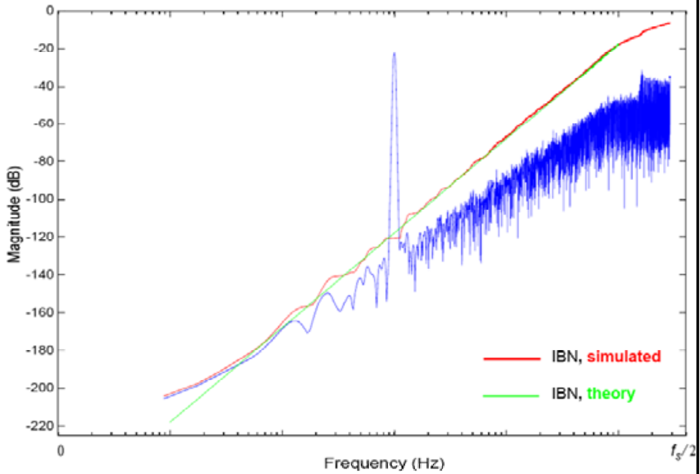
- Very involved dynamic due to the combination of non-linearity, CT and DT
- larger impact of circuit non-linearities
- Time constant tuning is needed for correct loop filtering
- Large sensitive to time uncertainty ("jitter")

CT-ΣΔ Ms: Basic concepts

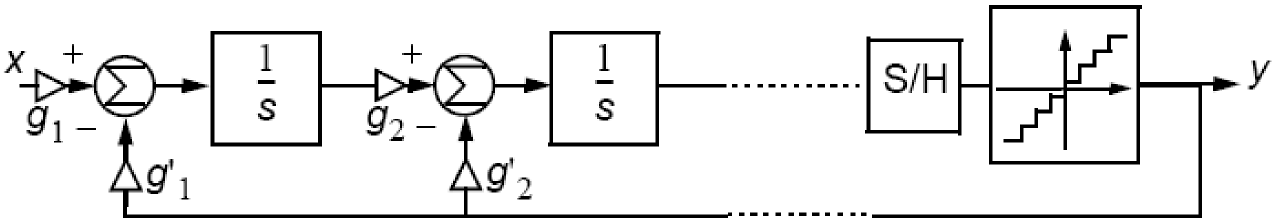
- Linear analysis of CT-ΣΔMs, assuming [Bree01]:
  - Linear model for the quantizer
  - DAC gain is unity in the signal bandwidth



$$Y(f) \cong \frac{H(f)}{1+H(f)} \cdot X(f) + \frac{1}{1+H(f)} \cdot E(f)$$



- Example: *L*th-order, *B*-bit single-loop architecture

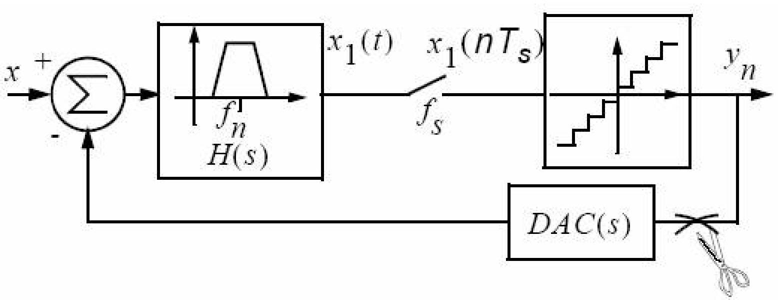


$$Y(f) \cong \frac{g_1}{g'_1} \cdot X(f) + (2\pi j f \tau)^L \cdot E_q(f) \quad \Rightarrow \quad DR = \frac{3(2^B-1)^2(2L+1)M^{2L+1}}{2\pi^{2L}}$$

CT-ΣΔ Ms: Synthesis methods

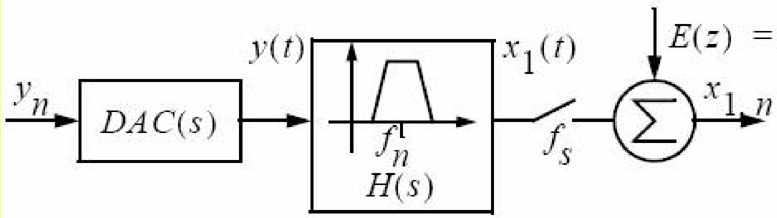
DT-to-CT synthesis method: pulse invariant transformation (freq. domain)

- Find an equivalent DT ΣΔM that fulfils the required specifications
- Based on a DT-to-CT equivalence [Cher00]



DAC	$H(z)$	$H(s)$
NRZ	$\frac{z^{-1}\cdot(1-z^{-1})}{1+z^{-2}}$	$\frac{\omega_o \cdot s}{s^2+\omega_o^2}$
RZ	$\frac{\left(1-\frac{\sqrt{2}}{2}\right)\cdot z^{-1}-\left(\frac{\sqrt{2}}{2}\cdot z^{-2}\right)}{1+z^{-2}}$	
HRZ	$\frac{\frac{\sqrt{2}}{2}\cdot z^{\ 1}-\left(\left(1-\frac{\sqrt{2}}{2}\right)\cdot z^{\ 2}\right)}{1+z^{-2}}$	

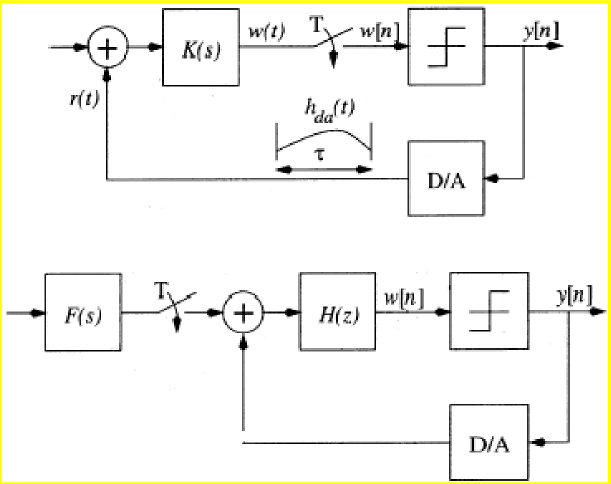
Open-loop configuration



$$\frac{X_1(z)}{Y(z)} = Z\left[L^{-1}[DAC(s)H(s)]\big|_{t = nT_s}\right]$$

DT-to-CT synthesis method: State-Space Representation (time domain)

- Operation of the loop filter is described by state-space equations
- Can be applied to an arbitrary feedback DAC waveform [Olia03b]



$$\frac{d\mathbf{x}(t)}{\mathrm{dt}} = \mathbf{F}\mathbf{x}(t) + \mathbf{G}r(t)$$
$$w(t) = \mathbf{C}\mathbf{x}(t)$$

$$\mathbf{x}(t) = e^{\mathbf{F}(t-t_0)}\mathbf{x}(t_0) + \int_{t_0}^{t} e^{\mathbf{F}(t-\lambda)}\mathbf{G}r(\lambda)d\lambda.$$

$$\mathbf{x}[n+1] = e^{\mathbf{F}T}\mathbf{x}[n] + y[n]\int_{0}^{T} e^{\mathbf{F}(T-\lambda)}\mathbf{G}h_{da}(\lambda)d\lambda.$$

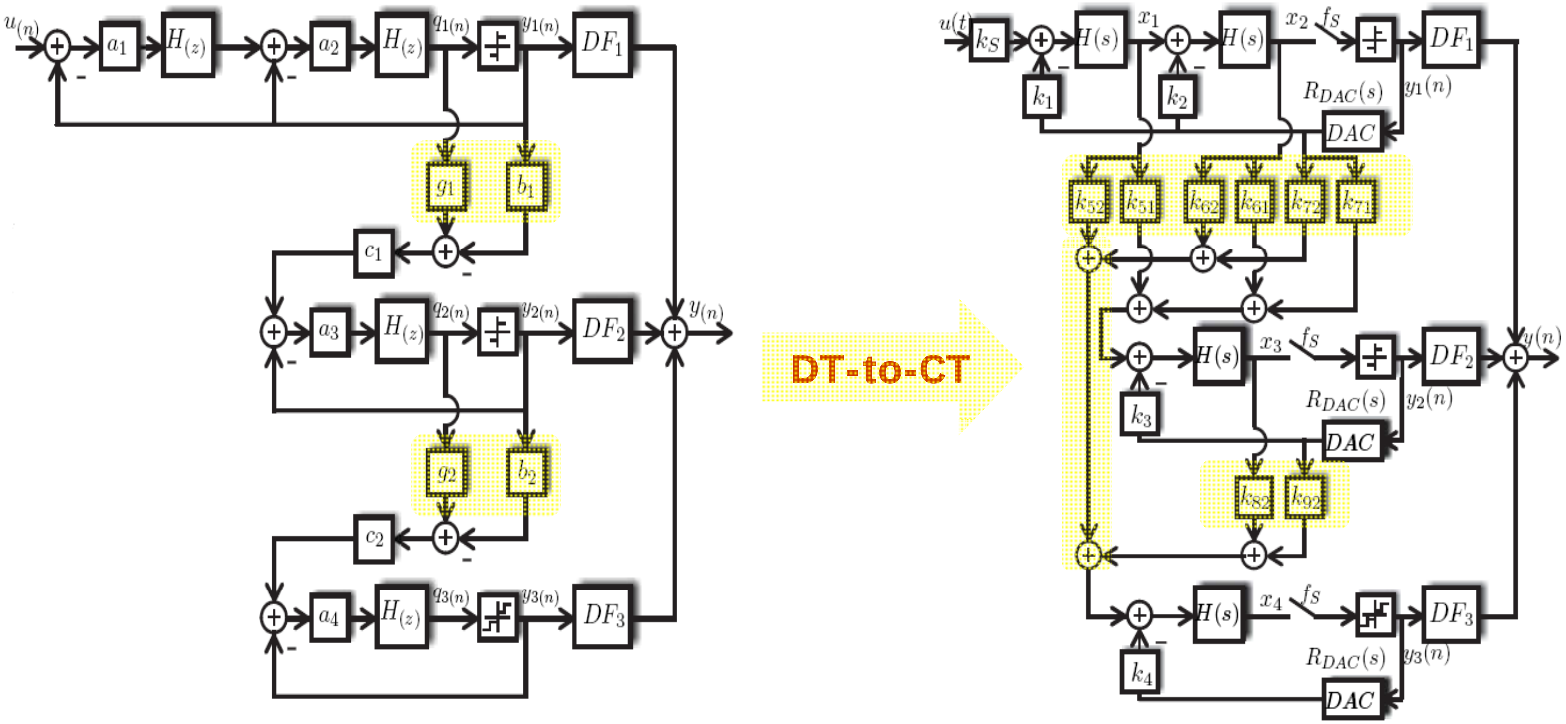
Equivalent DT system

$$\mathbf{x}[n+1] = \mathbf{A}\mathbf{x}[n] + \mathbf{B}y[n]$$
$$w[n] = \mathbf{C}\mathbf{x}[n].$$

$$\mathbf{A} = e^{\mathbf{F}T}$$
$$\mathbf{B} = \left[\int_{0}^{T} e^{\mathbf{F}(T-\lambda)}h_{\mathrm{da}}(\lambda)d\lambda\right]\mathbf{G}$$

Application of DT-to-CT method to cascade CT ΣΔMs

- Every state variable and DAC output must be connected to the integrator input of the ulterior stages in the cascade [Ortm01]
- Increases the number of analog components (transconductors and amplifiers)



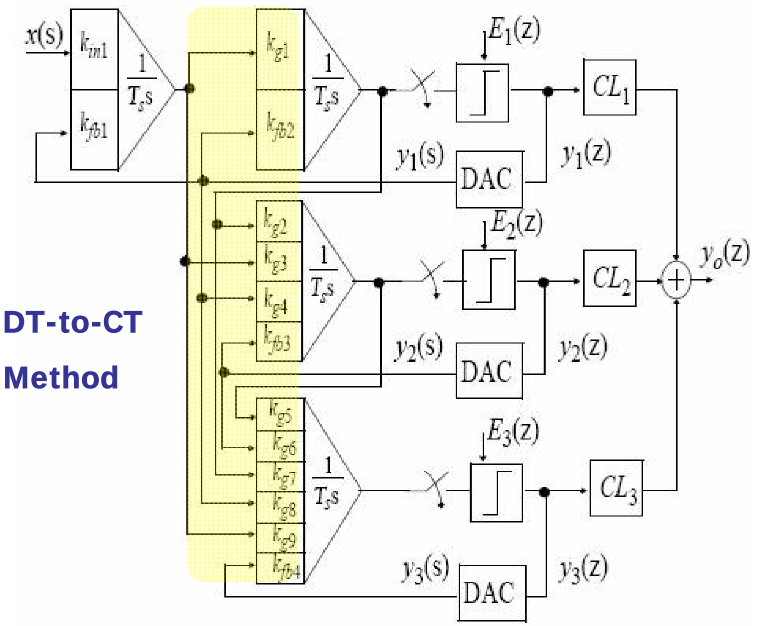
❒ Direct synthesis method [Bree01]

- Uses the desired NTF as a starting point, (as for the DT case)
- An Inverse Chevychev distribution of the NTF zeros has advantages in terms of SNR and stability

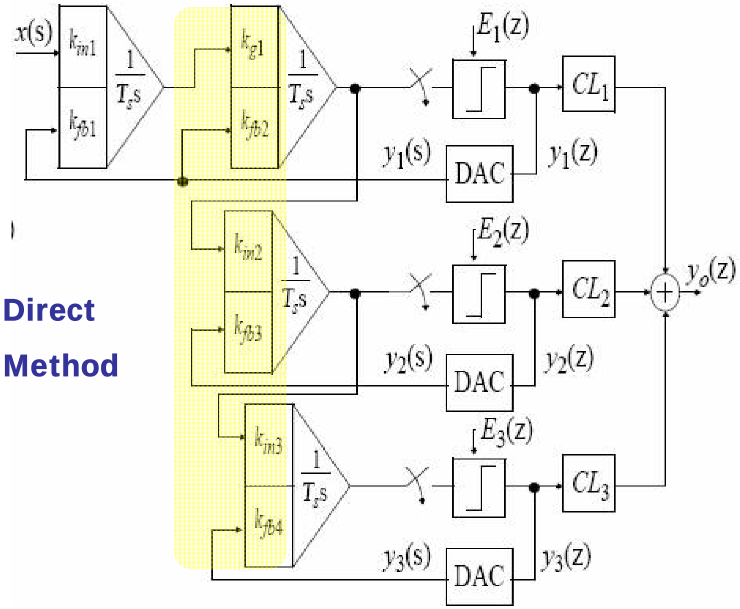
❒ Application to cascade architectures [Tort06]

- Optimum placement of poles/zeroes of the NTF
- Synthesis of both analog and digital part of the cascade CT ΣΔ Modulator
- Reduced number number of analog components

DT-to-CT Method

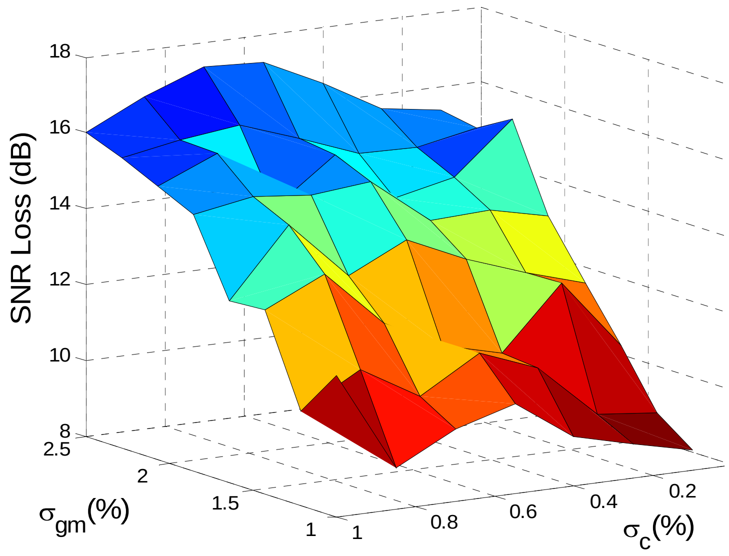


Direct Method

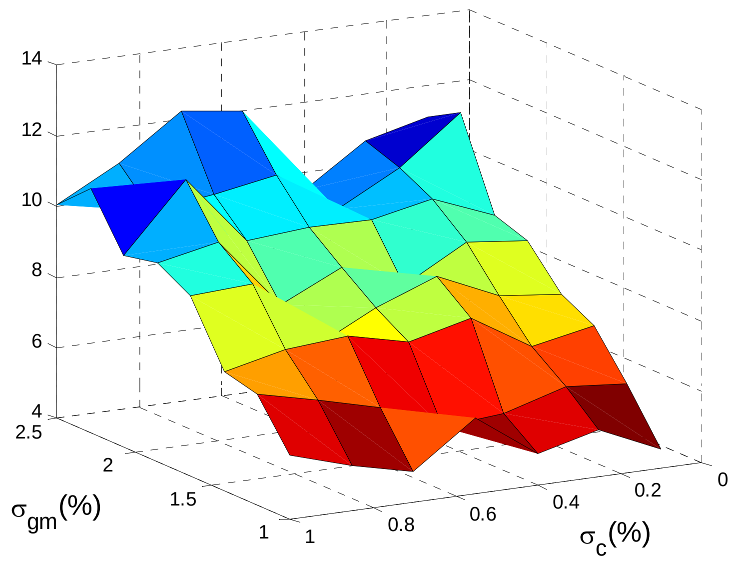


Direct synthesis of cascade architectures (I) [Tort06]

- Sensitivity to mismatch (gm,C)
- A 2-1-1 example

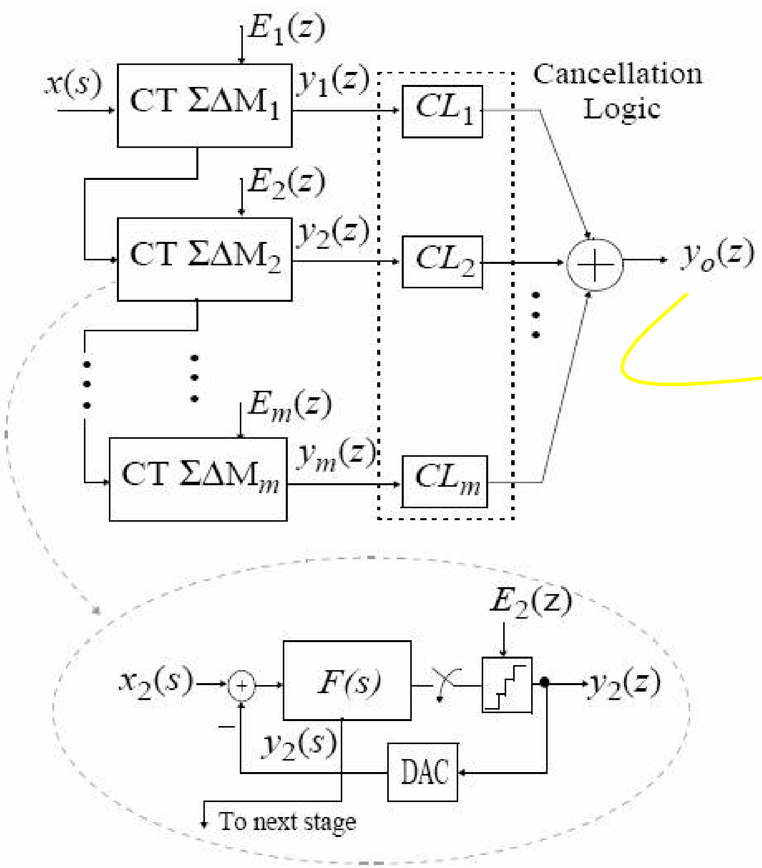


- DT-to-CT synthesis method



- Direct synthesis method

Direct synthesis of cascade architectures (II) [Tort06]



$$y_o(z) = \sum_{k=1}^{m} y_k(z) CL_k(z)$$

$$y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z_{ik} y_i(z)}{1 - Z_{kk}}$$

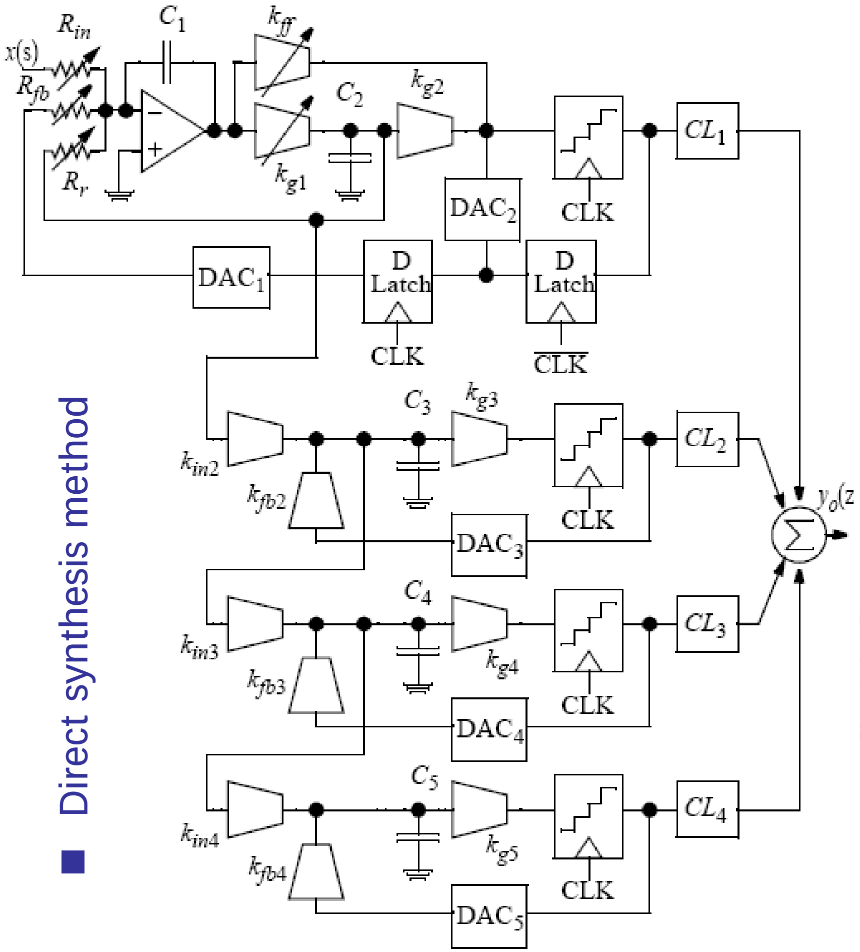
$$CL_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{mm}}$$

$$\left[Z_{km} \equiv Z\left(L^{-1}(H_D F_{km})\big|_{nT_s}\right)\right]$$

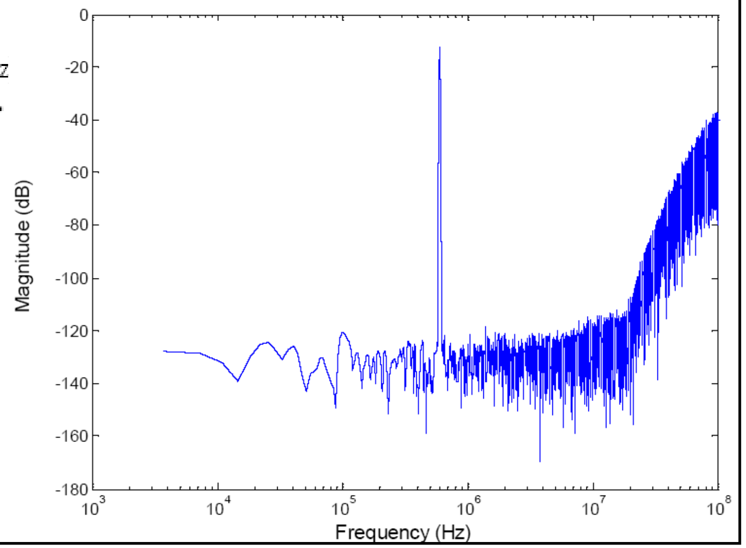
CT-ΣΔ Ms: Synthesis methods

- A case study: A 12-bit@20MHz, 4-b, 2-1-1 CT ΣΔM for VDSL [Tort06]

- Direct synthesis method



Parameter	Value
R_{in}, R_{fb}	1kΩ
R_r	2.9kΩ
$k_{g2} \dots k_{g5}$	50µA/V
k_{g1}	500µA/V
k_{ff}	120µA/V
$k_{in2} \dots k_{in4}, -k_{fb2} \dots -k_{fb4}$	450µA/V
C_1	7.5pF
$C_2 \dots C_5$	1.875pF



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