mmW Design in Silicon

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Outline

- Target applications for the Millimeter-wave frequency band
- Silicon technologies to address mmW complete solutions
  - Active devices on bulk and SOI technologies
  - Passive devices
- Silicon integrated solutions for mmW circuits
  - LNA mmW designs
  - Down-conversion mixers for mmW
  - Voltage controlled oscillators for mmW
  - Power amplifiers for mmW
  - mmW Assembly
- **Conclusions**

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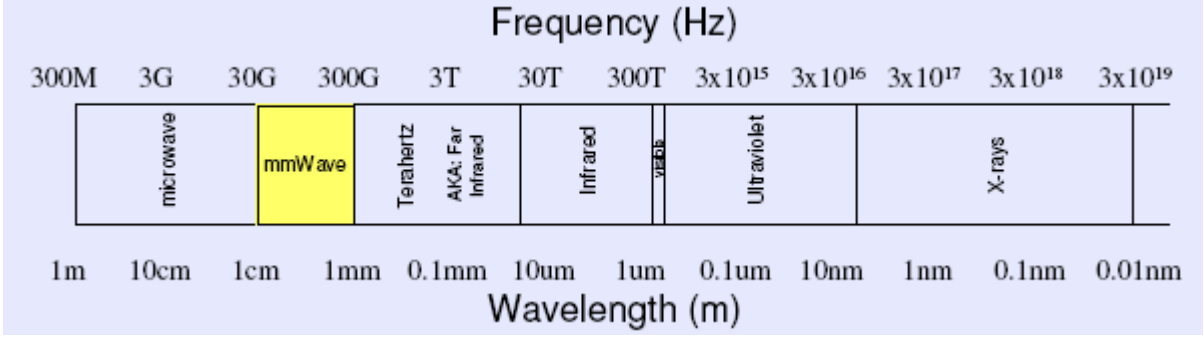
- **Conclusions**

Why the millimeter-wave (mmW) band?

- 30GHz to 300GHz frequency band ⇗ larger bandwidth
  - E.g. 5% of 60GHz is 3GHz, while of 6GHz is 300MHz
  - Enhances communications with very high speed data rate
- 10mm down to 1mm wave-lenght band ⇗ reduced size antenna
  - Enhances reduced area SiP/SoC integration
  - Better resolution for radar or imaging applications



Bandwidth Considerations

Standards / Bands	Central Frequency	Bandwidth	BW/Fc
GSM	900MHz	25MHz	~ 3%
DCS	1800MHz	25MHz	~ 1.5%
WCDMA B1	2150MHz	60MHz	~ 3%
BlueTooth / 802.11b/g	2400MHz	80MHz	~ 3%
UWB MBO	4GHz	500MHz	12.5%
802.11a	5GHz	Max 100MHz	Max 2%
802.15.3c*	60GHz	~ 7GHz	~ 12%
ACC 77GHz	77GHz	1GHz	~ 1.5%
UWB 79GHz	79GHz	4GHz	~ 5%

Wave-length considerations

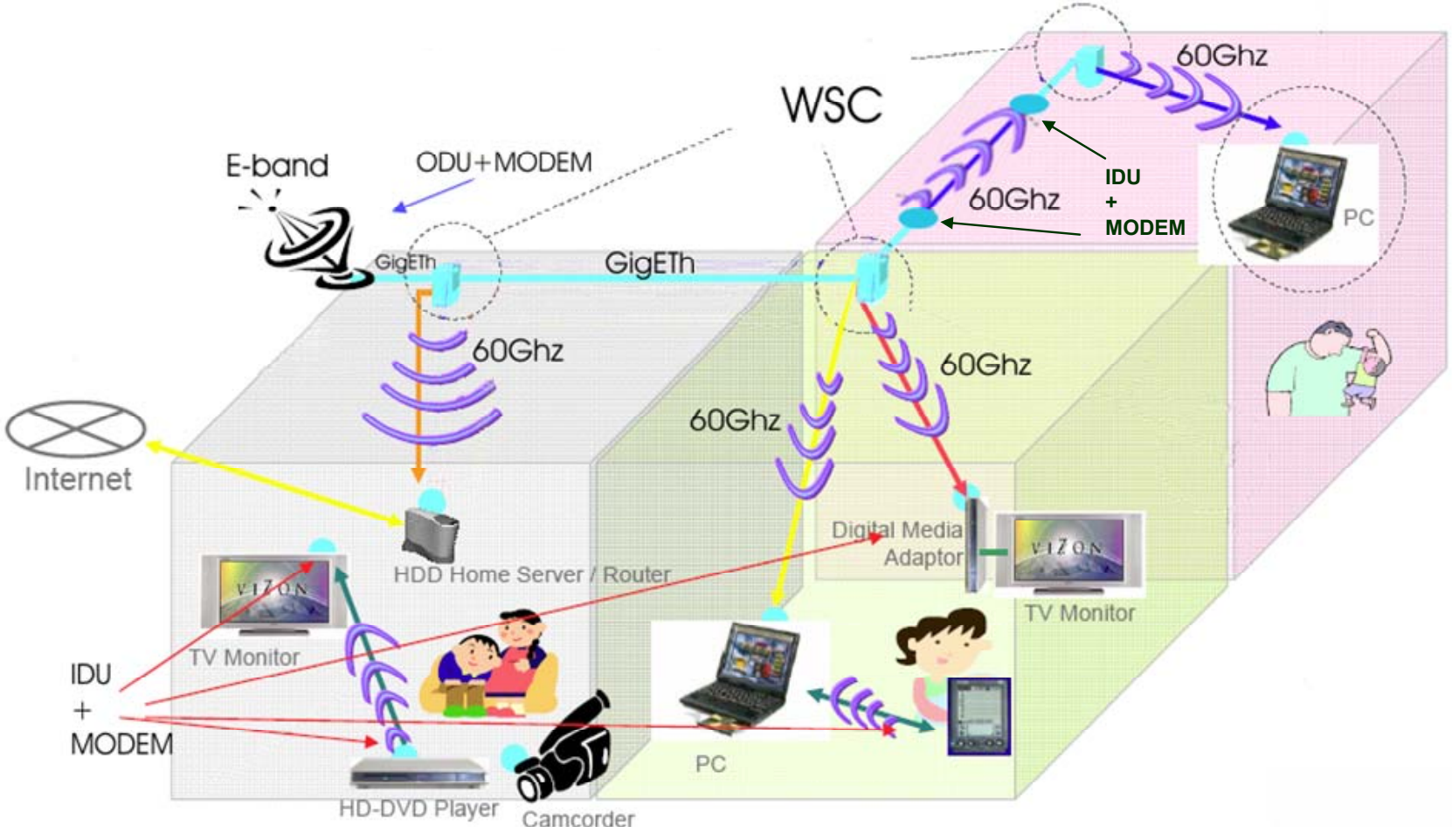
Bands	Frequency range	Vacuum λ range	Silicon λ range (*)
L Band	1 To 2 GHz	15 To 30cm	6 To 20cm
S Band	2 To 4 GHz	7.5 To 15 cm	3 To 10 cm
C Band	4 To 8 GHz	3.75 To 7.5 cm	1.5 To 5 cm
X Band	8 To 12 GHz	2.5 To 3.75 cm	1 To 2.5 cm
K_u Band	12 To 18 GHz	1.6 To 2.5 cm	0.6 To 1.7 cm
K Band	18 To 26 GHz	11.5 To 16.6 mm	4.5 To 11 mm
K_a Band	26 To 40 GHz	7.5 To 11.5mm	3 To 7.5 mm
Q Band	30 To 50 GHz	6 To 10mm	2.3 To 6.3 mm
U Band	40 To 60 GHz	5 To 7.5 mm	2 To 5 mm
V Band	46 To 56 GHz	5.3 To 6.5 mm	2.1 To 4.2 mm
W Band	56 To 100 GHz	3 To 5.3mm	1.2 To 3.5mm

(*) Hypothesis : Silicon ε_R = 3.2 To 4.7

mmW Communications Application Fields at a Glance

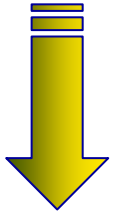
- High data-rate communications
  - Last Inch applications (57 to 66GHz bands)
    - Wireless HDMI video streaming
    - Short Range Ultra fast file transfer
  - Last Mile applications (71-76GHz, 81-86GHz licensed E-bands)
    - Telecom backhauls
- Low data-rate communications (94GHz, >100GHz bands)
  - Sensor network applications
- Automotive applications
  - Radar items:
    - Long range radar (ACC) (76-77GHz bands)
    - Short range radar (Stop & Go) (77-81GHz bands)
  - Ground to vehicle and vehicle to vehicle links (see HDR communications)
- Optical communications
- Chip to chip wireless communications

Example 1: Indoor network scenario and interfacing to the outdoor network

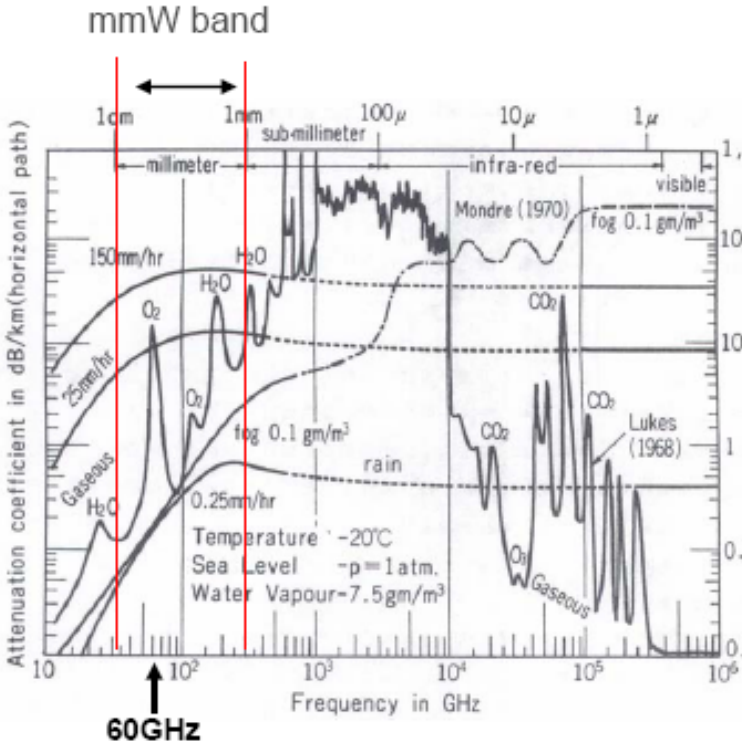


EM Propagation conditions in the mmW band

- Rain attenuation ~ 5dB/km in the 60GHz band
- Atmospheric oxygen absorption: 17dB/km in the 57 to 64GHz band

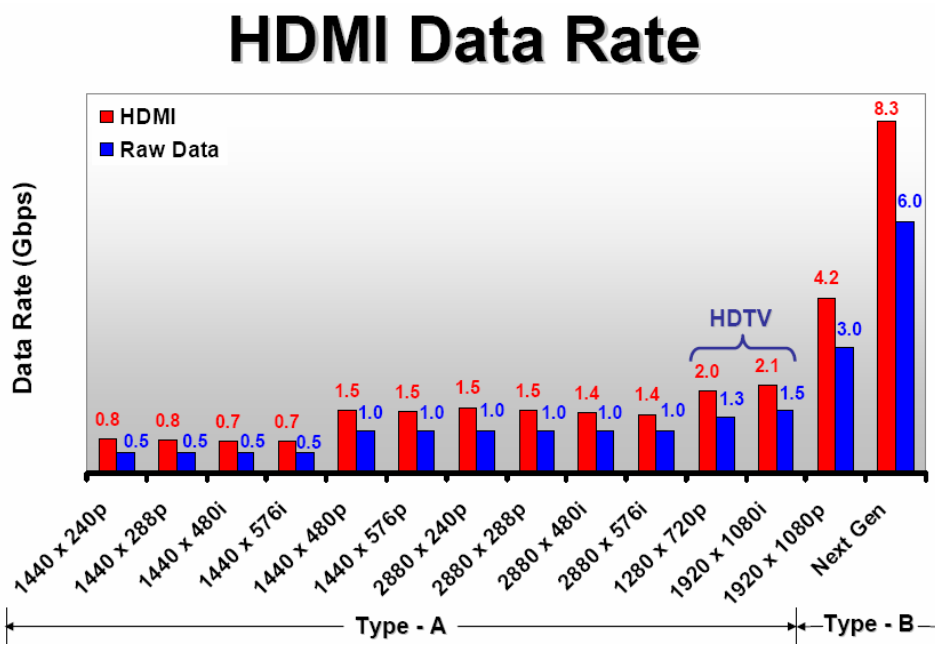


- short-range radio links with excellent immunity to blockers and intrusions
- frequency re-use (larger number of users)



Focus 1: Wireless HDMI Application Fields

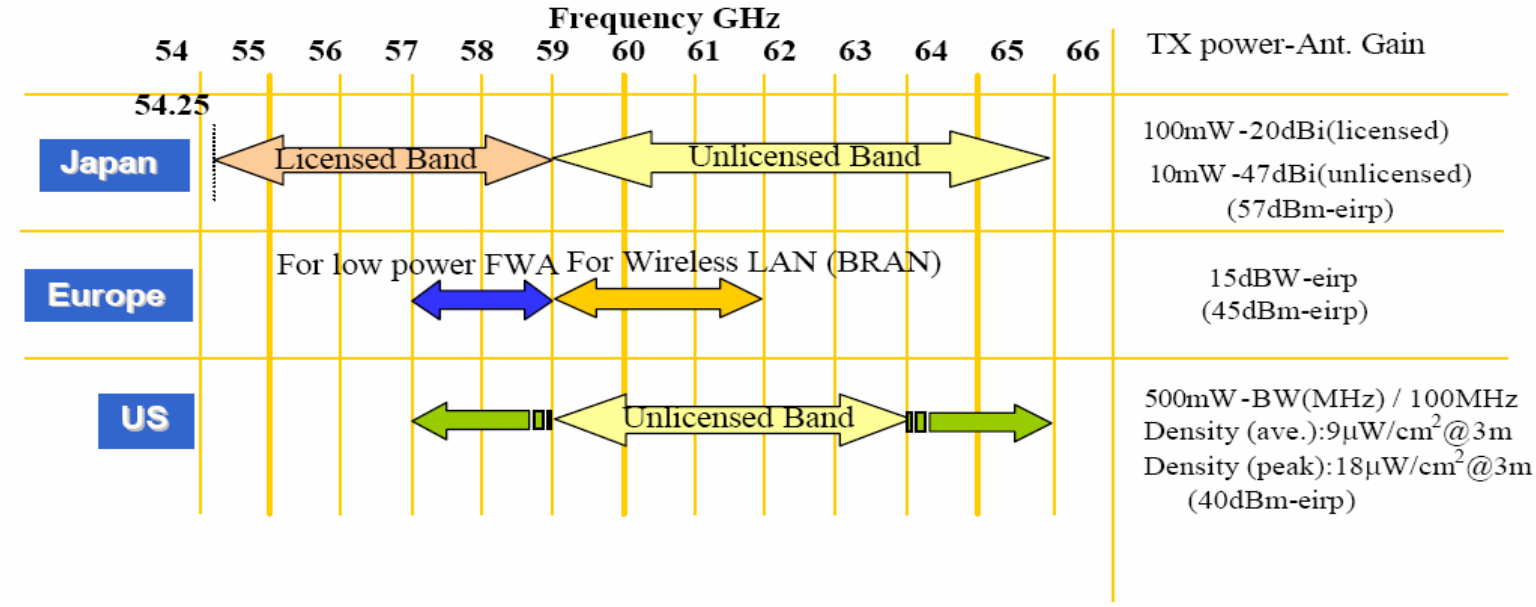
- Communications between nomadic devices (such as pocket HD, …)
- Communications between/with mobile devices such as: digital (still) cameras, mobile phones, PDAs
- HD video transmission on home TV's



ITEM	Dial up	Brodband	Wireless LAN				W PAN	Gigabit	
			11.b	11.a	11.n	11.n	UWB		
Data Rate	55 kbits	1,5 Mbits	11 Mbits	55 Mbits	100 Mbits	400 Mbits	500 Mbits	1 Gbits	2,5 Gbits
Complete work of Skakespeare (5 Mbytes)	12 min	27 sec	3,6 sec	0,8 sec	0,4 sec	0,1 sec	0,08 sec	0,04 sec	0,016 sec
CD-ROM (650 Mbytes)	1,1 days	58 min	7,8 min	1,6 min	52 sec	13 sec	10,4 sec	5,2 sec	2,1 sec
120 minute movie - TV quality (1 Gbyte)	1,7 days	1,5 hrs	12 min	2,4 min	1,4 min	21 sec	16 sec	8 sec	3,2 sec
120 minute movie - DVD (4,2 Gbytes)	6,9 days	6,2 hrs	50 min	10,2 min	5,6 min	1,4 min	1,12 min	34 sec	13,5 sec

60GHz Bands Licensing

- Several task groups work towards standardization:
  - IEEE 802.15.3c
  - ECMA TC48 in WiMedia frame
  - WirelessHD



On-going standardization in the 60GHz Band

Group	Forecasted by:	Characteristics	Web link
IEEE 802.15.3c (TG3c)	May 2009	PHY layer Standard based on millimeter waves. Target band-pass is 1-2 Gbit/s	www.ieee802.org/15/pub/TG3c.html
ECMA – TC48 (ex TC32-TG20)	Mid 2009	PHY+MAC Standard, low power, data rate 2-10 Gbit/s retro-compatible with HDCP part of HDMI	www.ecma-international.org/memento/TC48-M.html
WiMedia		Alliance which standardizes the UWB communications protocols. For the 60GHz band it is synchronized with TC48.	www.wimedia.org

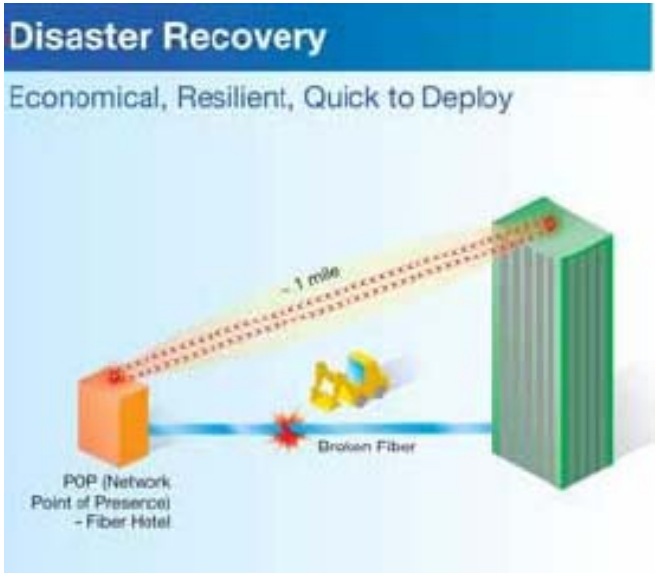
Focus on the 60GHz HDR standardization

- Data rate should be between 50Mb/s and 6Gb/s
- The channel size should be:
  - 1 GHz for Half rate approach
  - 2GHz for Full rate approach
- Two options are examined for the Modulation scheme:
  - Single Carrier: OOK,BPSK,GMSK,QPSK,8QAM,16QAM…
  - OFDM: BPSK,QPSK,16QAM,64QAM
- About the Antenna set-up:
  - Directive
  - Beam Forming
- So far, Impulse Radio seems to be abandoned for Device to Device communications

Example 2: Outdoor networks

Alternative Access
Access Diversity
Disaster Recovery

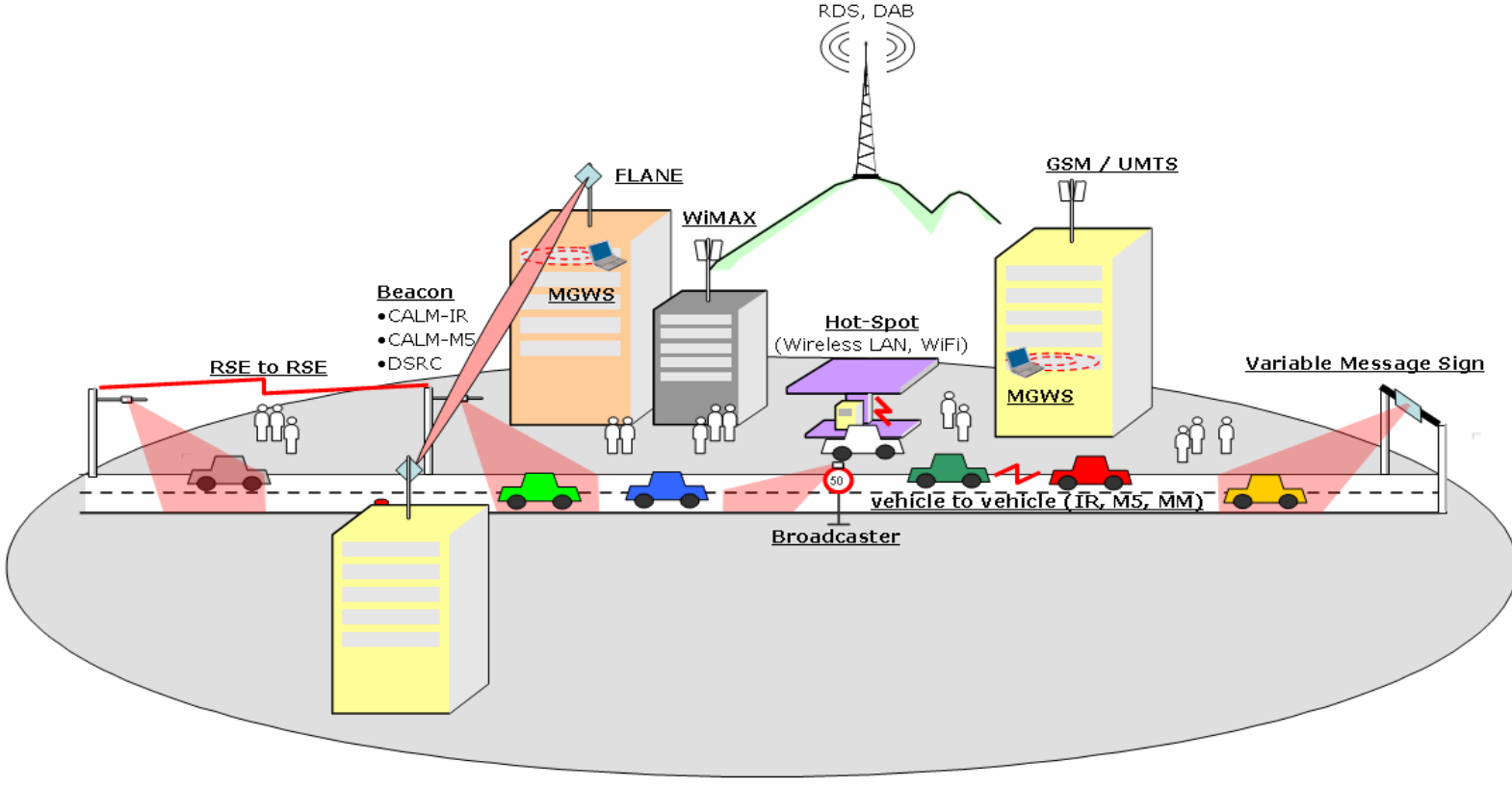
Wireless Backhaul
2G – 3G – 4G
WiFi – WiMAX



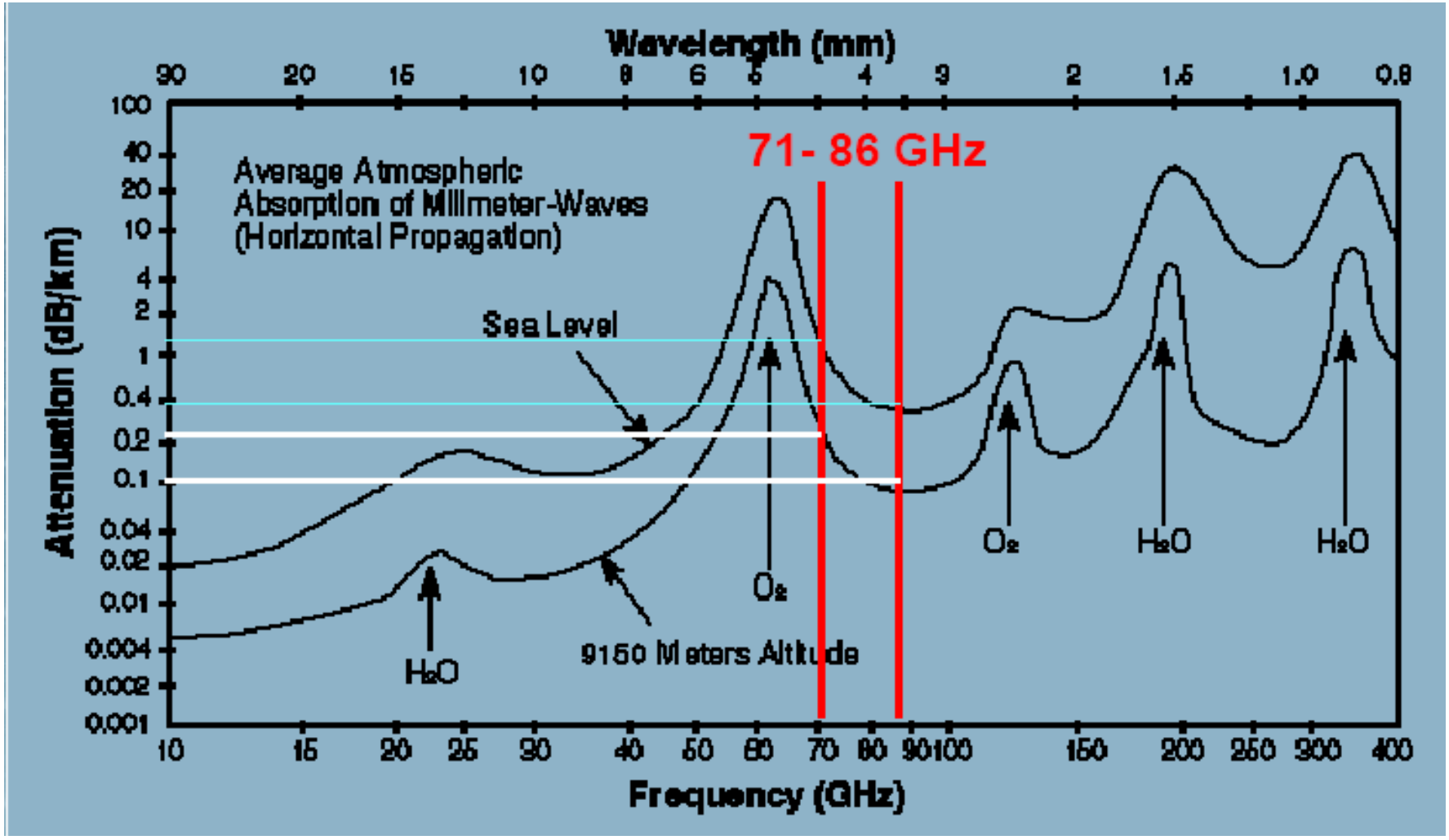
71 – 76 GHz ; 81 – 86 GHz; 92 – 95 GHz Bands
For 1 to 2 Km applications

Focus 2: Point to point link in an Intelligent Transport System

- Point-to-point links in the backbone of the Intelligent Transport System (ITS)
- Typical distance between ITS Road Side Equipment (RSE) to RSE is 300m.

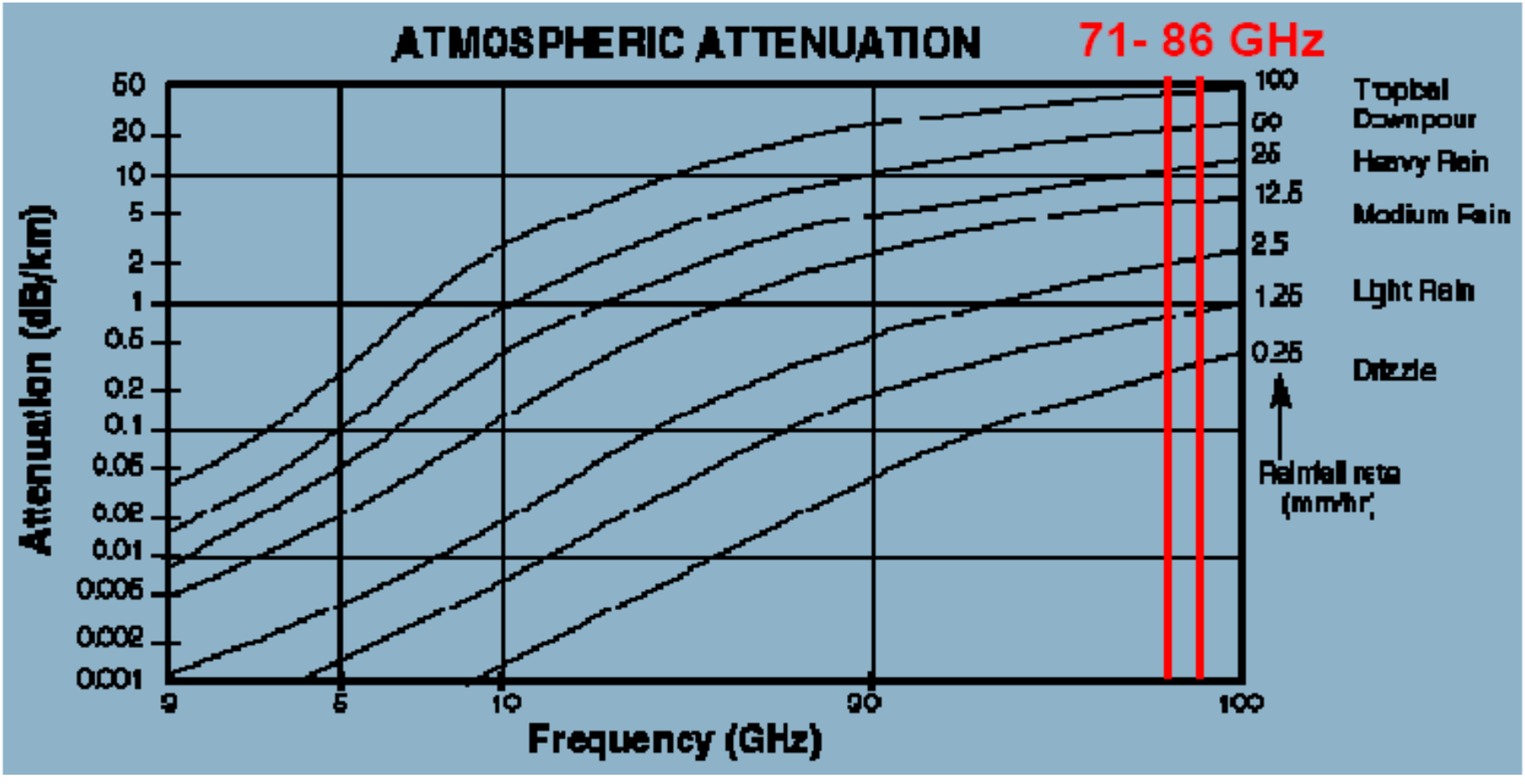


Atmospheric Absorption in 70GHz – 95GHz



From 70 to 95 GHz, oxygen absorption negligible less than 1 dB/km

Rain Losses in 70GHz – 95GHz



Light rain < 1 dB/km
Heavy rain = 10 dB/km
Downpour = 30 dB/km

Sand, dust, fog, snow, etc have no significan effect attenuation at mm-waves

Standardization for Outdoor Network

- US FCC Allowance:
  - 3 Allowed Bands:
    - 71-76 GHz; 81-86 GHz ; 92-95 GHz
  - Emitted Isotropic Radiated Power:
    - 55 dBW EIRP at 50 dB antenna gain
    - 41 dBW EIRP at 43 dB antenna gain
- European regulatory status:
  - 2 Bands approved by European regulators (EU and CEPT):
    - 71-76 GHz; 81-86 GHz
- World Wide regulatory status:
  - Goal is worldwide common radio band Goal is worldwide common radio band and spectrum rules.
  - Positive Feedback from Bahrain, Jordan, Australia, South Africa, Ghana, Nigeria, India, China, Brazil, Mexico, Canada

Example 3: Automotive applications contributing to road safety

For Safe speed & Safe following:

- Communication technologies to improve the detection, locating and evaluation of hazards
- New sensorial devices integrating obstacle detection and communication

For Lateral Support & Driver Monitoring:

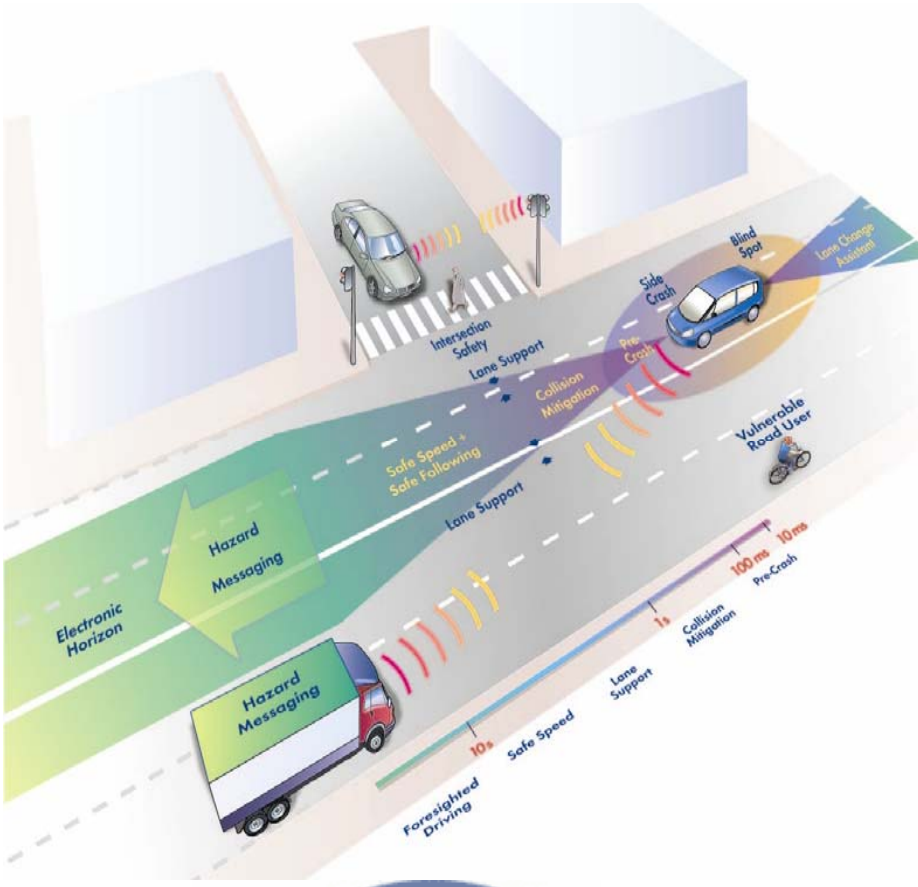
- Lane-keeping support system for situations with poor road and environmental conditions

For Intersection Safety:

- Concepts for sensors and communication aimed to road markings and crossing traffic recognition

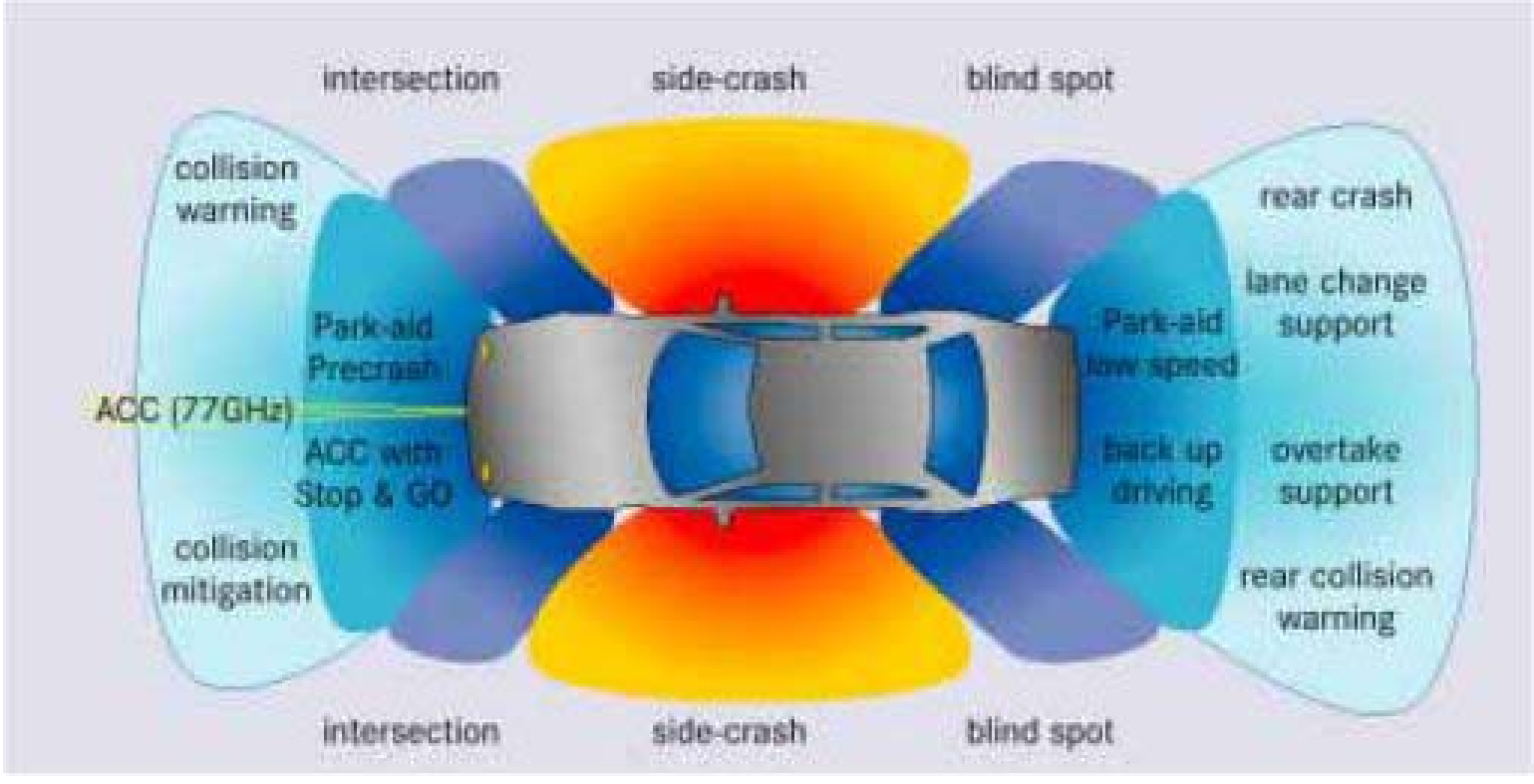
For Vulnerable Road Users & Collision Mitigation:

- Active 3D sensor technology for pre-crash and blind spot surveillance
- Location and classification of obstacles (cars, pedestrians, bikes, etc.)



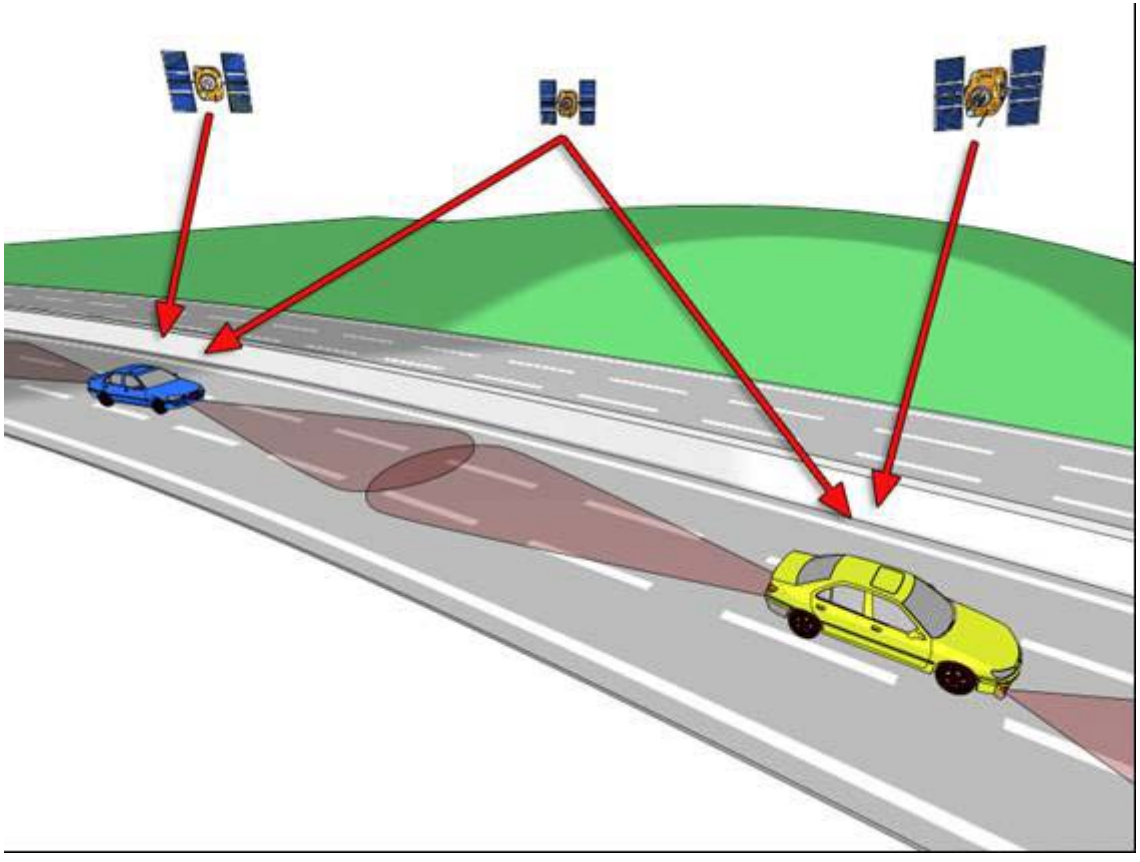
PReVENT

Focus 3: Automotive radar



Long Range 77GHz and Short Range UWB 79GHz Radars

Focus 3: And Smart vehicle …



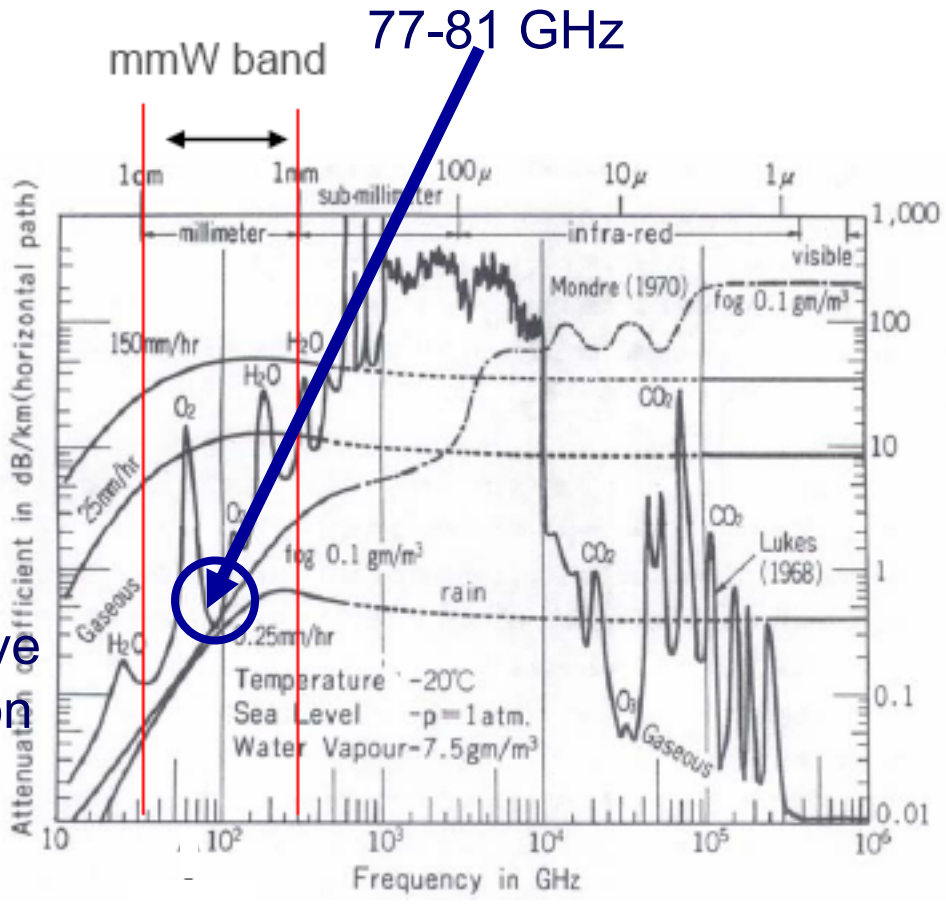
Communicating Vehicle in 60GHz or 79GHz Bands with absolute Positioning GPS or Gallileo

Atmospheric Attenuation

From 77 to 81 GHz, oxygen absorption is negligible less than 1 dB/km

Light rain < 1 dB/km
Heavy rain = 10 dB/km
Downpour = 30 dB/km

Sand, dust, fog, snow, etc have no significant effect attenuation at mm-waves



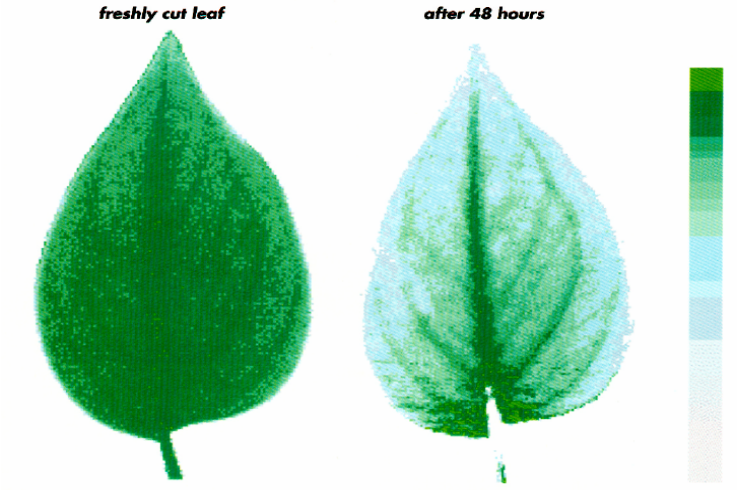
Standardization for Automotive Radar and Car to Car communications

- US FCC and ETSI Allowances:
  - 3 Allowed Bands for Automotive Radar:
    - 24 GHz (SRR) (up to 2012 in Europe: contest from Telecom and Spatial industries)
    - 76-77 GHz (LRR)
    - 77-81 GHz (SRR)
  - Emitted Isotropic Radiated Power in Europe:
    - 42 to 55 dBm EIRP for Short Range Radar
    - 55 dBm EIRP for Long Range Radar
  - 3 Allowed Bands for Car to Car Communications
    - 5-6 GHz with a contest from telecom industry
    - 64 GHz
    - 77-81 GHz

- World Wide regulatory status:
  - The 3 Radar Bands are allowed, and the 3 Car to Car too, up now.

Example 4: Emerging mmW imaging

www.millivision.com/images/HandHeldNew.jpg



- Security non-intrusive investigations
- Medical/biological imaging
- 94GHz and 120GHz Bands are allowed by FCC
- No standardization yet defined

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- **Conclusions**

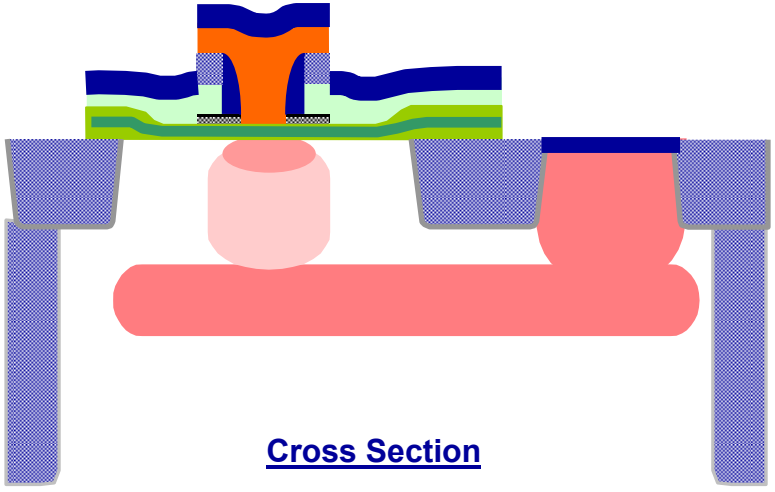
How did we get to Silicon technologies for mmW designs?

- mmW market held since decades by the III-V semiconductors
  - Niche market w.r.t. the total market volume in all SC industry
  - III-V SC show high manufacturing cost and reduced integration scale
- Since several years, full Silicon technologies become the technology integration platforms for mmW
  - **Technical Enabler**: the very high frequency performances of Si active devices
  - **Marketing Enabler**: the need for low-cost consumer products in the mmW frequency range

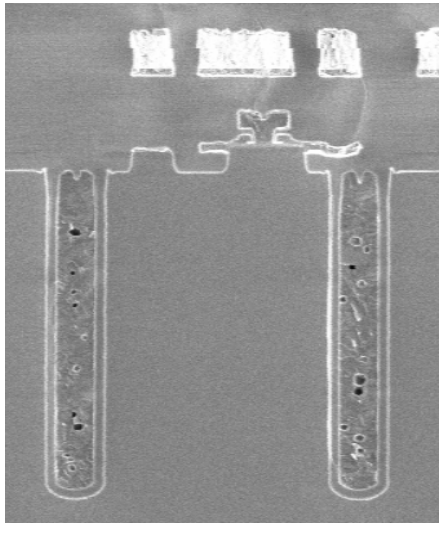
Silicon Technologies for mmW

- SiGe-C HBT:
  - 130nm HBT mmW technology.
- Nanometric CMOS Bulk:
  - 65 nm CMOS LP technology.
- SOI CMOS :
  - 65 nm CMOS LP HR SOI technology.

SiGe-C HBT Technology



Cross Section



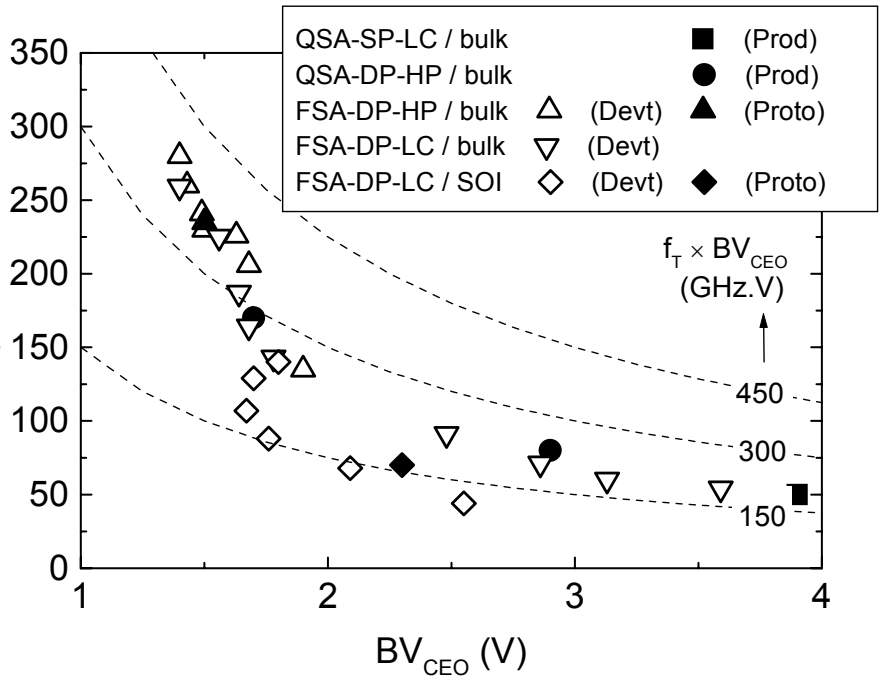
SEM Pictures

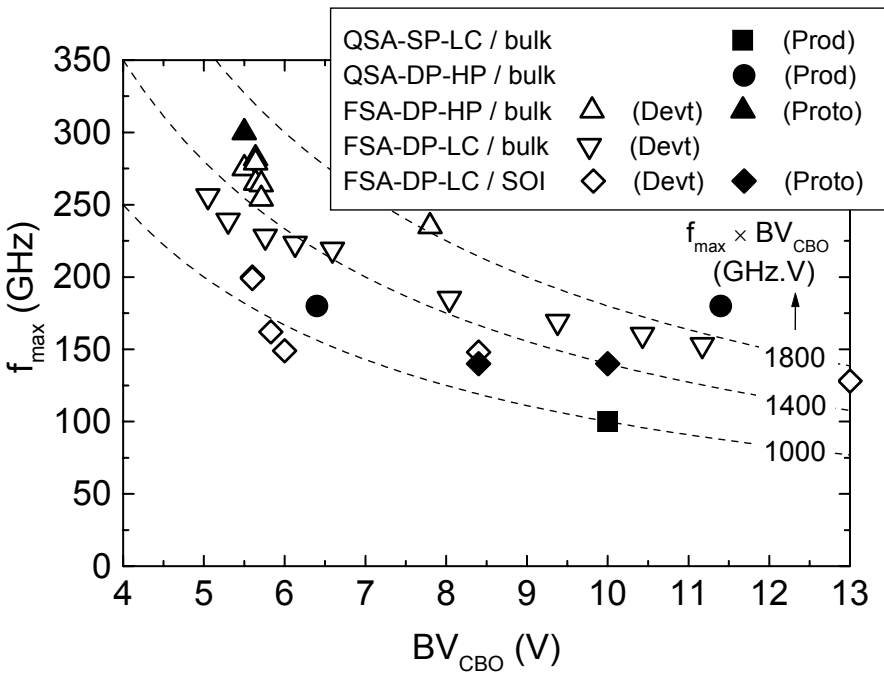
Substrate Resistivity: Medium resistivity (~10 Ω.cm) → substrate losses

Solution: High Altitude Thick metal layers (2) to reduce drastically the substrate losses

High Ft and Fmax transistors: up to 400GHz in research step.

130nm node SiGe:C HBT devices RF performances

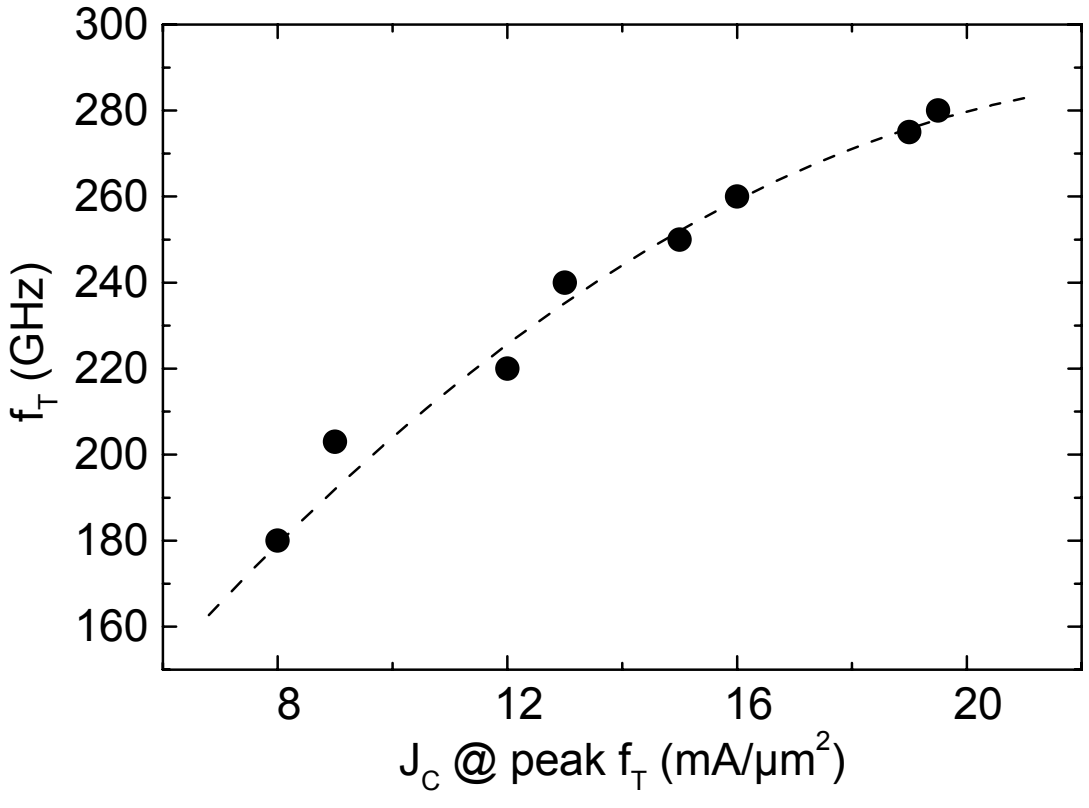




- Devices developed on purpose for high frequency/high speed operation mode
- High speed performance: f_T>200GHz, f_{max} > 300GHz obtained with FSA E-B architectures and HP collector
- Advantages over CMOS 65nm node: lower *1/f* noise, higher Z_{out}, higher voltage capability for a given speed
- f_{max} has reduced sensitivity to layout parasitics

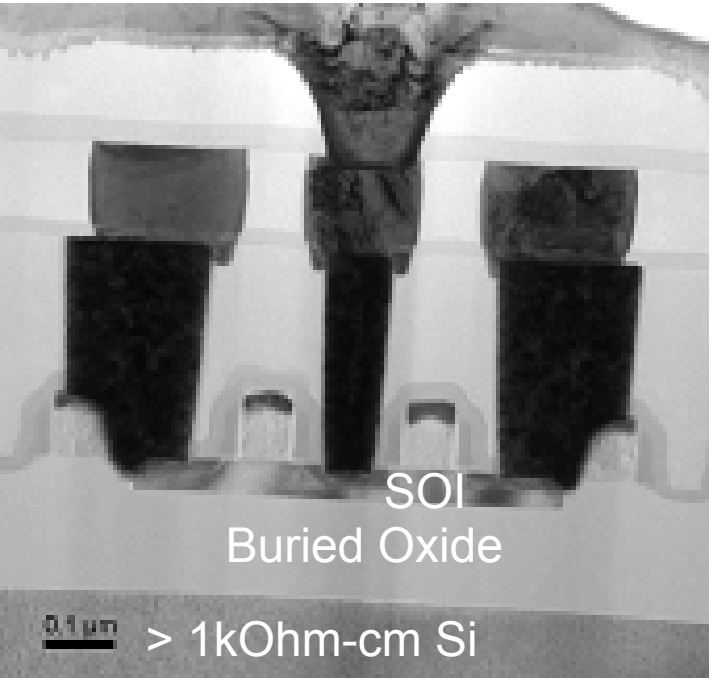
P. Chevalier, et al., ESSCIRC 2006 workshop

SiGe:C HBT scaling feature

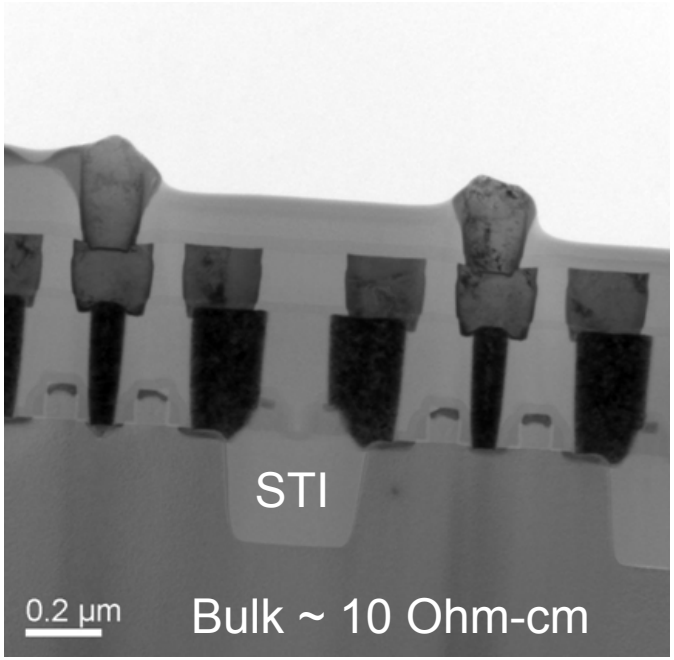


- Peak f_T occurs for different collector current densities across the technology nodes

Thin CMOS SOI/bulk LP RF technologies



65nm LP SOI technology
STMicroelectronics



65nm LP Bulk technology
STMicroelectronics

Medium resistivity (~10 Ω.cm) in bulk technologies → substrate losses

High resistivity (~1 KΩ.cm) cannot be used in case of bulk due to latch-up issues

- Solution: very good isolation and reduced losses thanks to High Resistivity substrates possible only on SOI

For a given CMOS technology node, LP or HP for RF applications ?

	LP 65nm	HP 65nm
Lg (nm)	~ 60	~ 32
max Jg(A/cm2)	~ 0.025	~ 40
Istandby SRAM bitcell @ Vdd ~ 0.6V	<10pA/µm	> 1nA/µm

- High Performance (HP) processes optimizations=>for increased speed:
  - Lower nominal gate length
  - Gate oxide much thinner for HP → higher gate leakage
- Consequences for HP:
  - Large Standby power

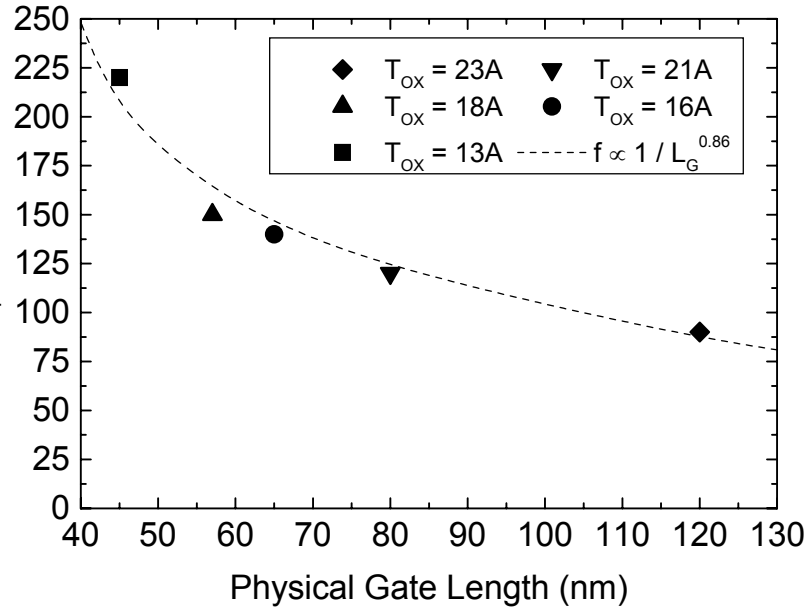
- **RF circuits are used mainly in portable products where the standby leakage is critical for the battery life**

- a mixed HP/LP process ? A two nominal gate lengths and Double Gate Oxide Process would increase too much the cost for portable products.

- **Conclusion: a pure LP process is mandatory**

Courtesy to C. Raynaud, STMicroectronics & CEA

Bulk and SOI CMOS devices RF performances

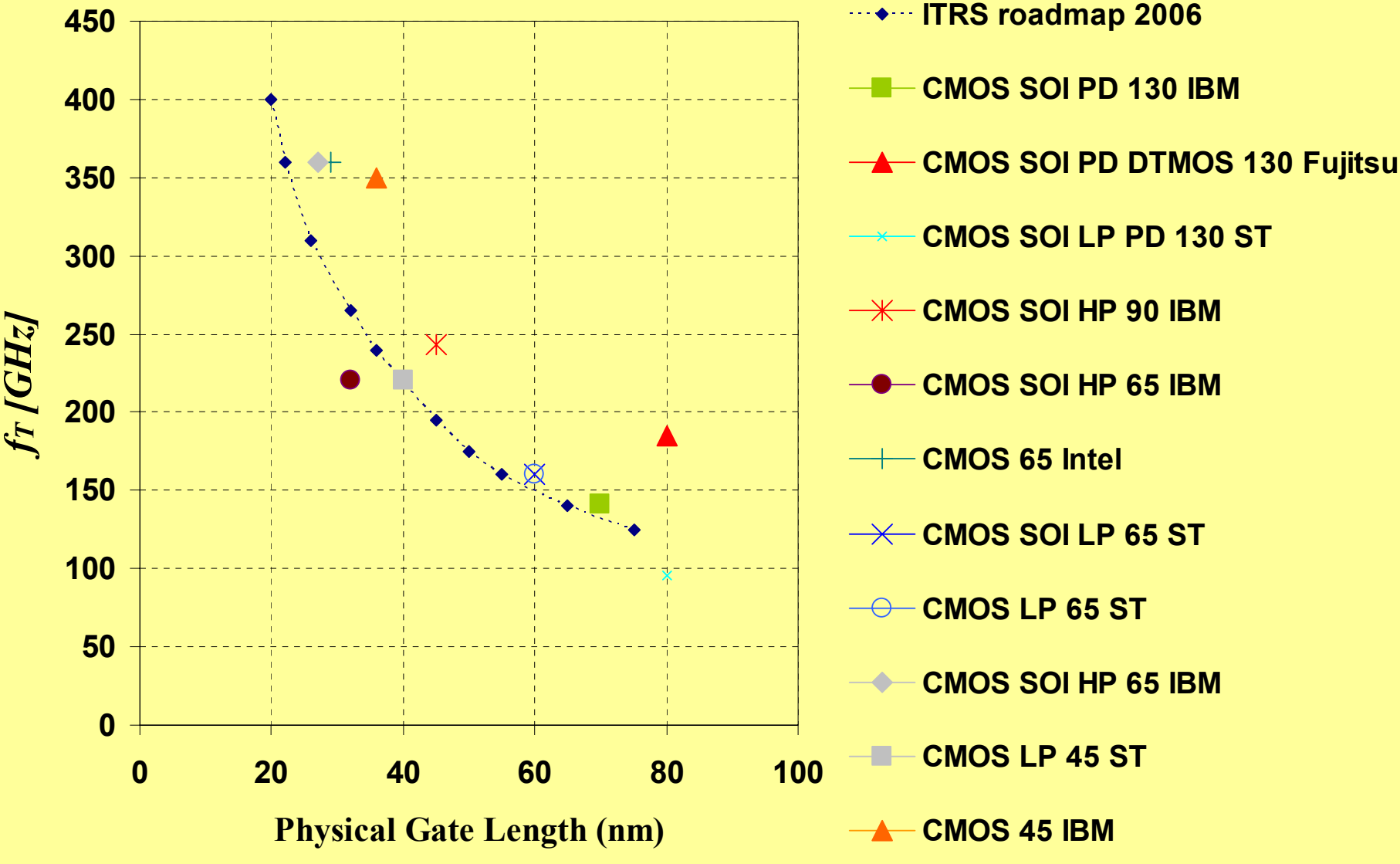


LP and GP devices

$$f_T \propto 1/L_g^{\alpha} \; (\alpha \sim 1)$$

- CMOS transistor architecture down to 65nm node: still uses poly gate, $\mu_{n,p}$ increased using several technology solutions
- Devices developed for digital applications and then fairly optimized for analog/RF
- In 65nm node, f_T values reaches 150GHz for LP devices and 200GHz for GP ones
- Bulk *AND* SOI devices show similar HF performances:
  - SOI FB CMOS suffers from Kink effect, but in HF has same characteristics as a identical layout bulk device
  - SOI BC CMOS is penalized in HF by their specific layout (Rg/ and Cgs /)

Evolution of f_T through CMOS technology nodes several foundries



Deep submicron technologies – Limitations to g_m increase

gm ∝ 1/Lg

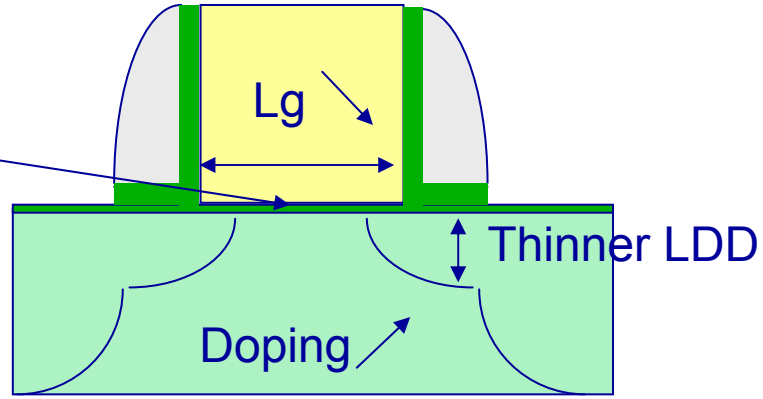
gm ∝ 1/tox

gm ∝ μ

Reduced tox

⇩

Gate tunneling current



- Gm increases with reducing Lg but gm is also degraded for advanced technologies:
- ***tox does not decrease as expected for a good scaling with Lg, due to gate leakage***
- ***Mobility degradation by doping increase***, especially to ensure Low leakage devices in a Low Power low standby current technology (less critical in the case of very Low v_T devices)
- ***Source and drain resistances increase*** due to thinner Low Doped Drain regions (same LDD depth for bulk and PD SOI technologies – thinner for ultra-thin FD SOI!)

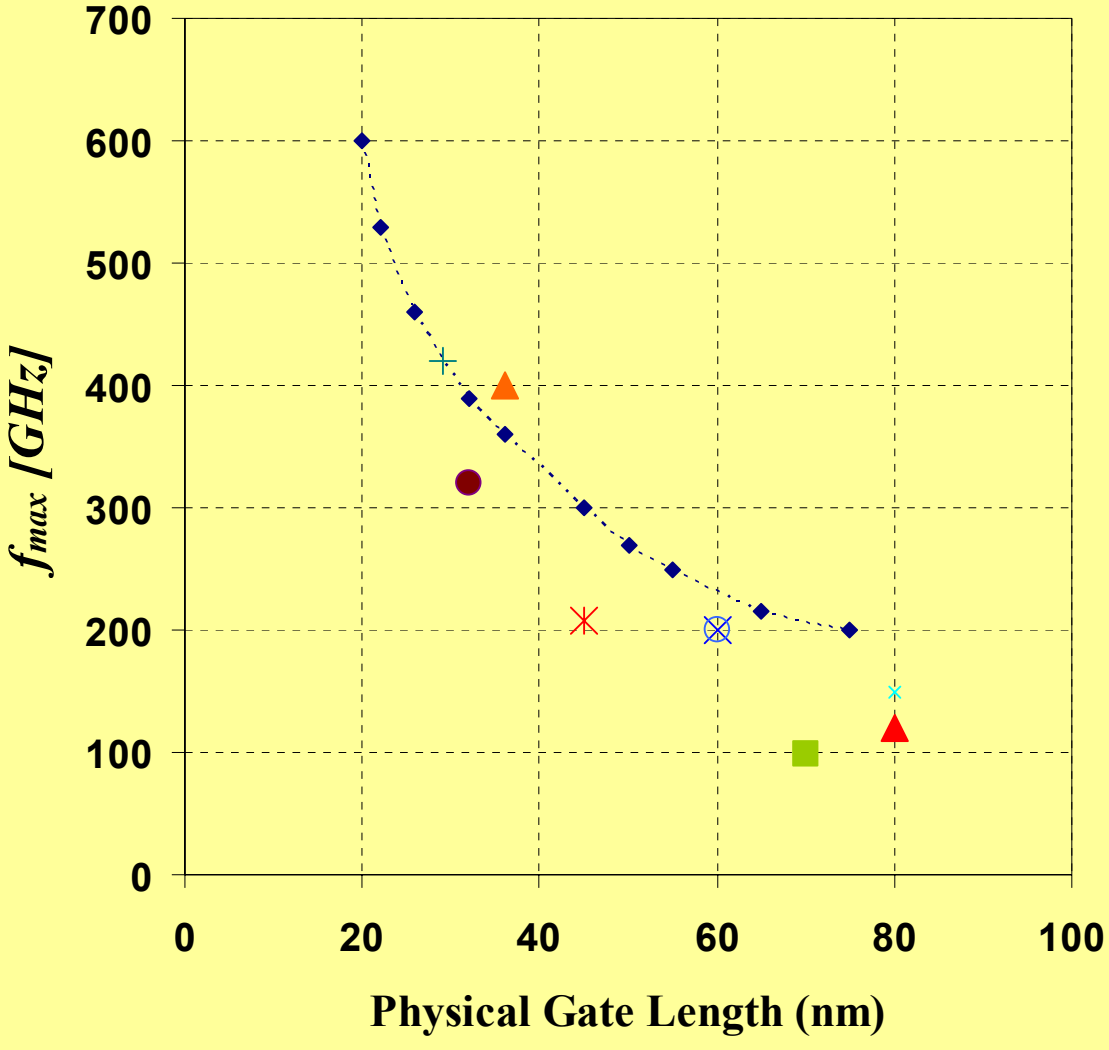
Courtesy to C. Raynaud, STMicroectronics & CEA

Deep submicron technologies – Techniques to increase g_m

- different “strain techniques” to increase mobility : Stress Memory Techniques (SMT), SiGe source-drain, stress liners, …
- use 45° rotated substrate (but valid only to increase mobility of PMOS)
- high K to limit gate leakage and decrease effective electrical gate oxide
- ultra thin SOI film to reduce doping level (v_T definition by metal gate work-function) but gate material issue to get low v_T and high v_T at the same time and influence of ultra thin SOI film + high k on mobility and low frequency noise not yet well known

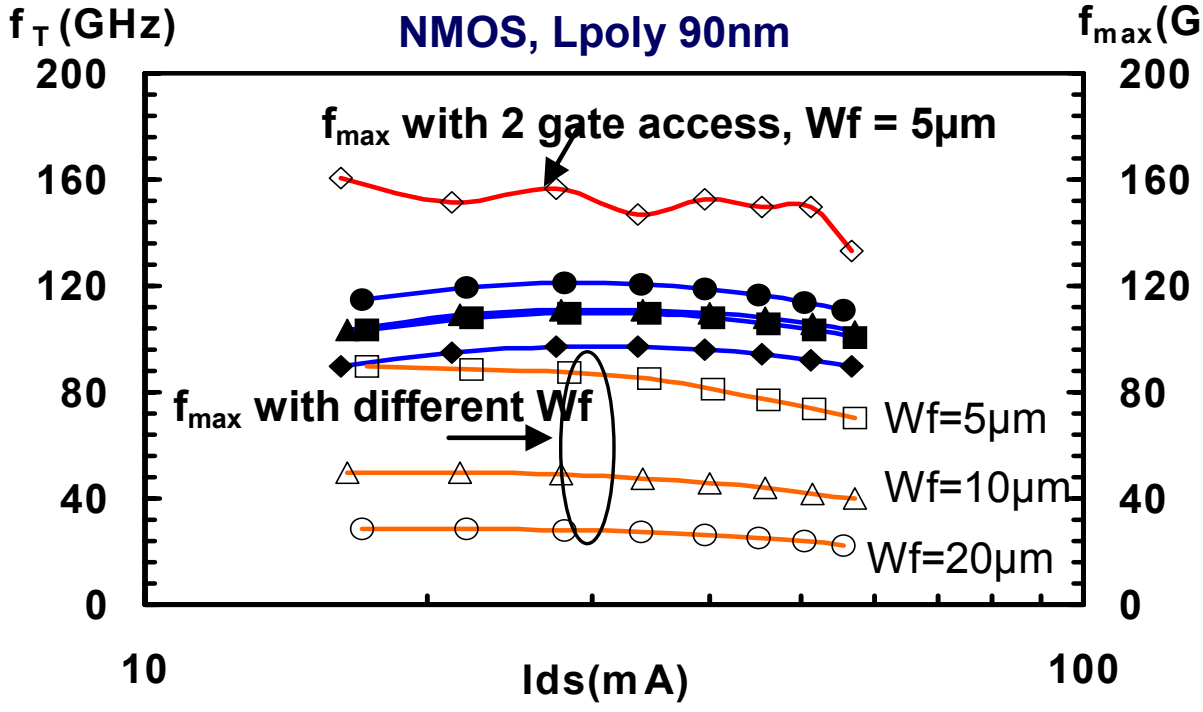
Courtesy to C. Raynaud, STMicroectronics & CEA

Bulk and SOI CMOS devices: f_{max} feature



- ITRS roadmap 2006
- CMOS SOI PD 130 IBM
- CMOS SOI PD DTMOS 130 Fujitsu
- CMOS SOI LP PD 130 ST
- CMOS SOI HP 90 IBM
- CMOS SOI HP 65 IBM
- CMOS 65 Intel
- CMOS SOI LP 65 ST
- CMOS LP 65 ST
- CMOS 45 IBM

Influence of MOS transistor layout over f_T and f_{max} parameters



130nm SOI process
STMicroelectronics

- Ft 8*(2*5*0.12) 2GA
- Ft 8*(2*5*0.12)
- Ft 2*(2*20*0.12)
- Ft 8*(1*10*0.12)
- Fmax 8*(2*5*0.12) 2GA
- Fmax 8*(2*5*0.12)
- Fmax 2*(2*20*0.12)
- Fmax 8*(1*10*0.12)

Transistor size: $n*(N_f*W_f*L_g)$ in µm

n = number of transistor cells in parallel

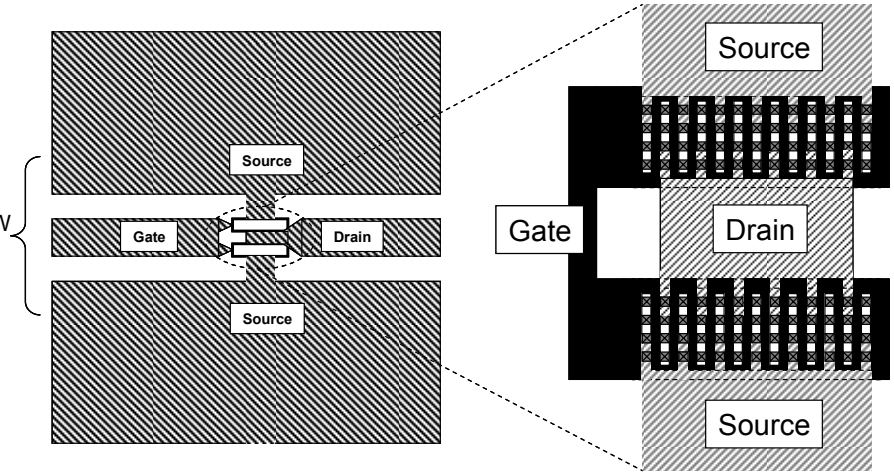
W_f = finger width

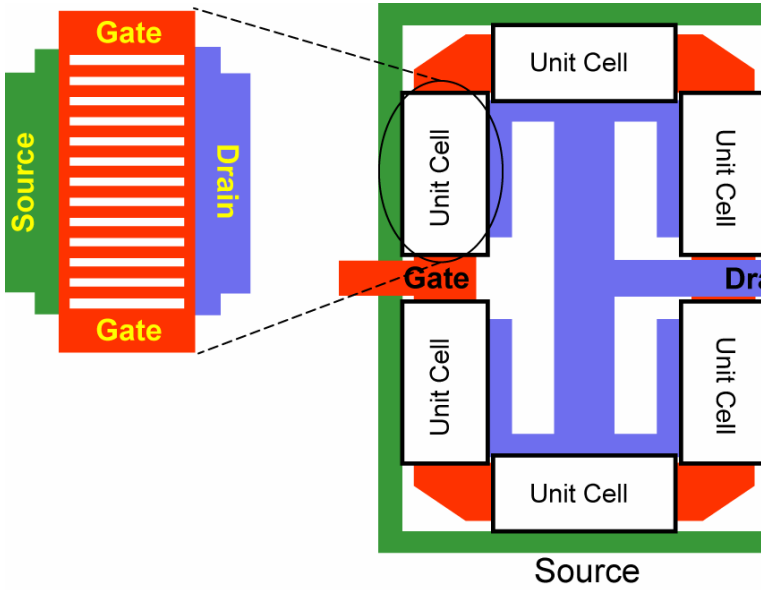
N_f = number of transistor fingers per cell

L_g = gate length

- **Optimal $W_{finger} \leq 5\mu m$**
- **Double sided gate access**

Examples: mmW NMOS transistor for maximal f_{max}





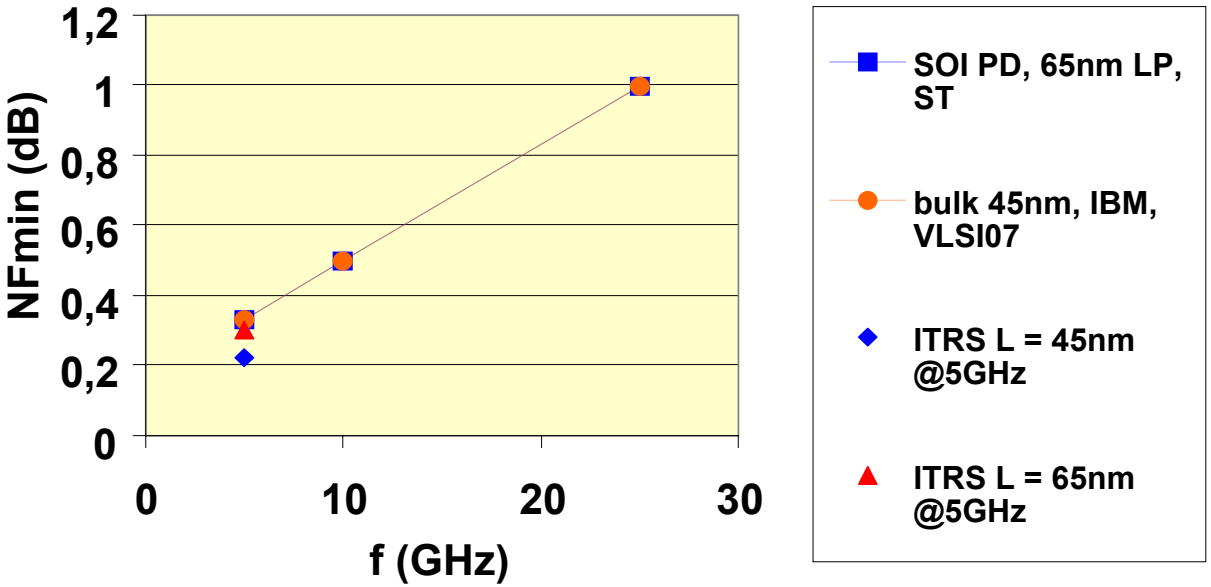
- Multi-finger approach
- Transistor divided into 2 equal parts
- Double gate contacts
- Z_0 matched coplanar access is insured

B. Martineau, et al., ESSCIRC 2007

- Array layout approach
- Double gate contacts
- Multi-path and circular interconnect for gate, drain and source connections

B. Heydari, et al., ISSCC 2007

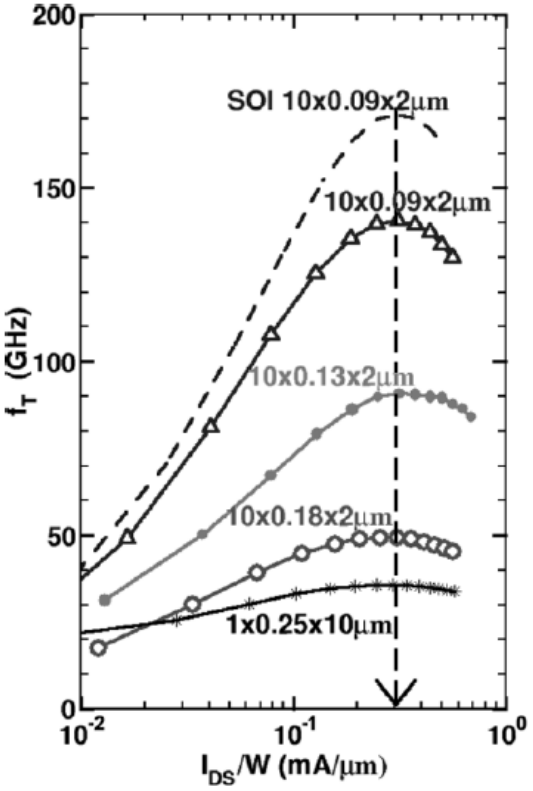
Bulk and SOI CMOS devices: NF_{min} feature



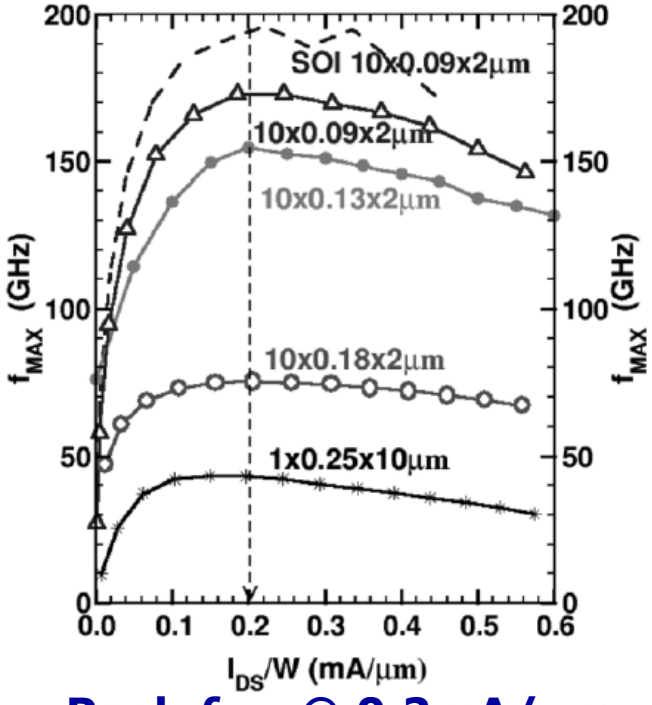
- NF_{min} is a linear function of frequency – it is a very difficult measurement in terms of accuracy (de – embedding is very complex in high frequency range)
- NF_{min} is degraded by high gate & source resistance => NF_{min} is dependent on layout
- No difference between bulk and SOI for same parasitic resistances and same g_m

Courtesy to C. Raynaud, STMicroectronics & CEA

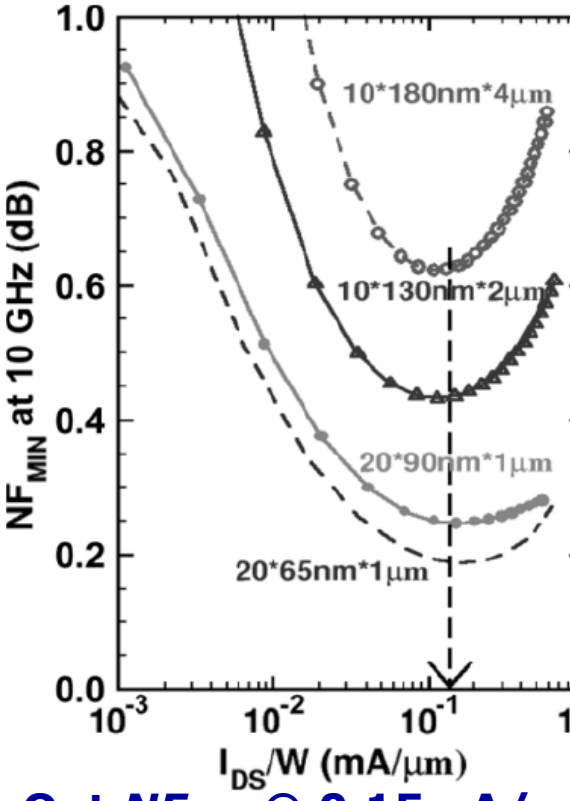
CMOS scaling features for mmW design



Peak f_T @ 0.3mA/µm



Peak f_{max} @ 0.2mA/µm

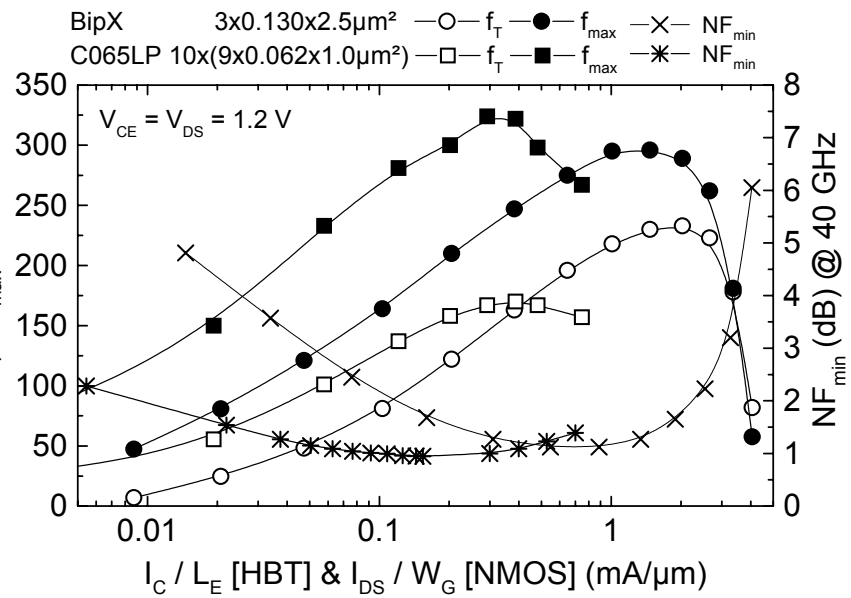


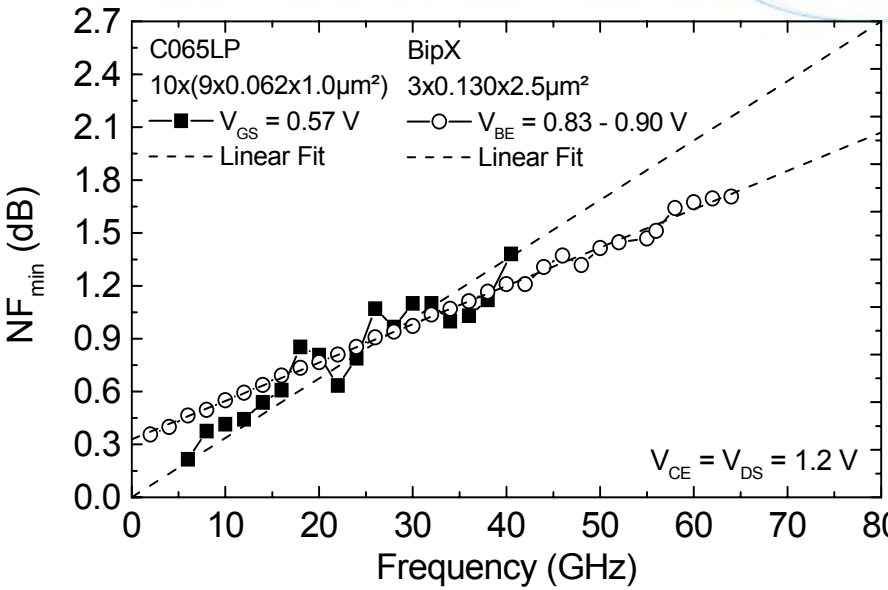
Opt NF_{min} @ 0.15mA/µ

- Constant current density bias ⇗ design robust to I_{DS} variation
- Compliant with design porting from one technology node to another

T.O. Dickson, et al., JSSCC Aug. 2006

HBT and CMOS Comparison





- Current difference for the peak value of f_T
- @ 40GHz, NF behavior better for MOS than for bipolar; trend reversed over 60GHz
- For a given f_{max}, better performance of the bipolar for large signal operation
- **Both types of devices are suited for mmW design with industrial margin**

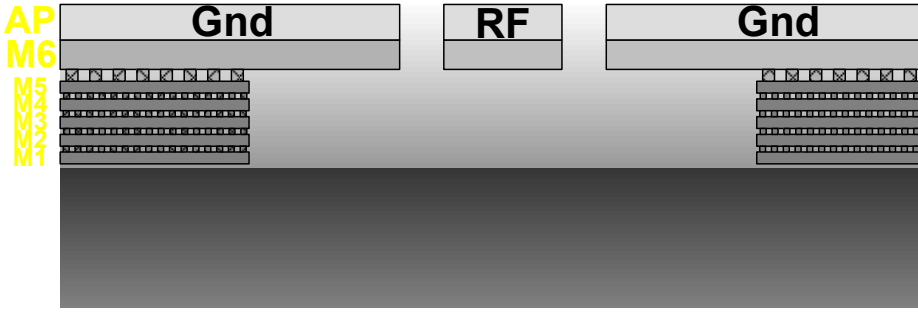
P. Chevalier, et al., ESSCIRC 2006 workshop

BEOL evolution through technology nodes

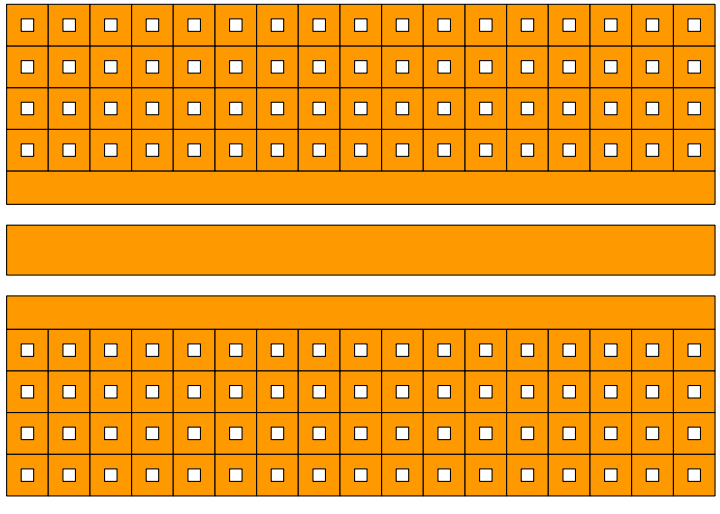
- **General trend:** when moving from one technology node to another
  - vertical shrink of Me and dielectric thickness
  - reduction of the Me pitch
- **Consequences:**
  - Lumped elements (inductors): larger ohmic and substrate losses
  - Distributed elements (Tlines): attenuation constant degradation
- **Possible solutions:**
  - Use mmW dedicated BEOL (e.g. 3 thick Me layers + thick IMD)
    ↳ *drawback:* application dedicated process
  - Use digital BEOL with max number of Me layers (e.g. 10 Me layers)
    ↳ *drawback:* cost
  - Increase the substrate resistivity (e.g SOI HR)
    ↳ *drawback:* cost & specific process

mmW Tlines in CMOS deep submicron BEOL

- Vertical shrink of BEOL imposes drastical layout design rules in terms of:
  - Me density per given square area
  - Electromigration rules (esp. High temperature)



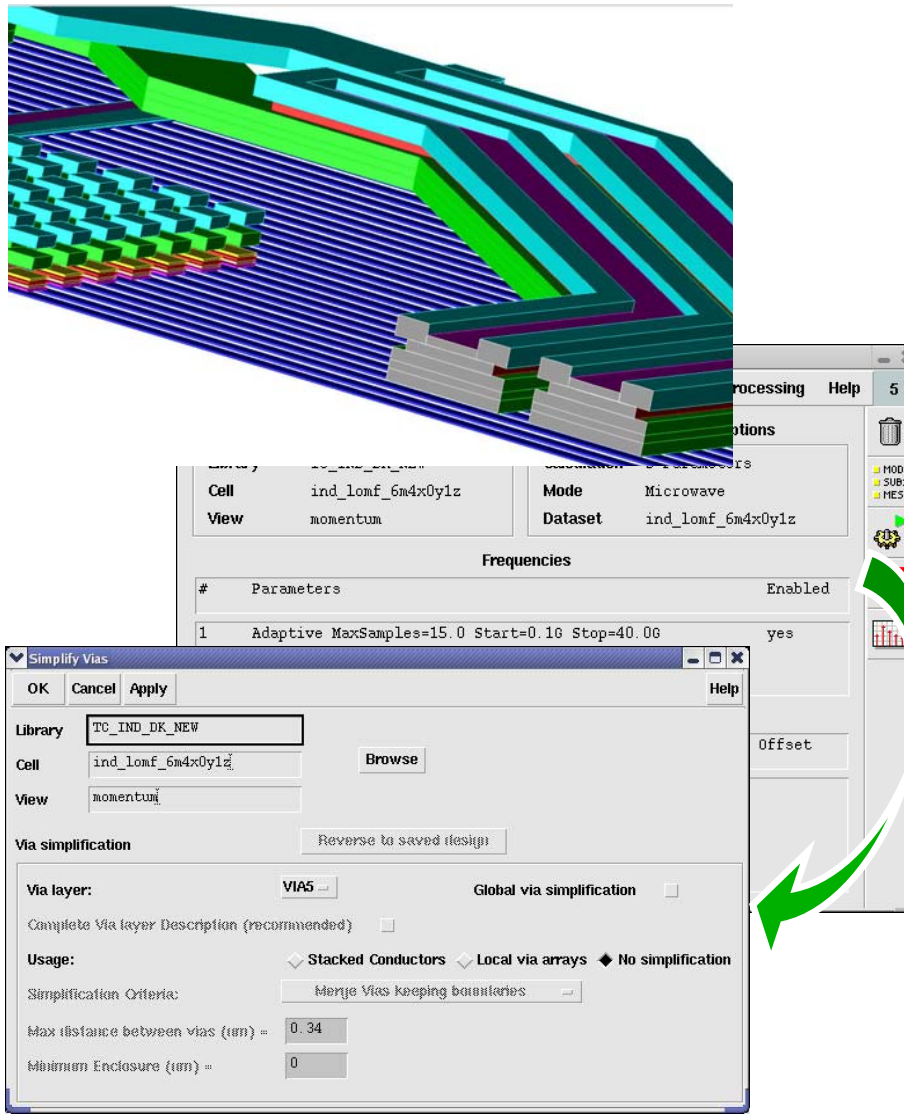
- DRM not very friendly for mmW Tline designer!
- The use of EM simulators is mandatory



N. Seller, et al., RFIC2007

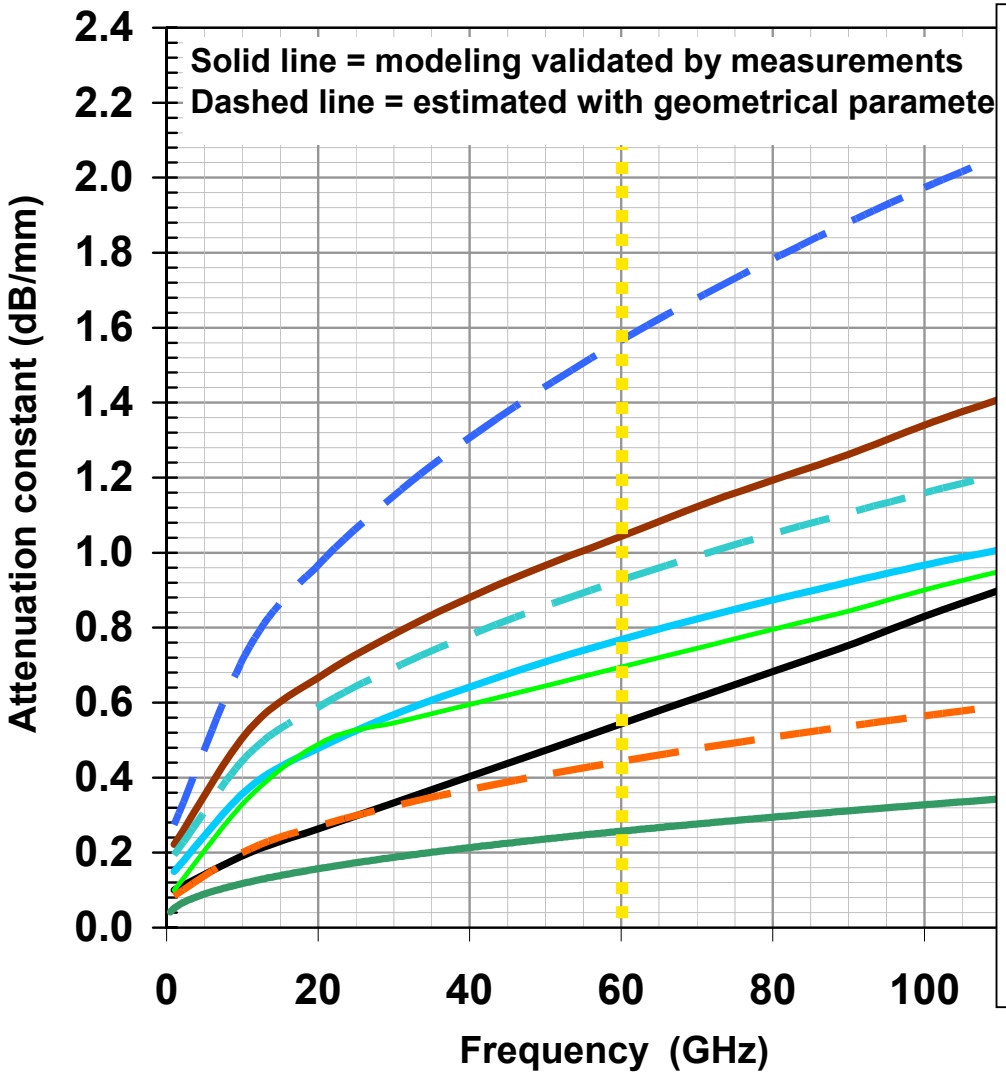
Example of complex lumped/distributed elements simulation with EM tool

- Passive device modeling on nanometer technologies up to mmW range:
  - inductors
  - transformers
  - transmission lines
- Unique and accurate technology file compliant with foundries DRM
- Layout preprocessing for easier setup
- High computation speed thanks to parallel data processing



Courtesy to V. Poisson, Agilent Technolgies

Measured attenuation constants for 50Ω Tlines



Charac. impedance :
Zc # 50 Ω

CMOS65 (6M1T) M6+Al / M1+M2
MS: w=2.4µm/h=1.74µm

BiCMOS9 (6M1T) M6+Al / M1+M2
MS: w=5.0µm/h=5.70µm

CMOS65 (7M2T) M7+Al / M1+M2
MS: w=4.3µm/h=3.24µm

CMOS90 (7M2T) M7+Al / M1+M2
MS: w=6.0µm/h=4.06µm

CMOS65 SOI (6M1T) M6+Al
CPW: w=12µm/s=5µm

CMOS120- SOI (6M1T) M1 to Al
CPW: w=26µm/s=22µm

BiCMOS9MW (6M3T) M6+Al / M1+M2
MS: w=12µm/h=7µm

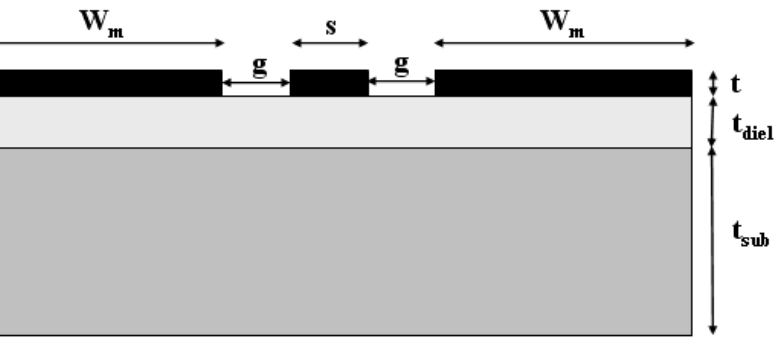
Above IC BCB Cu (t=2µm)
MS: w=24µm/h=10µm

Digital deep subµ BEOL

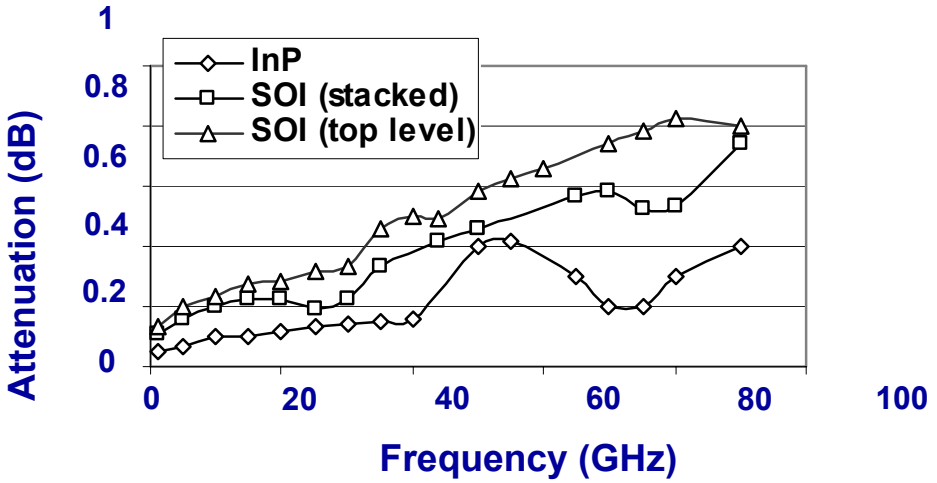
mmW dedicated BEOL

HR SOI performances up to 100 GHz

- Specific HR SOI CPW stacking all the metallizations has been realized and characterised up to 110 GHz



CPW cross section

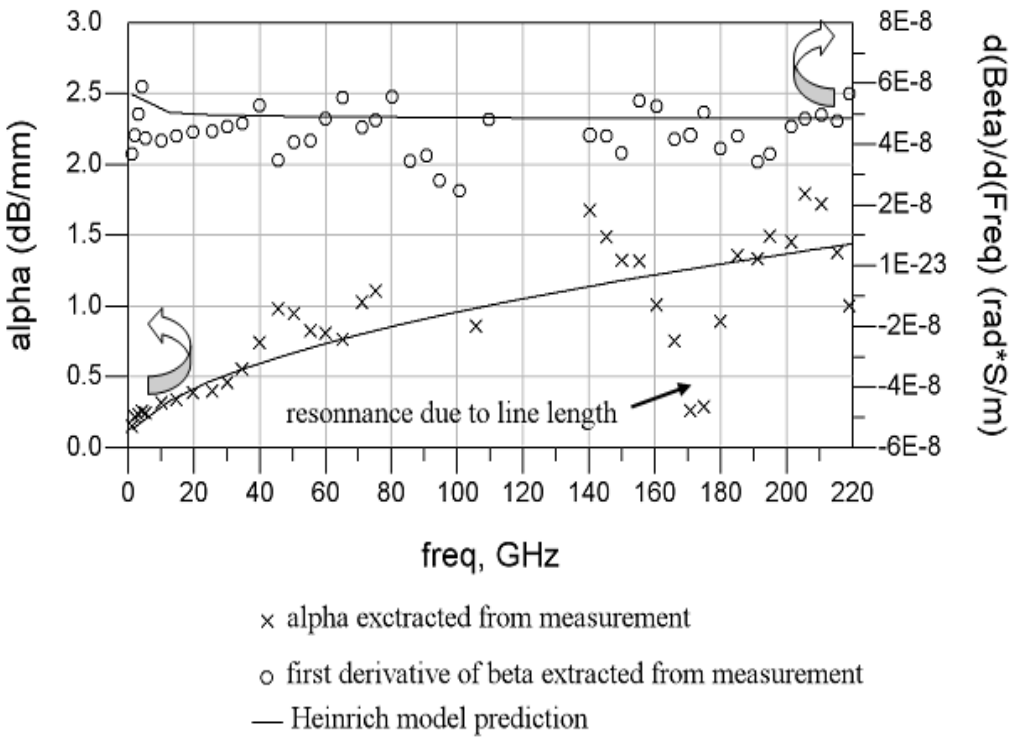


Dimension of the stacked CPW line: w = 26 µm, s = 22 µm

- The obtained performances are: α ~ 0.5 dB/mm @ 50 GHz

Courtesy to F. Gianesello, STMicroelectronics

G band (140 – 200 GHz)
CPW TL performances on SOI



attenuation in dB/mm and constant propagation characteristic for a CPW transmission line realized on HR SOI with s = 10 µm and g = 5 µm

α ~ 1.5 dB/mm @ 200 GHz on HR SOI

Not feasible in bulk

Courtesy to F. Gianesello, STMicroelectronics

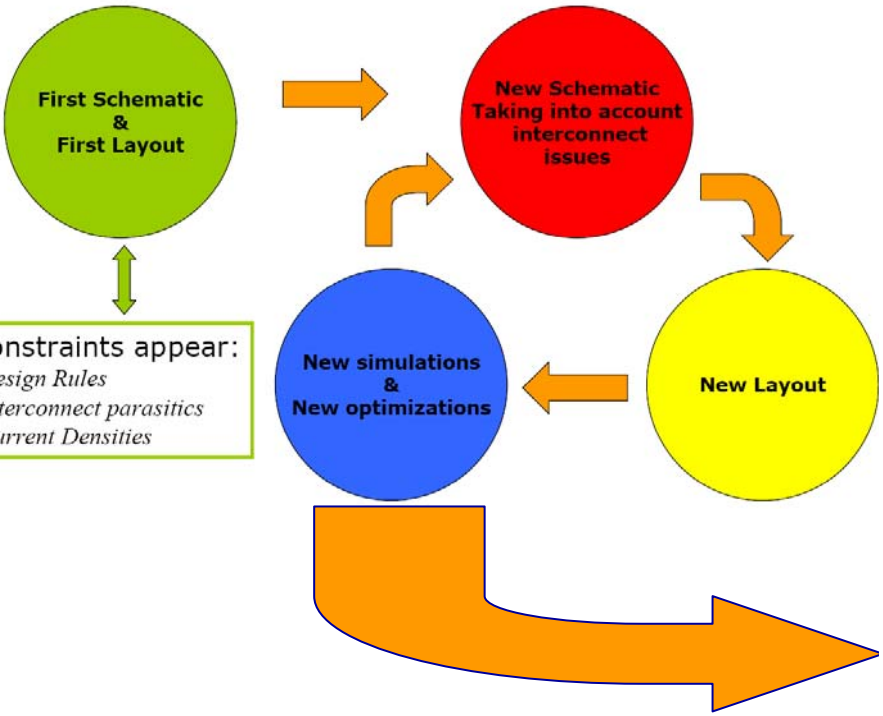
Outline

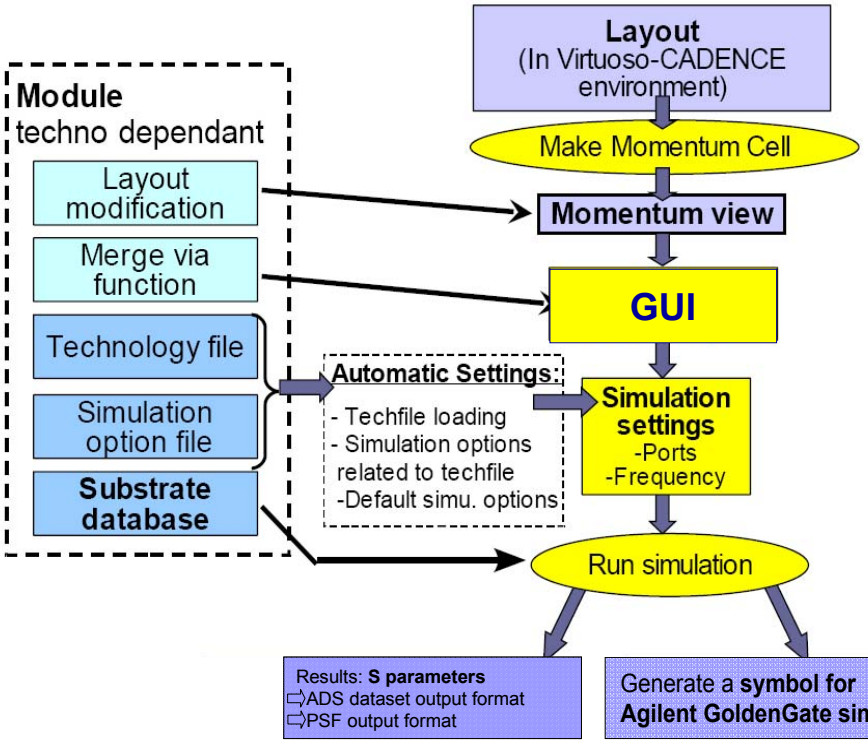
- Target applications for the Millimeter-wave frequency band
- Silicon technologies to address mmW complete solutions
  - Active devices on bulk and SOI technologies
  - Passive devices
- Silicon integrated solutions for mmW circuits
  - LNA mmW designs
  - Down-conversion mixers for mmW
  - Voltage controlled oscillators for mmW
  - Power amplifiers for mmW
  - mmW Assembly
- **Conclusions**

- Both for HDR Wireless communications and for radar applications, the heterodyne architecture is commonly used

- Non-exhaustive overview of critical building blocs of such an architecture:
  - Low Noise Amplifiers
  - Down-conversion mixers
  - Voltage Controlled Oscillators
  - Power Amplifiers

Millimeter Wave Design Methodology





- Example: Agilent Momentum is used in the standard flow from *virtuoso* CADENCE environment

Courtesy to V. Poisson, Agilent Technolgies and L. David, STMicroelectronics

mmW LNA Design Considerations

- Designs use either NMOS or HBT devices, in a cascade of simple amplification stages (typically 2 to 4)
- **Cascoded stages:**
  - **Pros:** easy to match simultaneously for noise and impedance, unconditionally stable (thus easy to measure!)
  - **Cons:**
    - NMOS: MAGNMOS < 10dB @ above 60GHz ⇗ several stages ⇗ increased equivalent NF
    - HBT: Enough room for 2 EB stacked junctions
- **Common source/emitter stages:**
  - **Pros:** better NF
  - **Cons:** potentially unstable; NMOS reliability at Vds=Vdd.
  - Use S/E degeneration in order to enhance linearity/stability, but loose some gain
- **Biasing:** CPW and/or µstrip lines
  - Serve for electrical biasing, impedance matching, and ESD strategy.
  - MOM capacitors used for AC decoupling of each individual stage

mmW State of the art LNA Solutions

$$FOM_{LNA} = \frac{G \cdot IIP_3 \cdot f}{(NF - 1) \cdot P_{DC}}$$

NA features	[6]	[5]	[14]	[17]	[19]	[15]	[58]	[59]	[44]
requency (GHZ)	80	62	61.3	58	40	64	61.5	59	58
ain (dB)	7.2	12.2	17.9	14.6	9.5	15.5	14.7	12	15
oise Figure (dB)	5.7	6	5.2	5.5	4	6.5	4.5	5	4.4
P3 (dBm) (recalc.)	6.25	14	-6.5	-6.8	4.5	-6.2	-8.5	-2	-8.4*
C power (mW)	70	10.4	21.6	24	40.8	47.88	10.8	8.1	4
rocess	65nm CMOS SOI	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS SOI	90nm CMOS	0.13um SiGe	0.13um SiGe	90nm CMOS
rea (mm^2)	0.98	0.48	0.856	0.14	NA	0.52	0.54	0.9	0.14
OM (GHz)	9.31	38	16.9	5.71	8.9	3.28	13.5	33.7	15.7

mmW State of the art LNA Solutions

$$FOM_{LNA} = \frac{G \cdot IIP_3 \cdot f}{(NF - 1) \cdot P_{DC}}$$

NA features	[6]	[5]	[14]	[17]	[19]	[15]	[58]	[59]	[44]
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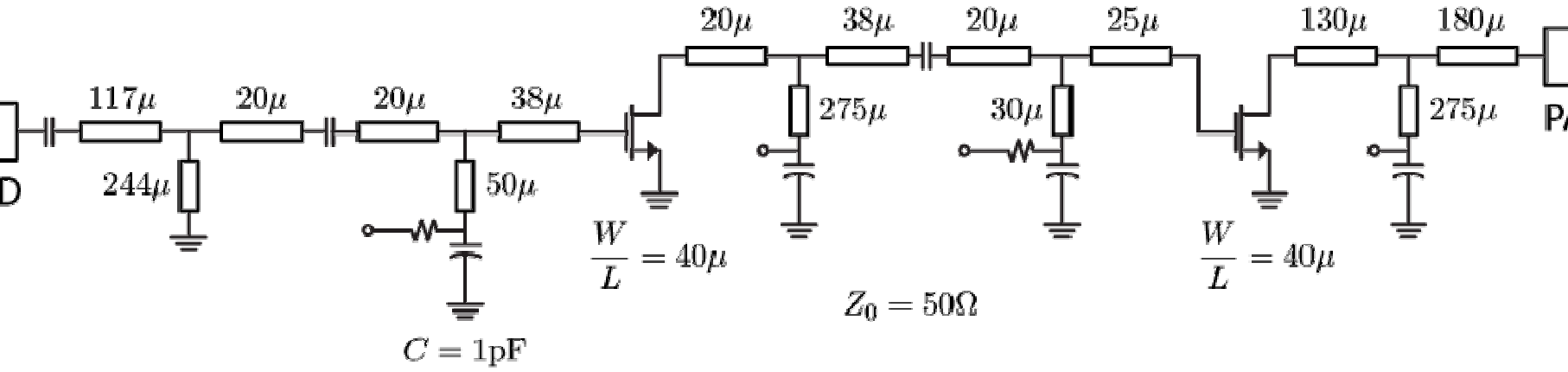
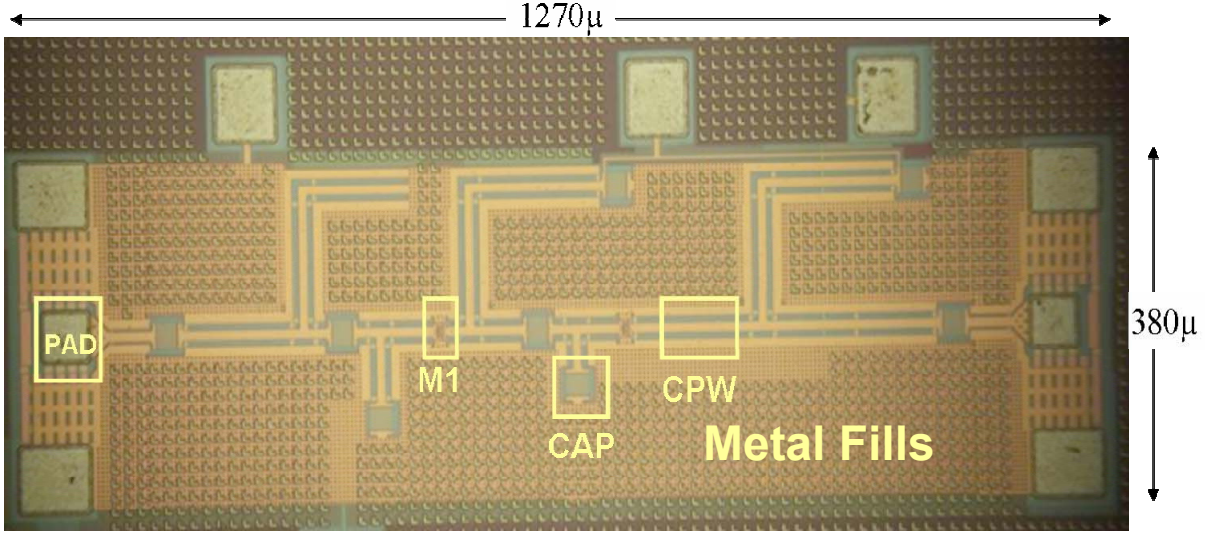
C power (mW)	70	10.4	21.6	24	40.8	47.88	10.8	8.1	4
rocess	65nm CMOS SOI	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS SOI	90nm CMOS	0.13um SiGe	0.13um SiGe	90nm CMOS
rea (mm^2)	0.98	0.48	0.856	0.14	NA	0.52	0.54	0.9	0.14
OM (GHz)	9.31	38	16.9	5.71	8.9	3.28	13.5	33.7	15.7

Example 1: Standard 90nm CMOS 62GHz LNA

B. Heydari, et al., ISSCC 2007





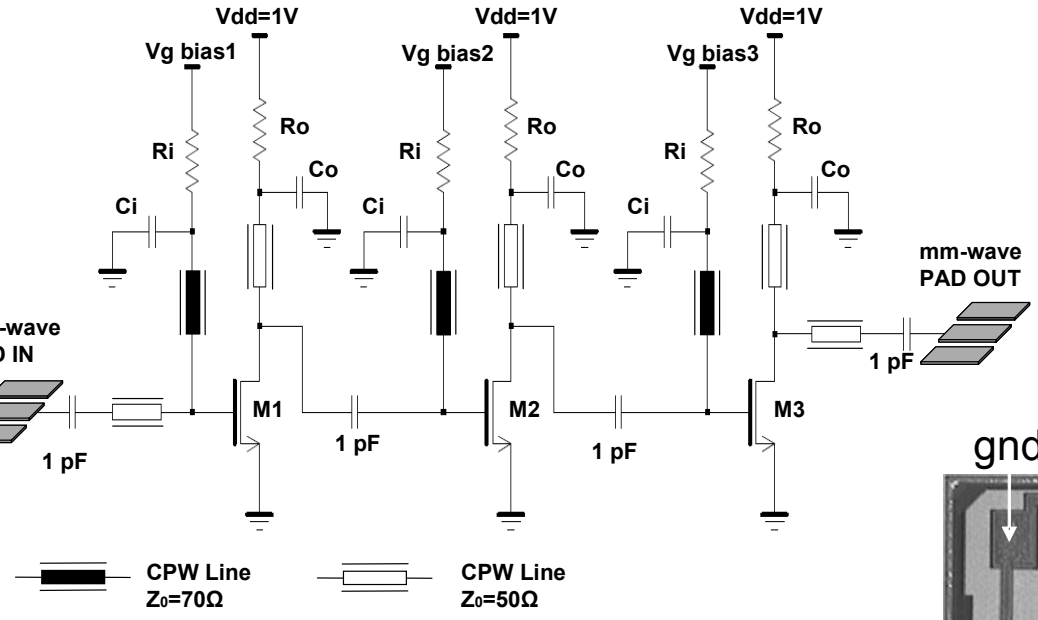
mmW State of the art LNA Solutions

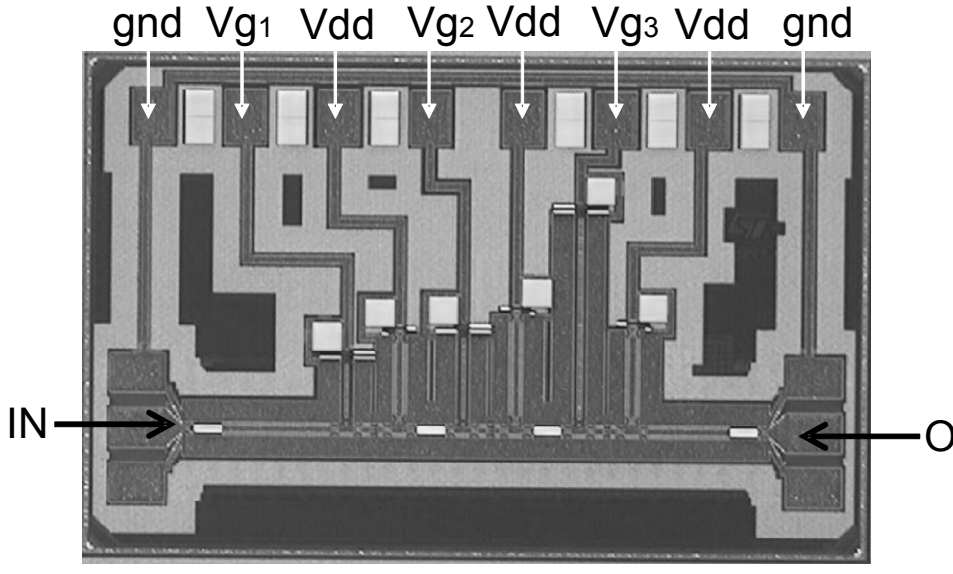
$$FOM_{LNA} = \frac{G \cdot IIP_3 \cdot f}{(NF - 1) \cdot P_{DC}}$$

NA features	[6]	[5]	[14]	[17]	[19]	[15]	[58]	[59]	[44]
requency (GHZ)	80	62	61.3	58	40	64	61.5	59	58
ain (dB)	7.2	12.2	17.9	14.6	9.5	15.5	14.7	12	15
oise Figure (dB)	5.7	6	5.2	5.5	4	6.5	4.5	5	4.4
P3 (dBm) (recalc.)	6.25	14	-6.5	-6.8	4.5	-6.2	-8.5	-2	-8.4*
C power (mW)	70	10.4	21.6	24	40.8	47.88	10.8	8.1	4
rocess	65nm CMOS SOI	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS SOI	90nm CMOS	0.13um SiGe	0.13um SiGe	90nm CMOS
rea (mm^2)	0.98	0.48	0.856	0.14	NA	0.52	0.54	0.9	0.14
OM (GHz)	9.31	38	16.9	5.71	8.9	3.28	13.5	33.7	15.7

Example 2: 65nm LP SOI CMOS 80GHz LNA

B. Martineau, et al., ESSCIRC 2007





Area = 0.98mm²
(incl. pads)

mmW State of the art LNA Solutions

$$FOM_{LNA} = \frac{G \cdot IIP_3 \cdot f}{(NF - 1) \cdot P_{DC}}$$

NA features	[6]	[5]	[14]	[17]	[19]	[15]	[58]	[59]	[44]
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ain (dB)	7.2	12.2	17.9	14.6	9.5	15.5	14.7	12	15
oise Figure (dB)	5.7	6	5.2	5.5	4	6.5	4.5	5	4.4
P3 (dBm) (recalc.)	6.25	14	-6.5	-6.8	4.5	-6.2	-8.5	-2	-8.4*
C power (mW)	70	10.4	21.6	24	40.8	47.88	10.8	8.1	4
rocess	65nm CMOS SOI	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS SOI	90nm CMOS	0.13um SiGe	0.13um SiGe	90nm CMOS
rea (mm^2)	0.98	0.48	0.856	0.14	NA	0.52	0.54	0.9	0.14
OM (GHz)	9.31	38	16.9	5.71	8.9	3.28	13.5	33.7	15.7

Example 3: 90nm CMOS 60GHz lumped LNA

E. Cohen et al., RFIC 2008

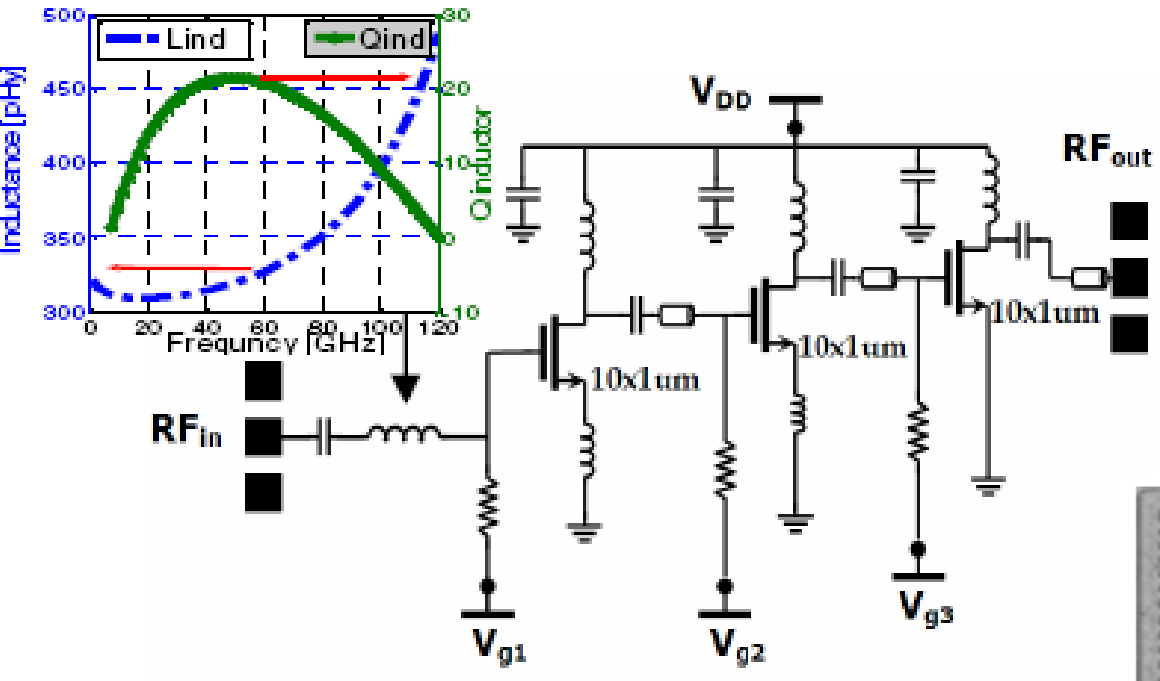


Fig. 5. Schematic of 3 stage CS design with input inductor.

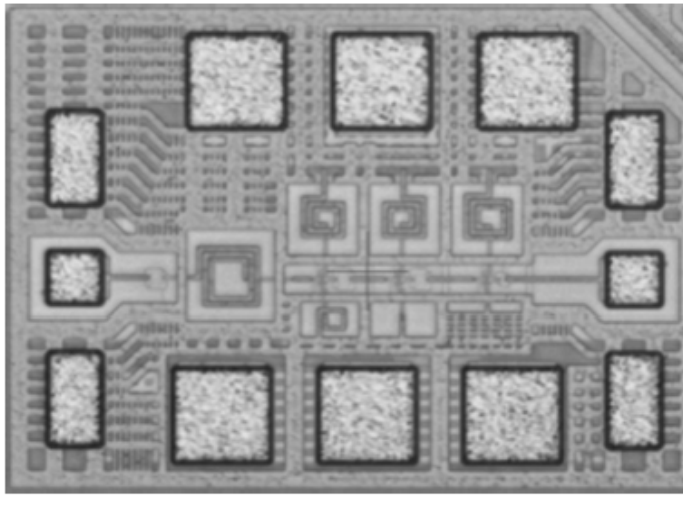
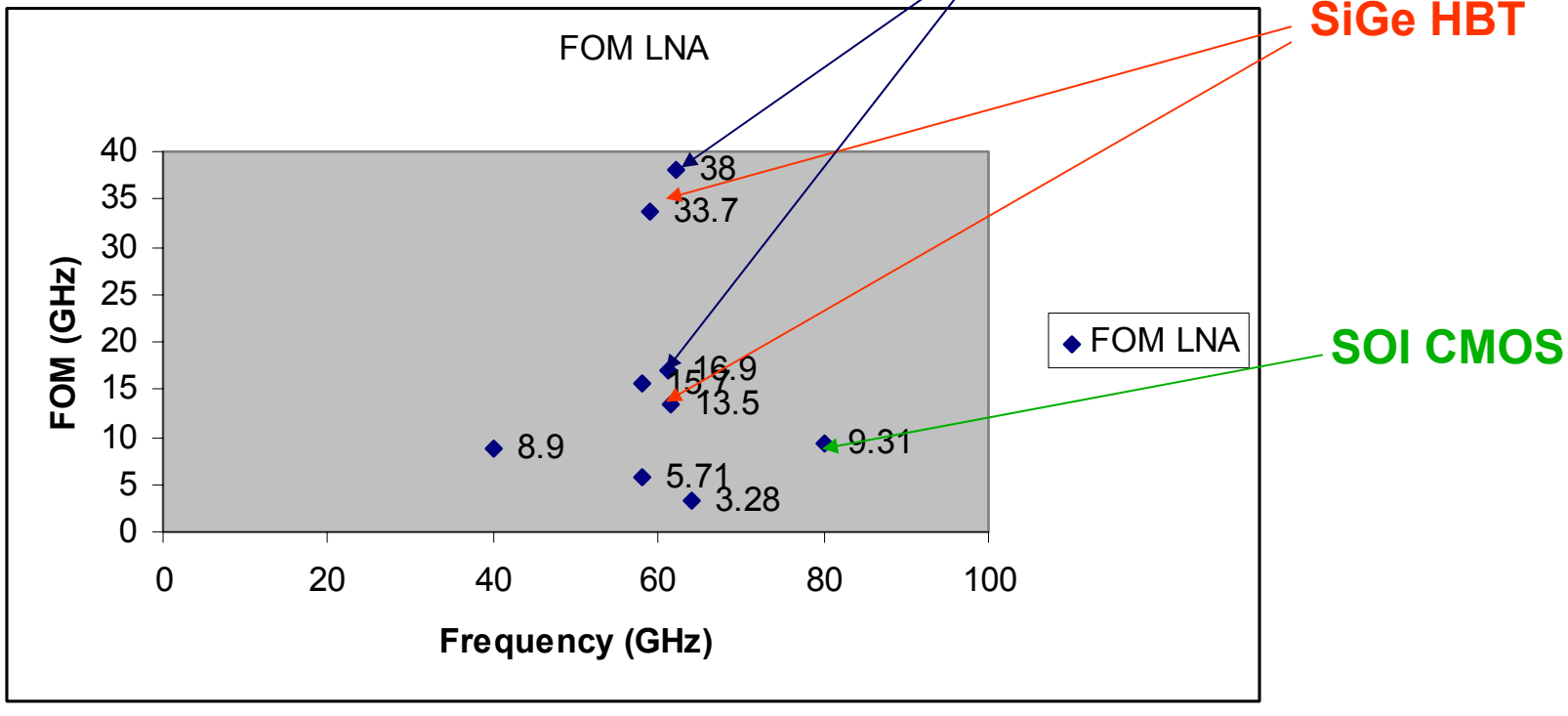


Fig. 6. LNA die 440 um x 320 um.

mmW State of the art LNA Solutions

$$FOM_{LNA} = \frac{G \cdot IIP_3 \cdot f}{(NF - 1) \cdot P_{DC}}$$



90nm CMOS

SiGe HBT

SOI CMOS

The LNA design performances depends on the NFmin, (Ft) of the process and the Matching network:

- mmW LNA is Designer dependent.
- CMOS and SiGe performances are similar.

mmW Down-conversion Mixers Design Considerations

- **Active mixers topologies:**
  - NMOS or HBT devices, Gilbert cells, Gm-cells, single or balanced inputs for RF and LO
  - **Pros:** high conversion gain value, need for reduced LO power, good noise figure
  - **Cons:** important power consumption, limited linearity, wide-band LO and RF ports matching sometimes difficult to obtain

- **Passive (resistive) mixers topologies:**
  - NMOS transistor LO-pumped on the gate or on the source, RF applied on the drain, the gate or combined with the LO on the gate
  - **Pros:** very linear large signal behavior, zero DC power consumption (supports low supply voltage)
  - **Cons:** conversion losses, sometimes need for higher LO power w.r.t. active mixers, LO to RF isolation sometimes low

- **For both categories:** sometimes sub-harmonic mixers (1/2, 1/3 LO signal)

mmW State of the art Down-conversion Mixers Solutions

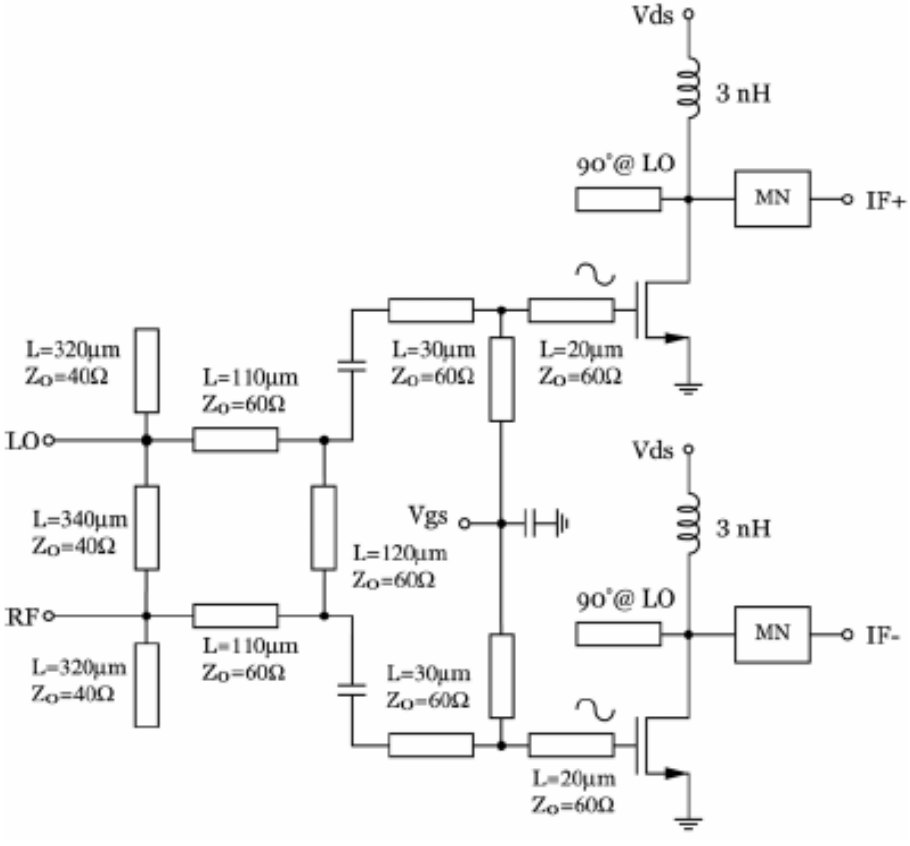
Mixer features	[23]	[24]	[25]	[26]	[27]	[16]	[60]
Frequency (GHz)	60	60	9 to 31	27	24	60	160
Conv. Gain (dB)	-2	-11.6	-1.1	-10.3	13	-12.5	-22
LO power (dBm)	0	4	9.7	0	NA	8.7	-10
IIP3 (dBm)	IIP1: -3.5	16.5	3	12.7	NA	IIP1: 5	NA
LO to RF Iso. (dB)	-12	NA	-27	-24	NA	34	NA
DC power (mW)	2.4	NA			6 (core)	~ 0	50
Process	130nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS SOI	0.18um CMOS	65 nm CMOS	0.13um SiGe
Topology	Active Single Ended	Resistive Single Ended	1/2 LO source pumped resistive	Gate pumped resistive	Active single balanced	Resistive singly balanced	Double Balanced Gilbert

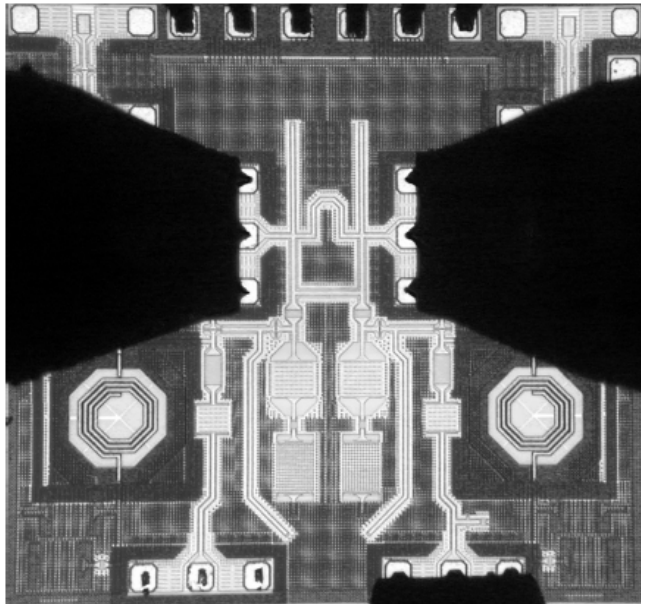
mmW State of the art Down-conversion Mixers Solutions

Mixer features	[23]	[24]	[25]	[26]	[27]	[16]	[60]
Frequency (GHz)	60	60	9 to 31	27	24	60	160
Conv. Gain (dB)	-2	-11.6	-1.1	-10.3	13	-12.5	-22
LO power (dBm)	0	4	9.7	0	NA	8.7	-10
IIP3 (dBm)	IIP1: -3.5	16.5	3	12.7	NA	IIP1: 5	NA
LO to RF Iso. (dB)	-12	NA	-27	-24	NA	34	NA
DC power (mW)	2.4	NA			6 (core)	~ 0	50
Process	130nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS SOI	0.18um CMOS	65 nm CMOS	0.13um SiGe
Topology	Active Single Ended	Resistive Single Ended	1/2 LO source pumped resistive	Gate pumped resistive	Active single balanced	Resistive singly balanced	Double Balanced Gilbert

Example 1: Digital 130nm CMOS active single gate mixer

S. Emami, et al., RFIC 2005





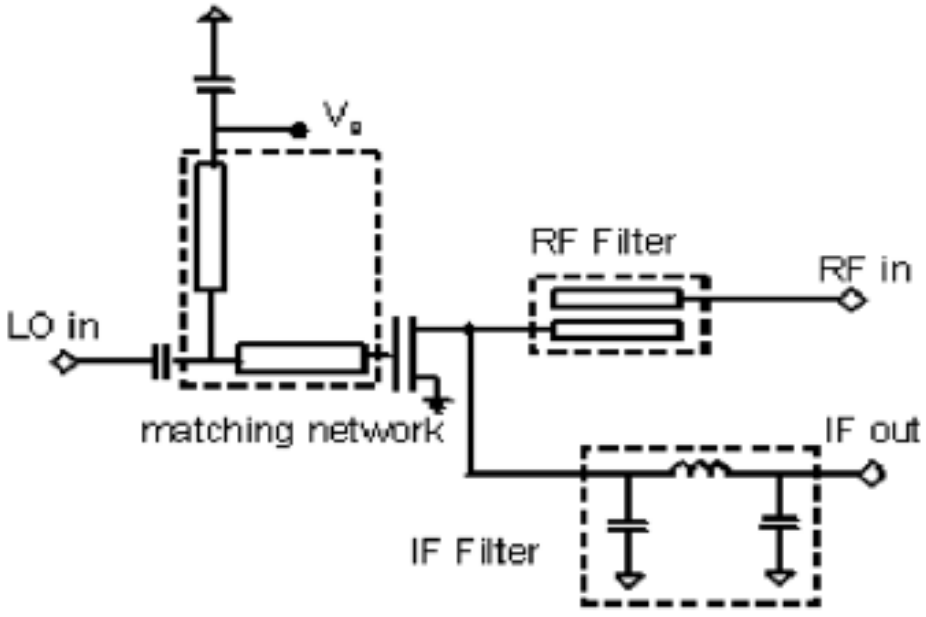
RF power: -25dBm
IF: diff, 2GHz, 50Ω
Mixer area = 1.6X1.7 mm²

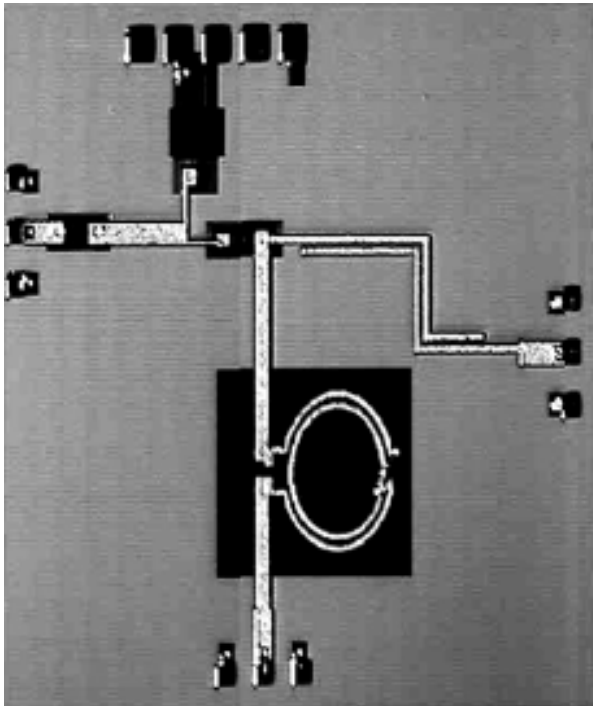
mmW State of the art Down-conversion Mixers Solutions

Mixer features	[23]	[24]	[25]	[26]	[27]	[16]	[60]
Frequency (GHz)	60	60	9 to 31	27	24	60	160
Conv. Gain (dB)	-2	-11.6	-1.1	-10.3	13	-12.5	-22
LO power (dBm)	0	4	9.7	0	NA	8.7	-10
IIP3 (dBm)	IIP1: -3.5	16.5	3	12.7	NA	IIP1: 5	NA
LO to RF Iso. (dB)	-12	NA	-27	-24	NA	34	NA
DC power (mW)	2.4	NA			6 (core)	~ 0	50
Process	130nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS SOI	0.18um CMOS	65 nm CMOS	0.13um SiGe
Topology	Active Single Ended	Resistive Single Ended	1/2 LO source pumped resistive	Gate pumped resistive	Active single balanced	Resistive singly balanced	Double Balanced Gilbert

Example 2: Digital 90nm CMOS passive (resistive) gate-pumped mixer

B.M. Motlagh, et al., IEEE M&W Comp. Letters, Jan. 2006





IIP3 + 3dB if Vds=150mV (power: 0.15mW)
IF: 2GHz, 50Ω
Mixer area = 2X2 mm²

mmW State of the art Down-conversion Mixers Solutions

Mixer features	[23]	[24]	[25]	[26]	[27]	[16]	[60]
Frequency (GHz)	60	60	9 to 31	27	24	60	160
Conv. Gain (dB)	-2	-11.6	-1.1	-10.3	13	-12.5	-22
LO power (dBm)	0	4	9.7	0	NA	8.7	-10
IIP3 (dBm)	IIP1: -3.5	16.5	3	12.7	NA	IIP1: 5	NA
LO to RF Iso. (dB)	-12	NA	-27	-24	NA	34	NA
DC power (mW)	2.4	NA			6 (core)	~ 0	50
Process	130nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS SOI	0.18um CMOS	65 nm CMOS	0.13um SiGe
Topology	Active Single Ended	Resistive Single Ended	1/2 LO source pumped resistive	Gate pumped resistive	Active single balanced	Resistive singly balanced	Double Balanced Gilbert

Example 1: 0.13µm SiGe:c BiCMOS double balanced Gilbert cell (part of a Trx)

E. Laskin, et al., RFIC 2007

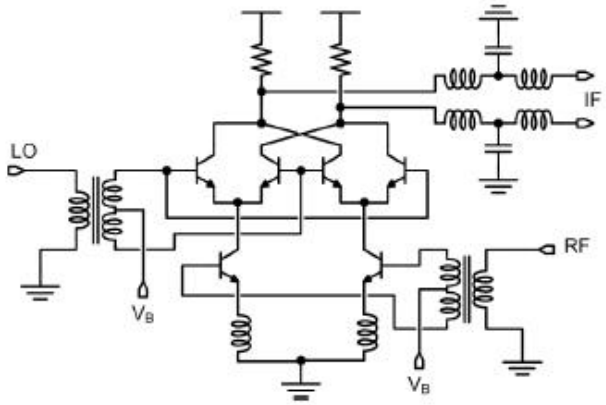


Fig. 3. Down-convert mixer schematic.

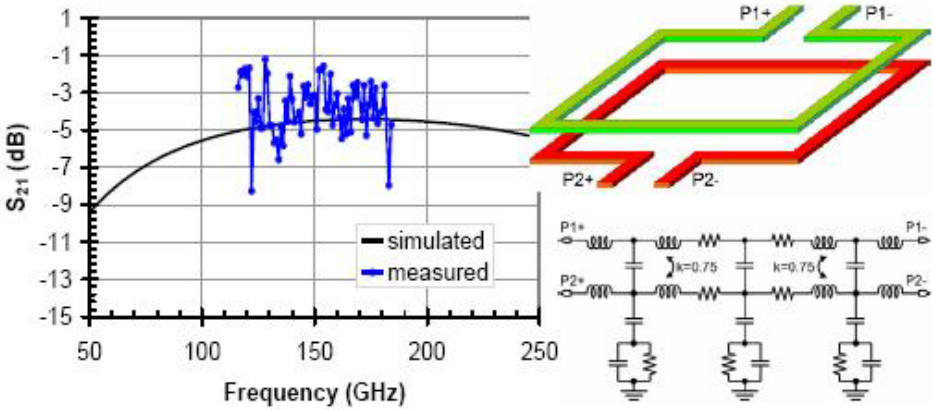
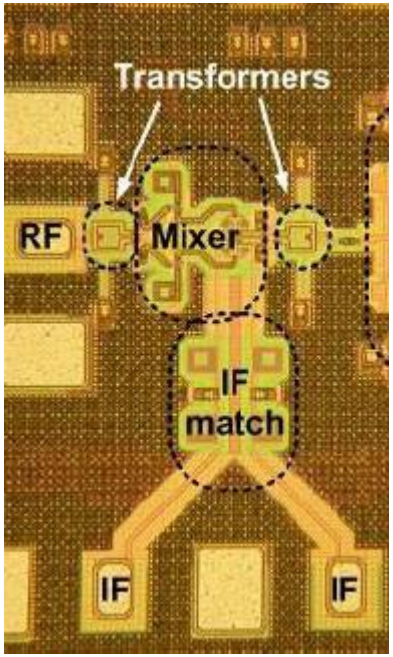


Fig. 4. Left: measured and simulated transformer S_{21}. Right: transformer layout and the 2-π model obtained from ASITIC.



IF: DC to 10GHz, 50Ω
Mixer area < 0.2mm²

mmW State of the art Down-conversion Mixers Solutions

- The Mixer Design performances depend on the Mixer Architecture:
  - Passive Mixers will
    - Have very high linearity,
    - Have very low power consumption
    - Have Need High LO power
    - Have Conversion Losses
    - Be made only with MOS transistors.
  - Active Mixers will
    - Have pour linearity,
    - Have high power consumption
    - Have Need Low LO power
    - Have Conversion Gain
    - Be made either with MOS transistors or SiGe HBT
  - In order to improve the linearity in active Mixers, MOS can be used in the signal gain and Bipolar in the LO switches.

mmW Voltage Controlled Oscillators Design Considerations

- Only fundamental mode oscillators treated here
- **Two principle schematics:**
  - Colpitts oscillators
  - Cross-coupled pairs with LC tank
- **Passive elements influence:** dedicated layout for (differential) varactors and inductors to improve Q-factor
- **Possible issue: the oscillator output power**
  - **Sol. 1:** low output power from the oscillating core + extra LO buffer
  - **Sol. 2:** increased power consumption in the oscillation core, no LO buffer ⇗ improved overall phase noise behavior and power consumption
- **Wide frequency tuning range required**:
  - include PVT variations + communications standard band (e.g. unlicensed 60GHz US band: 6.6%)
  - Partial DCO structures could answer.

mmW State of the art VCO Solutions

$$FOM_{VCO} = \left(\frac{f_0}{\Delta f}\right)^2 \cdot \frac{1}{L(f) \cdot P}$$

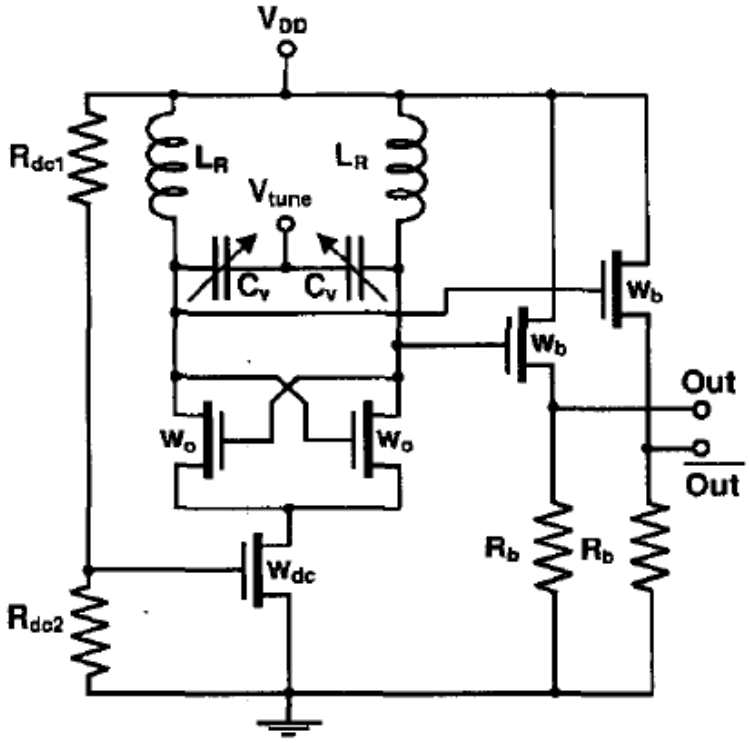
VCO features	[48]	[30]	[31]	[32]	[33]	[47]	[49]	[50]	[51]	[52]	[53]	[61]	[62]	[63]
Frequency (GHz)	56.5	77	60	51.6	28	62.1	60	70.1	54	40	60	96	42	21
utput Power (dBm)	-10	-13.8	-6.8	-30	NA	-15	NA	NA	NA	-8	-10	0.7	1	-6
ase Noise (dBc/Hz)	-89	-100.3	-94	-85	-112.9	-95	-100	-106.4	-118	-100.2	-99	-101.6	-90	-113
At delta f (MHz)	1	1	1	1	1	1	1	10	10	1	1	1	1	1
DC power (mW)	9.8	37.5	9.6	1	12	3.9	1.9	5.4	7.2	27	15	133	13	130
Process	130 nm CMOS	90 nm CMOS	90nm CMOS SOI	130nm CMOS	130nm CMOS	130nm CMOS	90 nm CMOS	65nm CMOS SOI	65nm CMOS	0.18µm CMOS	65nm CMOS	0.13um SiGe	0.13um SiGe	0.25um SiGe
Area (mm^2)	0.24	0.035	0.075	0.45	0.086	NA	0.015	0.027	0.23	0.625	0.05	0.12	0.4	0.1
FOM (dB)	174.5	182.3	179.75	179.25	190.9	184.95	193	175.7	184	177.9	182	180	171	178
Architecture	Cross Coupled LC	Colpitts	Cross Coupled LC	Cross Coupled LC	Cross coupled VCO	cross-coupled LC	Slow mode wave cross-coupled	Complem. LC cross-coupled	Cross Coupled LC	Standing wave mode	LC Cross Coupled DCO	Colpitts	Single ended CE	Colpitts Ballance
Tuning Range	9.80%	8.10%	14%	2.70%	6.70%	10%	0.20%	9.55%	11.50%	20%	17%	4.80%	NA	5.00%

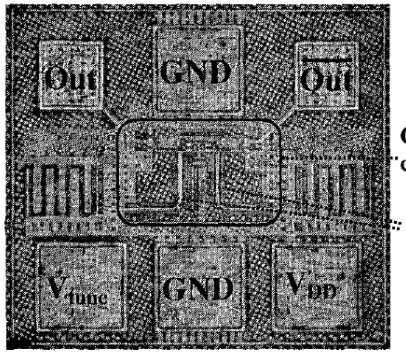
mmW State of the art VCO Solutions

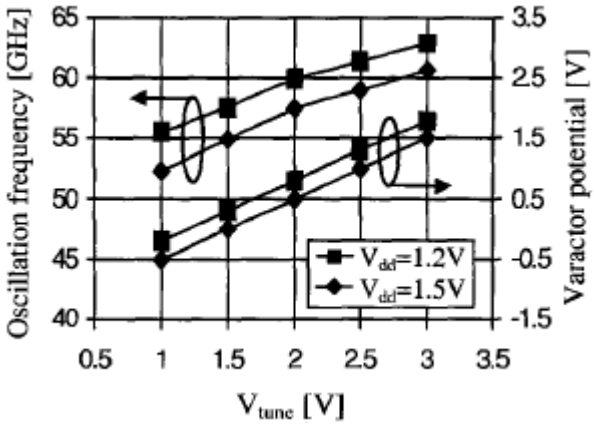
VCO features	[48]	[30]	[31]	[32]	[33]	[47]	[49]	[50]	[51]	[52]	[53]	[61]	[62]	[63]
Frequency (GHz)	56.5	77	60	51.6	28	62.1	60	70.1	54	40	60	96	42	21
Output Power (dBm)	-10	-13.8	-6.8	-30	NA	-15	NA	NA	NA	-8	-10	0.7	1	-6
Phase Noise (dBc/Hz)	-89	-100.3	-94	-85	-112.9	-95	-100	-106.4	-118	-100.2	-99	-101.6	-90	-113
At delta f (MHz)	1	1	1	1	1	1	1	10	10	1	1	1	1	1
DC power (mW)	9.8	37.5	9.6	1	12	3.9	1.9	5.4	7.2	27	15	133	13	130
Process	130 nm CMOS	90 nm CMOS	90nm CMOS SOI	130nm CMOS	130nm CMOS	130nm CMOS	90 nm CMOS	65nm CMOS SOI	65nm CMOS	0.18µm CMOS	65nm CMOS	0.13um SiGe	0.13um SiGe	0.25um SiGe
Area (mm^2)	0.24	0.035	0.075	0.45	0.086	NA	0.015	0.027	0.23	0.625	0.05	0.12	0.4	0.1
FOM (dB)	174.5	182.3	179.75	179.25	190.9	184.95	193	175.7	184	177.9	182	180	171	178
Architecture	Cross Coupled LC	Colpitts	Cross Coupled LC	Cross Coupled LC	Cross coupled VCO	cross-coupled LC	Slow mode wave cross-coupled	Complem. LC cross-coupled	Cross Coupled LC	Standing wave mode	LC Cross Coupled DCO	Colpitts	Single ended CE	Colpitts Ballance
Tuning Range	9.80%	8.10%	14%	2.70%	6.70%	10%	0.20%	9.55%	11.50%	20%	17%	4.80%	NA	5.00%

Example 1: 90nm SOI CMOS 60GHz cross-coupled LC VCO

F. Ellinger, et al., IMS 2004







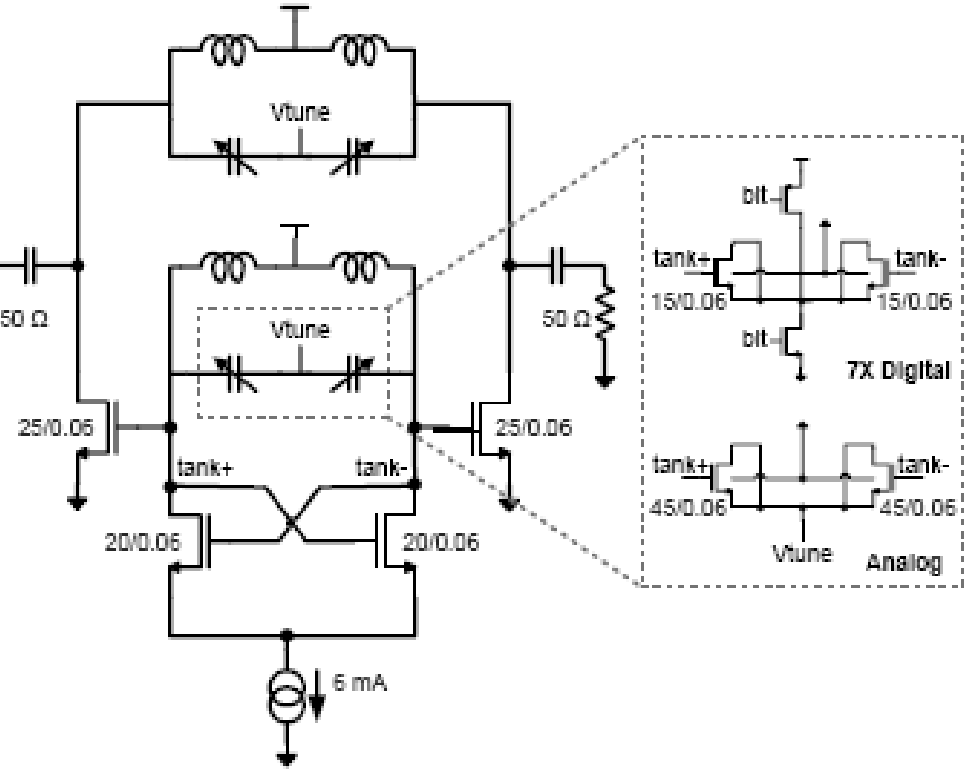
Area=0.3X0.25mm²
Std resistivity substrate (15Ω.cm)
Very large frequency tuning range by:
-Large varactor size (thick oxyde MOS caps)
-Small transistor size

mmW State of the art VCO Solutions

VCO features	[48]	[30]	[31]	[32]	[33]	[47]	[49]	[50]	[51]	[52]	[53]	[61]	[62]	[63]
Frequency (GHz)	56.5	77	60	51.6	28	62.1	60	70.1	54	40	60	96	42	21
Output Power (dBm)	-10	-13.8	-6.8	-30	NA	-15	NA	NA	NA	-8	-10	0.7	1	-6
Phase Noise (dBc/Hz)	-89	-100.3	-94	-85	-112.9	-95	-100	-106.4	-118	-100.2	-99	-101.6	-90	-113
At delta f (MHz)	1	1	1	1	1	1	1	10	10	1	1	1	1	1
DC power (mW)	9.8	37.5	9.6	1	12	3.9	1.9	5.4	7.2	27	15	133	13	130
Process	130 nm CMOS	90 nm CMOS	90nm CMOS SOI	130nm CMOS	130nm CMOS	130nm CMOS	90 nm CMOS	65nm CMOS SOI	65nm CMOS	0.18µm CMOS	65nm CMOS	0.13um SiGe	0.13um SiGe	0.25um SiGe
Area (mm^2)	0.24	0.035	0.075	0.45	0.086	NA	0.015	0.027	0.23	0.625	0.05	0.12	0.4	0.1
FOM (dB)	174.5	182.3	179.75	179.25	190.9	184.95	193	175.7	184	177.9	182	180	171	178
Architecture	Cross Coupled LC	Colpitts	Cross Coupled LC	Cross Coupled LC	Cross coupled VCO	cross-coupled LC	Slow mode wave cross-coupled	Complem. LC cross-coupled	Cross Coupled LC	Standing wave mode	LC Cross Coupled DCO	Colpitts	Single ended CE	Colpitts Ballance
Tuning Range	9.80%	8.10%	14%	2.70%	6.70%	10%	0.20%	9.55%	11.50%	20%	17%	4.80%	NA	5.00%

Example 2: 65nm CMOS 54GHz cross-coupled LC VCO with I-MOS varactor

S. Bozzola, et al., RFIC 2008



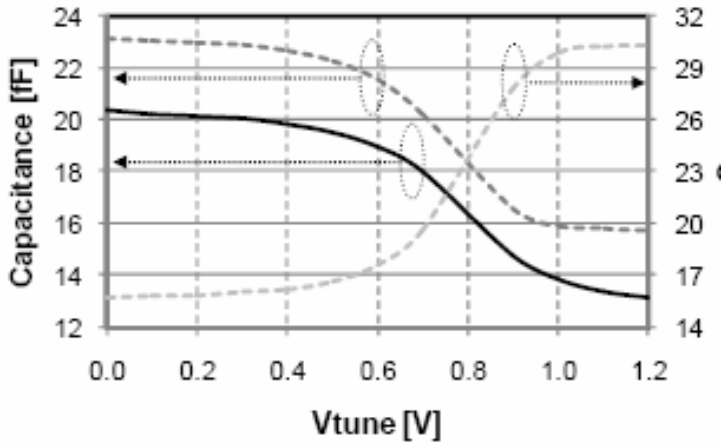


Fig. 2. Measured C-V characteristic (continuous line) simulated C-V characteristic and Q (dotted lines) of an I-M varactor with 15 fingers of 1 μm width , L = 0.06 μm.

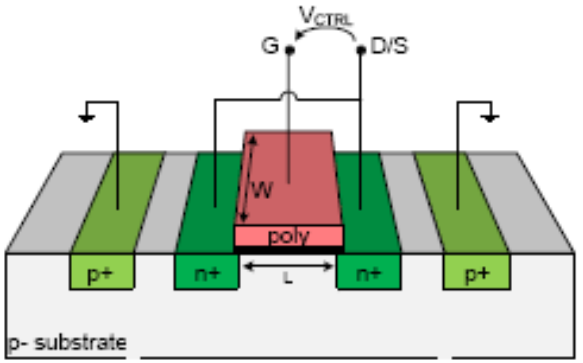


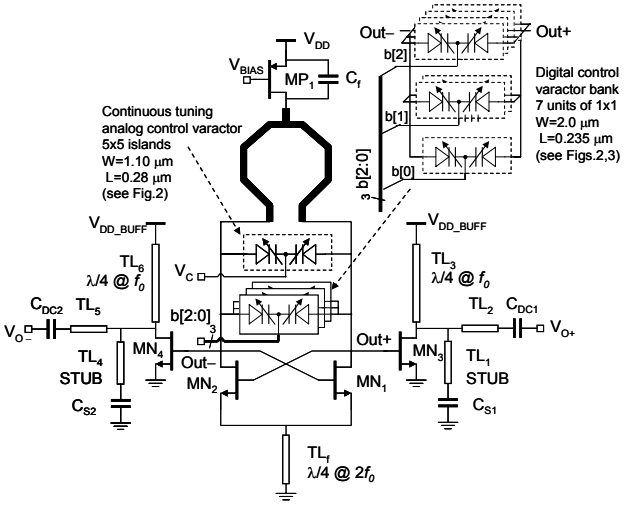
Fig. 1. Cross-section of an Inversion Mode N-MOS variable

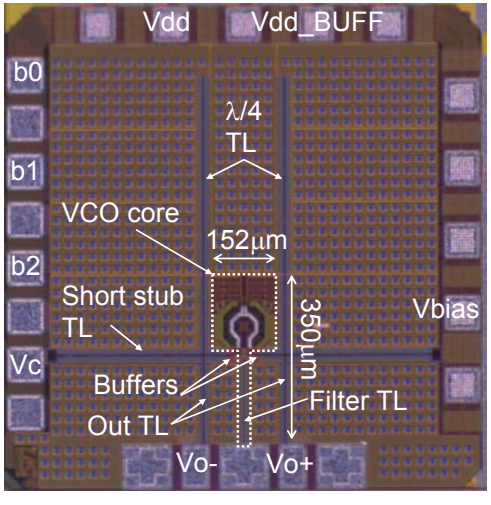
mmW State of the art VCO Solutions

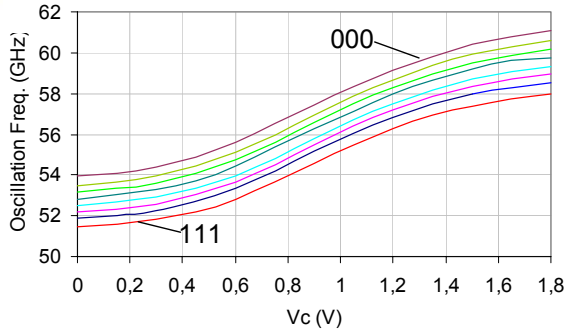
VCO features	[48]	[30]	[31]	[32]	[33]	[47]	[49]	[50]	[51]	[52]	[53]	[61]	[62]	[63]
Frequency (GHz)	56.5	77	60	51.6	28	62.1	60	70.1	54	40	60	96	42	21
Output Power (dBm)	-10	-13.8	-6.8	-30	NA	-15	NA	NA	NA	-8	-10	0.7	1	-6
Phase Noise (dBc/Hz)	-89	-100.3	-94	-85	-112.9	-95	-100	-106.4	-118	-100.2	-99	-101.6	-90	-113
At delta f (MHz)	1	1	1	1	1	1	1	10	10	1	1	1	1	1
DC power (mW)	9.8	37.5	9.6	1	12	3.9	1.9	5.4	7.2	27	15	133	13	130
Process	130 nm CMOS	90 nm CMOS	90nm CMOS SOI	130nm CMOS	130nm CMOS	130nm CMOS	90 nm CMOS	65nm CMOS SOI	65nm CMOS	0.18µm CMOS	65nm CMOS	0.13um SiGe	0.13um SiGe	0.25um SiGe
Area (mm^2)	0.24	0.035	0.075	0.45	0.086	NA	0.015	0.027	0.23	0.625	0.05	0.12	0.4	0.1
FOM (dB)	174.5	182.3	179.75	179.25	190.9	184.95	193	175.7	184	177.9	182	180	171	178
Architecture	Cross Coupled LC	Colpitts	Cross Coupled LC	Cross Coupled LC	Cross coupled VCO	cross-coupled LC	Slow mode wave cross-coupled	Complem. LC cross-coupled	Cross Coupled LC	Standing wave mode	LC Cross Coupled DCO	Colpitts	Single ended CE	Colpitts Ballance
Tuning Range	9.80%	8.10%	14%	2.70%	6.70%	10%	0.20%	9.55%	11.50%	20%	17%	4.80%	NA	5.00%

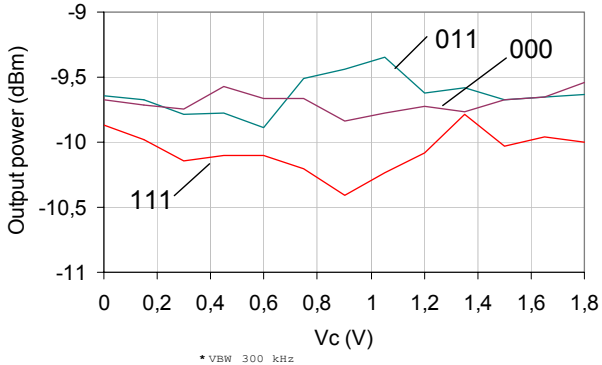
Example 3: 65nm CMOS 60GHz cross-coupled LC DCO

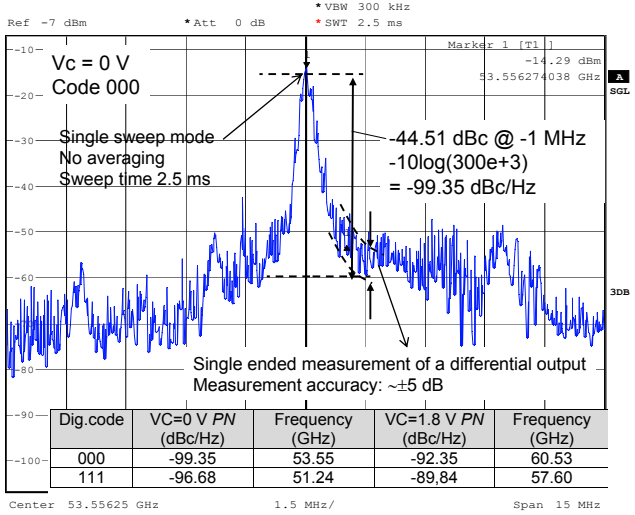
J.L Gonzalez, et al., RFIC 2009







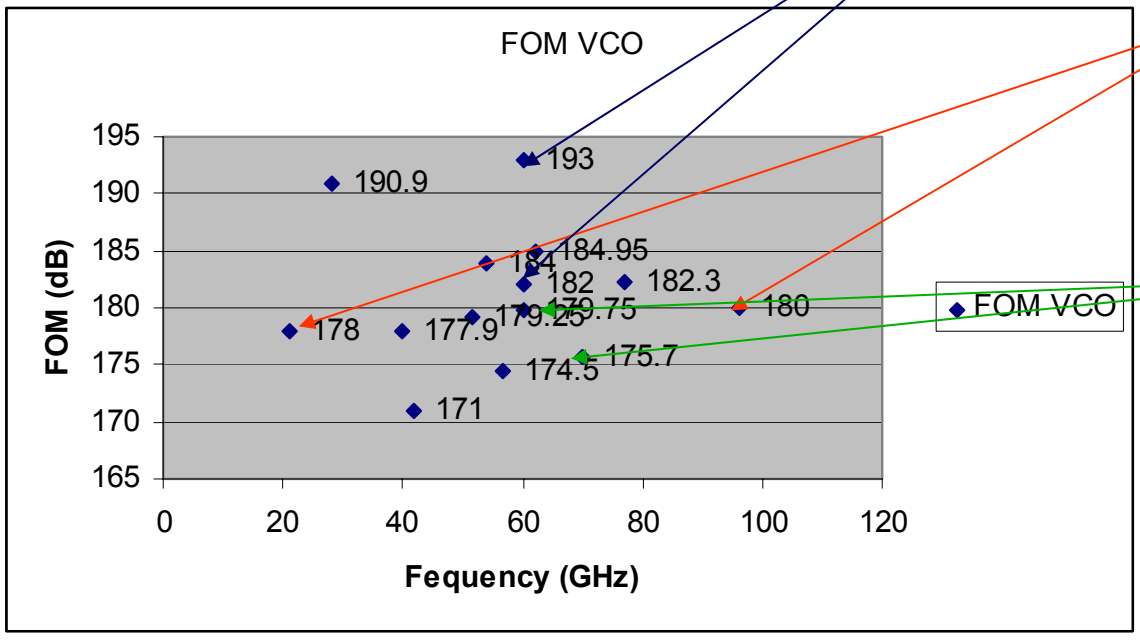




Dig.code	VC=0 V *PN* (dBc/Hz)	Frequency (GHz)	VC=1.8 V *PN* (dBc/Hz)	Frequency (GHz)
000	-99.35	53.55	-92.35	60.53
111	-96.68	51.24	-89,84	57.60

mmW State of the art VCO Solutions

$$FOM_{VCO} = \left(\frac{f_0}{\Delta f}\right)^2 \cdot \frac{1}{L(f)\cdot P}$$



Bulk CMOS

SiGe HBT

SOI CMOS

The VCO design performances in mmW mainly depends on Q factor of Varactors, 1/F noise being a criteria in narrow band:

mmW VCO is Varactor and Architecture dependent.

CMOS and SiGe performances are similar.

mmW Power Amplifiers Design Considerations

- **Designs use either NMOS or HBT devices, in a cascade of simple amplification stages (biased in class A or AB)**
  - First stage to get maximum gain (bias at peak fmax)
  - Following stages to maximize linearity

- **Cascoded stages:**
  - **Pros**: higher gain, larger output impedance, flat Ids/Vds characteristic
- **Common source/emitter stages:**
  - **Pros:** lower supply voltage ⇗ higher efficiency, better linearity
  - **Cons:** reduced reverse bias ⇗ complicates the input/output matching

- **Power supply Biasing: λ/4 RF chokes or lumped choke inductors**
- **Base biasing: sometimes uses a T° compensated circuit**

- **Output:** single or differential (towards differential antenna)

- **Power handling capability:**
  - High output power level (automotive radar, Last Mile wireless): SiGe HBT choice obvious
  - Mid power level: CMOS solutions possible ⇗ parallel power combining techniques

mmW State of the art PA Solutions

$$FOM_{PA} = P_{sat} \cdot G \cdot PAE \cdot f^2$$

PA features	[45]	[46]	[39]	[40]	[21]	[22]	[41]	[42]	[54]	[55]	[56]	[57]
Frequency (GHz)	63	60	44	40	60	60	62	60	85	77	77	60
at.Out Power (dBm)	12.5	7.8	10.6	10.4	8	7	11.5	12.3	21	17.5	14.4	20
Peak PAE (%)	14	3	8	2.9	7	4	8.2	8.8	3.4	12.8	15.7	12.7
3dB BW (GHz)	4	6.7	37.2	6	7	20	4	22	24	15	NA	7
S21 (dB)	15	13.5	13.5	7	10	11.5	14.3	5.6	8	17	20	18
O1CP (dBm)	10	7	7.5	NA	5	1.5	10.5	9	NA	14.5	12	13.1
DC power (mW)	84	NA	99	300	110	125	150	90	NA	400	195	248
Area (mm^2)	0.15	1.8	0.7	2.04	1.13	0.61	0.18	0.26	0.26	2.4	0.6	0.1
Technology	90nm CMOS	130nm CMOS	90nm CMOS	0.18um CMOS	90nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	0.12um SiGe	0.12um SiGe	0.12um SiGe	0.12ur SiGe
FOM (W.GHz)	312.4	14.5688	39.8	2.5	15.9	10.2	120	19.5	195	2138	2563	2884
Architecture	3 stages diff transformer coupled	5 cascode stages X2 /Doherty	2 brd-band amps + 2 brd-side couplers	3 stages Cascode/ single	3 stages Cascode/ single	3 stages CS / Single	3 stages CS+ comb.	2 stages diff transformer coupled	Broadband Combiner	4 stages CE single Combiner	3 stages Cascode CE(2x)	single stage push-pu cascod

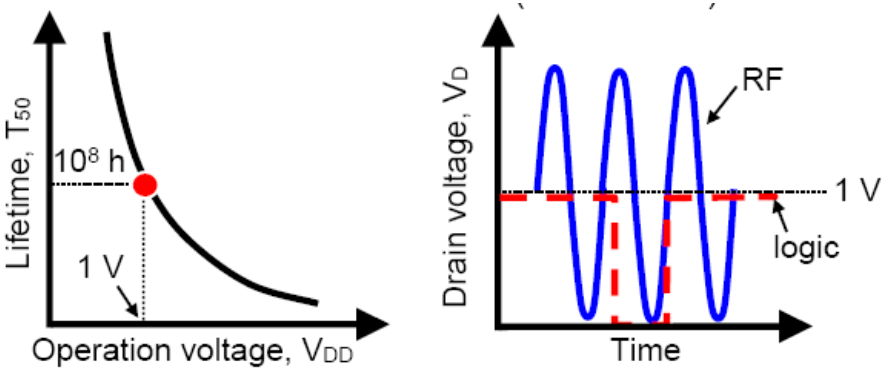
mmW State of the art PA Solutions

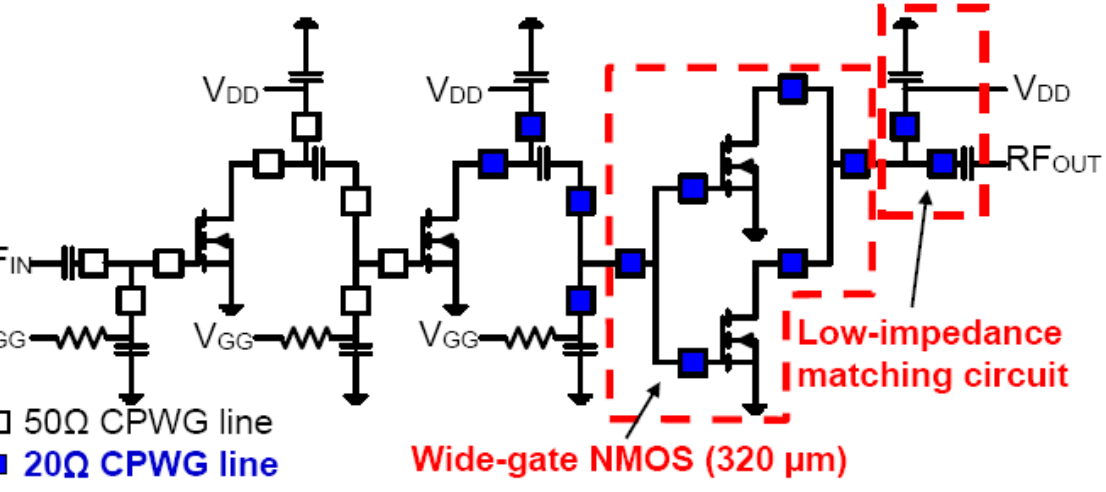
$$FOM_{PA} = P_{sat} \cdot G \cdot PAE \cdot f^2$$

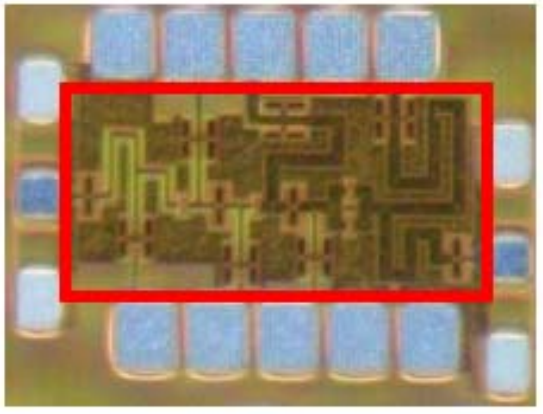
PA features	[45]	[46]	[39]	[40]	[21]	[22]	[41]	[42]	[54]	[55]	[56]	[57]
Frequency (GHz)	63	60	44	40	60	60	62	60	85	77	77	60
at.Out Power (dBm)	12.5	7.8	10.6	10.4	8	7	11.5	12.3	21	17.5	14.4	20
Peak PAE (%)	14	3	8	2.9	7	4	8.2	8.8	3.4	12.8	15.7	12.7
3dB BW (GHz)	4	6.7	37.2	6	7	20	4	22	24	15	NA	7
S21 (dB)	15	13.5	13.5	7	10	11.5	14.3	5.6	8	17	20	18
O1CP (dBm)	10	7	7.5	NA	5	1.5	10.5	9	NA	14.5	12	13.1
DC power (mW)	84	NA	99	300	110	125	150	90	NA	400	195	248
Area (mm^2)	0.15	1.8	0.7	2.04	1.13	0.61	0.18	0.26	0.26	2.4	0.6	0.1
Technology	90nm CMOS	130nm CMOS	90nm CMOS	0.18um CMOS	90nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	0.12um SiGe	0.12um SiGe	0.12um SiGe	0.12ur SiGe
FOM (W.GHz)	312.4	14.5688	39.8	2.5	15.9	10.2	120	19.5	195	2138	2563	2884
Architecture	3 stages diff transformer coupled	5 cascode stages X2 /Doherty	2 brd-band amps + 2 brd-side couplers	3 stages Cascode/ single	3 stages Cascode/ single	3 stages CS / Single	3 stages CS+ comb.	2 stages diff transformer coupled	Broadband Combiner	4 stages CE single Combiner	3 stages Cascode CE(2x)	single stage push-pu cascoc

Example 1: 90nm CMOS 0.7-V Operation 60-GHz CMOS PA

M. Tanomura, et al.,IEEE ISSCC, Feb. 2008







Die size: 560 μm x 280 μm
(without PAD area)

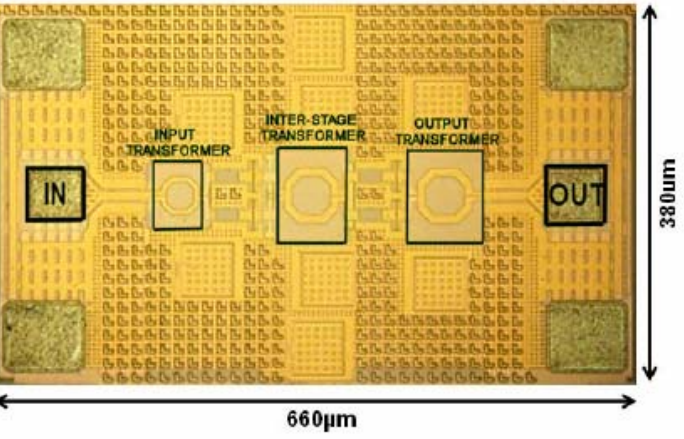
mmW State of the art PA Solutions

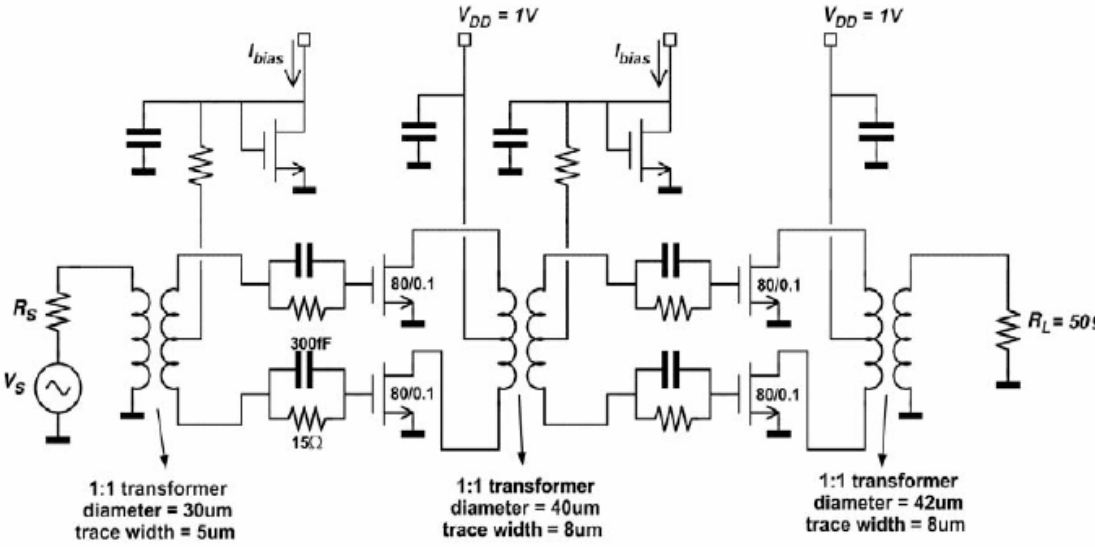
$$FOM_{PA} = P_{sat} \cdot G \cdot PAE \cdot f^2$$

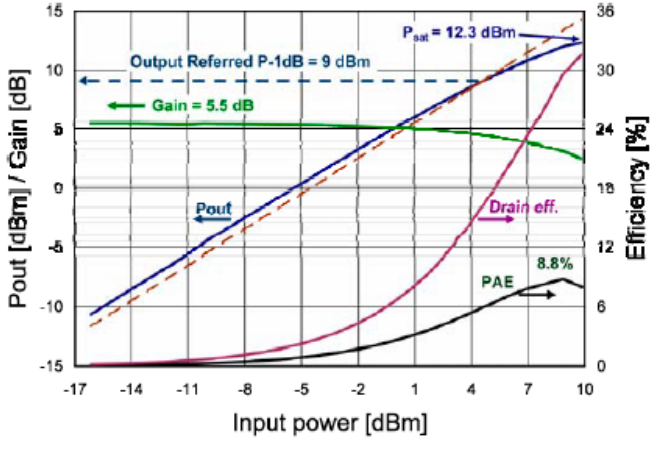
PA features	[45]	[46]	[39]	[40]	[21]	[22]	[41]	[42]	[54]	[55]	[56]	[57]
Frequency (GHz)	63	60	44	40	60	60	62	60	85	77	77	60
at.Out Power (dBm)	12.5	7.8	10.6	10.4	8	7	11.5	12.3	21	17.5	14.4	20
Peak PAE (%)	14	3	8	2.9	7	4	8.2	8.8	3.4	12.8	15.7	12.7
3dB BW (GHz)	4	6.7	37.2	6	7	20	4	22	24	15	NA	7
S21 (dB)	15	13.5	13.5	7	10	11.5	14.3	5.6	8	17	20	18
O1CP (dBm)	10	7	7.5	NA	5	1.5	10.5	9	NA	14.5	12	13.1
DC power (mW)	84	NA	99	300	110	125	150	90	NA	400	195	248
Area (mm^2)	0.15	1.8	0.7	2.04	1.13	0.61	0.18	0.26	0.26	2.4	0.6	0.1
Technology	90nm CMOS	130nm CMOS	90nm CMOS	0.18um CMOS	90nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	0.12um SiGe	0.12um SiGe	0.12um SiGe	0.12ur SiGe
FOM (W.GHz)	312.4	14.5688	39.8	2.5	15.9	10.2	120	19.5	195	2138	2563	2884
Architecture	3 stages diff transformer coupled	5 cascode stages X2 /Doherty	2 brd-band amps + 2 brd-side couplers	3 stages Cascode/ single	3 stages Cascode/ single	3 stages CS / Single	3 stages CS+ comb.	2 stages diff transformer coupled	Broadband Combiner	4 stages CE single Combiner	3 stages Cascode CE(2x)	single stages push-pu cascod

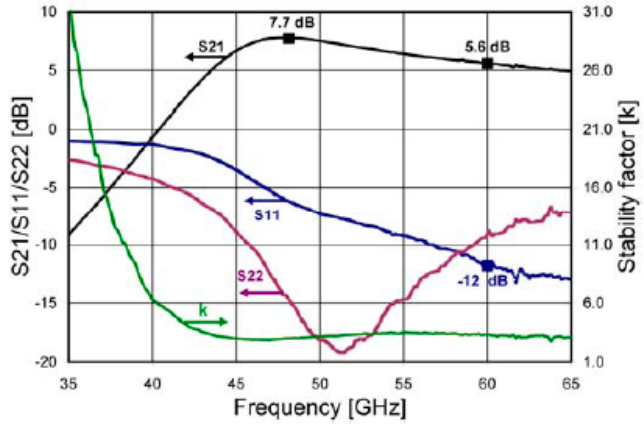
Example 2: 60GHz Transformer Coupler PA in 90nm CMOS

D. Chowdhury, et al.,IEEE ISSCC, Feb. 2008









mmW State of the art PA Solutions

$$FOM_{PA} = P_{sat} \cdot G \cdot PAE \cdot f^2$$

PA features	[45]	[46]	[39]	[40]	[21]	[22]	[41]	[42]	[54]	[55]	[56]	[57]
Frequency (GHz)	63	60	44	40	60	60	62	60	85	77	77	60
at.Out Power (dBm)	12.5	7.8	10.6	10.4	8	7	11.5	12.3	21	17.5	14.4	20
Peak PAE (%)	14	3	8	2.9	7	4	8.2	8.8	3.4	12.8	15.7	12.7
3dB BW (GHz)	4	6.7	37.2	6	7	20	4	22	24	15	NA	7
S21 (dB)	15	13.5	13.5	7	10	11.5	14.3	5.6	8	17	20	18
O1CP (dBm)	10	7	7.5	NA	5	1.5	10.5	9	NA	14.5	12	13.1
DC power (mW)	84	NA	99	300	110	125	150	90	NA	400	195	248
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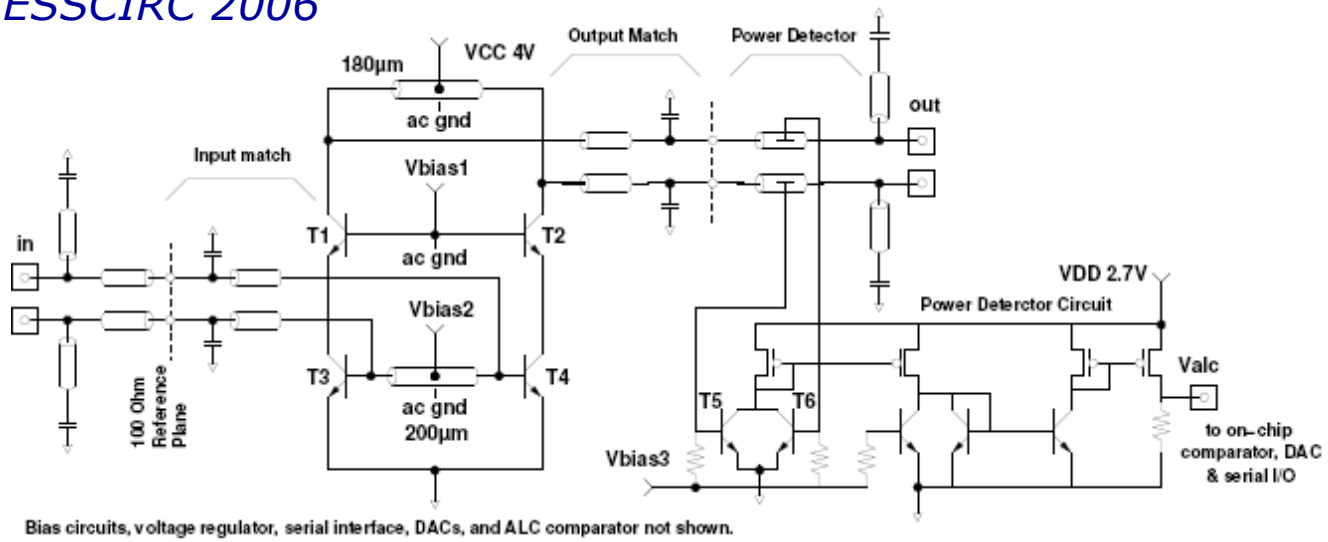
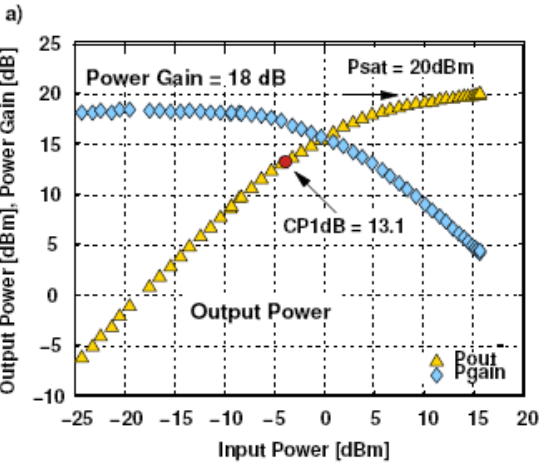
Technology	90nm CMOS	130nm CMOS	90nm CMOS	0.18um CMOS	90nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	0.12um SiGe	0.12um SiGe	0.12um SiGe	0.12u SiGe
FOM (W.GHz)	312.4	14.5688	39.8	2.5	15.9	10.2	120	19.5	195	2138	2563	2884
Architecture	3 stages diff transformer coupled	5 cascode stages X2 /Doherty	2 brd-band amps + 2 brd-side couplers	3 stages Cascode/ single	3 stages Cascode/ single	3 stages CS / Single	3 stages CS+ comb.	2 stages diff transformer coupled	Broadband Combiner	4 stages CE single Combiner	3 stages Cascode CE(2x)	single stage push-p cascod

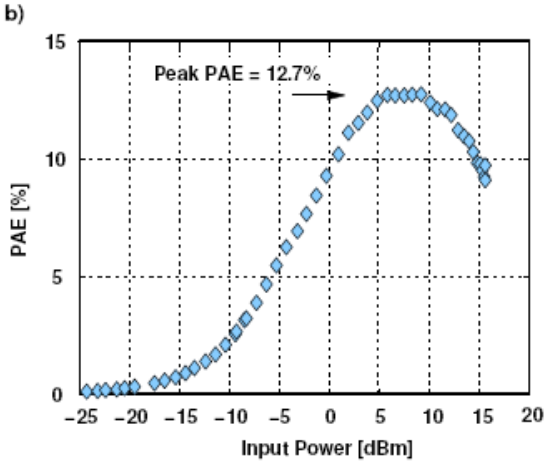
Example 1: 0.13µm SiGe:C BiCMOS 60GHz 10dBm PA with ALC

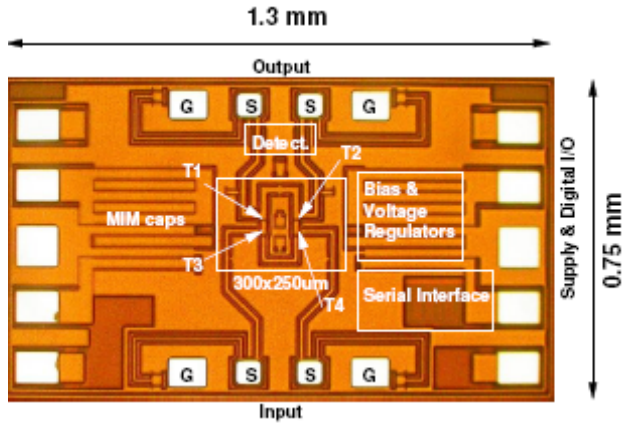
U.R. Pfeiffer, ESSCIRC 2006



Bias circuits, voltage regulator, serial interface, DACs, and ALC comparator not shown.







mmW State of the art PA Solutions

$$FOM_{PA} = P_{sat} \cdot G \cdot PAE \cdot f^2$$

PA features	[45]	[46]	[39]	[40]	[21]	[22]	[41]	[42]	[54]	[55]	[56]	[57]
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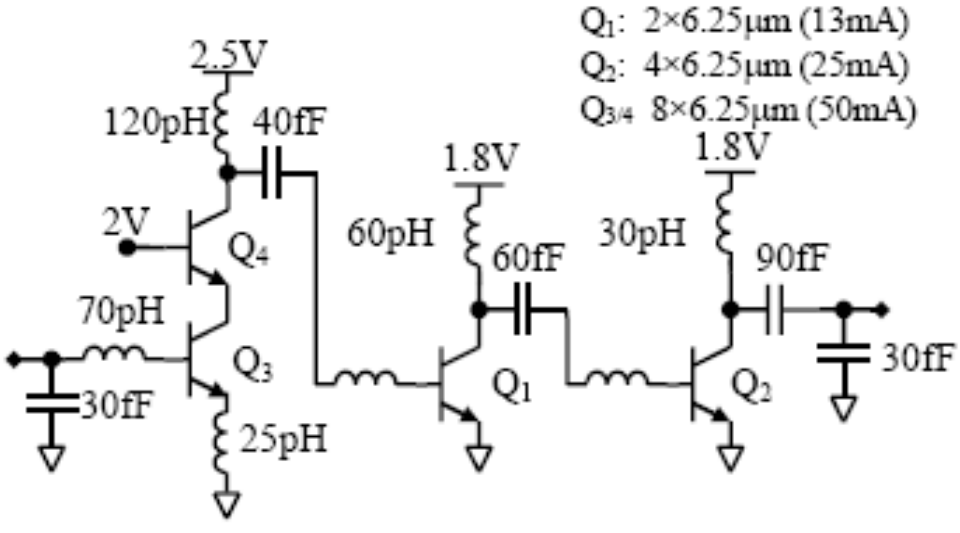
Peak PAE (%)	14	3	8	2.9	7	4	8.2	8.8	3.4	12.8	15.7	12.7
3dB BW (GHz)	4	6.7	37.2	6	7	20	4	22	24	15	NA	7
S21 (dB)	15	13.5	13.5	7	10	11.5	14.3	5.6	8	17	20	18
O1CP (dBm)	10	7	7.5	NA	5	1.5	10.5	9	NA	14.5	12	13.1
DC power (mW)	84	NA	99	300	110	125	150	90	NA	400	195	248
Area (mm^2)	0.15	1.8	0.7	2.04	1.13	0.61	0.18	0.26	0.26	2.4	0.6	0.1
Technology	90nm CMOS	130nm CMOS	90nm CMOS	0.18um CMOS	90nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	0.12um SiGe	0.12um SiGe	0.12um SiGe	0.12u SiGe
FOM (W.GHz)	312.4	14.5688	39.8	2.5	15.9	10.2	120	19.5	195	2138	2563	2884
Architecture	3 stages diff transformer coupled	5 cascode stages X2 /Doherty	2 brd-band amps + 2 brd-side couplers	3 stages Cascode/ single	3 stages Cascode/ single	3 stages CS / Single	3 stages CS+ comb.	2 stages diff transformer coupled	Broadband Combiner	4 stages CE single Combiner	3 stages Cascode CE(2x)	single stage push-p cascod

Example 2: 0.13µm SiGe:C BiCMOS 77GHz 14.4dBm PA

S. Nicolson, et al., IMS 2007



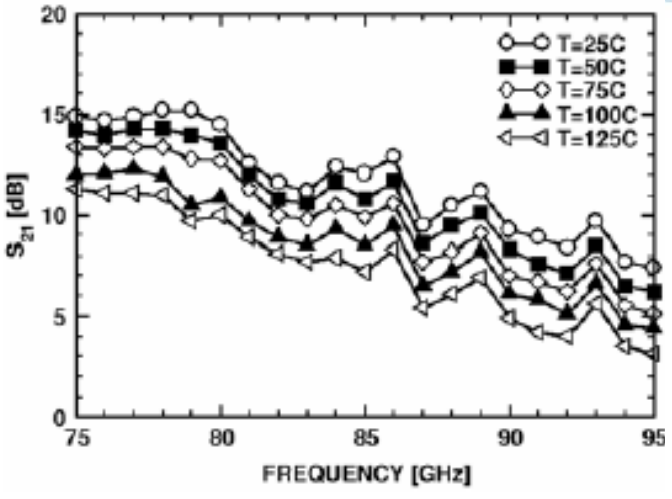
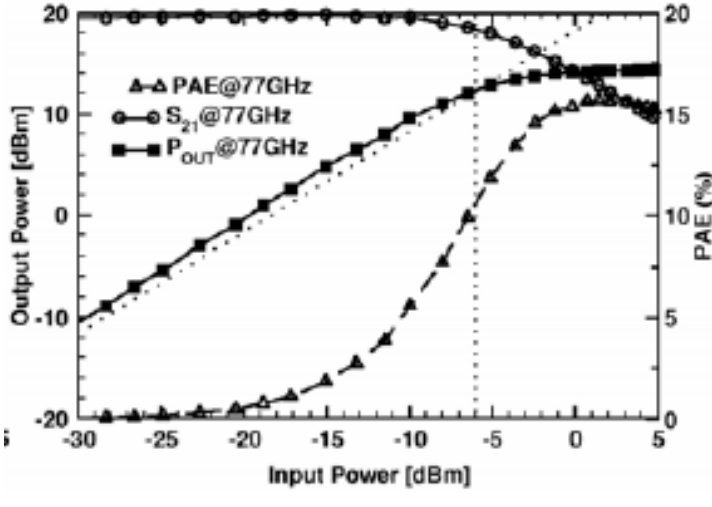


Fig. 13. PA gain over temperature.

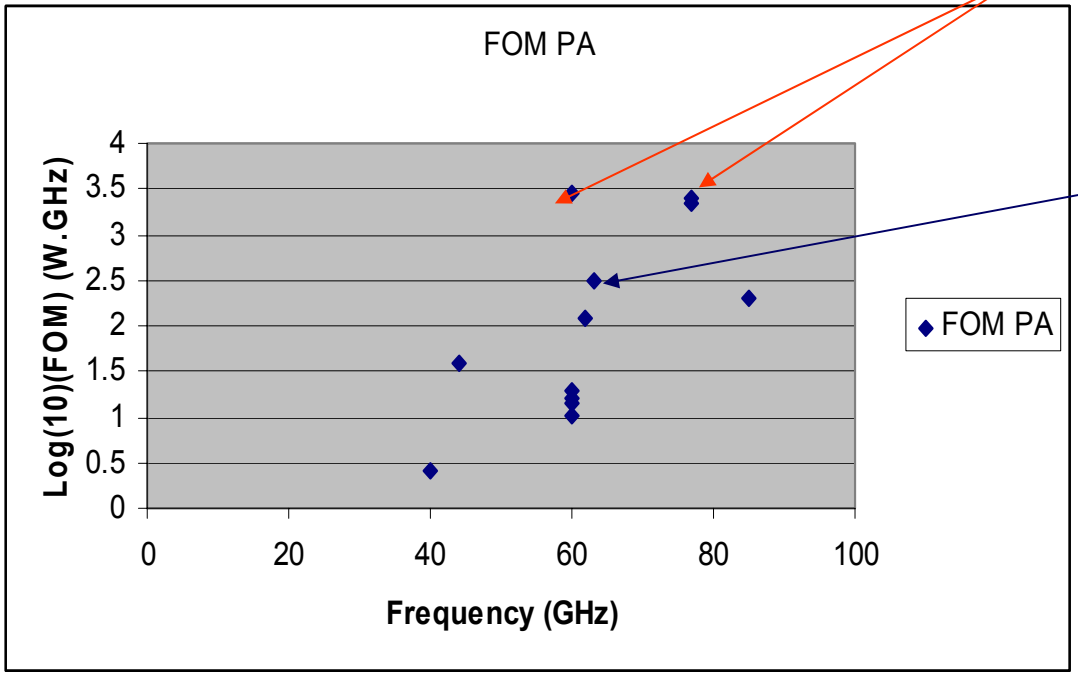


mmW State of the art PA Solutions

$$FOM_{PA} = P_{sat} \cdot G \cdot PAE \cdot f^2$$

SiGe HBT

Bulk CMOS

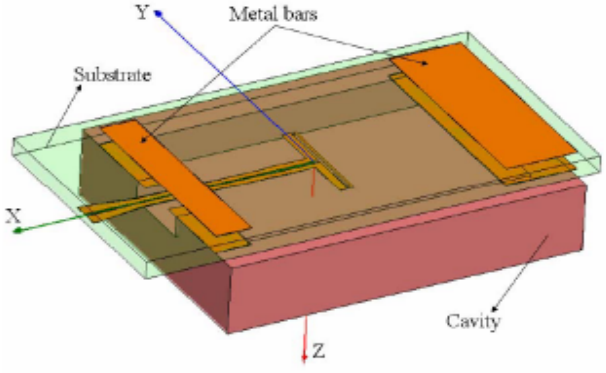


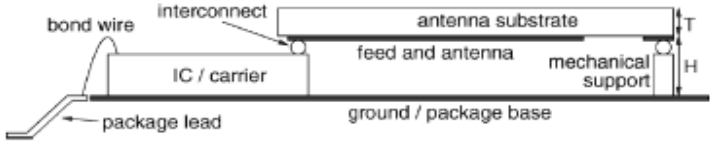
The PA design performances in mmW mainly depends the available Power gain:

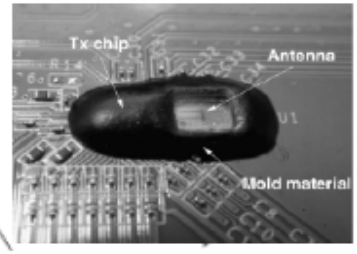
- mmW PA is Technology dependent dependent.
- Best SiGe FOM is one decade over Best CMOS performance.

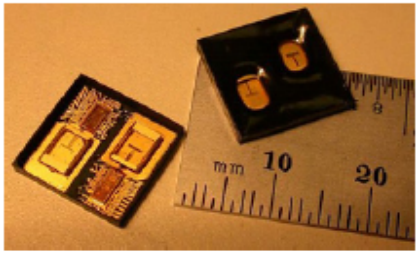
And …
The Package and the Antenna make the Difference…

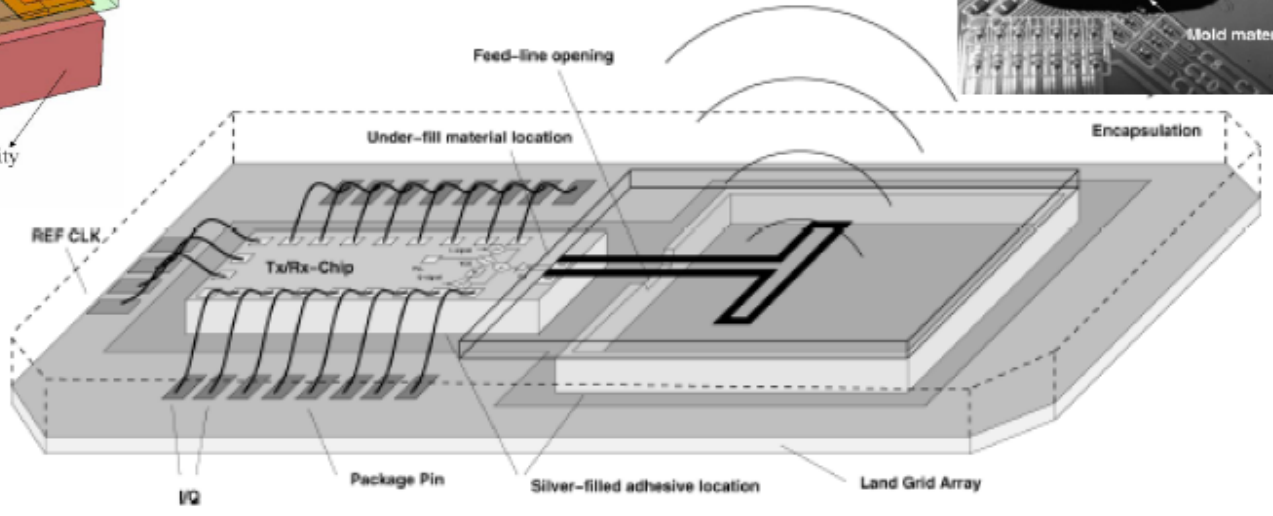
Antenna Substrate	Antenna type	Gain, frequency	Bandwidth	Package Size	Technology	Advantages	Drawbacks
Quartz	Folded-dipole with cavity	7dBi, 60 GHz	14%	13x13mm	Flip-chip LGA	Good performance, Low-cost packaging	Critical assembly, Reliability











Ref. U.R.Pfeiffer, J.Gryzyb, D.Liu, et.al., A Chip-Scale Packaging technology for 60GHz Wireless Chipsets, IEEE Transactions on MTT, Aug.2006

20 dBm PA with 7dBi antenna performs 700Mbs at 10meters in directive conditions, demonstrated at ISSCC 06 by IBM.

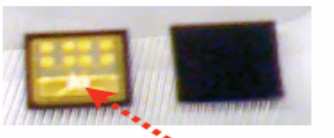
And …
The Package and the Antenna make the Difference…

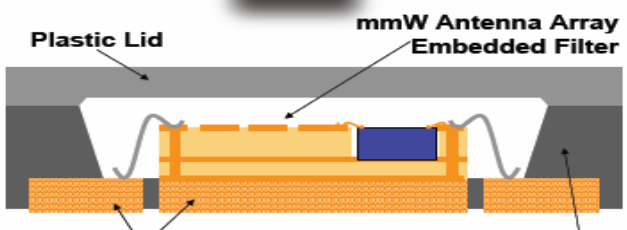
Integrated mmW BGA and QFN Technology

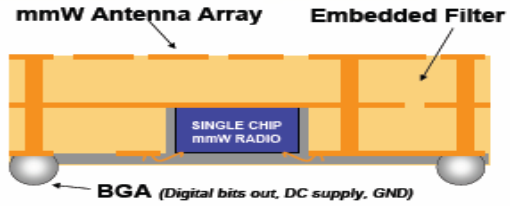
GEDC

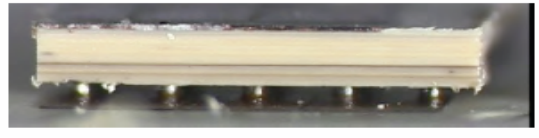
QFN test socket

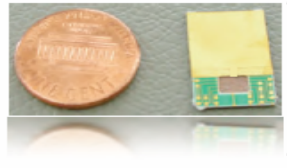
QFN Module
Integrated Antenna
5x 5 mm²



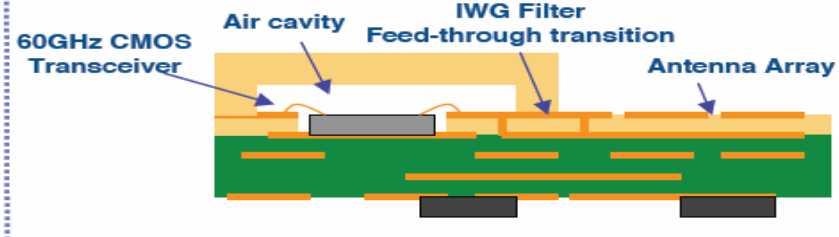








BGA Module
Integrated Antenna
15x 15 mm²



Ref: J.Laskar & all « 60GHz CMOS 90nm Radio with Integrated signal processor » Proceeding IEEE ISSCC 08

7 dBm PA with 12 dBi antenna aray performs 3Gbs at 1meter in 30° beam conditions, demonstrated at ISSCC 08.

And …
The Package and the Antenna make the Difference…

18.6 A Low-Power Fully Integrated 60GHz Transceiver System with OOK Modulation and On-Board Antenna Assembly

Jri Lee, Yenlin Huang, Yentso Chen, Hsinchia Lu, Chiajung Chang

National Taiwan University, Taipei, Taiwan

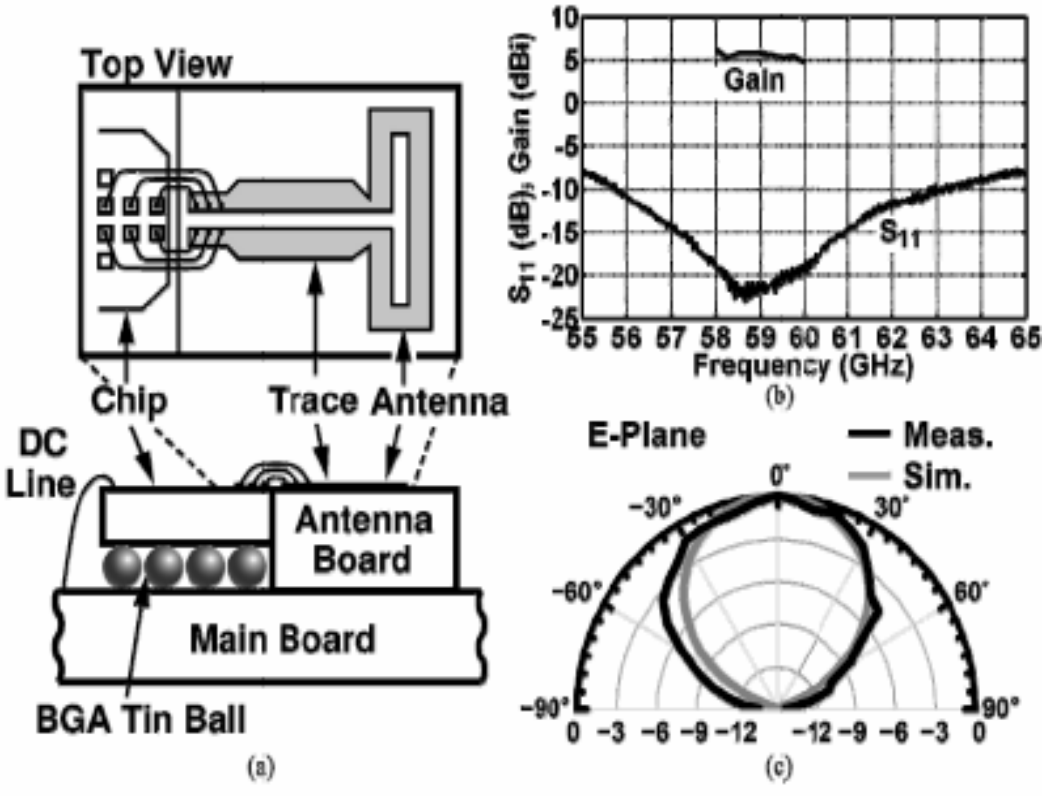


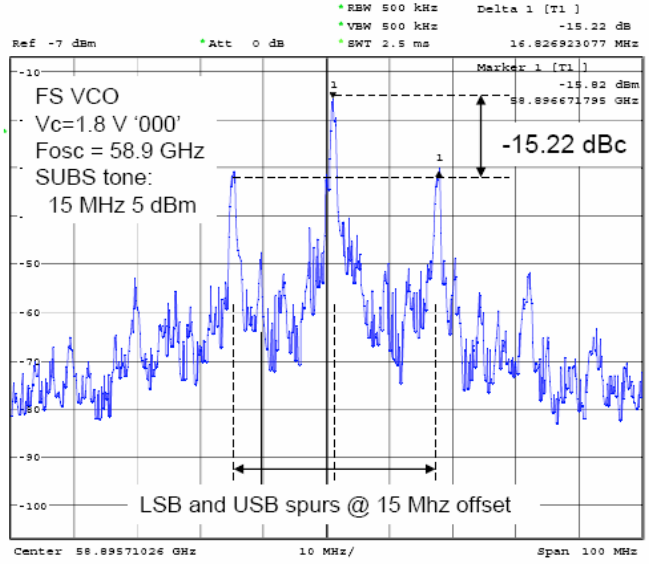
Figure 18.6.5: (a) Chip and antenna assembly, (b) S_{11} and gain of the dipole antenna (equipment limited), (c) antenna pattern (E-plane).

7 dBm PA with 4 dBi antenna performs 3Gbs at 3cm in 180° beam conditions, presented at ISSCC 09.

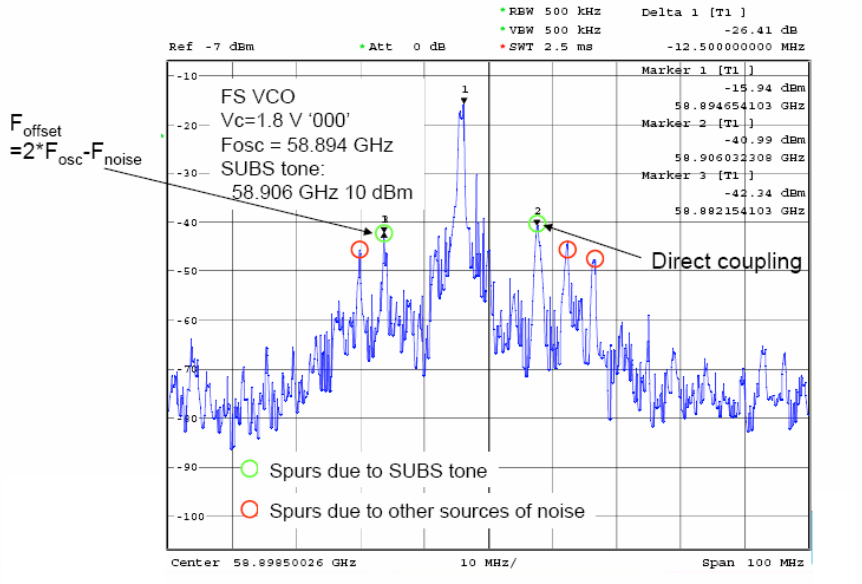
And …
What About the coupling effects…

Impact of substrate noise

- Low frequency substrate noise:



- High frequency substrate noise:



Thanks to Jose-Luis Gonzalez UPC Barcelona:
At 60GHz in the medium resistive substrate the direct mixing or harmonic mixing phenomena seems to be of very strong importance. This study is on going.

Assembly in Summary.

- **DON'T FORGET!**
  - The Package and the Antenna could participate to the global performance up to 50%.
  - The Antenna strategy will define the needed PA output power and the requirement or not of a Beam forming architecture.
  - The Package will include the Circuit and the Antenna.
  - mmW Substrate coupling seems to forbid robust solutions in ZIF architecture.

- The Trade Off:
  - Performances Versus Cost!
  - How to have a very efficient antenna in Low cost package?
  - How to have low Lossy paths in Low cost package?

Outline

- Target applications for the Millimeter-wave frequency band
- Silicon technologies to address mmW complete solutions
  - Active devices on bulk and SOI technologies
  - Passive devices
- Silicon integrated solutions for mmW circuits
  - LNA mmW designs
  - Down-conversion mixers for mmW
  - Voltage controlled oscillators for mmW
  - Power amplifiers for mmW
  - mmW Assembly
- **Conclusions**

Industrial Silicon mmW applications SWOT (I)

- **STRENGTH**
  - Mobile communications and wireless connectivity applications are:
    - Excellent enablers for 60GHz WLAN/WPAN applications
    - Driving force for CMOS & BiCMOS mmW Technology Platforms
  - System mmW experience exists from III-V / discrete components
  - University Design Know-How
  - mmW VLSI integration capabilities with Si based technologies

- **WEAKNESS**
  - Low incidence of consumer-oriented projects so far (for very high volumes)
  - Lack of true leadership on standards definition (national conflict of interest?)
  - Industry design large scale experience in mmW has still to be acquired
  - Experience in industrial robust mmW packaging solutions to be acquired
  - Need to find Low Cost Solutions for mmW Antennas and Packages

Industrial Silicon mmW applications SWOT (I)

• OPPORTUNITIES

- Automotive applications, at mid-term, may become:
  - Enablers for radar applications
  - Driving force for mmW BiCMOS Technology Platforms
- Si technology mmW capability is a « More than Moore » feature which opens opportunities for leadership in specific areas
- mmW-oriented VLSI CAD Design Platforms availability to come
- Emerging applications for THz integrated devices:
  - Imaging for Medical and Safety /Security Applications
  - 100Gb/s Ethernet Fiber Optics communications

• THREATS

- Economic crisis may delay mmW consumer applications ramp-up
- Competition between geographical areas for standard supremacy
- Use of leading edge 300mm fabs requires several Billions € market in CMOS approach
- BiCMOS offer is limited to few foundries which limit second sources possibilities.

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