Overcoming Offset

Prof. Kofi Makinwa

Electronic Instrumentation Laboratory / DIMES
Delft University of Technology
Delft, The Netherlands

email: k.a.a.makinwa@tudelft.nl

TUDelft
Delft University of Technology

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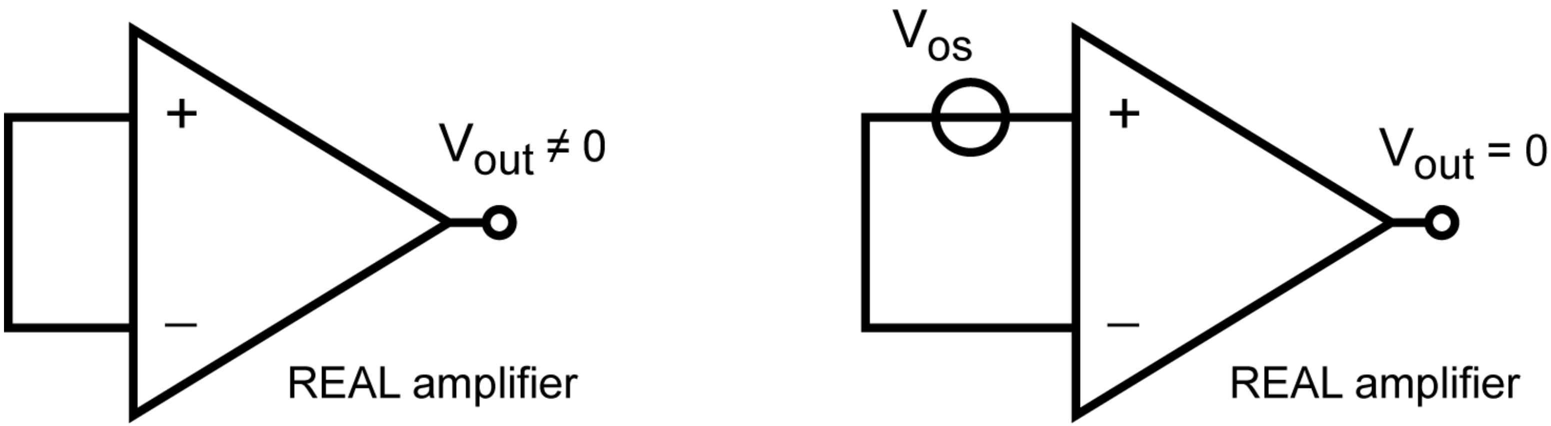
Motivation

- The offset of amplifiers realized in standard IC technologies is typically in the **millivolt** range
- However, many analog circuits e.g. opamps, comparators, ADCs and DACs require amplifiers with **microvolt** offsets
- Also, many sensors (e.g. thermopiles, bridges, hall-effect sensors etc.) output DC signals that need to be processed with **microvolt** precision
- This tutorial will focus on **dynamic** offset-cancellation (DOC) techniques, with which offset can be reduced to the **microvolt** level.

Outline

- Differential amplifiers
  - Offset and 1/*f* noise
- Dynamic Offset Cancellation (DOC)
  - Auto-zeroing
  - Correlated Double-Sampling (CDS)
  - Chopping
- Summary
- References

What is Offset?



- When the input of a REAL amplifier is shorted, $V_{out} \neq 0$!
- The **offset** V_{os} is the input voltage required to make $V_{out} = 0$. It is typically in the range: 100µV to 10mV.

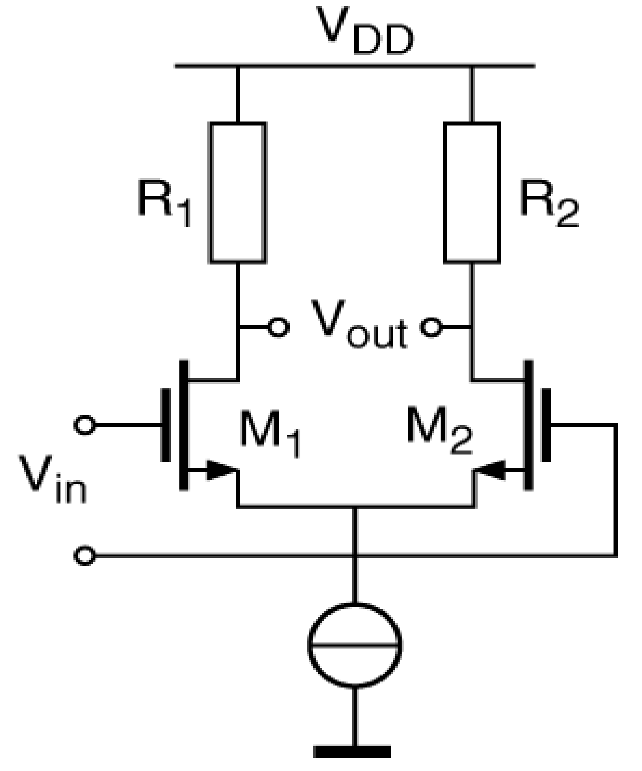
- Note: In CMOS, input offset currents are negligible.

Differential Amplifiers

Differential amplifiers are often used to amplify DC signals.

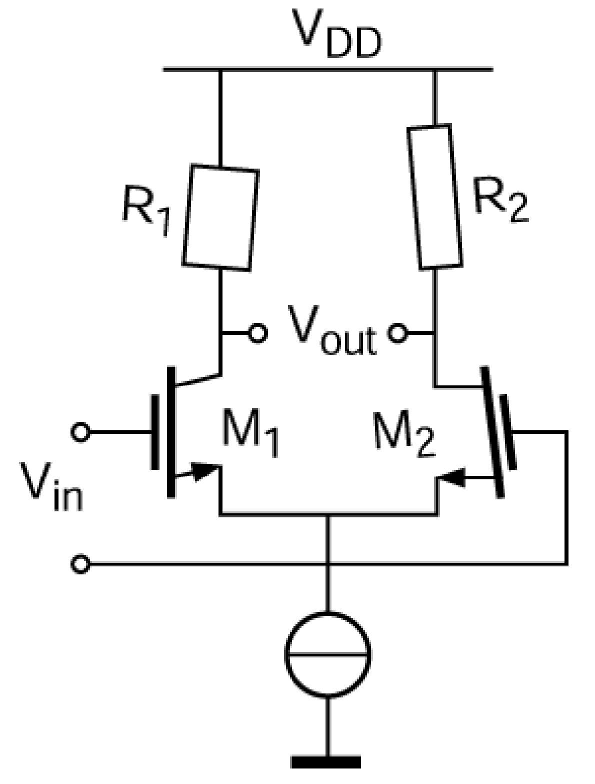
Their balanced structure is

- Nominally offset free
- Rejects common-mode and power supply interference
- Easily realized in both CMOS and bipolar technologies



Offset in Differential Amplifiers

Component mismatch
e.g. $R_1 \neq R_2$, $M_1 \neq M_2 \Rightarrow$ **offset**



Mismatch is mainly due to

- Doping variations
- Lithographic errors
- Packaging & local stress

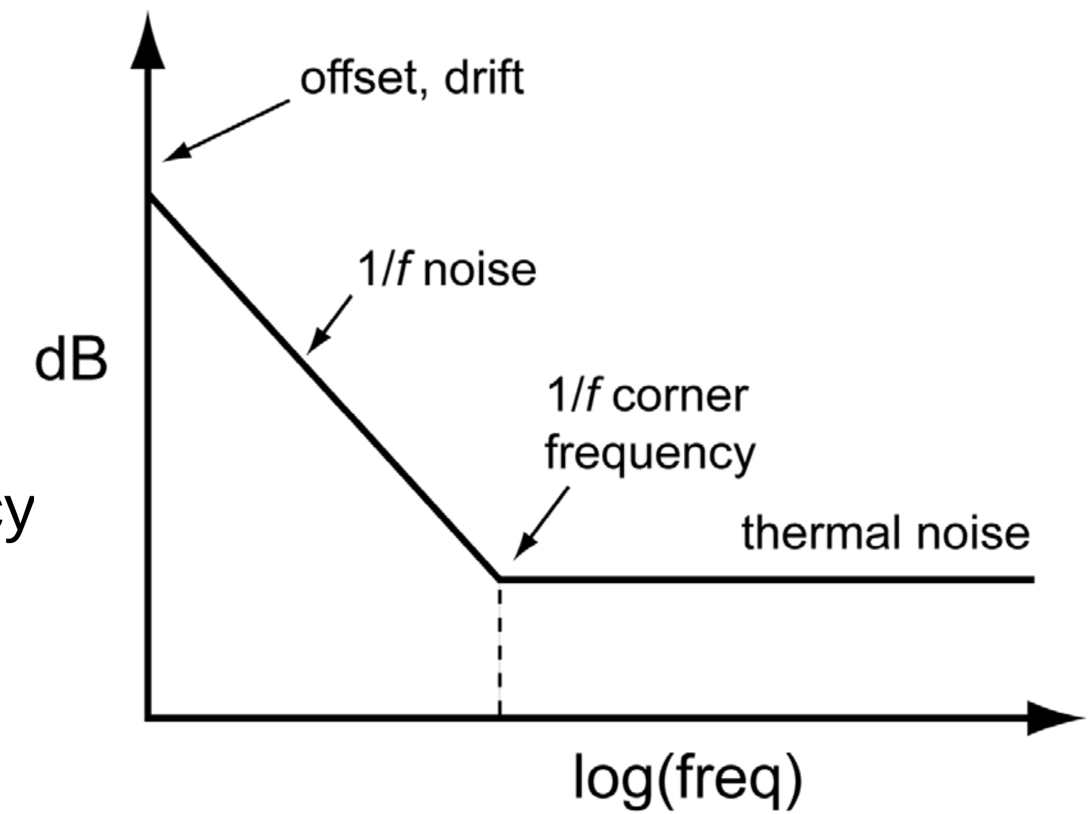
All things being equal

- Bipolar $\Rightarrow V_{os} \sim 0.1\text{mV}$
- CMOS $\Rightarrow V_{os}$ is 10 -100x worse!

Amplifier Behaviour Near DC

Characterized by

- Offset
- Drift
- 1/*f* (flicker) noise
- Thermal noise
- 1/*f* corner frequency



What to Do?

Offset and 1/*f* noise are part of life!

But we can reduce offset "enough" by

1. Using "large" devices and good layout[1] ⇒ 1mV
2. Trimming ⇒ 100μV drift over temperature (MOS)
3. Dynamic offset-cancellation (DOC) techniques ⇒ 1μV

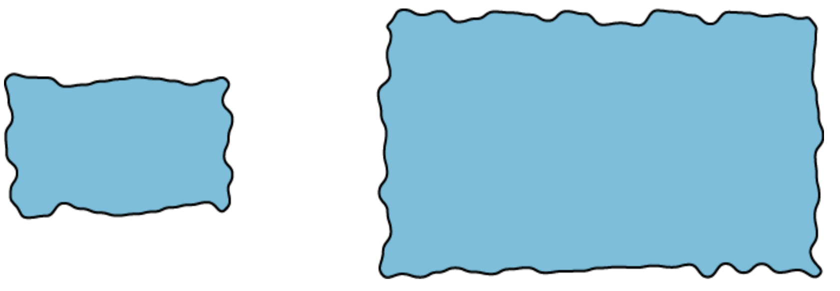
DOC techniques also

- Reduce drift and 1/*f* noise
- Improve PSRR and CMRR

Mismatch

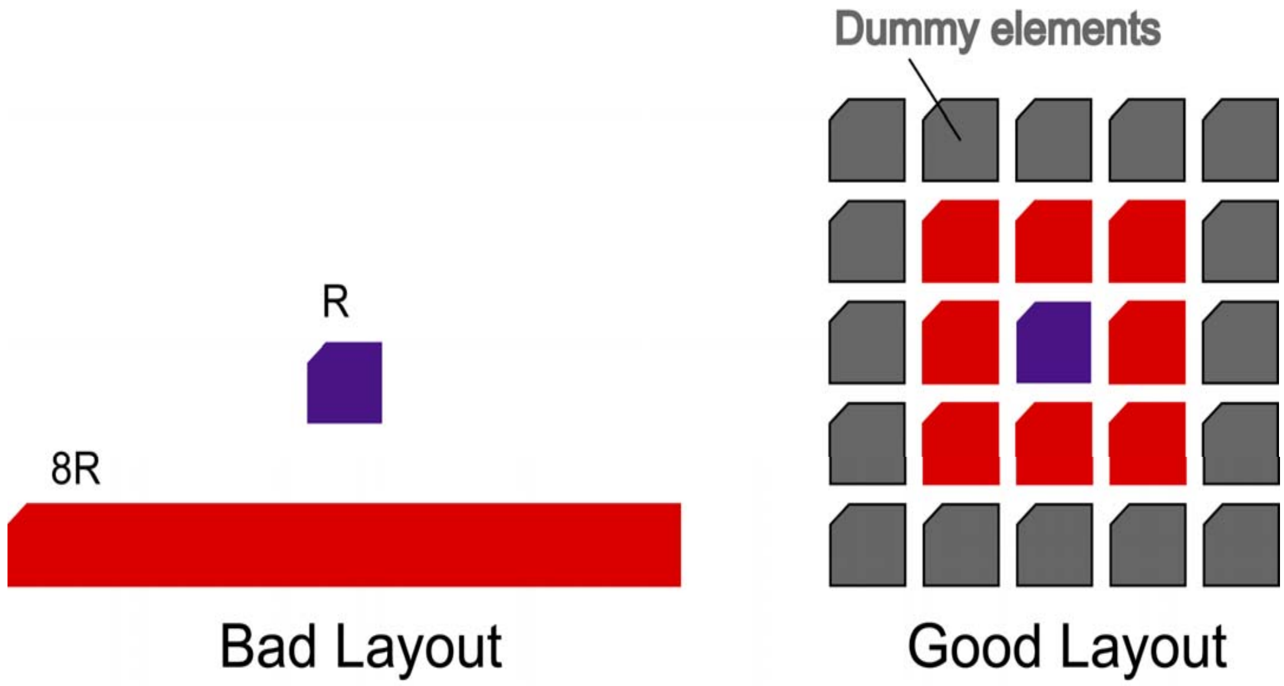
Determined by:

1. Lithographic accuracy e.g. $R = \rho L/W$
   $\Rightarrow \Delta R/R \sim \Delta L/L + \Delta W/W$
   $\Rightarrow$ Matching improves with area!



2. Doping Variations $\Rightarrow \Delta R/R$ limited to 0.1% even for large neighboring resistors
3. Mechanical stress due to metal lines or packaging

Good Layout Helps!



Good layout $\Rightarrow$

- Large Devices
- Exclusive use of unit cells (and dummies)
- Currents in unit cells flow in the same direction

Trimming

⇒ Cancel offset by adjusting an on-chip component

✓ Low circuit complexity

✓ Minimal effect on circuit bandwidth

✗ Requires test equipment

✗ Does not reduce drift or 1/*f* noise

✗ Requires an analog memory, e.g.

- Fusible links (Zener diodes)
- Laser-trimmed resistors
- PROM + DAC (component array)

Trimming a BJT Differential Amp

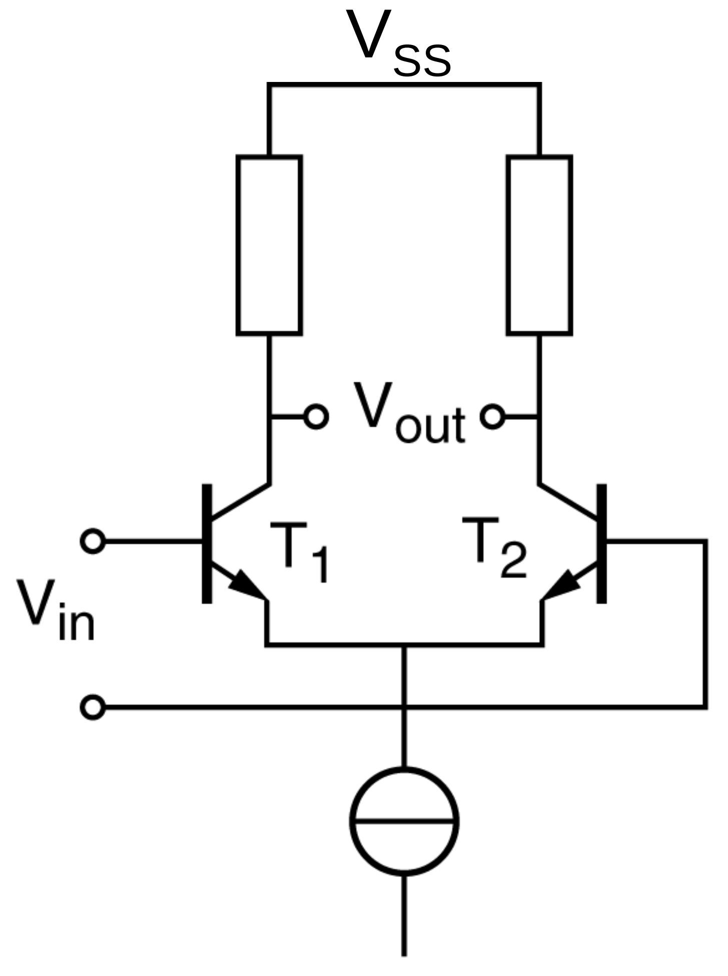
$$V_{os} = V_T \left(\frac{\Delta R}{R} + \frac{\Delta I_S}{I_S} \right)$$

$V_T = kT/q = 26mV$ @ 300K

- $V_{OS} \sim 0.1mV$ is possible!

After trimming (via ΔR)

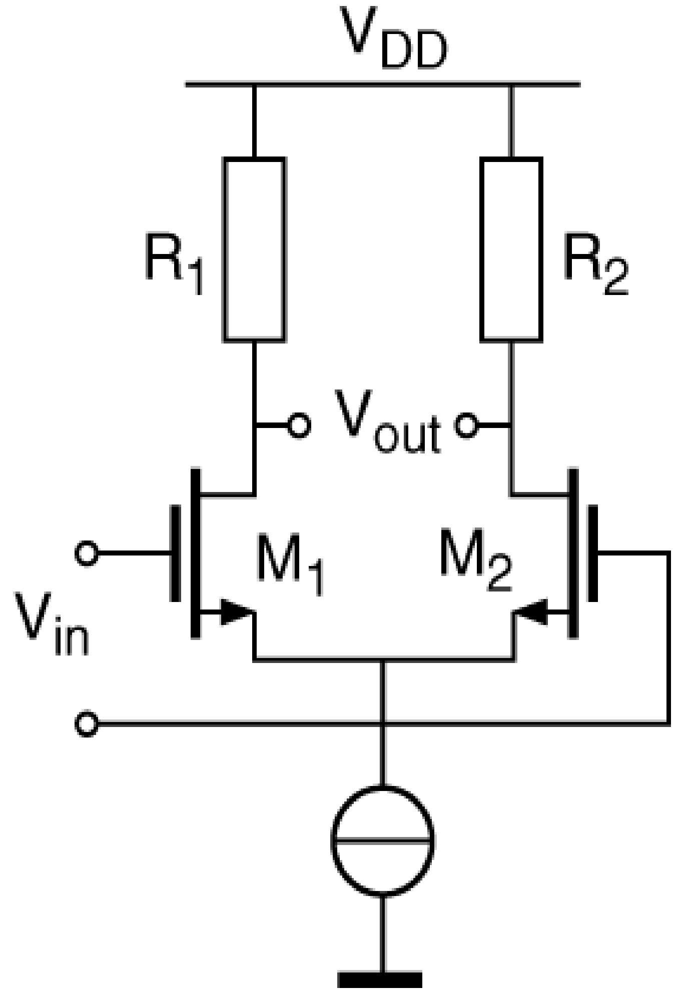
- $V_{OS} \sim 0$
- Also temperature coefficient of V_{OS} (TCV_{os}) ~ 0



Trimming a MOSFET Diff. Amp (1)

$$V_{os} = \Delta V_{TH} + \frac{I_D}{g_m}\left(\frac{\Delta R}{R} + \frac{\Delta \beta}{\beta}\right)$$

where $\beta = \mu C_{ox}(W/L)$



- ΔV_{TH} ~ 1mV
  and temp. independent
- I_D/g_m is temp. dependent

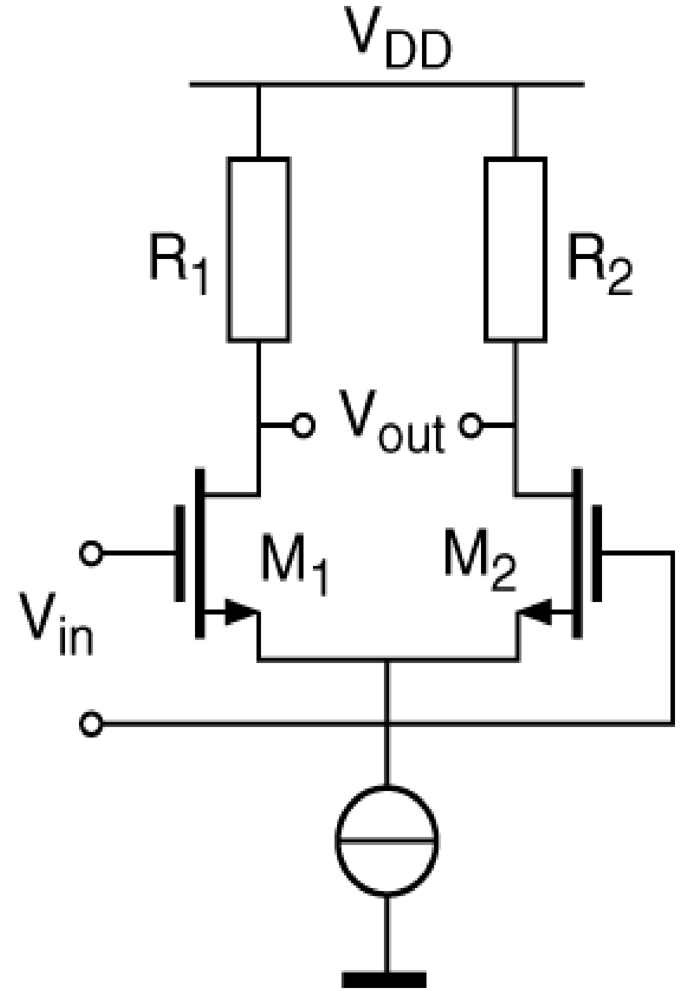
After trimming

- V_{OS} ~ 0 but TCV_{OS} ~ 1µV/°C
- Much worse than bipolar!

Trimming a MOSFET Diff. Amp (2)

$$V_{os} = \Delta V_{TH} + \frac{I_D}{g_m}\left(\frac{\Delta R}{R} + \frac{\Delta\beta}{\beta}\right)$$

where $\beta = \mu C_{ox}(W/L)$



Better trimming

- Trim V_{TH} & β *independently* at room temperature!
  $\Rightarrow$ TCV_{OS} ~ 0.33µV/°C (3σ)

M. Bolatkale et al., ISSCC 08

Trimming: Summary

- Simple, does not limit BW
- Does not reduce drift or 1/*f* noise
- Requires test equipment and an analog memory

- Works very well with BJT diff. amps
since it nulls both V_{OS} and TCV_{OS}
- Works less well with MOSFET diff. pairs
poorly defined $TCV_{OS} \Rightarrow$ 100µV drift over temp.

- Higher performance $\Rightarrow$ Dynamic offset cancellation

Dynamic Offset Cancellation (DOC)

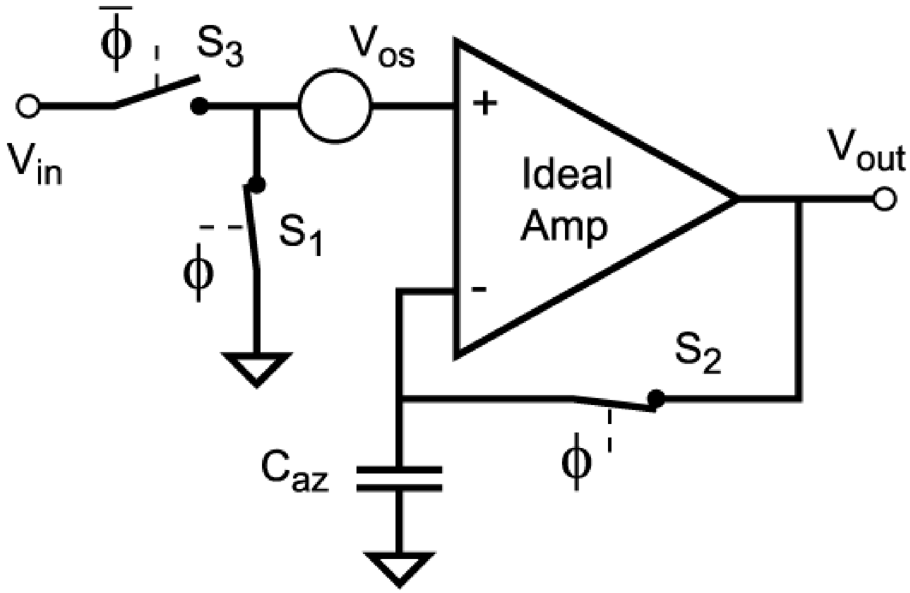
Two basic methods[2]

1. Measure the offset somehow and then subtract it from the input signal $\Rightarrow$ Auto-zeroing

2. Modulate the offset away from DC and then filter it out $\Rightarrow$ Chopping

Both methods also reduce low frequency noise and improve common-mode & power supply rejection

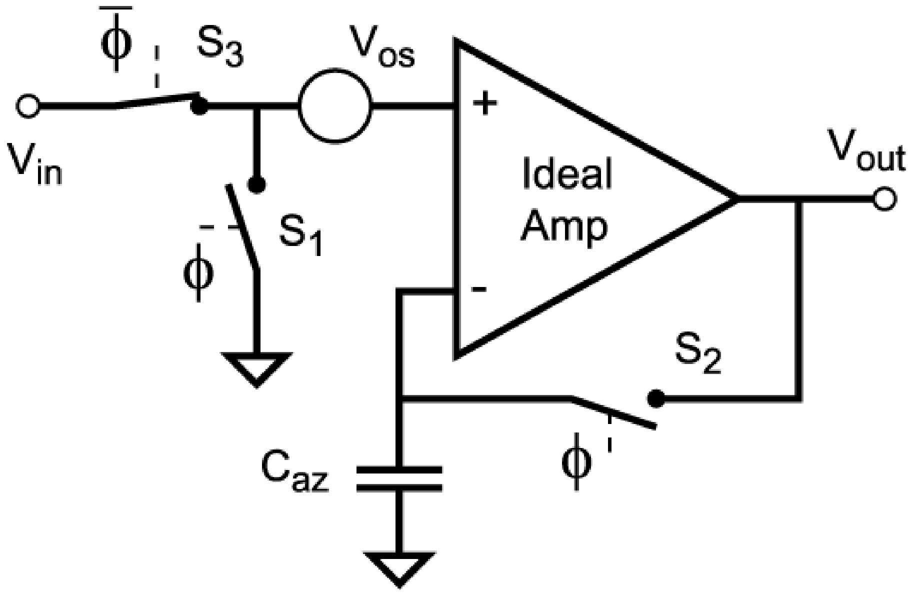
Auto-zero Principle (1)



Auto-zero phase

- S_1, S_2 closed, S_3 open $\Rightarrow$ $V_{out} = V_{os}$
  $\Rightarrow$ offset stored on C_{az}
- Amplifier is unavailable

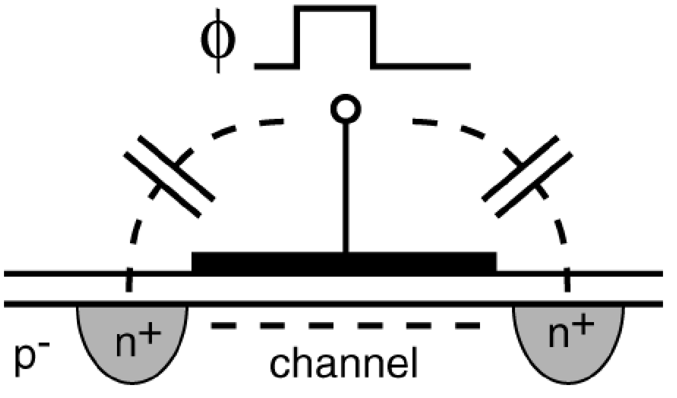
Auto-zero Principle (2)



Amplification phase:

- S_1, S_2 open, S_3 closed $\Rightarrow$ V_{in} is amplified
- *Finite* voltage gain A $\Rightarrow$ error in sampled offset
  $\Rightarrow$ input-referred residual offset $V_{res} = V_{os}/(A+1)$
- Charge injection is also a problem …

Charge Injection (1)

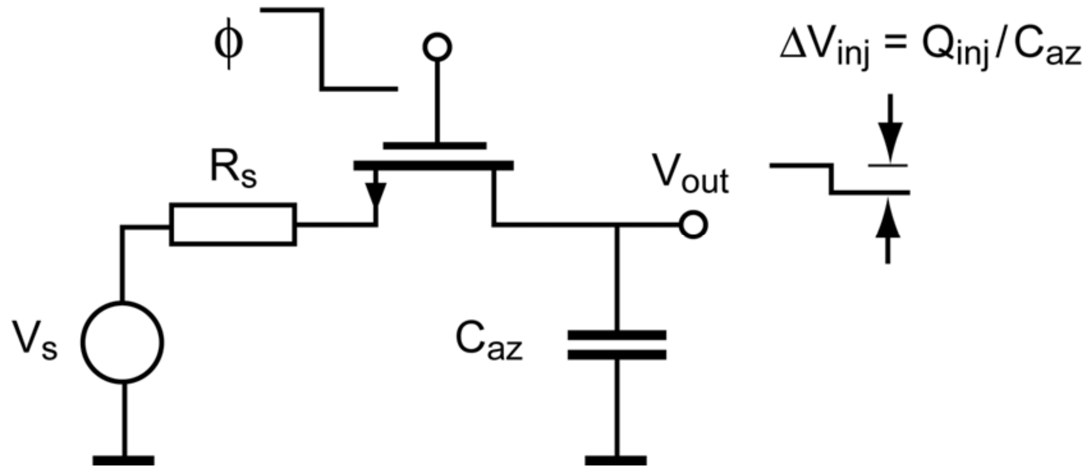


Consists of two components

1. Channel charge, $Q_{ch}= WLC_{ox}(V_{GS}-V_t)$
2. Charge transfer via the overlap capacitance between gate and source/drain $\Rightarrow$ clock feed-through

Problematic when a MOSFET switches **OFF**.

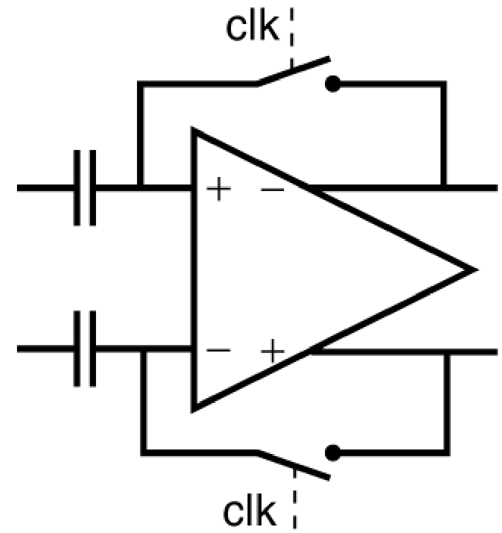
Charge Injection (2)



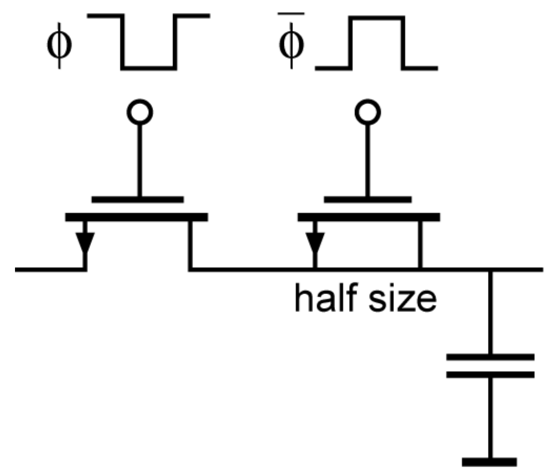
CI error voltage ΔV_{inj} depends on many factors[3,4]

- Source voltage and impedance
- Clock amplitude & slew rate
- Transistor area (WL) (smaller $\Rightarrow$ better)
- Value of C_{az} (larger $\Rightarrow$ better)
- In 0.7µm CMOS, minimum-size NMOS, 2.5V step & 10pF $\Rightarrow$ ΔV_{inj} ~ 250µV

Mitigating Charge Injection (CI)

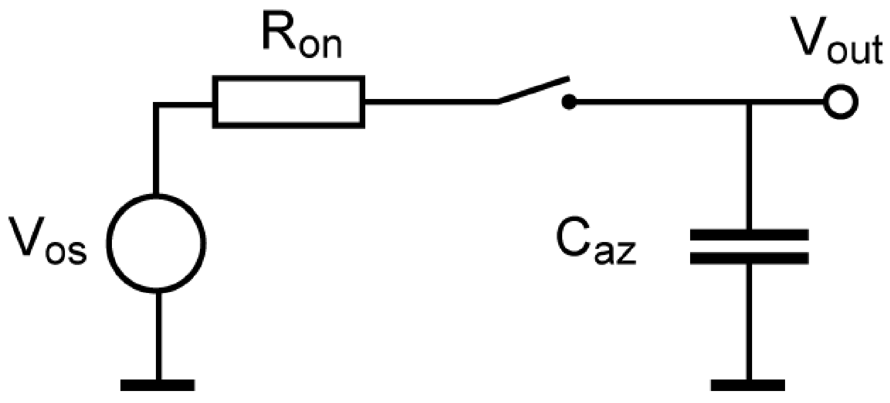


- Use differential topologies
  ⇒ CI is a common-mode signal
  ⇒ 1st order cancellation
- Use small switches & big caps
  (subject to noise & BW requirements)



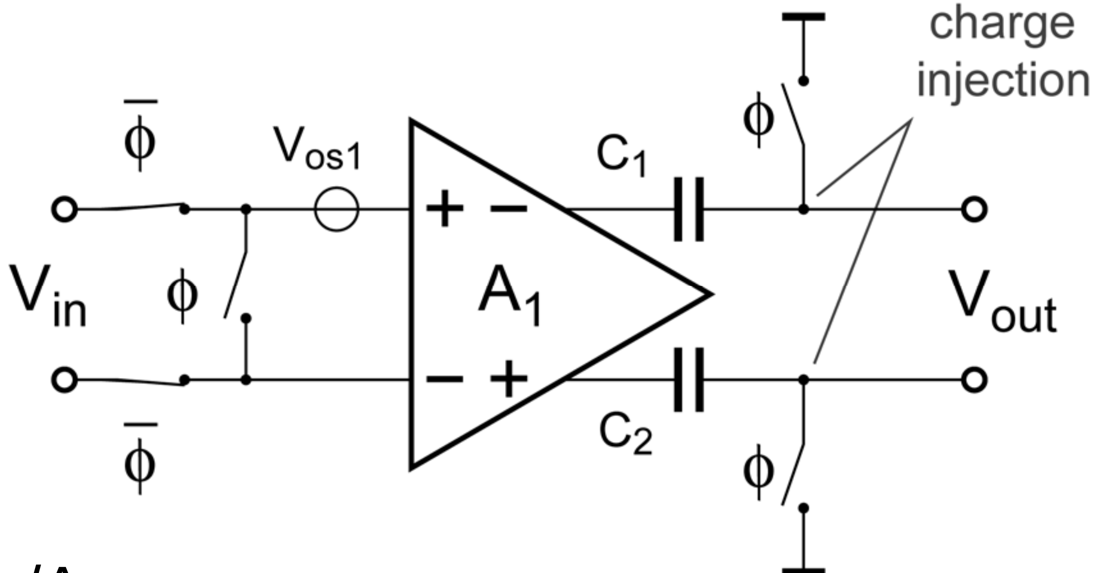
- For single-ended topologies
  dummy switches help[3,4]
- **But** area of main switch will be
  ~2x minimum size ⇒ more CI
  ⇒ limited benefit

Sampling the offset: kT/C noise



- Thermal noise of R_{on} is filtered by C_{az}
- When the switch is opened the instantaneous noise voltage is held on C_{az}
- Total noise power = kT/C_{az} (10pF @ 300K $\Rightarrow$ 20.3µV)
- Large capacitance $\Rightarrow$ accurate sampling of V_{os}

Output-Referred Auto-zeroing



$V_{res} = \Delta V_{inj}/A_1$

- Amplifier's offset is now completely cancelled[5,6]
- Gain of 1st amplifier reduces effects of charge injection and kT/C noise $\Rightarrow$ sampling capacitors can be smaller
- **But** too much gain $\Rightarrow$ clipping! $\Rightarrow$ A_1 is typically < 200

Residual Offset of Auto-zeroing

Determined by

- Charge injection
- Leakage on C_{az}
- Finite amplifier gain

In practice

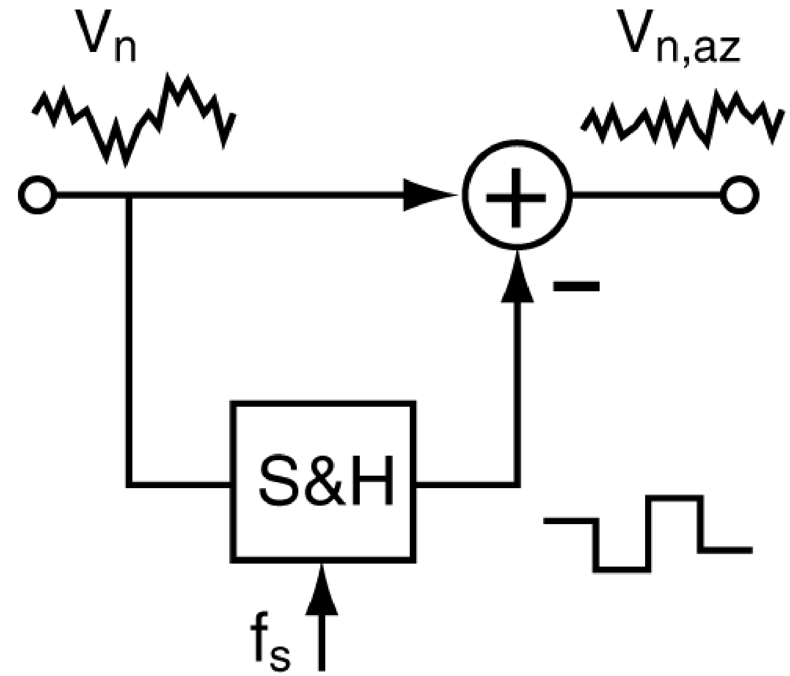
- Minimum size switches
- C_{az} as large as possible (sometimes external)
- Multi-stage amplifier topologies

Results in residual offsets of 1-10μV

Residual Noise of Auto-zeroing (1)

$V_{n,az}(f) = V_n(f)*(1 - H(f))$

H(f) is the frequency response of the S&H



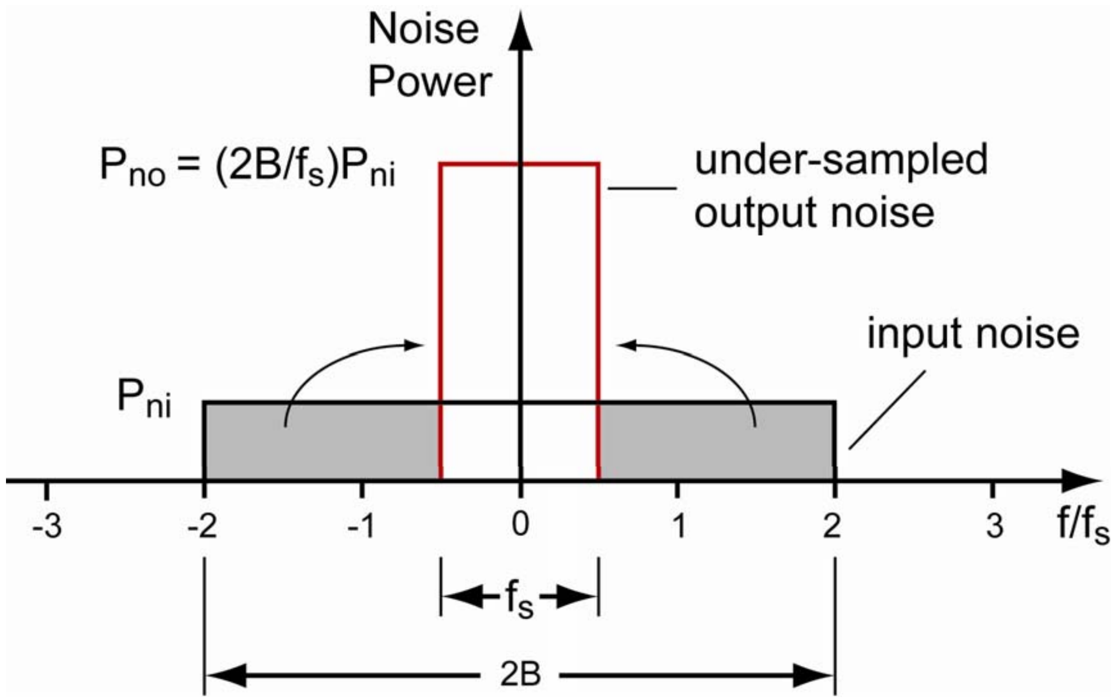
$H(f) = \mathrm{sinc}(\pi f/f_s) \Rightarrow$ LPF

$\Rightarrow$ 1 - H(f) is a HPF

$\Rightarrow$ reduction of both offset and 1/*f* noise

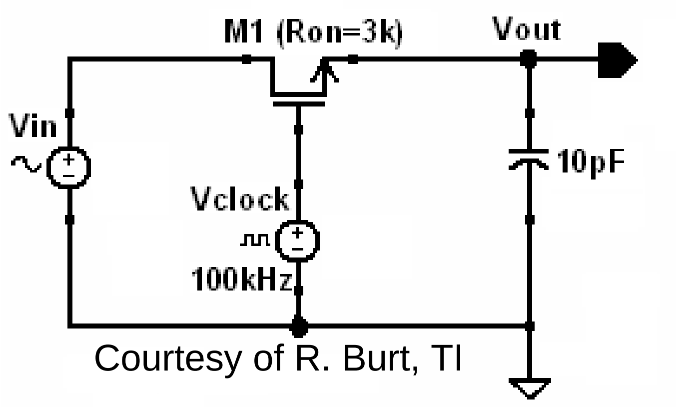
$\Rightarrow$ but sampled thermal noise will fold back to DC

Residual Noise of Auto-zeroing (2)

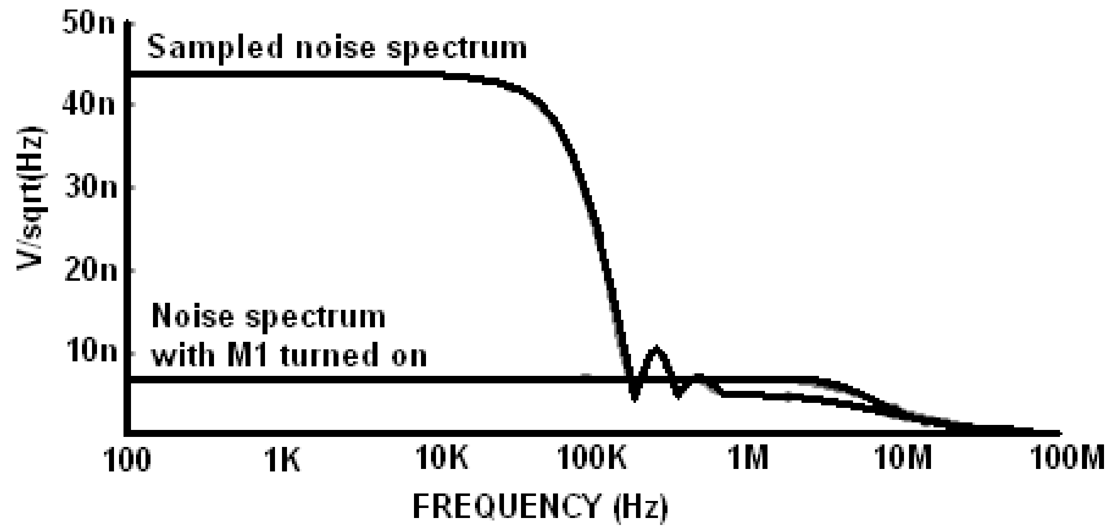


- **Noise** bandwidth $B > f_s$ (due to settling considerations) $\Rightarrow$ input noise will fold back (alias) to DC
- The result is then LP filtered by the $\mathrm{sinc}(\pi f/f_s)$ function

Residual Noise of Auto-zeroing (3)

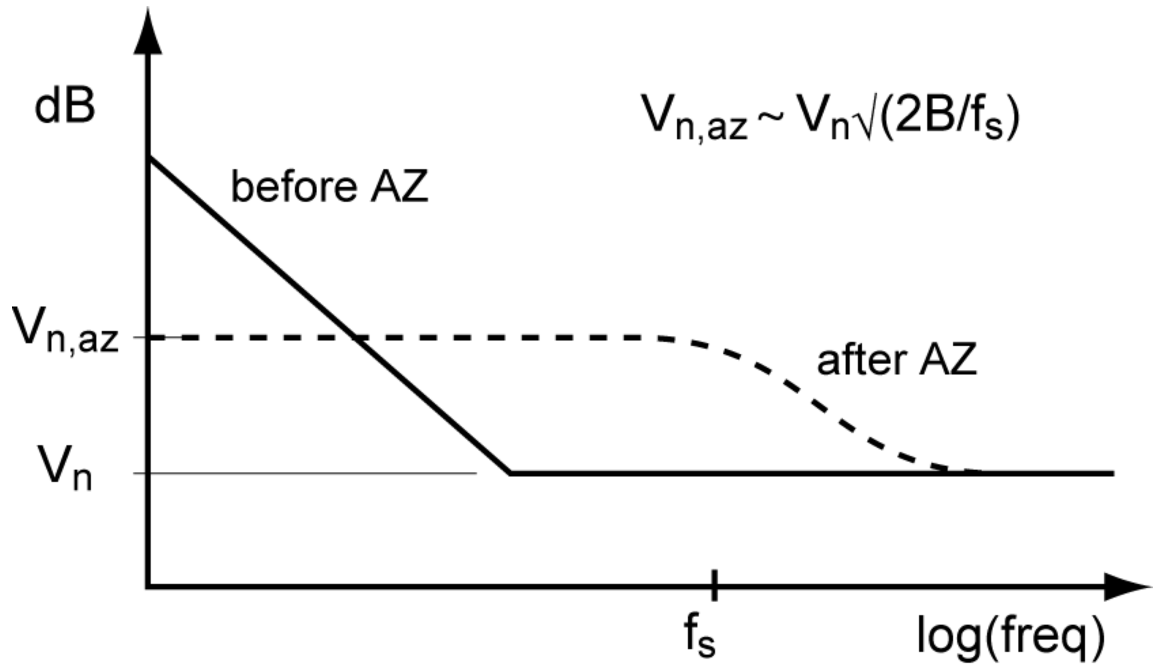


Courtesy of R. Burt, TI



- S&H with 100kHz clock & 50% duty-cycle
- Noise aliasing ⇒ 6x increase in LF noise voltage!
- Notches at multiples of **2**fclock due to 50% duty cycle[2]
- Sampled noise spectrum obtained with Pnoise[9,10]

Residual Noise of Auto-zeroing (4)



- Detailed analysis[2] $\Rightarrow$ significant reduction of 1/*f* noise **IF** f_s >> 1/*f* corner frequency
- Noise aliasing $\Rightarrow$ LF power increased by the under-sampling factor (USF) = $2B/f_s$ $\Rightarrow$ factor 3 to 6 in volts

Continuous Output

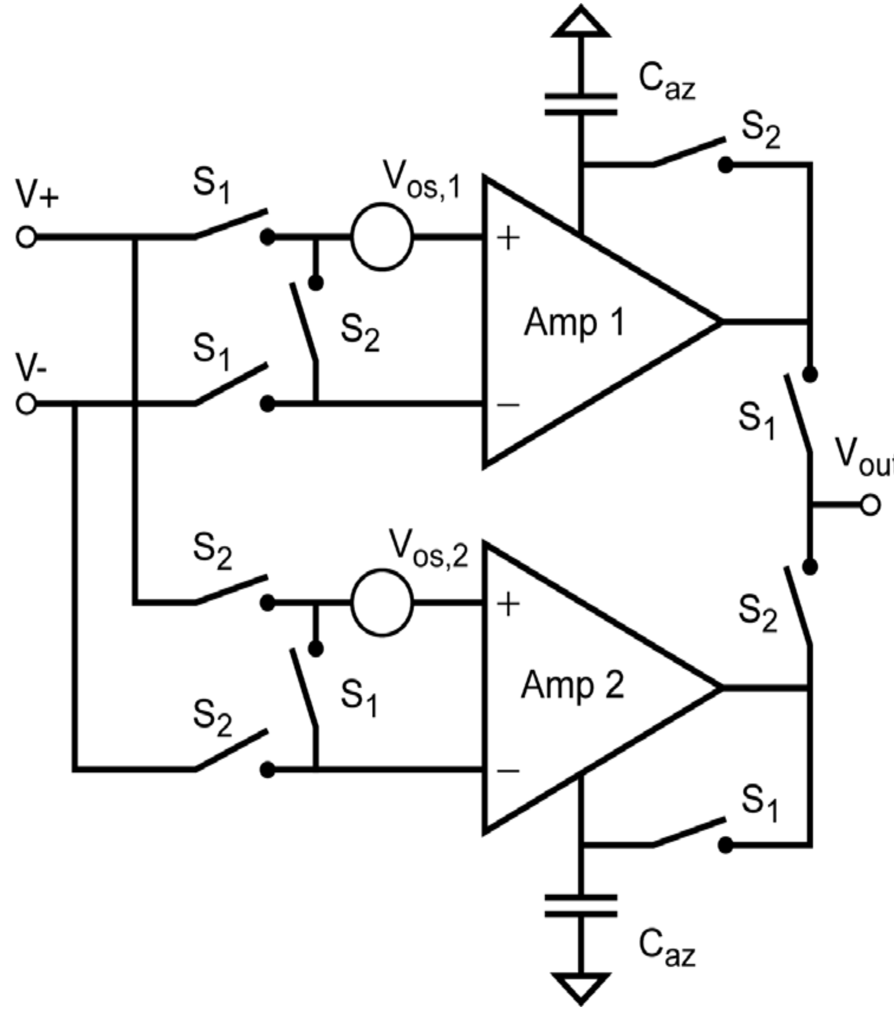
- Basic auto-zero principle $\Rightarrow$ the amplifier is not continuously available

Solutions

- Two AZ'ed amplifiers connected in parallel
  $\Rightarrow$ Ping-pong architecture
- An AZ'ed amplifier nulls the offset of another amplifier
  $\Rightarrow$ Offset stabilization

AZ Ping-Pong Amplifier

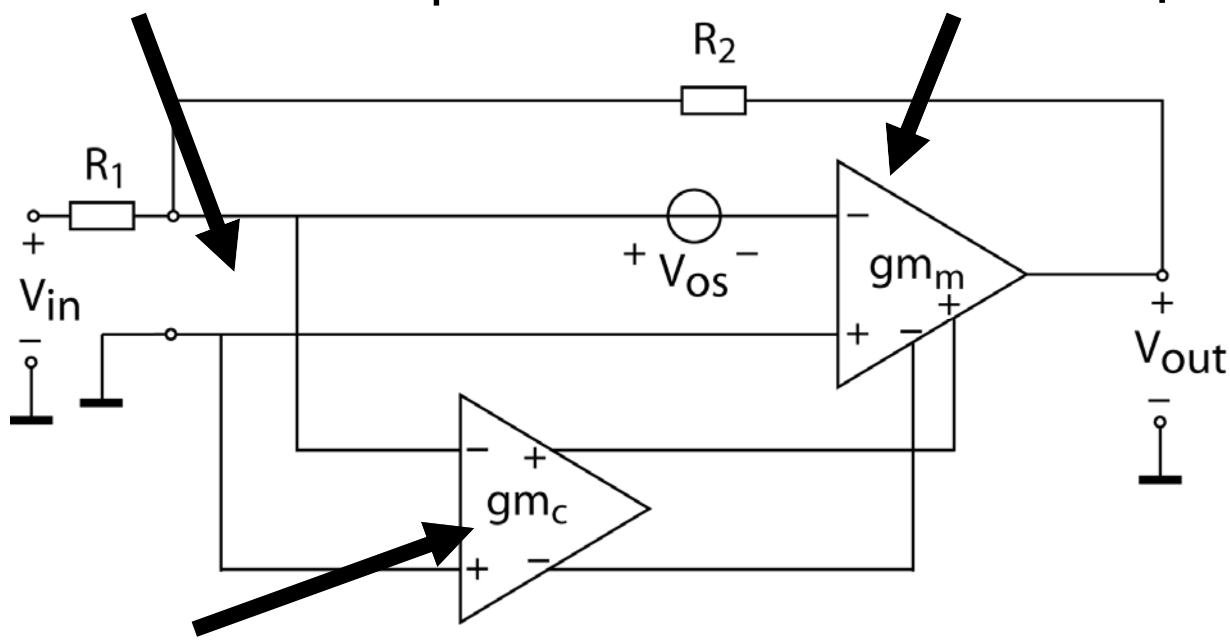
- Input signal "bounced" between two auto-zeroed amplifiers[11,12]
- Output V_{out} is then a quasi-continuous signal
- But switching spikes limit performance
- Randomized switching reduces spikes[13]



Offset Stabilization (OS)

Negative feedback
⇒ offset visible at input

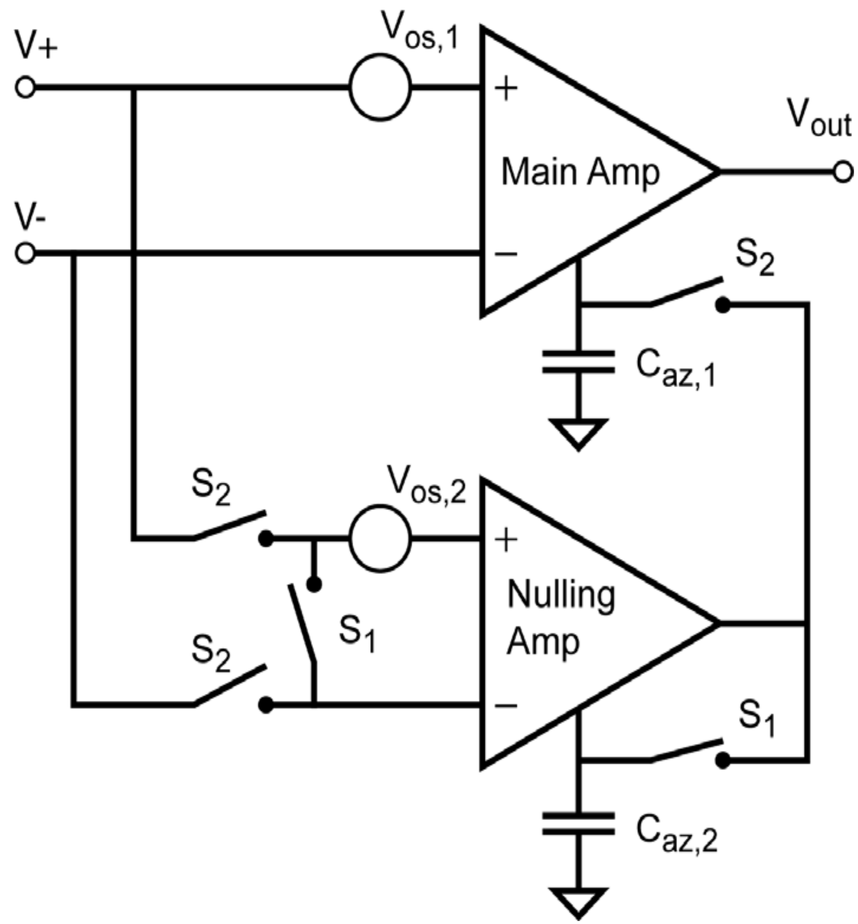
High bandwidth
main amplifier



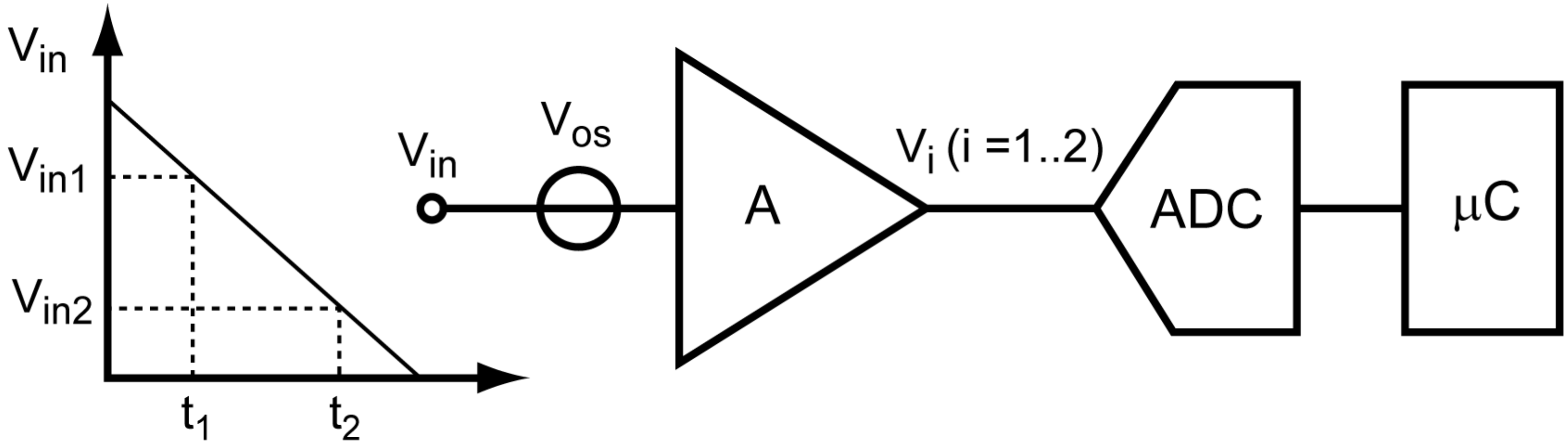
- Also called continuous-time AZ
- Low bandwidth, low offset compensating amplifier
  ⇒ Auto-zeroed or chopped

AZ Offset-Stabilized Amplifier

- Auto-zeroed nulling amp cancels the offset of main amplifier[14,15]
- Continuous output and less spikes
- But poor overload performance, i.e. when $V_+ - V_- > V_{os}$
- Amplifier cannot be used as a comparator



Correlated Double Sampling (CDS)

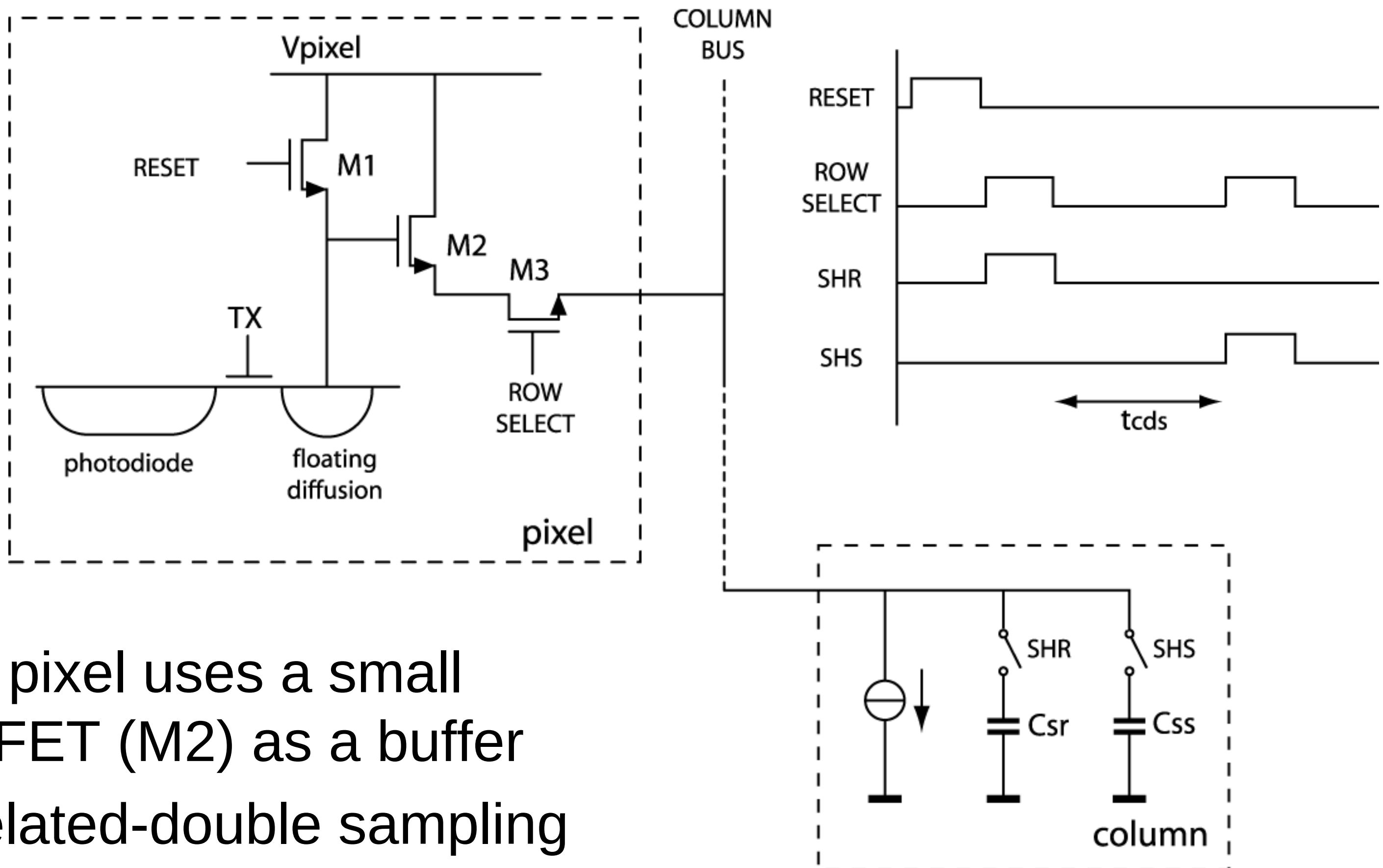


- Sometimes only a signal **difference** is required e.g. in image sensors
- Phase 1: $V_1 = A(V_{in1} + V_{os})$
- Phase 2: $V_2 = A(V_{in2} + V_{os})$

$\Rightarrow (V_1 - V_2) = A(V_{in1} – V_{in2})$

- CDS also suppresses 1/*f* noise

CMOS Image Sensors

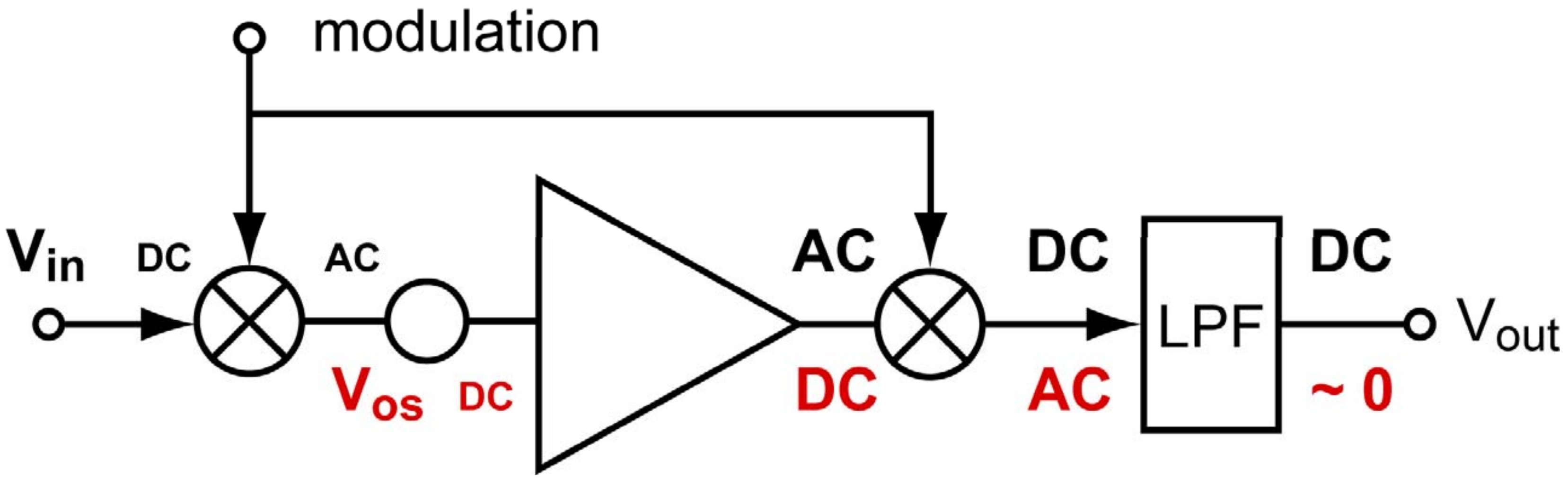


- Each pixel uses a small MOSFET (M2) as a buffer
- Correlated-double sampling removes offset and 1/*f* noise

Auto-Zeroing: Summary

- Offsets in the range of 1-10μV can be achieved
- No loss of bandwidth with appropriate amplifier topologies (ping-pong, offset-stabilization)
- Sampled data technique $\Rightarrow$ kT/C noise is an issue
- Noise aliasing will occur $\Rightarrow$ increased LF noise
- DOC technique of choice in sampled-data systems e.g. switched-capacitor filters, ADCs etc.

Chopping Principle

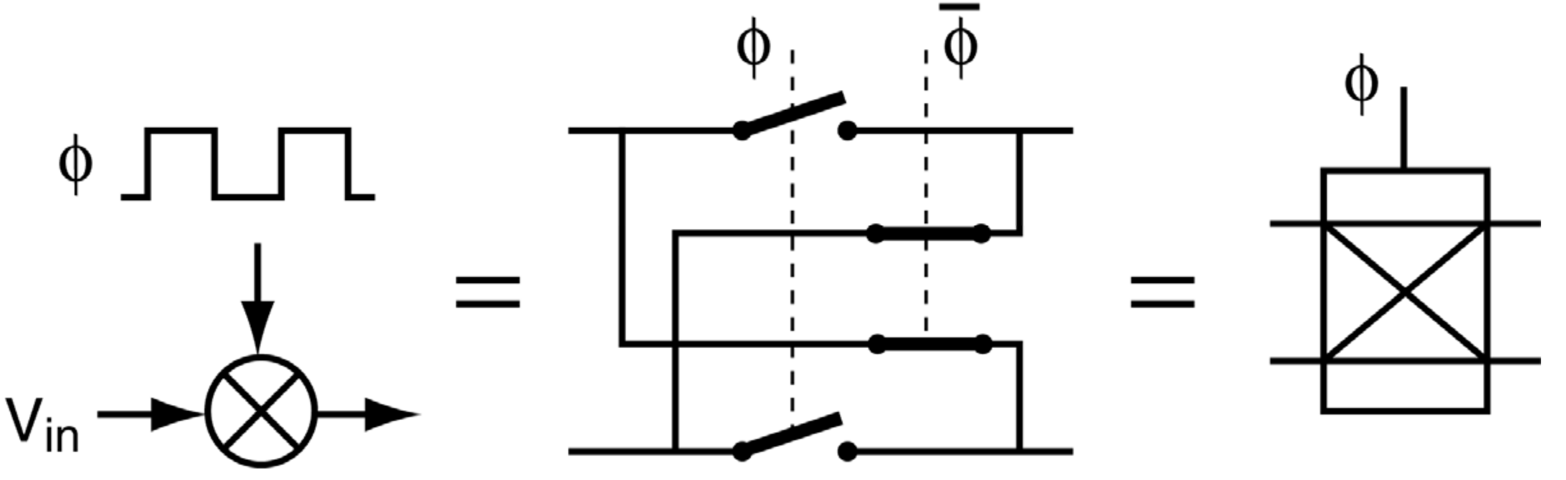


Signal is modulated, amplified and then demodulated[16]

+ Output signal is continuously available

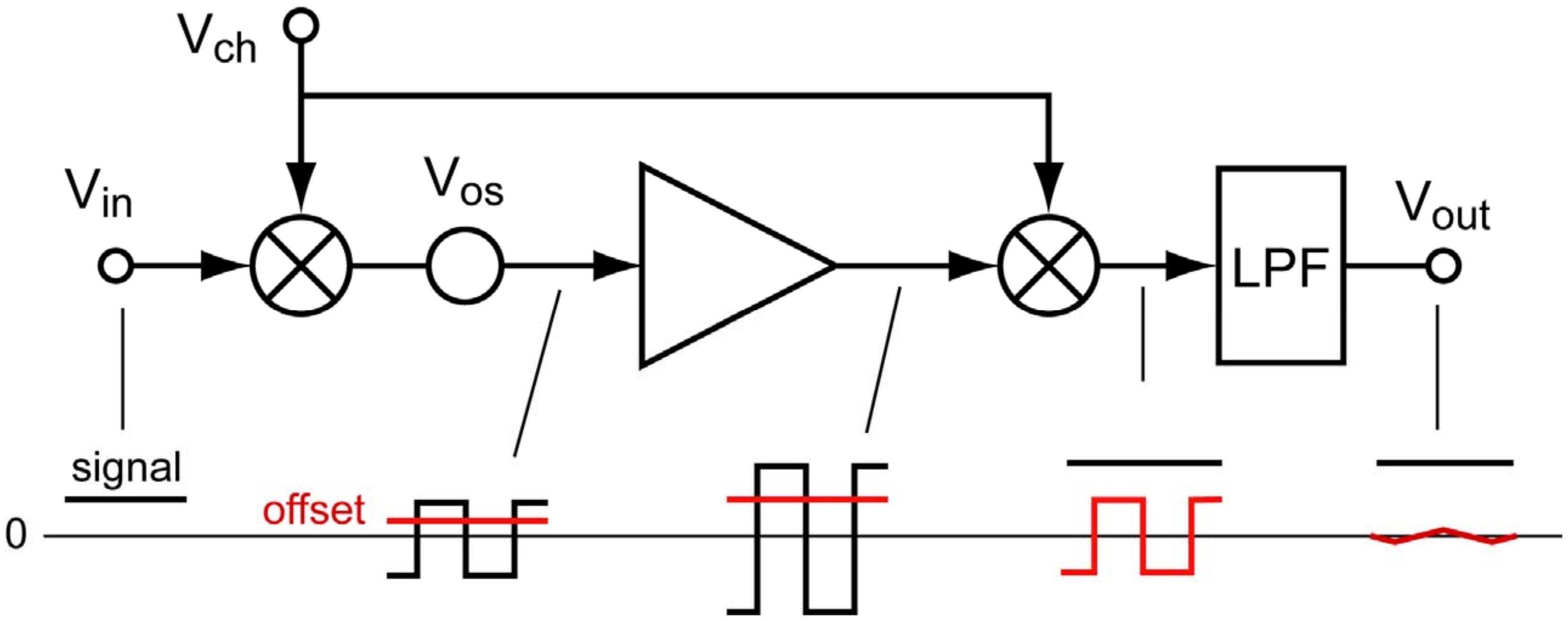
- Low-pass filter required

Square-wave Modulation



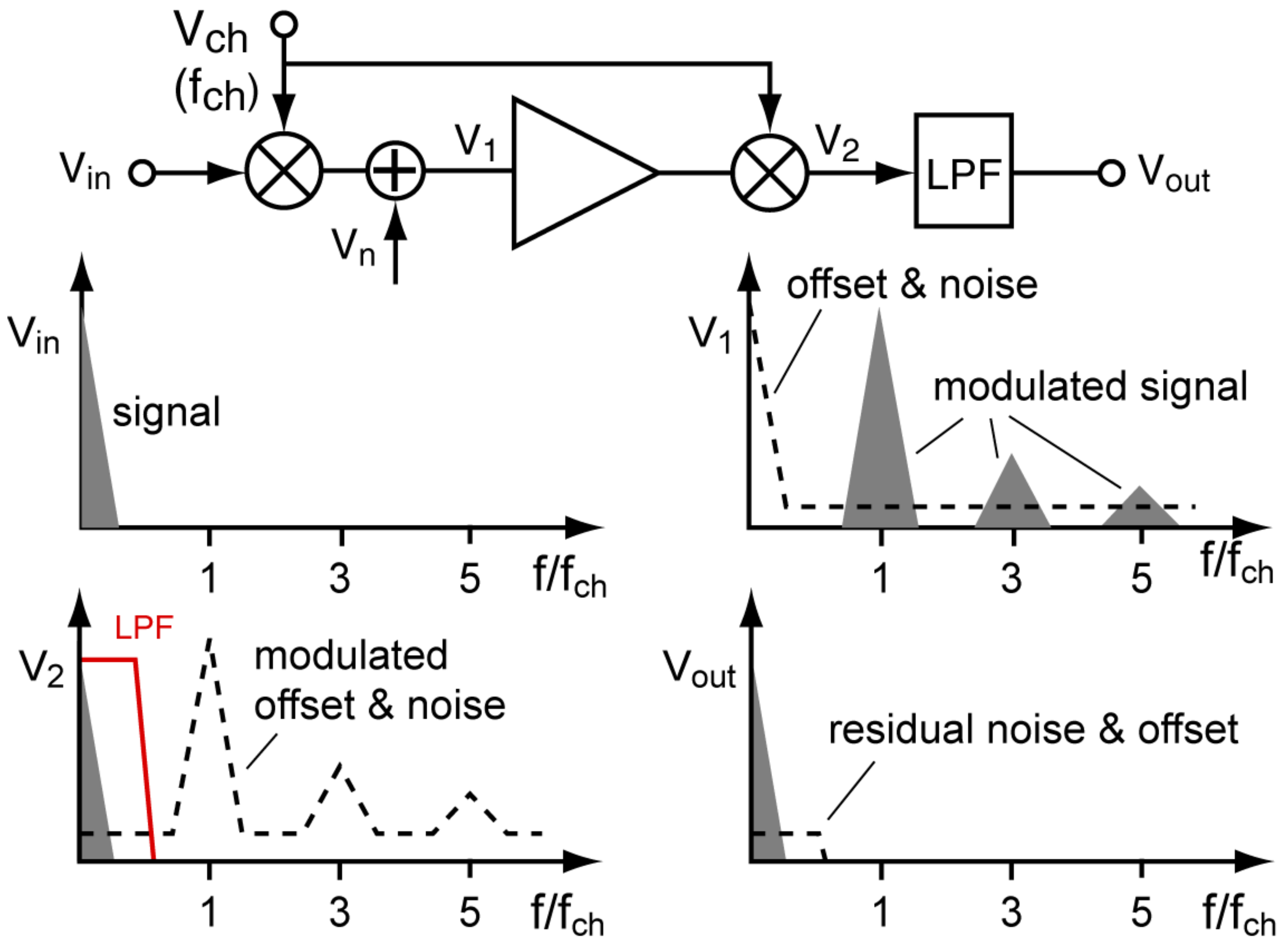
- Easily generated modulating signal
- Modulator is a simple polarity-reversing switch
- Switches are easily realized in CMOS

Chopping in the Time Domain

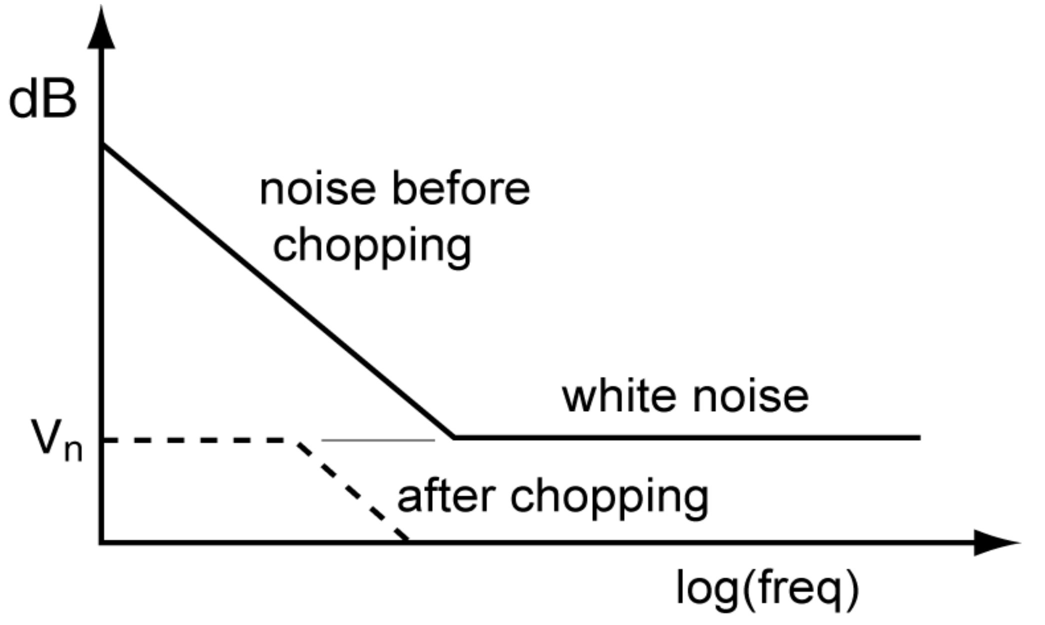


- V_{res} = 0 **IF** duty-cycle of V_{ch} is exactly 50% $\Rightarrow$ flip-flop
- If V_{os} = 10mV & f_{ch} = 50kHz, then 1ns skew $\Rightarrow$ V_{res} = 1µV

Chopping in the Frequency Domain

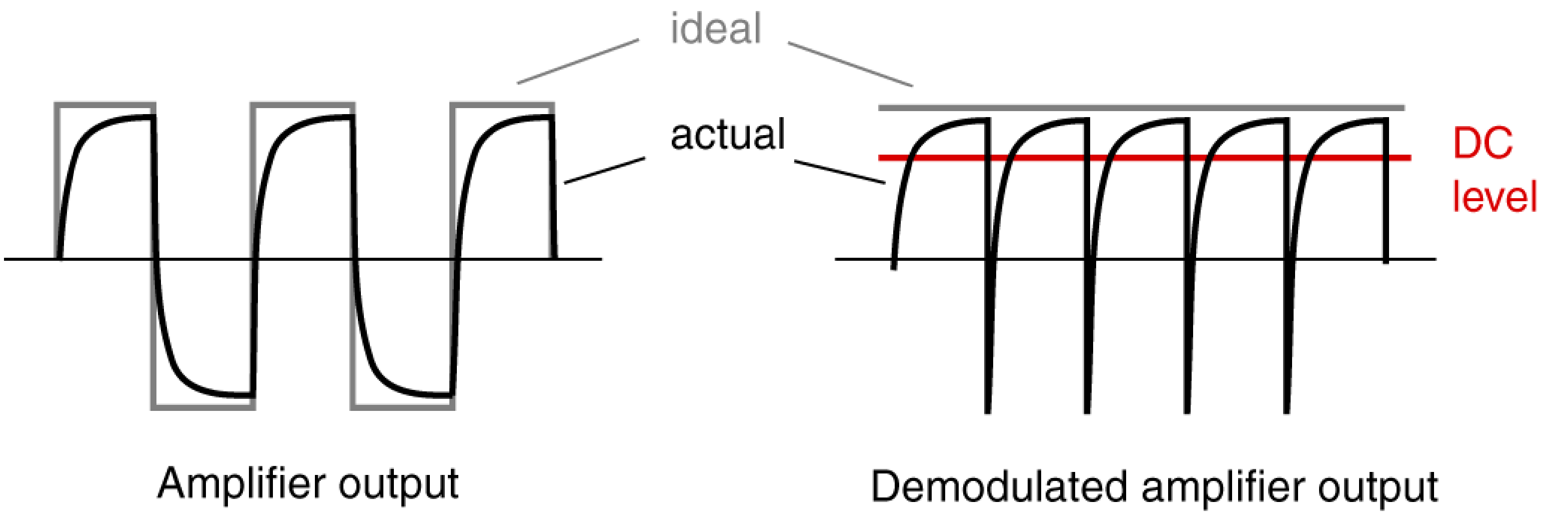


Residual Noise of Chopping



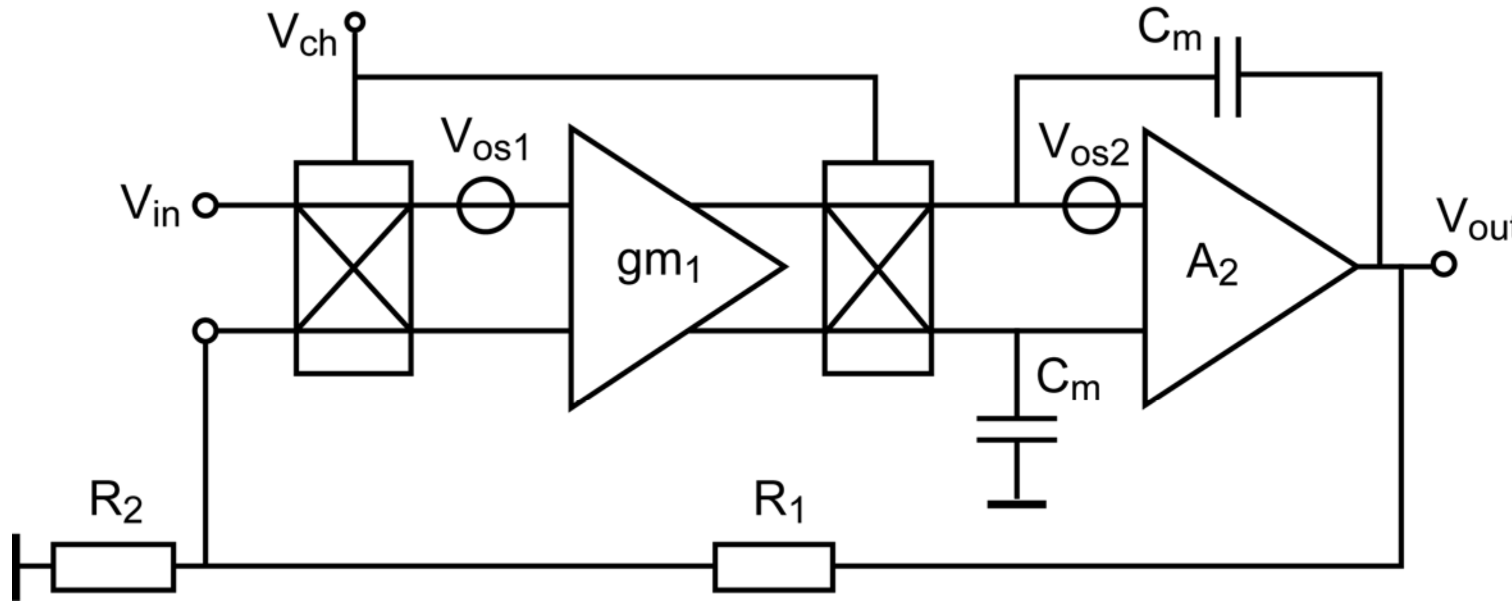
- 1/*f* noise is **completely** removed
  IF f_{ch} > 1/*f* corner frequency
- Significantly better than auto-zeroing!

Bandwidth & Gain Accuracy



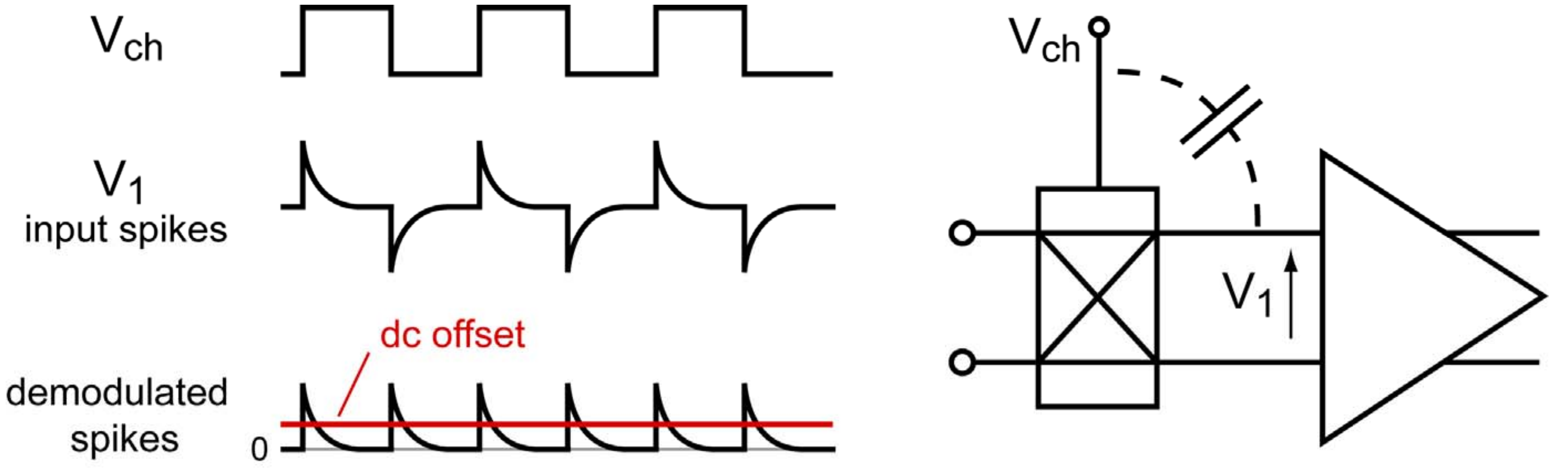
- Limited BW $\Rightarrow$ lower effective gain A_{eff}
  and chopping artifacts at even harmonics of f_{ch}
- Gain error < 10% $\Rightarrow$ BW > $6.4f_{ch}$

Chopper Opamp with Feedback



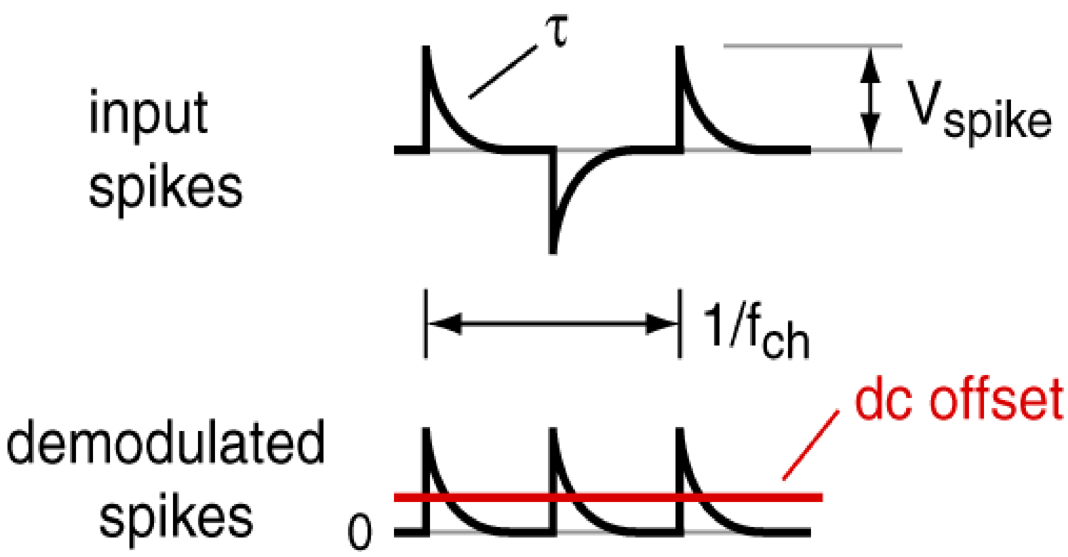
- Feedback resistors ⇒ Accurate gain[17,18]
- To suppress V_{os2}, A_1 should have high gain
- Miller capacitors C_m also suppress ripple
- Minimum ripple ⇒ high chopping frequencies

Residual Offset of Chopping (1)



- Due to mismatched charge injection and clock feed-through at the input chopper[19,20]
- Causes a typical offset of 1-10μV
- Input spikes ⇒ bias current (typically 50pA)

Residual Offset of Chopping (2)



- Residual offset[2] = $2f_{ch} V_{spike}\tau$
- Spike shape (τ) depends on source impedance
  e.g. feedback resistors around an opamp

Design Considerations

Input chopper

- Use minimum size switches
- Good layout $\Rightarrow$ symmetric, balanced clock coupling
- Ensure that switches "see" equal impedances
- Use a flip-flop to ensure an exact 50% duty-cycle

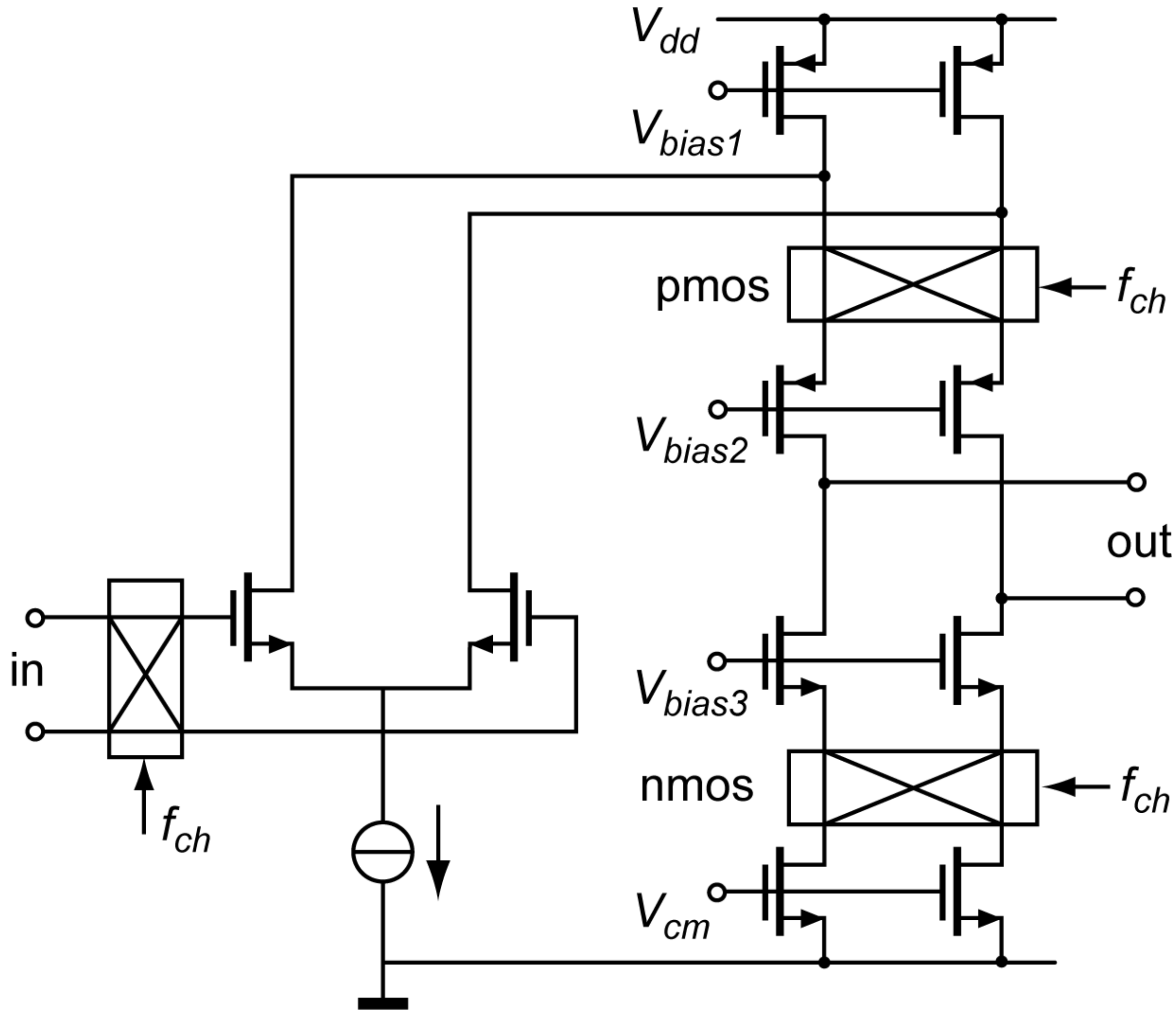
Chopping frequency f_{ch}

- Higher than 1/*f* noise corner frequency
- Not **too** high, as the residual offset increases with f_{ch}

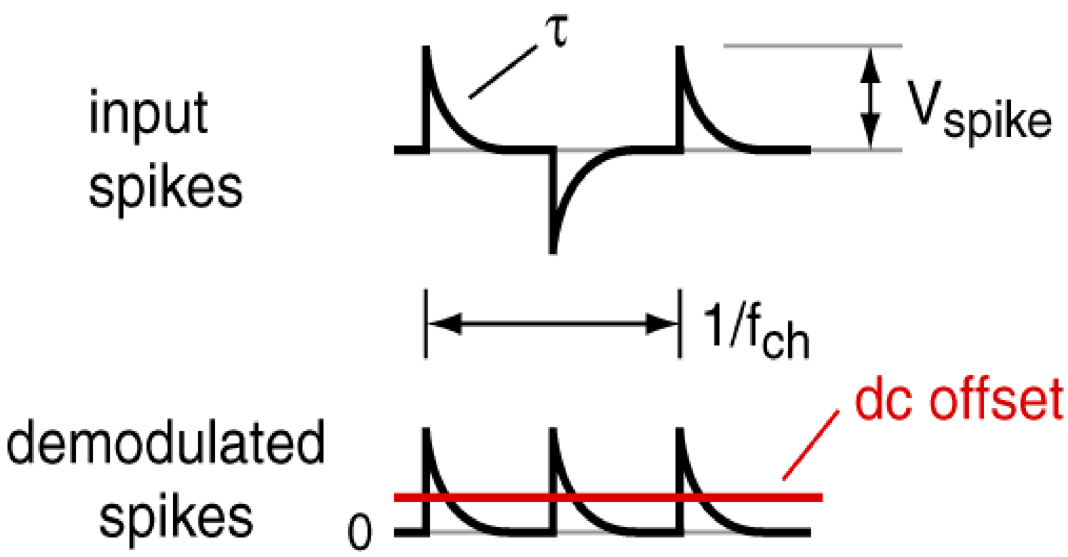
Amplifier BW >> f_{ch} to minimize gain errors

Chopped Transconductor[22]

- Choppers see low & symmetric impedances
- Allows high freq chopping
- PMOS chopper demodulates signal
- NMOS chopper DEMs NMOS current sources

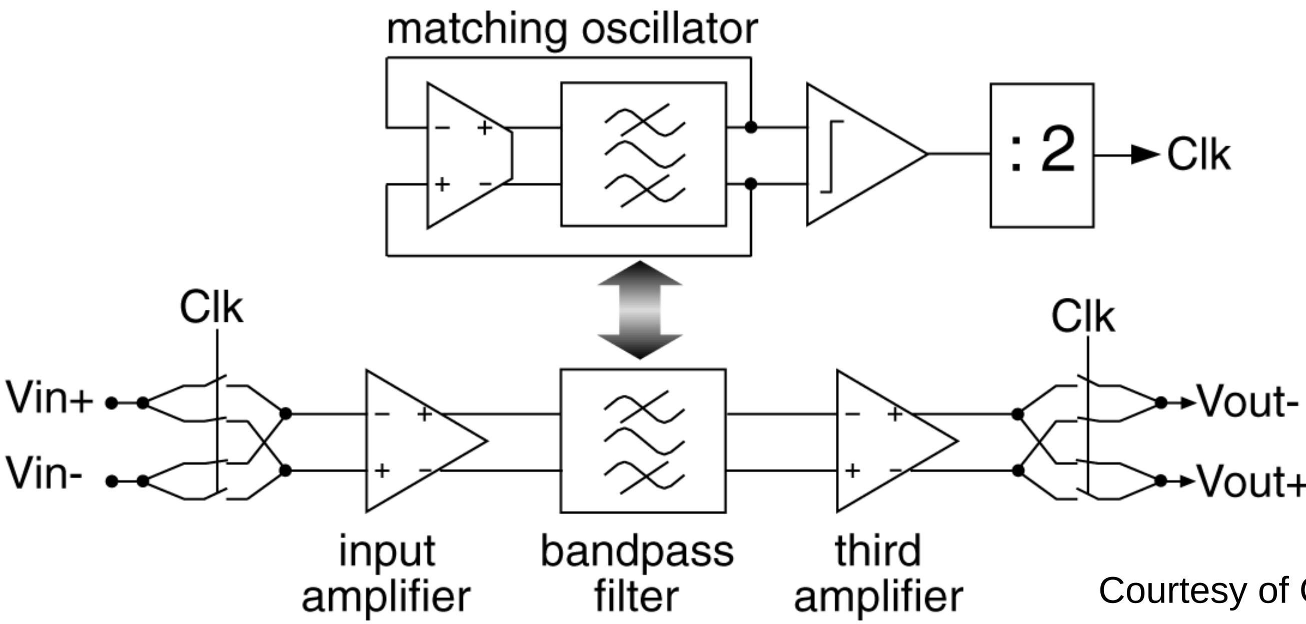


Lower Residual Offset



- Residual offset^2 = $2f_{ch}\,V_{spike}\tau$
- Low residual offset ⇒ reduce chopping frequency, reduce load impedances OR reduce spike amplitude

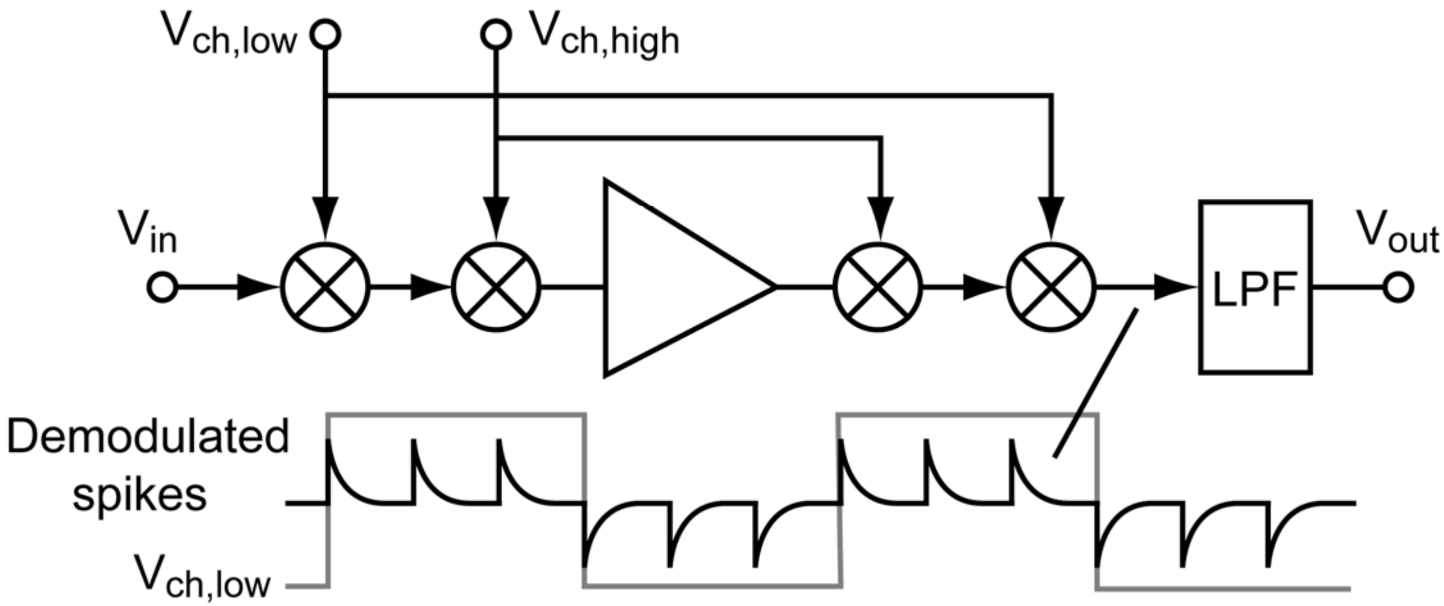
Band-Pass Filtering



Courtesy of C. Hagleitner, IBM

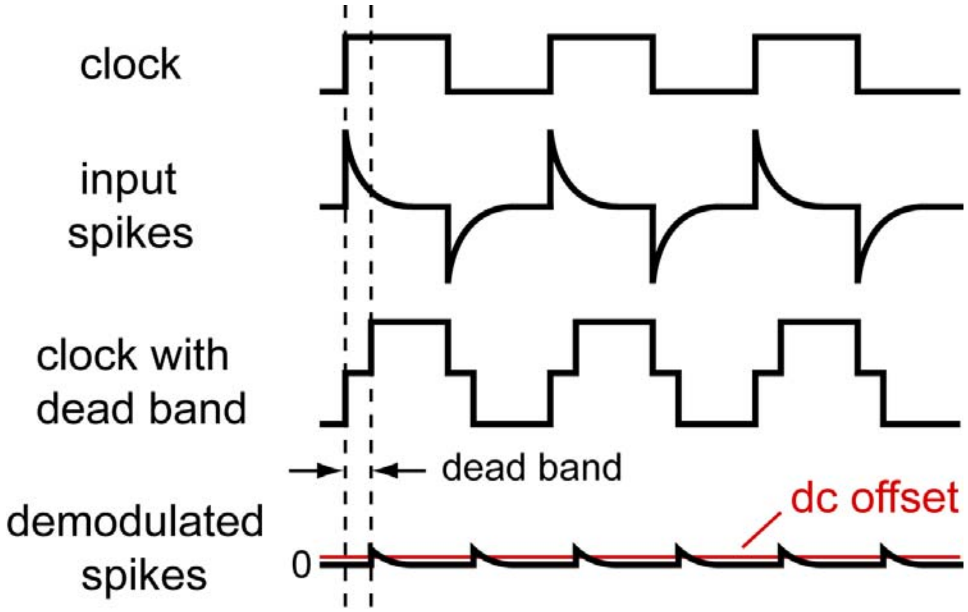
- Spike spectrum is “whiter” than that of modulated signal
  ⇒ BP filter will reduce **relative** spike amplitude[19,23,24]
- Clock frequency tracks BP filter's center frequency
  ⇒ low Q filter, Q ~ 5
- Residual offset ~ 0.5μV!

Nested Chopping



- Inner HF chopper removes 1/*f* noise
- Outer LF chopper removes residual offset[21]
- Residual offset ~ 100nV, but reduced bandwidth
- Note: input choppers should not be merged!

Dead-Banding



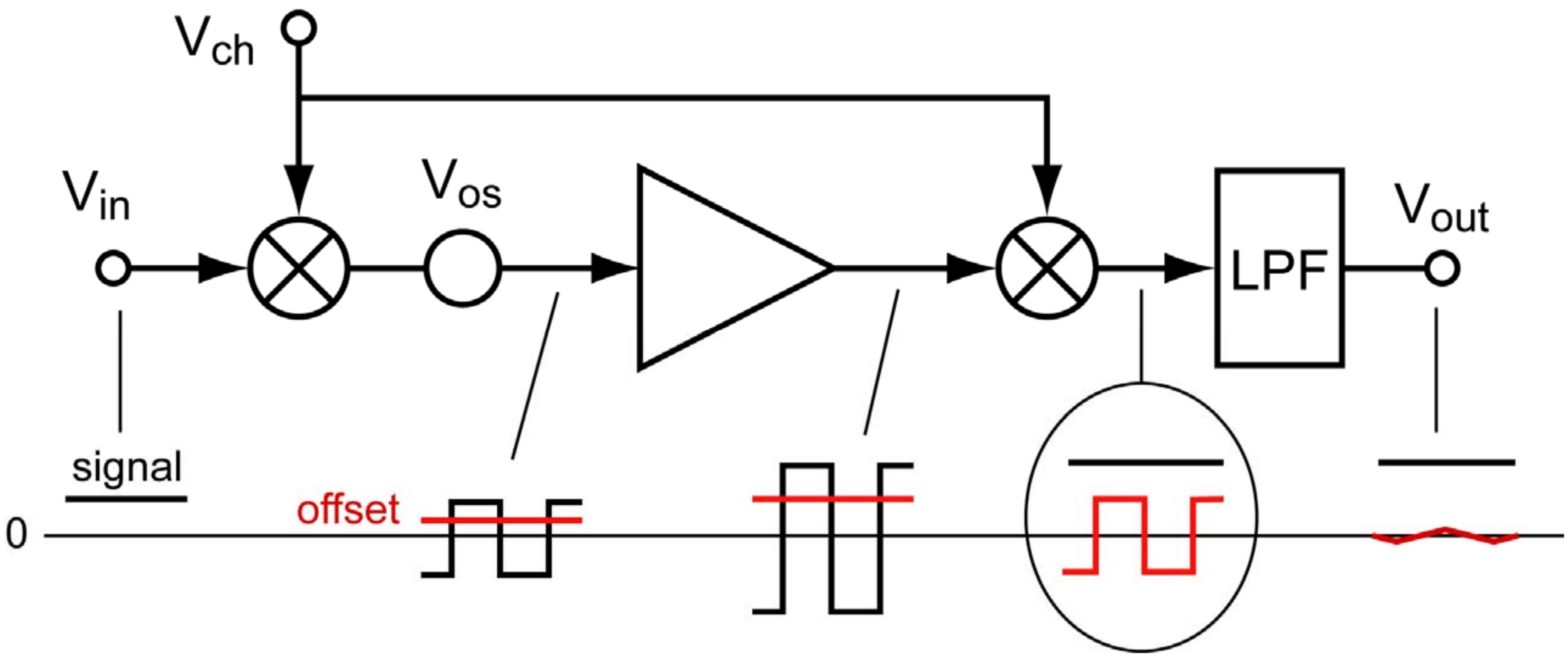
- During dead-band amplifiers output is tri-stated[26,27,28]
- Residual offset ~ 200nV!
- BUT loss of gain and aliasing due to S&H action
  $\Rightarrow$ slightly worse noise performance

Dealing with Spikes: Overview

- BP Filtering: ~ 0.5μV offset, complex clock timing
- Dead-banding: ~ 200nV offset, wide BW
- Nested chopping: ~ 100nV offset, but limited BW

Last two techniques represent best compromise between offset magnitude and circuit complexity

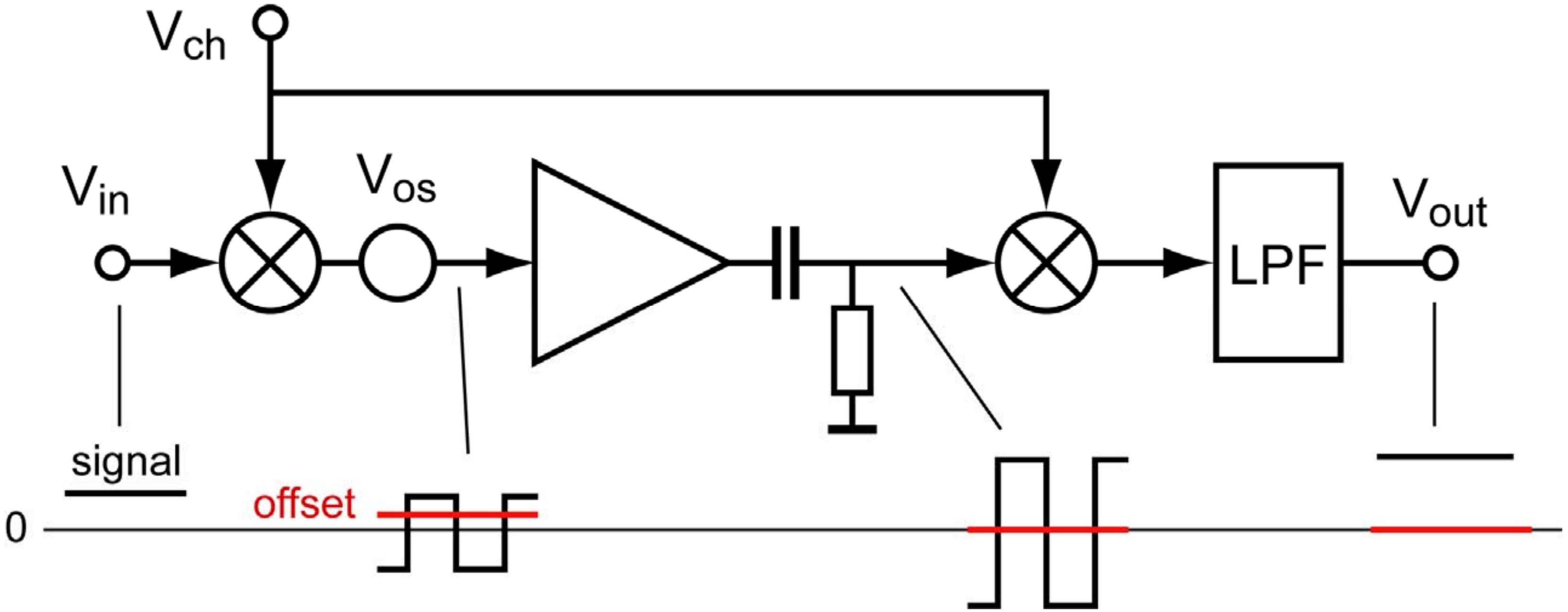
Chopping Artifacts (Ripple)



Modulated offset ⇒ chopping artifacts (ripple)

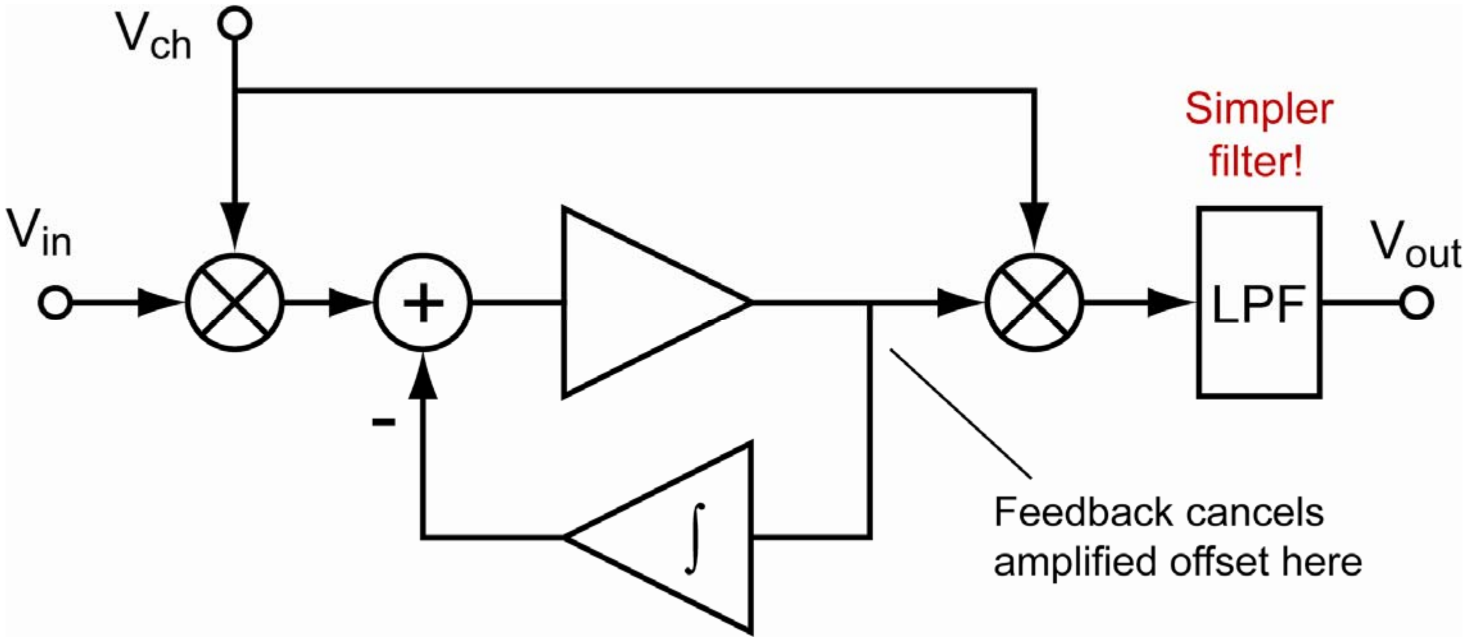
- Can be removed by a low-pass filter
- BUT filter cut-off frequency must be quite low ⇒ difficult to realize on chip

AC Coupling



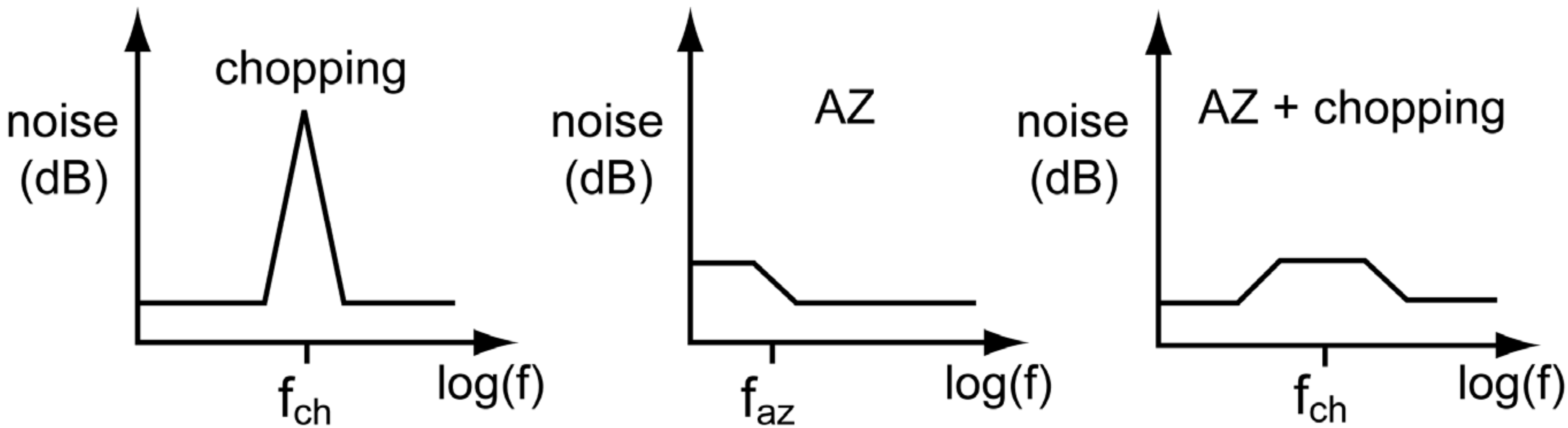
- AC coupling blocks the amplifier's offset
  ⇒ no output ripple!
- But cut-off frequency must again be quite low

DC Servo Loop



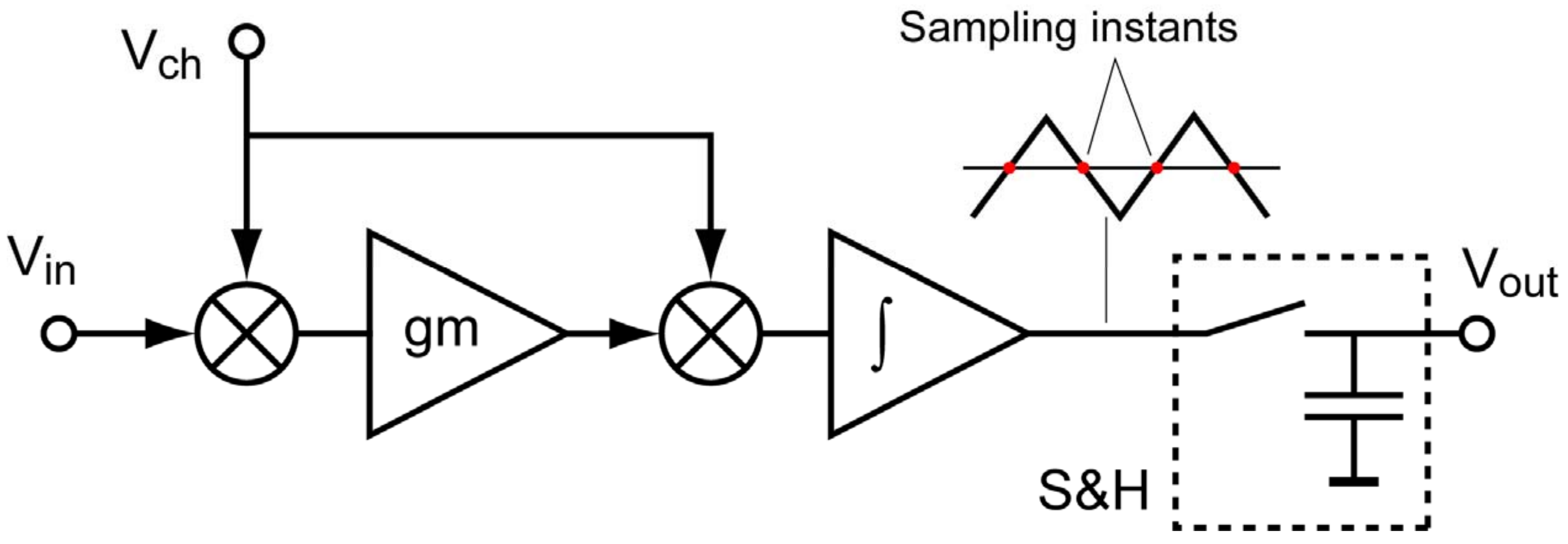
- DC “servo” loop suppress the amplifier’s offset[34,35]
- Integrator is not in the main signal path
  $\Rightarrow$ much easier to realize a low cut-off frequency
- Residual ripple can be removed by a simple LPF

Auto-zeroing and Chopping



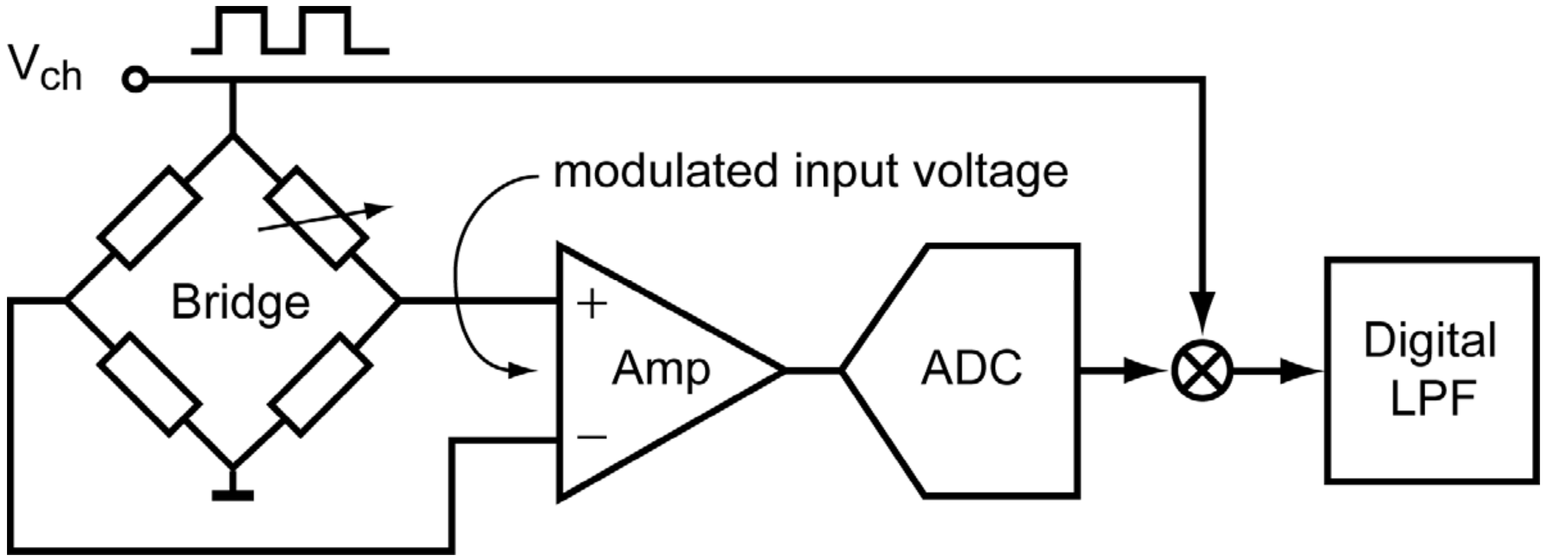
- Compared to standard AZ, significantly improves LF noise performance[30,31,32,33]
- Much less ripple than with chopping alone
- Choosing $f_{ch} = 2f_{az} \Rightarrow$ residual offset of auto-zeroing is exactly averaged $\Rightarrow$ aliased noise has notch at DC

Switched Capacitor Filter



- Chopped offset is integrated & the triangular ripple is then sampled at the zero-crossings[9,37,38]
- SC filter essentially eliminates residual ripple
- Filter introduces delay and a (small) noise penalty

Digital Filtering



- Chopped signal is digitized
- Demodulation is done digitally[31,39]
- Chopper artifacts are removed by a digital LPF e.g. a sinc filter with notches at f_{ch}

Dealing with Artifacts: Overview

Reduce the amplifier's initial offset

- Auto-zeroing and chopping: increased noise
- DC servo: still requires some analog filtering
- Switched capacitor filtering

Digital Filtering

- Very low cut-off frequencies can be realized
- Decimation filter of a $\Sigma\Delta$ ADC can be used to remove chopper artifacts $\Rightarrow$ no extra overhead

Chopping: Summary

- Offsets in the range of 50nV-10µV can be achieved
- Timing skew limits offset reduction to about 60dB
- Fundamental loss of bandwidth (unless offset-stabilized topologies can be used)
- Eliminates 1/*f* noise, noise floor set by thermal noise
- DOC technique of choice when noise or offset performance is paramount e.g. in biomedical amplifiers, low-power opamps, smart sensors etc.

Some Caveats

- Chopping and auto-zeroing rely on amplifier linearity
- Amplifier non-linearity will result in a residual offset!
- Presence of timing jitter $\Rightarrow$ variable settling (AZ) or non-50% duty-cycles (chopping) $\Rightarrow$ voltage noise
- Finite switch resistance $\Rightarrow$ trade-off between CI, thermal noise and BW limitations

Summary

- Offset and 1/*f* are part of life!
- Trimming
  - reduces offset but not 1/*f* noise
  - simple, no loss of bandwidth
- Auto-zeroing
  - eliminates 1/*f* noise, but noise aliasing ⇒ LF noise
  - Auto-zero period ⇒ Loss of bandwidth
  - CT operation ⇒ OS and Ping-pong topologies
- Chopping
  - eliminates 1/*f* noise ⇒ best noise efficiency
  - LPF ⇒ loss of bandwidth (unless OS is used)
- Nested DOC techniques ⇒ sub-microvolt offset